MOTOROLA

DL156/D
REV 4

Fast Static RAM
Component and Module Data

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Fast Static RAM
Component and Module Data

Motorola offers a broad range of fast SRAMs for virtually any digital data processing system application. This data book contains complete specifications for individual FSRAM circuits in data sheet form, as well as an explanation of Motorola's reliability and quality program and an applications section.

For information on Dynamic RAM devices, please refer to DL155/D.

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MCM69L818A	256K x 18	7.5/8.5/9.5/10.5	Late Write HSTL, 3.3 V	3–154
MCM69L819	256K x 18	8/9	Late Write LVTTL, 3.3 V	3–173
MCM69L819A	256K x 18	7.5/8.5/9.5/10.5	Late Write LVTTL, 3.3 V	3–191
MCM69L820	256K x 18	8/9	Late Write 2.5 V I/O, 3.3 V	3–209
MCM69L820A	256K x 18	7.5/8.5/9.5/10.5	Late Write 2.5 V I/O, 3.3 V	3–227
MCM69P536A	32K x 36	5/6/7	Pipelined BurstRAM, 3.3 V	4–175
MCM69P536B	32K x 36	4/4.5/5/6/7	Pipelined BurstRAM, 3.3 V	4–186
MCM69P536c	32K x 36	4/4.5/5/6/7	Pipelined BurstRAM, 3.3 V	4–197
MCM69P618A	64K x 18	4/4.5/5/6/7	Pipelined BurstRAM, 3.3 V	4–102
MCM69P618C	64K x 18	4/4.5/5/6/7	Pipelined BurstRAM, 3.3 V	4–113
MCM69P737	128K x 36	3.5/3.8/4	Flow–Through BurstRAM, 3.3 V	4–51
MCM69P819	256K x 18	3.5/3.8/4	Pipelined BurstRAM, 3.3 V	4–19
MCM69Q536	32K x 36	6/8/10	Single address, separate I/O SRAM	5–167
MCM69Q618	64K x 18	6/8/10	Single address, separate I/O SRAM	5–190
MCM69R536	32K x 36	5/6/7/8	Late Write HSTL, 3.3 V	3–245
MCM69R537	32K x 36	5/6/7/8	Late Write LVTTL, 3.3 V	3–264
MCM69R538	32K x 36	56/7/8	Late Write 2.5 V I/O, 3.3 V	3–283
MCM69R539	32K x 36	4.5/5	Late Write HSTL, dual clock, 3.3 V	3–302
MCM69R618	64K x 18	5/6/7/8	Late Write HSTL, 3.3 V	3–245
MCM69R619	64K x 18	5/6/7/8	Late Write LVTTL, 3.3 V	3–264
MCM69R620	64K x 18	5/6/7/8	Late Write 2.5 V I/O, 3.3 V	3–283
MCM69R621	64K x 18	4.5/5	Late Write 2.5 V I/O, dual clock, 3.3 V	3–302
MCM69R736	128K x 36	7/8	Late Write HSTL, 3.3 V	3–3
MCM69R736A	128K x 36	7/8	Late Write HSTL, 3.3 V	3–22
MCM69R737	128K x 36	7/8	Late Write LVTTL, 3.3 V	3–41
MCM69R737A	128K x 36	5/6/7/8	Late Write LVTTL, 3.3 V	3–59
MCM69R738	128K x 36	7/8	Late Write LVTTL 2.5 V I/O, 3.3 V	3–77
MCM69R738A	128K x 36	5/6/7/8	Late Write LVTTL 2.5 V I/O, 3.3 V	3–95

Device	Org	Access Time (ns)	Comments	Page
MCM69R739A	128K x 36	4.2/4.5/5	Late Write HSTL, dual clock, 3.3 V	3–113
MCM69R818	256K x 18	7/8	Late Write HSTL, 3.3 V	3–3
MCM69R818A	256K x 18	7/8	Late Write HSTL, 3.3 V	3–22
MCM69R819	256K x 18	7/8	Late Write LVTTL, 3.3 V	3–41
MCM69R819A	256K x 18	5/6/7/8	Late Write LVTTL, 3.3 V	3–59
MCM69R820	256K x 18	7/8	Late Write LVTTL 2.5 V I/O, 3.3 V	3–77
MCM69R820A	256K x 18	5/6/7/8	Late Write LVTTL 2.5 V I/O, 3.3 V	3–95
MCM69R821A	256K x 18	4.2/4.5/5	Late Write HSTL, dual clock, 3.3 V	3–113
MCM69T618	64K x 18	5/6/7	Synchronous pipelined cache tag, 3.3 V	5–3
MCM6926	128K x 8	8/10/12/15	Revolutionary pinout, 3.3 V	2–94
MCM6926A	128K x 8	8/10/12/15	Revolutionary pinout, 3.3 V	2–101
MCM6926–C	128K x 8	8/10/12/15	Revolutionary pinout, 3.3 V, Industrial Temperature	2–108
MCM6929	256K x 4	8/10/12/15	Revolutionary pinout, 3.3 V	2–145
MCM6929A	256K x 4	8/10/12/15	Revolutionary pinout, 3.3 V	2–152
MCM6929–C	256K x 4	8/10/12/15	Revolutionary pinout, 3.3 V, Industrial Temperature	2–159
MCM6946	512K x 8	10/12/15	Revolutionary pinout, 3.3 V	2–18
MCM6949	1M x 4	10/12/15	Revolutionary pinout, 3.3 V	2–34
MCM72FB8ML	256K x 72	117/100 MHz	Multichip module, flow–through, 3.3 V	6–3
MCM72F10	8MB	8/9/12	Flow–through synchronous BurstRAM, 3.3 V	6–66
MCM72F9	4MB	8/9/12	Flow–through synchronous BurstRAM, 3.3 V	6–75
MCM72F8	2MB	8/9/12	Flow–through synchronous BurstRAM, 3.3 V	6–75
MCM72F7	1MB	9/10/12	Flow–through synchronous BurstRAM, 3.3 V	6–85
MCM72F6	512KB	9/10/12	Flow–through synchronous BurstRAM, 3.3 V	6–85
MCM72PB8ML	256K x 72	166/133 MHz	Multichip module, flow–through, 3.3 V	6–3
MPC2105B	512KB	66 MHz	BurstRAM secondary cache module for PowerPC PReP/CHRP, 5 V	6–21
MPC2105P	512KB	66 MHz	BurstRAM secondary cache module for PowerPC PReP/CHRP, 5 V	6–37
MPC2106B	1M	66 MHz	BurstRAM secondary cache module for PowerPC PReP/CHRP, 5 V	6–21
MPC2604GA	32K x 36	66 MHz	Integrated Level2 cache for PowerPC Microprocessors	5–109
MPC2605	32K x 72	66 MHz	Integrated Level2 cache for PowerPC Microprocessors	5–80
MPC27T415	16K x 15	9/10/12	cache tag RAM for PowerPC Microprocessors, 3.3 V	5–27
MPC27T416	16K x 16	9/10/12	Cache tag RAM for PowerPC Microprocessors, 3.3 V	5–12

FSRAM SELECTOR GUIDE

SYNCHRONOUS

Late Write RAMs

Description	Organi–zation	V_{CC}	Motorola Part Number	Pin Count	Packaging	Cycle Time (ns Max)	Pro–duction	Comments	Page #
4M	256K x 18	3.3 V	MCM69R818	119	(ZP) PBGA	7/8	Now	Not recommended for new designs. Suggest MCM69R818A.	3–3
			MCM69R819	119	(ZP) PBGA	7/8	Now	Not recommended for new designs. Suggest MCM69R819A.	3–41
			MCM69R820	119	(ZP) PBGA	7/8	Now	Not recommended for new designs. Suggest MCM69R820A.	3–77
			MCM69L818	119	(ZP) PBGA	7/8	Now	Not recommended for new designs. Suggest MCM69L818A.	3–135
			MCM69L819	119	(ZP) PBGA	8/9	Now	Not recommended for new designs. Suggest MCM69L819A.	3–173
			MCM69L820	119	(ZP) PBGA	8/9	Now	Not recommended for new designs. Suggest MCM69L820A.	3–209
	128K x 36		MCM69R736	119	(ZP) PBGA	7/8	Now	Not recommended for new designs. Suggest MCM69R736A.	3–3
			MCM69R737	119	(ZP) PBGA	7/8	Now	Not recommended for new designs. Suggest MCM69R737A.	3–41
			MCM69R738	119	(ZP) PBGA	7/8	Now	Not recommended for new designs. Suggest MCM69R738A.	3–77
			MCM69L736	119	(ZP) PBGA	7/8	Now	Not recommended for new designs. Suggest MCM69L736A.	3–135
			MCM69L737	119	(ZP) PBGA	8/9	Now	Not recommended for new designs. Suggest MCM69L737A.	3–173
			MCM69L738	119	(ZP) PBGA	8/9	Now	Not recommended for new designs. Suggest MCM69L738A.	3–209
	256K x 18	3.3 V	MCM69R818A	119	(ZP) PBGA	5/6/7/8	2Q97	Late write interface. Register/Register. HSTL I/Os. Samples now.	3–22
			MCM69R819A	119	(ZP) PBGA	5/6/7/8	2Q97	Late write interface. Register/Register. LVTTL I/Os. Samples now.	3–59
			MCM69R820A	119	(ZP) PBGA	5/6/7/8	2Q97	Late write interface. Register/Register. 2.5 V I/Os. Samples now.	3–95
			MCM69R821A	119	(ZP) PBGA	4.2/4.5/5	2Q97	Late write interface. Register/Register. HSTL I/Os. Dual clock. Samples now.	3–113
			MCM69L818A	119	(ZP) PBGA	7.5/8.5/9.5/10.5 Latency	2Q97	Late write interface. Register/Latch. HSTL I/Os. Samples now.	3–154
			MCM69L819A	119	(ZP) PBGA	7.5/8.5/9.5/10.5 Latency	2Q97	Late write interface. Register/Latch LVTTL I/Os. Samples now.	3–191
			MCM69L820A	119	(ZP) PBGA	7.5/8.5/9.5/10.5 Latency	2Q97	Late write interface. Register/Latch 2.5 V I/Os. Samples now.	3–227
	128K x 36		MCM69R736A	119	(ZP) PBGA	5/6/7/8	2Q97	Late write interface. Register/Register. HSTL I/Os. Samples now.	3–22
			MCM69R737A	119	(ZP) PBGA	5/6/7/8	2Q97	Late write interface. Register/Register. LVTTL I/Os. Samples now.	3–59
			MCM69R738A	119	(ZP) PBGA	5/6/7/8	2Q97	Late write interface. Register/Register. 2.5 V I/Os. Samples now.	3–95
			MCM69R739A	119	(ZP) PBGA	4.2/4.5/5	2Q97	Late write interface. Register/Register. HSTL I/Os. Dual clock. Samples now.	3–113
			MCM69L736A	119	(ZP) PBGA	7.5/8.5/9.5/10.5 Latency	2Q97	Late write interface. Register/Latch. HSTL I/Os. Samples now.	3–154
			MCM69L737A	119	(ZP) PBGA	7.5/8.5/9.5/10.5 Latency	2Q97	Late write interface. Register/Latch. LVTTL I/Os. Samples now.	3–191
			MCM69L738A	119	(ZP) PBGA	7.5/8.5/9.5/10.5 Latency	2Q97	Late write interface. Register/Latch. 2.5 V I/Os. Samples now.	3–227

Late Write RAMs (Continued)

1M	64K x 18	3.3 V	MCM69R618	119	(ZP) PBGA	5/6/7/8	Now	Late write interface. Register/Register. HSTL I/Os. Samples now.	3–245
			MCM69R619	119	(ZP) PBGA	5/6/7/8	Now	Late write interface. Register/Register. LVTTL I/Os. Samples now.	3–264
			MCM69R620	119	(ZP) PBGA	5/6/7/8	Now	Late write interface. Register/Register. 2.5 V I/Os. Samples now.	3–283
			MCM69R621	119	(ZP) PBGA	4.5/5	Now	Late write interface. Register/Register. HSTL I/Os. Dual clock. Samples now.	3–302
			MCM69L618	119	(ZP) PBGA	7.5/8.5/9.5/10.5 Latency	Now	Late write interface. Register/Latch HSTL I/Os. Samples now.	3–324
			MCM69L619	119	(ZP) PBGA	7.5/8.5/9.5/10.5 Latency	Now	Late write interface. Register/Latch LVTTL I/Os. Samples now.	3–343
			MCM69L620	119	(ZP) PBGA	7.5/8.5/9.5/10.5 Latency	Now	Late write interface. Register/Latch 2.5 V I/Os. Samples now.	3–362
	32K x 36		MCM69R536	119	(ZP) PBGA	5/6/7/8	Now	Late write interface. Register/Register. HSTL I/Os. Samples now.	3–245
			MCM69R537	119	(ZP) PBGA	5/6/7/8	Now	Late write interface. Register/Register. LVTTL I/Os.. Samples now.	3–264
			MCM69R538	119	(ZP) PBGA	5/6/7/8	Now	Late write interface. Register/Register. 2.5 V I/Os. Samples now.	3–283
			MCM69R539	119	(ZP) PBGA	4.5/5	Now	Late write interface. Register/Register. HSTL I/Os. Dual clock. Samples now.	3–302
			MCM69L536	119	(ZP) PBGA	7.5/8.5/9.5/10.5 Latency	Now	Late write interface. Register/Latch HSTL I/Os. Samples now.	3–324
			MCM69L537	119	(ZP) PBGA	7.5/8.5/9.5/10.5 Latency	Now	Late write interface. Register/Latch LVTTL I/Os. Samples now.	3–343
			MCM69L538	119	(ZP) PBGA	7.5/8.5/9.5/10.5 Latency	Now	Late write interface. Register/Latch 2.5 V I/Os. Samples now.	3–362

SYNCHRONOUS

BurstRAMs™

Description	Organi–zation	V_{CC}	Motorola Part Number	Pin Count	Packaging	Access Time (ns Max)	Pro–duction	Comments	Page #
4M	256K x 18	3.3 V	MCM69P819	100 119	(TQ) TQFP (ZP) PBGA	3.5/3.8/4	Now	Pipelined BurstRAM for servers, switches, and workstations.	4–19
			MCM69F819	100 119	(TQ) TQFP (ZP) PBGA	7.5/8/8.5	Now	Flow–through BurstRAM for servers, switches, and workstations.	4–3
	128K x 36	3.3 V	MCM69P737	100 119	(TQ) TQFP (ZP) PBGA	3.5/3.8/4	Now	Pipelined BurstRAM for servers, switches, and workstations.	4–51
			MCM69F737	100 119	(TQ) TQFP (ZP) PBGA	7.5/8/8.5	Now	Flow–through BurstRAM for servers, switches, and workstations.	4–35
2M	64K x 32	3.3 V	MCM63P631	100	(TQ) TQFP	4.5/7/8	Now	100 MHz pipelined BurstRAM, for desktop PCs and communications applications.	4–67
1M	64K x 18	3.3 V	MCM69F618A	100	(TQ) TQFP	8.5/9/10/12	Now	Flow–through BurstRAM, 3.3 V only. Convert to MCM69F618C.	4–80
			MCM69F618C	100	(TQ) TQFP	8.5/9/10/12	3Q97	5 V tolerant on all pins. 3.3 V core supply. Samples 3Q97.	4–91
			MCM69P618A	100	(TQ) TQFP	4/4.5/5/6/7	Now	Pipelined BurstRAM, 3.3 V only. Convert to MCM69P618C.	4–102
			MCM69P618C	100	(TQ) TQFP	4/4.5/5/6/7	3Q97	5 V tolerant on all pins. 3.3 V core supply. Samples 3Q97.	4–113
		5 V	MCM67B618A	52	(FN) PLCC	9/10/12	Now	Flow–through BurstRAM for Pentium™, MIPS. Convert to MCM69B618C.	4–124
			MCM67C618A	52	(FN) PLCC	5/7	Now	Pipelined BurstRAM for Pentium. Convert to MCM69C618C.	4–133
	32K x 36	3.3 V	MCM69F536A	100	(TQ) TQFP	8.5/9/10/12	Now	Flow–through BurstRAM, 3.3 V only.	4–142
			MCM69F536B	100	(TQ) TQFP	8.5/9/10/12	Now	Flow–through BurstRAM, 5 V tolerant I/Os.	4–153
			MCM69F536C	100	(TQ) TQFP	8.5/9/10/12	3Q97	5 V tolerant on all pins. 3.3 V core supply. Samples 3Q97.	4–164
			MCM69P536A	100	(TQ) TQFP	4/4.5/5/6/7	Now	Pipelined BurstRAM, 3.3 V only.	4–175
			MCM69P536B	100	(TQ) TQFP	4/4.5/5/6/7	Now	Pipelined BurstRAM, 5 V tolerant I/Os.	4–186
			MCM69P536C	100	(TQ) TQFP	4/4.5/5/6/7	3Q97	5 V tolerant on all pins. 3.3 V core supply. Samples 3Q97.	4–197

Tag RAMs

Tag RAMs	64K x 18	3.3 V	MCM69T618	100 119	(TQ) TQFP (ZP) PBGA	5/6/7	Now Now	100 MHz Data/Tag RAM. For MIPS R5000, Pentium Pro and graphics accelerators applications.	5–3
	16K x 16	5 V	MPC27T416	80	(TQ) TQFP	9/10/12	Now	Cache tag RAM for PowerPC. 14 tag bits, 2 status bits.	5–12
	16K x 15	5 V	MPC27T415	80	(TQ) TQFP	9/10/12	Now	Cache tag RAM for PowerPC. 12 tag bits, 3 status bits. Drop in replacement for IDT71216.	5–27

CAMs

CAMs	16K x 64	3.3 V	MCM69C432	100	(TQ) TQFP	180 ns Match Time	2Q97	Content addressable memory for communication applications. 16K connections.	5–42
	4K x 64	3.3 V	MCM69C232	100	(TQ) TQFP	160 ns Match Time	Now	Content addressable memory for communication applications. 4K connections.	5–61

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SYNCHRONOUS

Integrated Cache Solutions

Description	Organi-zation	V_{CC}	Motorola Part Number	Pin Count	Packaging	Access Time (ns Max)	Pro-duction	Comments	Page #
Integrated Cache Solutions	32K x 72	3.3 V	MPC2605	241	(ZP) PBGA	66 MHz	2Q97	Integrated L2 cache for PowerPC processors.One component for 256KB, two for 512KB, and four for 1MB L2 cache solution. Samples 2Q97.	5–80
	32K x 36	5 V	MPC2604GA	357	(ZP) PBGA	66 MHz	Now	Integrated L2 cache for PowerPC processors.Two components for 256KB, four for 512KB L2 cache solution.	5–109

Separate and Dual I/O Devices

4M	512K x 9	5 V	MCM67Q909	86	(ZP) PBGA	5/6	Now	General synchronous separate I/O with write pass through. 3.3 V output levels.	5–137
1M	128K x 9	5 V	MCM67Q709	86	(ZP) PBGA	5/6	Now	General synchronous separate I/O with write pass through. 3.3 V output levels. Replaces the MCM67Q709.	5–147
			MCM67Q709A	86	(ZP) PBGA	5/6	Now	General synchronous separate I/O with write pass through. 3.3 V output levels. Replaces the MCM67Q709.	5–157
	32K x 36	3.3 V	MCM69Q536	176	(TQ) TQFP	6/8/10	2Q97	Single address, separate I/O. NetRAM™ .	5–167
			MCM69D536	176	(TQ) TQFP	6/8/10	2Q97	Dual address, dual I/O. NetRAM.	5–177
	64K x 18	3.3 V	MCM69Q618	100	(TQ) TQFP	6/8/10	2Q97	Single address, separate I/O. NetRAM.	5–190
			MCM69D618	100	(TQ) TQFP	6/8/10	2Q97	Dual address, dual I/O. NetRAM.	5–200
	16K x 16	5 V	MCM62990A	52	EN (PLCC)	15/20/25	Now	For telecom switches and buffers	5–213
Line Buffer	8K x 8	5 V	MCM62X308	28	300 (J) SOJ	15/17	Now	Line buffer for processing digital data.	5–220

ASYNCHRONOUS

Density	Organi-zation	V_{CC}	Motorola Part Number	Pin Count	Packaging Package width in mils	Access Time (ns Max)	Pro-duction	Comments	Page #
4M	512K x 8	5 V	MCM6246	36	400 (WJ) SOJ	17/20/25/35	Now	Output enable. Revolutionary pinout.	2–12
		3.3 V	MCM6946	36 44	400 (WJ) SOJ TSOP	10/12/15	3Q97	For telecom, storage and computing applications. Samples 3Q97.	2–18
	256K x 16	3.3 V	MCM6343	44 44	400 (YJ) SOJ TSOP	10/12/15	1Q98	For telecom, storage and computing applications. Samples 4Q97.	2–3
	1M x 4	5 V	MCM6249	32	400 (WJ) SOJ	20/25/35	Now	Output enable. Revolutionary pinout.	2–28
		3.3 V	MCM6949	32 44	400 (WJ) SOJ TSOP	10/12/15	4Q97	For telecom, storage, and computing applications. Samples 3Q97.	2–34
1M	64K x 18	5 V	MCM67A618A	52	(FN) PLCC	10/12/15	Now	General asynchronous, latched address and data.	2–44
	64K x 16	3.3 V	MCM6323A	44	400 (YJ) SOJ TSOP	10/12/15	4Q97	Industrial temperature offered. DSP applications. Samples 2Q97. Replaces MCM6323.	2–55
	128K x 8	5 V	MCM6226B	32	300 (EJ), 400 (XJ) SOJ	15/17/20/25/35	Now	Evolutionary pinout.	2–64
		5 V	MCM6226BB	32	300 (EJ), 400 (XJ) SOJ	15/17/20/25/35	Now	Evolutionary pinout.	2–70
		5 V	MCM6726B	32	400 (WJ) SOJ	8/10/12	Now	Not recommended for new designs. Suggest MCM6726D.	2–76
		5 V	MCM6726C	32	400 (WJ) SOJ	6/7	Now	Revolutionary pinout.	2–82
		5 V	MCM6726D	32	400 (WJ) SOJ	8/10/12	Now	Revolutionary pinout. Will replace MCM6726B.	2–88
		3.3 V	MCM6926	32	400 (WJ) SOJ	8/10/12/15	Now	Revolutionary pinout.	2–94
		3.3 V	MCM6926A	32	400 (WJ) SOJ	8/10/12/15	3Q97	Revolutionary pinout. Will replace MCM6926. Samples now.	2–101
		3.3 V	MCM6926–C	32	400 (WJ) SOJ	8/10/12/15	3Q97	Revolutionary pinout. Industrial	2–108
	256K x 4	5 V	MCM6229B	28	300 (EJ), 400 (XJ) SOJ	15/17/20/25/35	Now	Evolutionary pinout.	2–115
		5 V	MCM6229BB	28	300 (EJ), 400 (XJ) SOJ	15/17/20/25/35	Now	Evolutionary pinout.	2–121
		5 V	MCM6729B	32	400 (WJ) SOJ	8/10/12	Now	Not recommended for new designs. Suggest MCM6729D.	2–127
		5 V	MCM6729C	32	400 (WJ) SOJ	6/7	Now	Revolutionary pinout.	2–133
		5 V	MCM6729D	32	400 (WJ) SOJ	8/10/12	Now	Revolutionary pinout. Will replace MCM6729B.	2–139
		3.3 V	MCM6929	32	400 (WJ) SOJ	8/10/12/15	Now	Revolutionary pinout.	2–145
		3.3 V	MCM6929A	32	400 (WJ) SOJ	8/10/12/15	3Q97	Revolutionary pinout. Will replace MCM6929. Samples now.	2–152
		3.3 V	MCM6929–C	32	400 (WJ) SOJ	8/10/12/15	3Q97	Revolutionary pinout, Industrial.	2–159
	1M x 1	5 V	MCM6227B	28	300 (J), 400 (WJ) SOJ	15/17/20/25/35	Now	For telecom, IC tester applications, and storage.	2–166

ASYNCHRONOUS

Density	Organi–zation	V_{CC}	Motorola Part Number	Pin Count	Packaging Package width in mils	Access Time (ns Max)	Pro–duction	Comments	Page #
DSPRAM™	8K x 24	5 V	MCM56824A	52	(FN) PLCC	20/25/35	Now	Designed for DSP56001 applications. Replaces 38K x 8s.	2–219
256K	16K x 16	5 V	MCM62996	52	(FN) PLCC	15/20/25	Now	Choice of 5V or 3.3 V power supplies for output buffers. For wide bus applications.	2–172
		5 V	MCM62995A	52	(FN) PLCC	15/20/25	Now	DSP96000 and RISC applications. Latched address inputs.	2–178
	32K x 8	5 V	MCM6206BA	28	300 (EJ) SOJ	12/15/20/25	Now	Replaces MCM6206D.	2–189
		5 V	MCM6706B	28	300 (J) SOJ	8/10/12	Now	Evolutionary pinout.	2–195
		5 V	MCM6706BR	32	300 (J) SOJ	6/7/8	Now	Revolutionary pinout.	2–201
	64K x 4	5 V	MCM6709B	28	300 (J) SOJ	8/10/12	Now	Evolutionary pinout.	2–207
		5 V	MCM6709BR	28	300 (J) SOJ	6/7/8	Now	Revolutionary pinout.	2–213

FAST STATIC RAM MODULES
(Contact Fast Static RAM Marketing for Custom Fast SRAM Modules)

Multichip Modules

Description	Organization	Functionality	Memory Size	Bus Speed (Max)	Pro–duction	Packaging	Motorola Part Number	Page #
Multichip Modules	256K x 72	Flow–Through Burst	16MB	100/117 MHz	3Q97	Flip Chip Multichip Module Laminate	MCM72FB8ML	6–3
		Pipelined Burst	16MB	133/166 MHz	3Q97		MCM72PB8ML	6–3

PowerPC Processor Applications

Description	Chip Set	Functionality	Cache Size	Bus Speed (Max)	Pro–duction	Packaging	Motorola Part Number	Page #
PowerPC Cache Modules with 16K x 15 CacheTag	PowerPC CHRP Platforms	Flow–Through Burst	512KB Cache	66 MHz	Now	178 Pin Card Edge DIMM (DG)	MPC2105B	6–21
		Flow–Through Burst	1MB	66 MHz	Now		MPC2106B	6–21
PowerPC Cache Modules with 16K x 15 CacheTag	PowerPC CHRP Platforms	Pipelined Burst	512KB Cache	Up to 66 MHz	1Q97	178 Pin Card Edge DIMM (DG)	MPC2105P	6–37

Pentium Processor Applications

Description	Organization	Functionality	Cache Size	Bus Speed (Max)	Pro–duction	Packaging	Motorola Part Number	Page #
Coast Modules	64K x 64	Piped Burst 8 Bit TAG	512KB Cache	66 MHz	1Q97	160 Pin Card Edge DIMM (DG)	MCM64PE64	6–51

Networking and Buffer Applications Asynchronous Modules

Description	Organization	Access Time (Max)	Production	Packaging	Comments	Motorola Part Number	Page #
Standard Asynchronous FSRAM Modules	1M x 32	20/25 ns	1Q97	72 Pin SIMM (SG)	Uses eight 1M x 4 SRAMs	MCM321024	6–52
	512K x 32	20/25 ns	1Q97	72 Pin SIMM (SG)	Uses four 512K x 8 SRAMs	MCM32515	6–59

Networking and Buffer Applications Synchronous Modules

Description	Organization	Access Time (Max)	Production	Packaging	Comments	Motorola Part Number	Page #
Standard Synchronous FSRAM Modules	64K x 72 512KB	9/10/12 ns	Now	168 Pin DIMM (DG)	Flow–through synchronous BurstRAM	MCM72F6DG	6–85
	128K x 32 1 MB	9/10/12 ns	Now	168 Pin DIMM (DG)	Flow–through synchronous BurstRAM	MCM72F7DG	6–85
	512K x 72 2MB	8/9/12 ns	Now	168 Pin DIMM (DG)	Flow–through synchronous BurstRAM	MCM72F8DG	6–75
	1M x 72 4 MB	8/9/12 ns	Now	168 Pin DIMM (DG)	Flow–through synchronous BurstRAM	MCM72F9DG	6–75
	2M x 72 8 MB	8/9/12 ns	Now	168 Pin DIMM (DG)	Flow–through synchronous BurstRAM	MCM72F10DG	6–66

2

Asynchronous Fast SRAMs

256K x 16
3.3 V MCM6343 2–3

512K x 8
5 V MCM6246 2–12
3.3 V MCM6946 2–18

1M x 4
5 V MCM6249 2–28
3.3 V MCM6949 2–34

64K x 18
5 V MCM67A618A 2–44

64K x 16
3.3 V MCM6323A 2–55

128K x 8
5 V MCM6226B 2–64
5 V MCM6226BB 2–70
5 V MCM6726B 2–76
5 V MCM6726C 2–82
5 V MCM6726D 2–88
3.3 V MCM6926 2–94
3.3 V MCM6926A 2–101
3.3 V MCM6926–C 2–108

256K x 4
5 V MCM6229B 2–115
5 V MCM6229BB 2–121
5 V MCM6729B 2–127
5 V MCM6729C 2–133
5 V MCM6729D 2–139
3.3 V MCM6929 2–145
3.3 V MCM6929A 2–152
3.3 V MCM6929–C 2–159

1M x 1
5 V MCM6227B 2–166

16K x 16
5 V MCM62996 2–172
5 V MCM62995A 2–178

32K x 8
5V MCM6206BA 2–189
5 V MCM6706B 2–195
5 V MCM6706BR 2–201

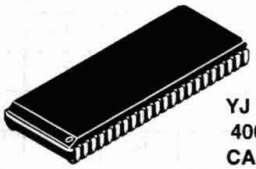
64K x 4
5 V MCM6709B 2–207
5 V MCM6709BR 2–213

8K x 24
5 V MCM56824A 2–219

MCM6343

Product Preview

256K x 16 Bit 3.3 V Asynchronous Fast Static RAM



YJ PACKAGE
400 MIL SOJ
CASE 919–01

TS PACKAGE
TSOP TYPE II
CASE 924A–01

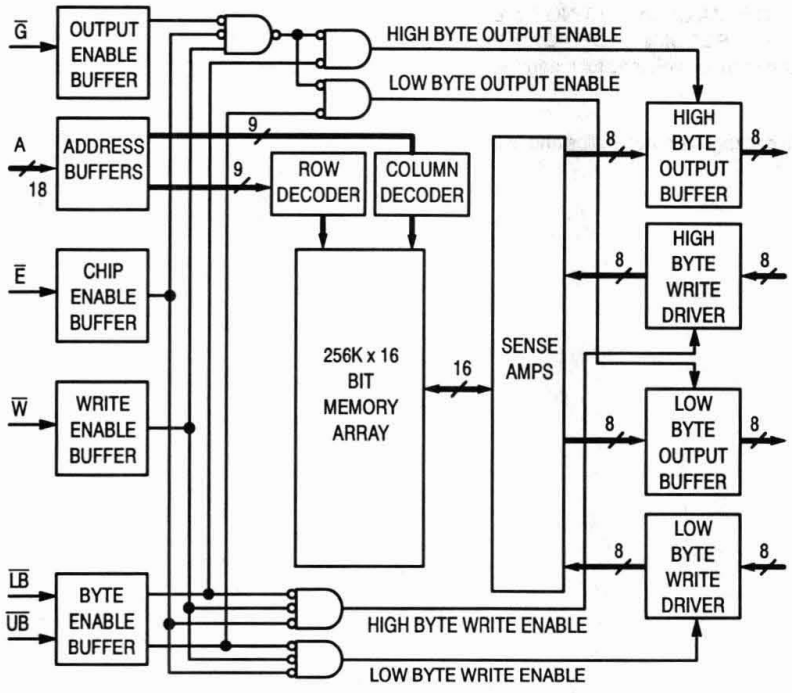
The MCM6343 is a 4,194,304 bit static random access memory organized as 262,144 words of 16 bits. Static design eliminates the need for external clocks or timing strobes.

The MCM6343 is equipped with chip enable ($\overline{E}$), write enable ($\overline{W}$), and output enable ($\overline{G}$) pins, allowing for greater system flexibility and eliminating bus contention problems. Separate byte enable controls ($\overline{LB}$ and $\overline{UB}$) allow individual bytes to be written and read. $\overline{LB}$ controls the lower bits DQ0 to DQ7, while $\overline{UB}$ controls the upper bits DQ8 to DQ15.

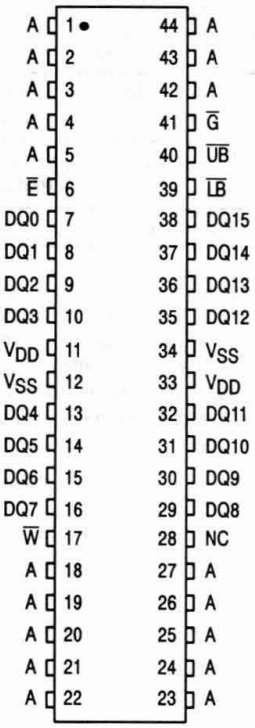
The MCM6343 is available in a 400 mil, 44–lead small–outline SOJ package and a 44–lead TSOP Type II package.

- Single 3.3 V ± 0.3 V Power Supply
- Fast Access Time: 10/12/15 ns
- Equal Address and Chip Enable Access Time
- All Inputs and Outputs are TTL Compatible
- Data Byte Control
- Fully Static Operation
- Power Operation: 250/240/230 mA Maximum, Active AC
- Commercial and Standard Industrial Temperature Option: – 40 to + 85°C

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

A0 – A17	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{UB}$	Upper Byte
$\overline{LB}$	Lower Byte
DQ0 – DQ15	Data Input/Output
V_{DD}	+ 3.3 V Power Supply
V_{SS}	Ground
NC	No Connection

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

REV 1
3/4/97

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{LB}$	$\overline{UB}$	Mode	V_{DD} Current	DQ0 – DQ7	DQ8 – DQ15
H	X	X	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	High–Z
L	H	H	X	X	Output Disabled	I_{DDA}	High–Z	High–Z
L	X	X	H	H	Output Disabled	I_{DDA}	High–Z	High–Z
L	L	H	L	H	Low Byte Read	I_{DDA}	D_{out}	High–Z
L	L	H	H	L	High Byte Read	I_{DDA}	High–Z	D_{out}
L	L	H	L	L	Word Read	I_{DDA}	D_{out}	D_{out}
L	X	L	L	H	Low Byte Write	I_{DDA}	D_{in}	High–Z
L	X	L	H	L	High Byte Write	I_{DDA}	High–Z	D_{in}
L	X	L	L	L	Word Write	I_{DDA}	D_{in}	D_{in}

ABSOLUTE MAXIMUM RATINGS (See Notes)

Rating		Symbol	Value	Unit
Supply Voltage		V_{DD}	– 0.5 to + 4.6	V
Voltage on Any Pin		V_{in}	– 0.5 to V_{DD} + 0.5	V
Output Current per Pin		I_{out}	± 20	mA
Package Power Dissipation		P_D	TBD	W
Temperature Under Bias	Commercial Industrial	T_{bias}	– 10 to + 85 – 45 to + 90	°C
Operating Temperature	Commercial Industrial	T_A	0 to + 70 – 45 to + 85	°C
Storage Temperature		T_{stg}	– 55 to + 150	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. All voltages are referenced to V_{SS}.
3. Power dissipation capability will be dependent upon package characteristics and use environment.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V ± 0.3 V, T_A = 0 to 70°C, Unless Otherwise Noted)
(T_A = – 40 to + 85°C for Industrial Temperature Offering)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{DD} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{DD} + 0.3 V dc; V_{IH} (max) = V_{DD} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{DD})		$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{DD})		$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage	(I_{OL} = + 4.0 mA) (I_{OL} = + 100 µA)	V_{OL}	—	0.4 V_{SS} + 0.2	V
Output High Voltage	(I_{OH} = – 4.0 mA) (I_{OH} = – 100 µA)	V_{OH}	2.4 V_{DD} – 0.2	—	V

POWER SUPPLY CURRENTS

Parameter		Symbol	0 to 70°C	– 40 to + 85°C	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max)	MCM6343–10: t_{AVAV} = 10 ns MCM6343–12: t_{AVAV} = 12 ns MCM6343–15: t_{AVAV} = 15 ns	I_{CC}	250 240 230	260 250 240	mA
AC Standby Current (V_{CC} = max, $\overline{E}$ = V_{IH}, No other restrictions on other inputs)	MCM6343–10: t_{AVAV} = 10 ns MCM6343–12: t_{AVAV} = 12 ns MCM6343–15: t_{AVAV} = 15 ns	I_{SB1}	50 50 45	55 55 50	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V) (V_{CC} = max, f = 0 MHz)		I_{SB2}	5	5	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V ± 0.3 V, T_A = 0 to + 70°C, Unless Otherwise Noted)
(T_A = – 40 to + 85°C for Industrial Temperature Offering)

Logic Input Timing Measurement Reference Level ..... 1.50 V
Logic Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

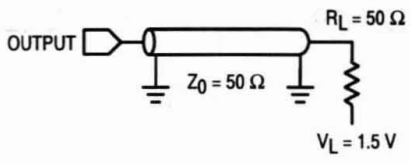
Output Timing Reference Level ..... 1.50 V
Output Load ..... See Figure 1

2

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM6343–10		MCM6343–12		MCM6343–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	10	—	12	—	15	—	ns	3
Address Access Time	t_{AVQV}	—	10	—	12	—	15	ns	
Enable Access Time	t_{ELQV}	—	10	—	12	—	15	ns	4
Output Enable Access Time	t_{GLQV}	—	5	—	6	—	7	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	3	—	3	—	3	—	ns	5, 6, 7
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	5, 6, 7
Enable High to Output High–Z	t_{EHQZ}	0	5	0	6	0	7	ns	5, 6, 7
Output Enable High to Output High–Z	t_{GHQZ}	0	5	0	6	0	7	ns	5, 6, 7
Byte Enable Access Time	t_{BLQV}	—	5	—	6	—	7	ns	
Byte Enable Low to Output Active	t_{BLQX}	0	—	0	—	0	—	ns	5, 6, 7
Byte High to Output High–Z	t_{BHQZ}	0	5	0	6	0	7	ns	5, 6, 7

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
6. Transition is measured ± 200 mV from steady–state voltage.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E} \le V_{IL}$, $\overline{G} \le V_{IL}$).

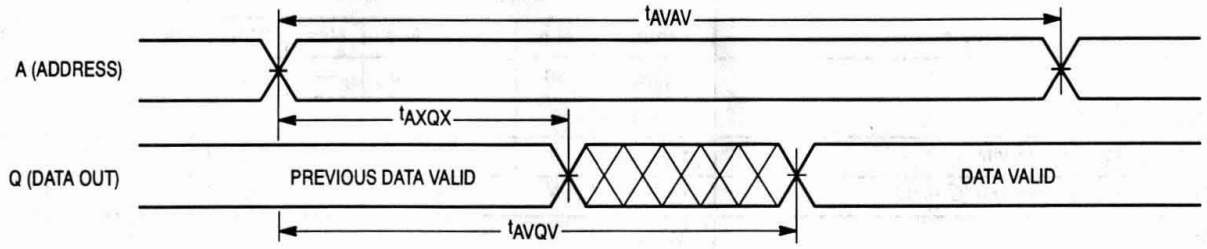


TIMING LIMITS

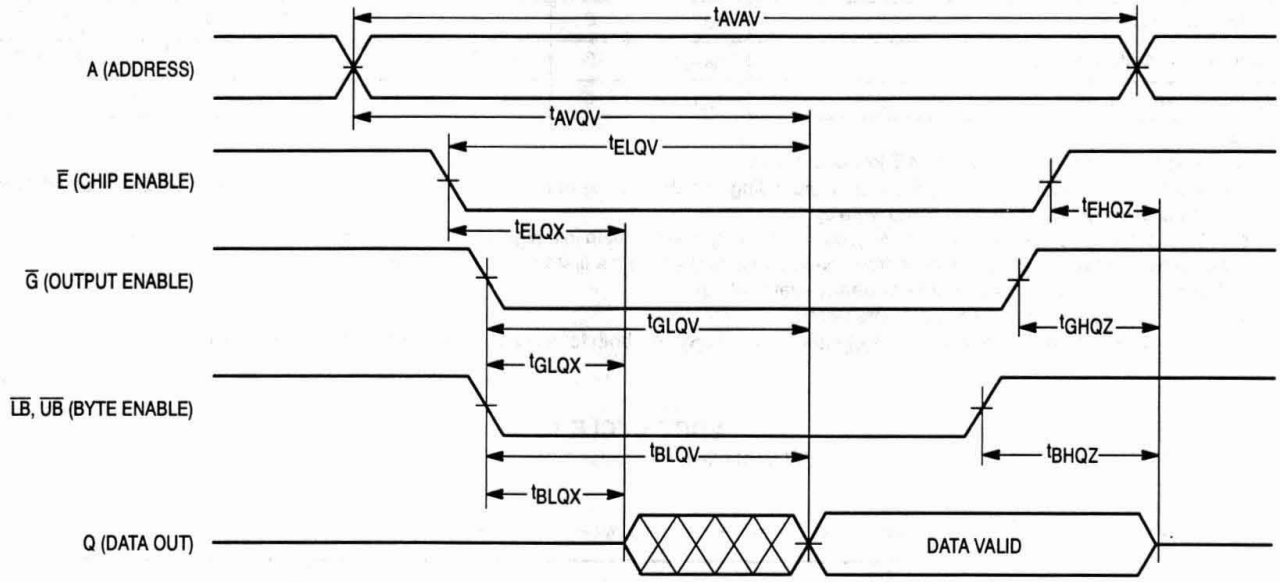
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Figure 1. AC Test Load

READ CYCLE 1 (See Note 8)



READ CYCLE 2 (See Note 4)

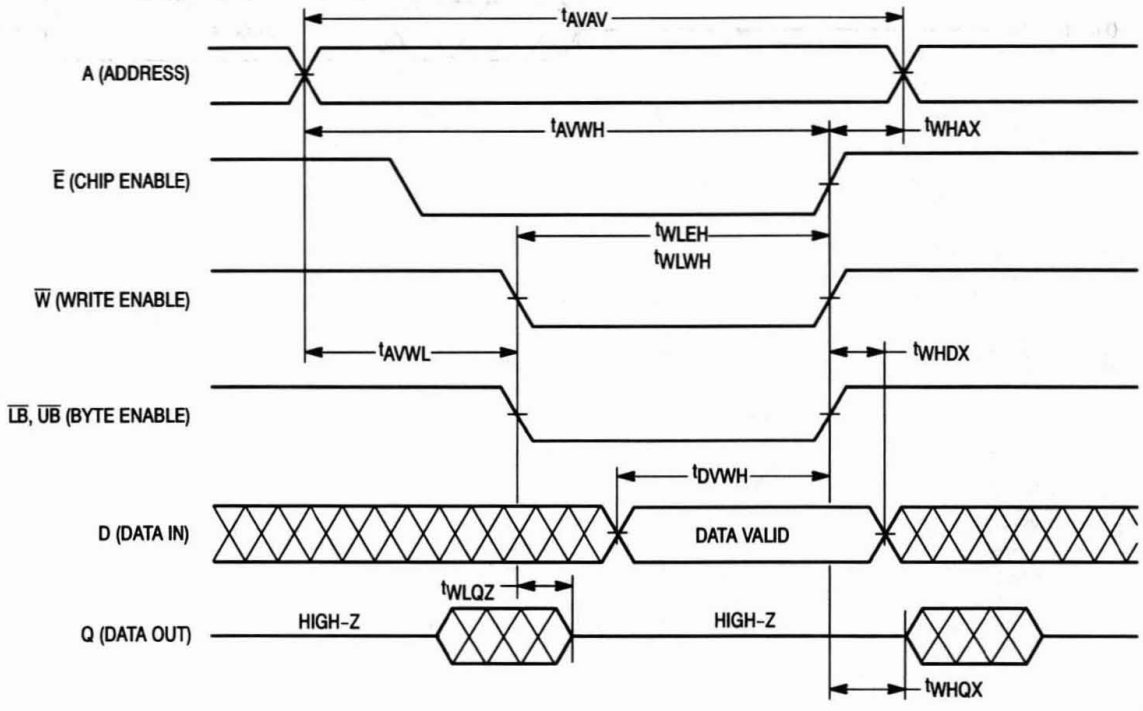


WRITE CYCLE 1 ($\overline{W}$ Controlled; See Notes 1, 2, and 3)

Parameter	Symbol	MCM6343–10		MCM6343–12		MCM6343–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	10	—	12	—	15	—	ns	4
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	9	—	10	—	12	—	ns	
Address Valid to End of Write ($\overline{G}$ High)	t_{AVWH}	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	9	—	10	—	12	—	ns	
Write Pulse Width ($\overline{G}$ High)	t_{WLWH} t_{WLEH}	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	5	—	6	—	7	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	5	0	6	0	7	ns	5, 6, 7
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	5, 6, 7
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
4. All write cycle timings are referenced from the last valid address to the first transitioning address.
5. Transition is measured ± 200 mV from steady–state voltage.
6. This parameter is sampled and not 100% tested.
7. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1
($\overline{W}$ Controlled; See Notes 1, 2, and 3)

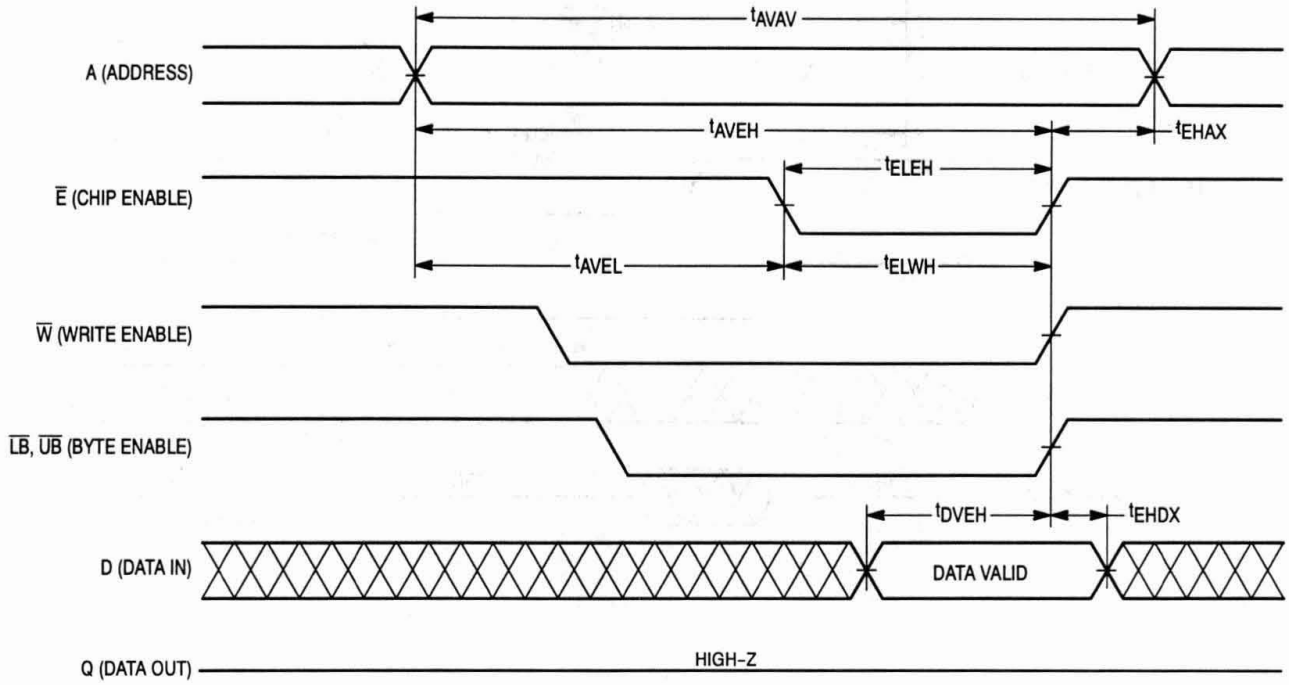


WRITE CYCLE 2 ($\overline{E}$ Controlled; See Notes 1, 2, and 3)

Parameter	Symbol	MCM6343–10		MCM6343–12		MCM6343–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	10	—	12	—	15	—	ns	4
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	9	—	10	—	12	—	ns	
Address Valid to End of Write ($\overline{G}$ High)	t_{AVEH}	8	—	9	—	10	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	9	—	10	—	12	—	ns	5, 6
Enable to End of Write ($\overline{G}$ High)	t_{ELEH}, t_{ELWH}	8	—	9	—	10	—	ns	5, 6
Data Valid to End of Write	t_{DVEH}	5	—	6	—	7	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2
($\overline{E}$ Controlled; See Notes 1, 2, and 3)

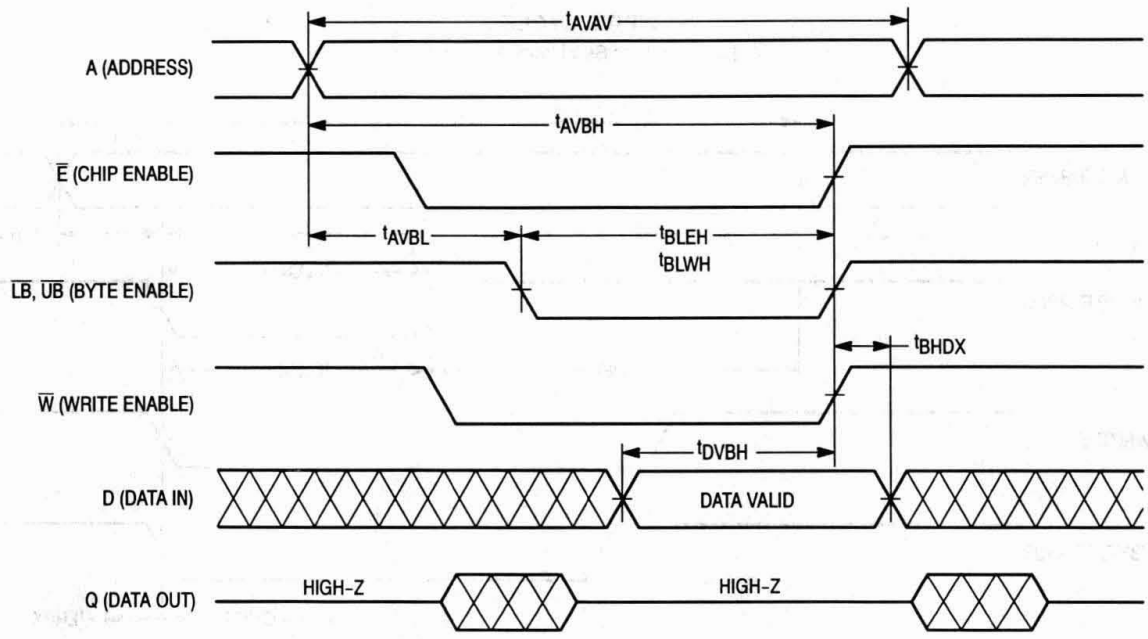


WRITE CYCLE 3 ($\overline{E}$ Controlled; See Notes 1, 2, and 3)

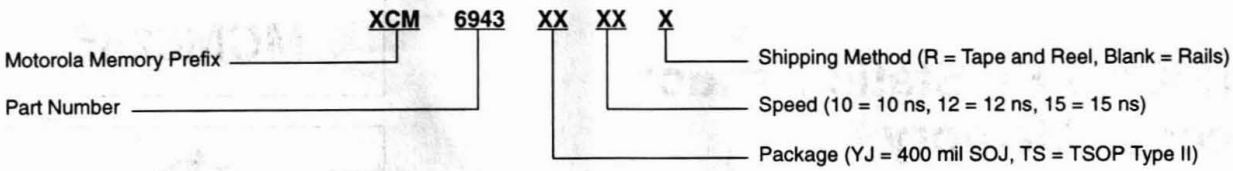
Parameter	Symbol	MCM6343–10		MCM6343–12		MCM6343–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	10	—	12	—	15	—	ns	4
Address Setup Time	t_{AVBL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVBH}	9	—	10	—	12	—	ns	
Address Valid to End of Write ($\overline{G}$ High)	t_{AVBH}	8	—	9	—	10	—	ns	
Byte Pulse Width	t_{BLWH} t_{BLEH}	9	—	10	—	12	—	ns	
Byte Pulse Width ($\overline{G}$ High)	t_{BLWH} t_{BLEH}	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVBH}	5	—	6	—	7	—	ns	
Data Hold Time	t_{BHDX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
4. All write cycle timings are referenced from the last valid address to the first transitioning address.

WRITE CYCLE 3
($\overline{E}$ Controlled; See Notes 1, 2, and 3)



ORDERING INFORMATION
(Order by Full Part Number)


XCM 6943 XX XX X
Motorola Memory Prefix
Part Number
Shipping Method (R = Tape and Reel, Blank = Rails)
Speed (10 = 10 ns, 12 = 12 ns, 15 = 15 ns)
Package (YJ = 400 mil SOJ, TS = TSOP Type II)

2

Full Commercial Part Numbers —	MCM6343YJ10	MCM6343YJ10R	MCM6343TS10
	MCM6343YJ12	MCM6343YJ12R	MCM6343TS12
	MCM6343YJ15	MCM6343YJ15R	MCM6343TS15
Full Industrial Part Numbers —	SCM6343YJ10A	SCM6343YJ10AR	SCM6343TS10A*
	SCM6343YJ12A	SCM6343YJ12AR	SCM6343TS12A*
	SCM6343YJ15A	SCM6343YJ15AR	SCM6343TS15A*

* Not available in Tape and Reel.

MCM6246

2

512K x 8 Bit Static Random Access Memory

WJ PACKAGE
400 MIL SOJ
CASE 893–01

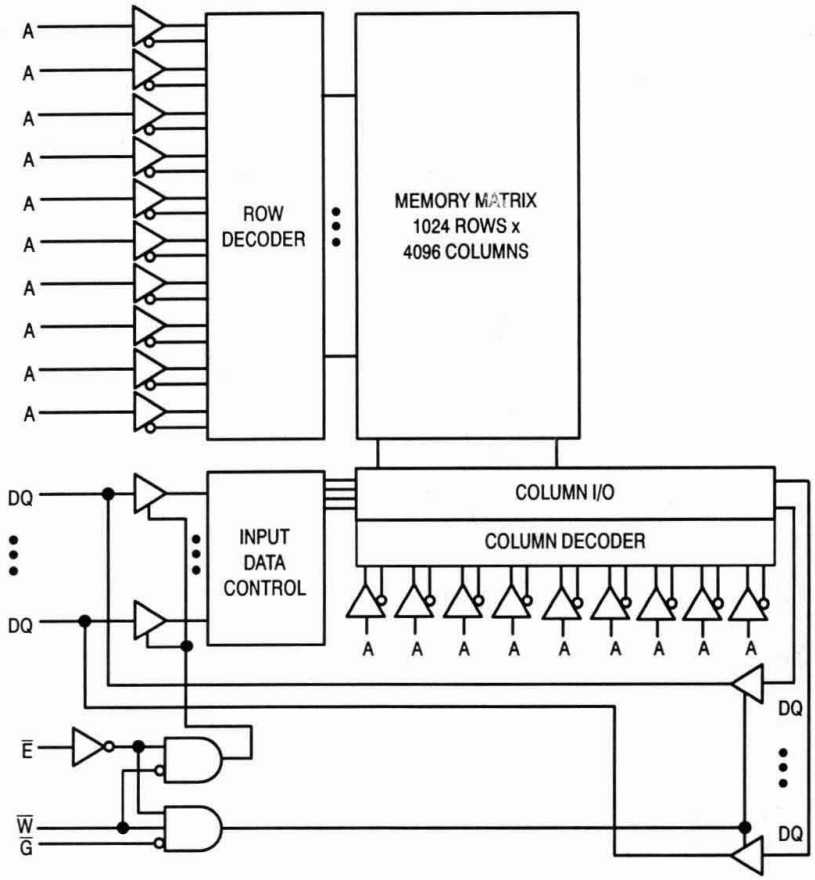
The MCM6246 is a 4,194,304 bit static random access memory organized as 524,288 words of 8 bits. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6246 is equipped with chip enable ($\overline{E}$) and output enable ($\overline{G}$) pins, allowing for greater system flexibility and eliminating bus contention problems. Either input, when high, will force the outputs into high impedance.

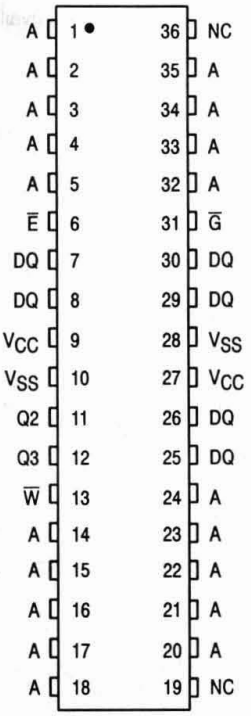
The MCM6246 is available in a 400 mil, 36–lead surface–mount SOJ package.

- Single 5 V ± 10% Power Supply
- Fast Access Time: 17/20/25/35 ns
- Equal Address and Chip Enable Access Time
- All Inputs and Outputs are TTL Compatible
- Three–State Outputs
- Power Operation: 205/200/185/170 mA Maximum, Active AC

BLOCK DIAGRAM



PIN ASSIGNMENT


A 1 36 NC
A 2 35 A
A 3 34 A
A 4 33 A
A 5 32 A
$\overline{E}$ 6 31 $\overline{G}$
DQ 7 30 DQ
DQ 8 29 DQ
V_{CC} 9 28 V_{SS}
V_{SS} 10 27 V_{CC}
Q2 11 26 DQ
Q3 12 25 DQ
$\overline{W}$ 13 24 A
A 14 23 A
A 15 22 A
A 16 21 A
A 17 20 A
A 18 19 NC

PIN NAMES

A	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
DQ	Data Input/Output
NC	No Connection
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

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10/9/96

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	Not Selected	High–Z	—	I_{SB1}, I_{SB2}
L	H	H	Output Disabled	High–Z	—	I_{CCA}
L	L	H	Read	D_{out}	Read	I_{CCA}
L	X	L	Write	High–Z	Write	I_{CCA}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns).

** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 2.0 ns).

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter		Symbol	Min	Typ	Max	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max)	MCM6246–17: t_{AVAV} = 17 ns	I_{CC}	—	—	205	mA
	MCM6246–20: t_{AVAV} = 20 ns		—	185	200	
	MCM6246–25: t_{AVAV} = 25 ns		—	170	185	
	MCM6246–35: t_{AVAV} = 35 ns		—	155	170	
AC Standby Current (V_{CC} = max, $\overline{E}$ = V_{IH}, No other restrictions on other inputs)	MCM6246–17: t_{AVAV} = 17 ns	I_{SB1}	—	55	60	mA
	MCM6246–20: t_{AVAV} = 20 ns		—	55	60	
	MCM6246–25: t_{AVAV} = 25 ns		—	45	50	
	MCM6246–35: t_{AVAV} = 35 ns		—	35	40	
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V) (V_{CC} = max, f = 0 MHz)		I_{SB2}	—	10	15	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except Clocks and DQs $\overline{E}$, $\overline{G}$, $\overline{W}$	C_{in} C_{ck}	4 5	6 8	pF
Input/Output Capacitance	DQ	$C_{I/O}$	5	8	pF

2

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1a

READ CYCLE TIMING (See Note 1)

Parameter	Symbol	MCM6246–17		MCM6246–20		MCM6246–25		MCM6246–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	17	—	20	—	25	—	35	—	ns	2, 3
Address Access Time	t_{AVQV}	—	17	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	—	17	—	20	—	25	—	35	ns	4
Output Enable Access Time	t_{GLQV}	—	6	—	6	—	8	—	10	ns	
Output Hold from Address Change	t_{AXQX}	5	—	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	5	—	5	—	5	—	ns	5, 6, 7
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	ns	5, 6, 7
Enable High to Output High–Z	t_{EHQZ}	—	8	—	8	—	10	—	12	ns	5, 6, 7
Output Enable High to Output High–Z	t_{GHQZ}	—	8	—	8	—	10	—	12	ns	5, 6, 7
Power Up Time	t_{ELICCH}	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	—	17	—	20	—	25	—	35	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low/$\overline{E}$ going high.
5. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1b.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E} \le V_{IL}$, $\overline{G} \le V_{IL}$).

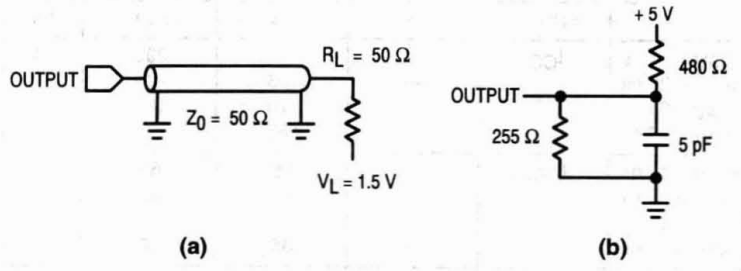
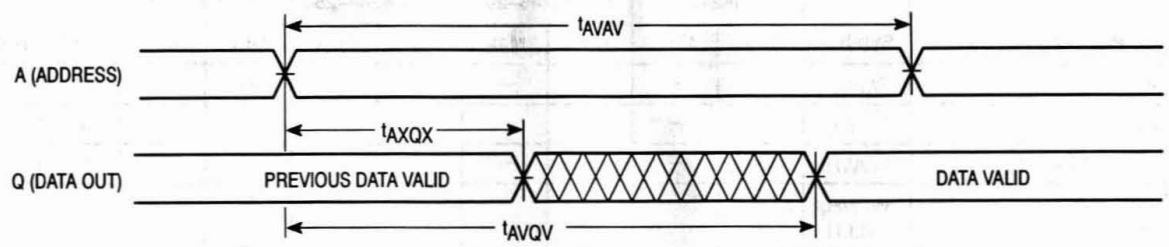


Figure 1. AC Test Loads

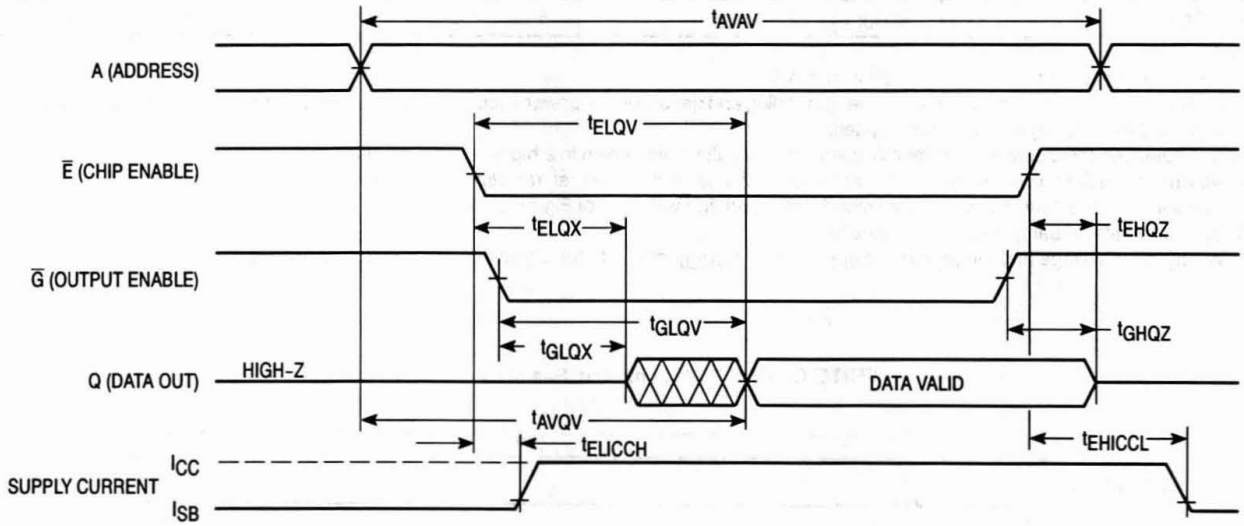
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 8)



READ CYCLE 2 (See Note)



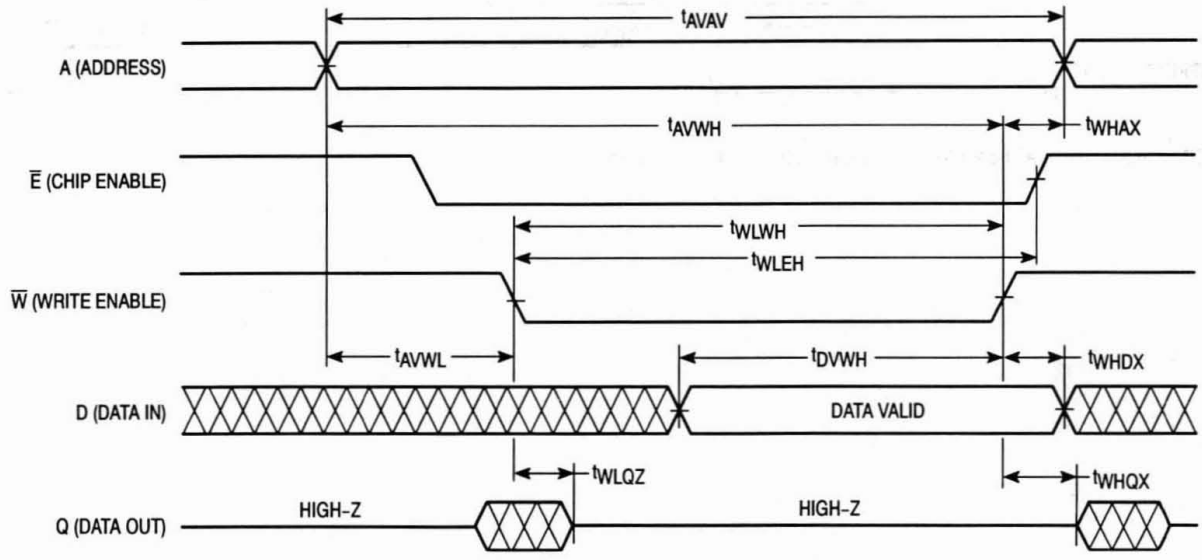
NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low/ $\overline{E}$ going high.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	MCM6246–17		MCM6246–20		MCM6246–25		MCM6246–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	17	—	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	14	—	14	—	17	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	13	—	13	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVWH}	10	—	10	—	10	—	15	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	9	0	9	0	10	0	15	ns	5,6,7
Write High to Output Active	t_{WHQX}	5	—	5	—	5	—	5	—	ns	5,6,7
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
4. All write cycle timings are referenced from the last valid address to the first transitioning address.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1b.
6. This parameter is sampled and not 100% tested.
7. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

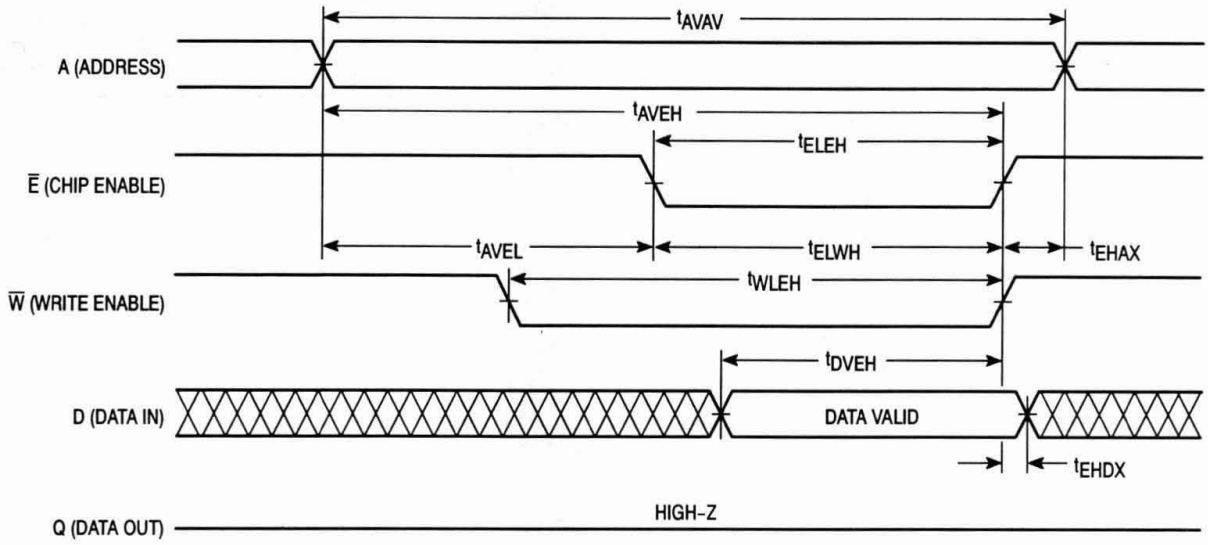


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	MCM6246–17		MCM6246–20		MCM6246–25		MCM6246–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	17	—	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	14	—	14	—	17	—	20	—	ns	
Enable Pulse Width	t_{ELEH}, t_{ELWH}	14	—	14	—	17	—	20	—	ns	5,6
Write Pulse Width	t_{WLEH}	14	—	14	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	9	—	10	—	10	—	15	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, and 3)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6246 XX XX XX

- Motorola Memory Prefix
- Part Number
- Package (WJ = 400 mil SOJ)
- Speed (17 = 17 ns, 20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
- Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6246WJ17 MCM6246WJ17R2
MCM6246WJ20 MCM6246WJ20R2
MCM6246WJ25 MCM6246WJ25R2
MCM6246WJ35 MCM6246WJ35R2

MCM6946

2

Product Preview

512K x 8 Bit Static Random Access Memory

The MCM6946 is a 4,194,304 bit static random access memory organized as 524,288 words of 8 bits. Static design eliminates the need for external clocks or timing strobes.

The MCM6946 is equipped with chip enable ($\overline{E}$) and output enable ($\overline{G}$) pins, allowing for greater system flexibility and eliminating bus contention problems. Either input, when high, will force the outputs into high impedance.

The MCM6946 is available in a 400 mil, 36–lead surface–mount SOJ package and a 44–lead TSOP Type II package.

- Single 3.3 V ± 10% Power Supply
- Fast Access Time: 10/12/15 ns
- Equal Address and Chip Enable Access Time
- All Inputs and Outputs are TTL Compatible
- Three–State Outputs
- Power Operation: 185/180/175 mA Maximum, Active AC
- Commercial and Standard Industrial Temperature Option: – 40 to + 85°C

YJ PACKAGE
400 MIL SOJ
CASE 893–01

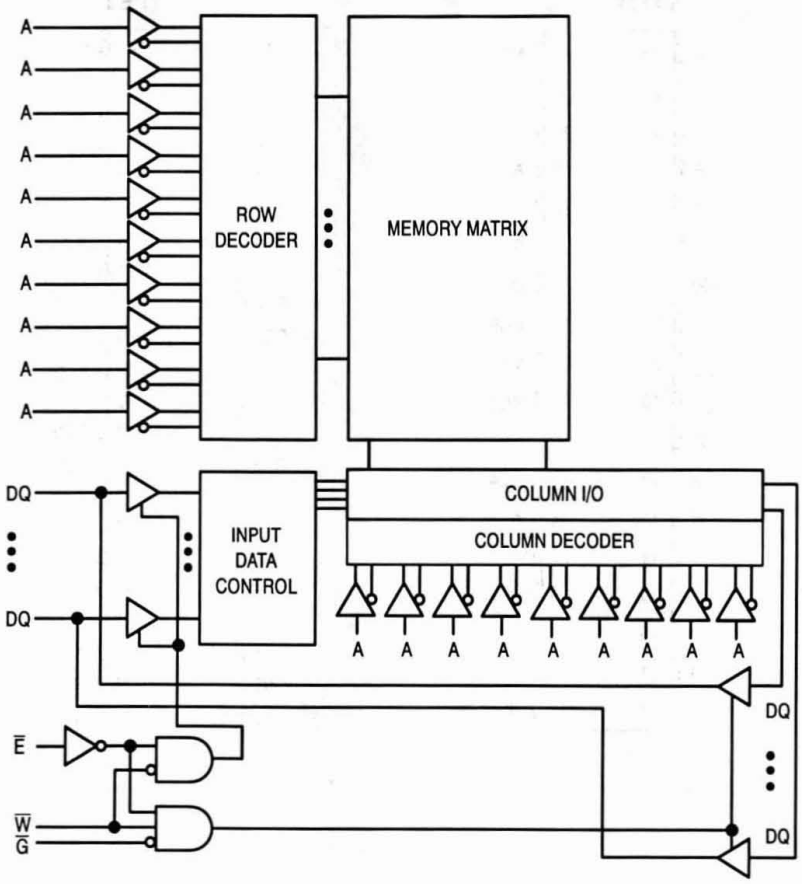
TS PACKAGE
TSOP TYPE II
CASE 924A–01

PIN NAMES	
A0 – A18	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
DQ0 – DQ7	Data Input/Output
NC	No Connection
V_{CC}	+ 3.3 V Power Supply
V_{SS}	Ground

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

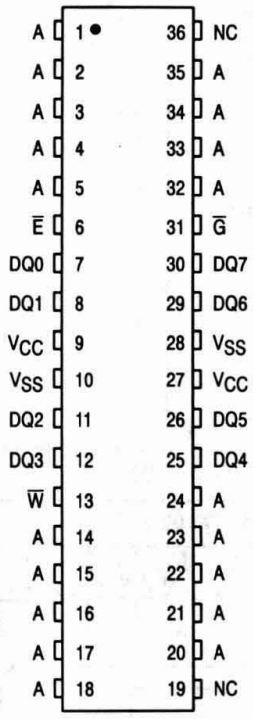
REV 2
3/4/97

BLOCK DIAGRAM

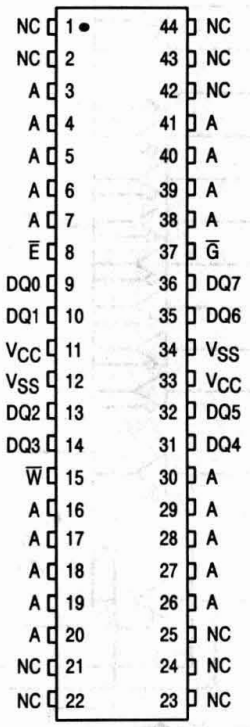


PIN ASSIGNMENTS

400 MIL SOJ



TSOP TYPE II



TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	Not Selected	High–Z	—	I_{SB1}, I_{SB2}
L	H	H	Output Disabled	High–Z	—	I_{CCA}
L	L	H	Read	D_{out}	Read	I_{CCA}
L	X	L	Write	High–Z	Write	I_{CCA}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating		Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}		V_{CC}	– 0.5 to + 5.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}		V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)		I_{out}	± 20	mA
Power Dissipation		P_D	1.0	W
Temperature Under Bias	Commercial Industrial	T_{bias}	– 10 to + 85 – 45 to + 90	°C
Operating Temperature	Commercial Industrial	T_A	0 to + 70 – 45 to + 85	°C
Storage Temperature — Plastic		T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)
(T_A = – 40 to + 85°C for Industrial Temperature Offering)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	3.0	3.0	3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns).
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 2.0 ns).

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter		Symbol	0 to 70°C	– 40 to + 85°C	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max)	MCM6946–10: t_{AVAV} = 10 ns	I_{CC}	185	195	mA
	MCM6946–12: t_{AVAV} = 12 ns		180	190	
	MCM6946–15: t_{AVAV} = 15 ns		175	185	
AC Standby Current (V_{CC} = max, $\overline{E}$ = V_{IH}, No other restrictions on other inputs)	MCM6946–10: t_{AVAV} = 10 ns	I_{SB1}	50	55	mA
	MCM6946–12: t_{AVAV} = 12 ns		50	55	
	MCM6946–15: t_{AVAV} = 15 ns		45	50	
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V) (V_{CC} = max, f = 0 MHz)		I_{SB2}	5	5	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except Clocks and DQs	C_{in}	4	6	pF
	$\overline{E}$, $\overline{G}$, $\overline{W}$	C_{ck}	5	8	
Input/Output Capacitance	DQ	$C_{I/O}$	5	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)
(T_A = – 40 to + 85°C for Industrial Temperature Offering)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM6946–10		MCM6946–12		MCM6946–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	10	—	12	—	15	—	ns	3
Address Access Time	t_{AVQV}	—	10	—	12	—	15	ns	
Enable Access Time	t_{ELQV}	—	10	—	12	—	15	ns	4
Output Enable Access Time	t_{GLQV}	—	5	—	6	—	7	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	3	—	3	—	3	—	ns	5, 6, 7
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	5, 6, 7
Enable High to Output High–Z	t_{EHQZ}	0	5	0	6	0	7	ns	5, 6, 7
Output Enable High to Output High–Z	t_{GHQZ}	0	5	0	6	0	7	ns	5, 6, 7

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
6. Transition is measured ± 200 mV from steady–state voltage.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E} \le V_{IL}$, $\overline{G} \le V_{IL}$).

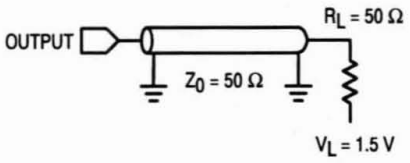
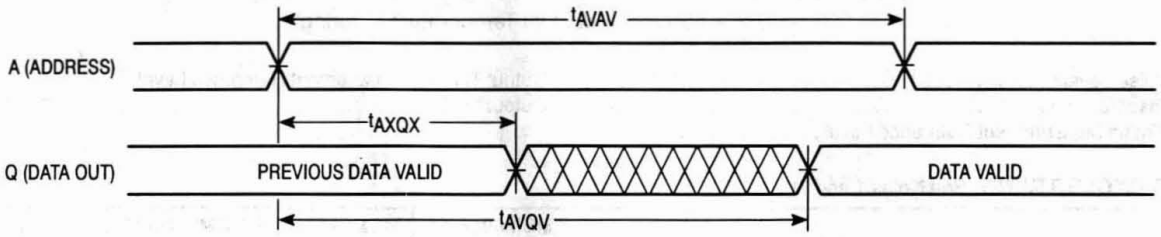


Figure 1. AC Test Load

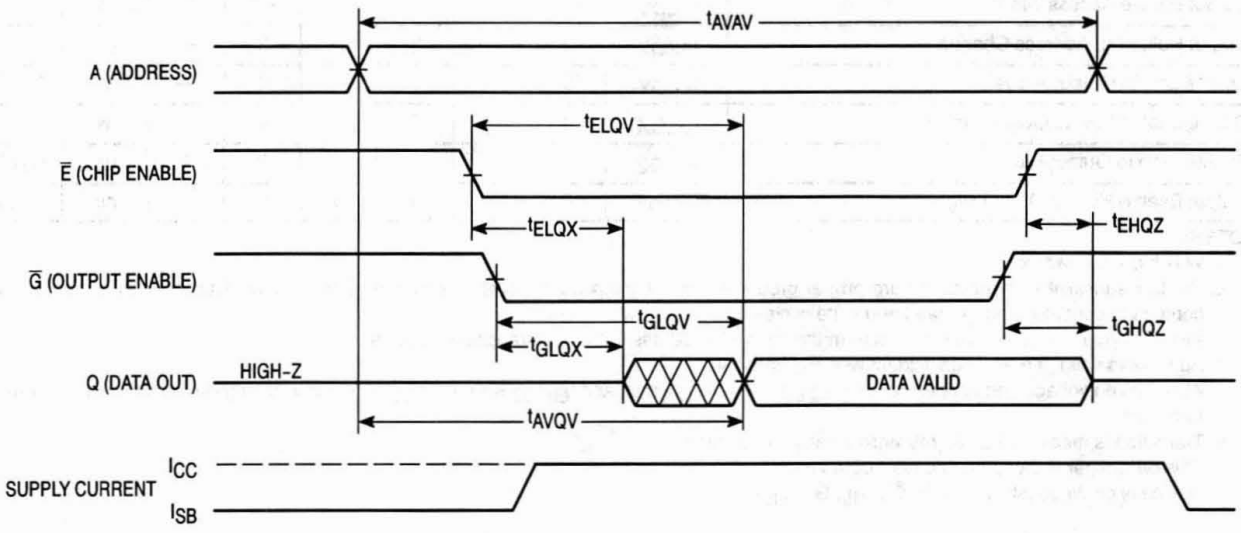
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 8)



READ CYCLE 2 (See Note 4)

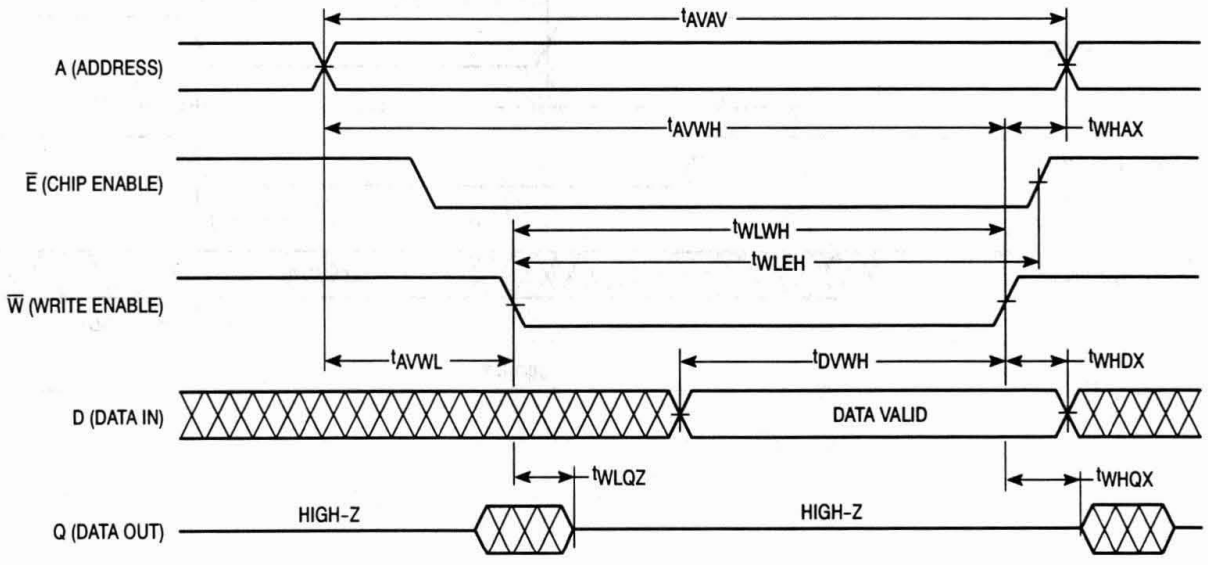


WRITE CYCLE 1 ($\overline{W}$ Controlled; See Notes 1, 2, and 3)

Parameter	Symbol	MCM6946–10		MCM6946–12		MCM6946–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	10	—	12	—	15	—	ns	4
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	9	—	10	—	12	—	ns	
Address Valid to End of Write ($\overline{G}$ High)	t_{AVWH}	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	9	—	10	—	12	—	ns	
Write Pulse Width ($\overline{G}$ High)	t_{WLWH} t_{WLEH}	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	5	—	6	—	7	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	5	0	6	0	7	ns	5, 6, 7
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	5, 6, 7
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
4. All write cycle timings are referenced from the last valid address to the first transitioning address.
5. Transition is measured ± 200 mV from steady–state voltage.
6. This parameter is sampled and not 100% tested.
7. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled; See Notes 1, 2, and 3)

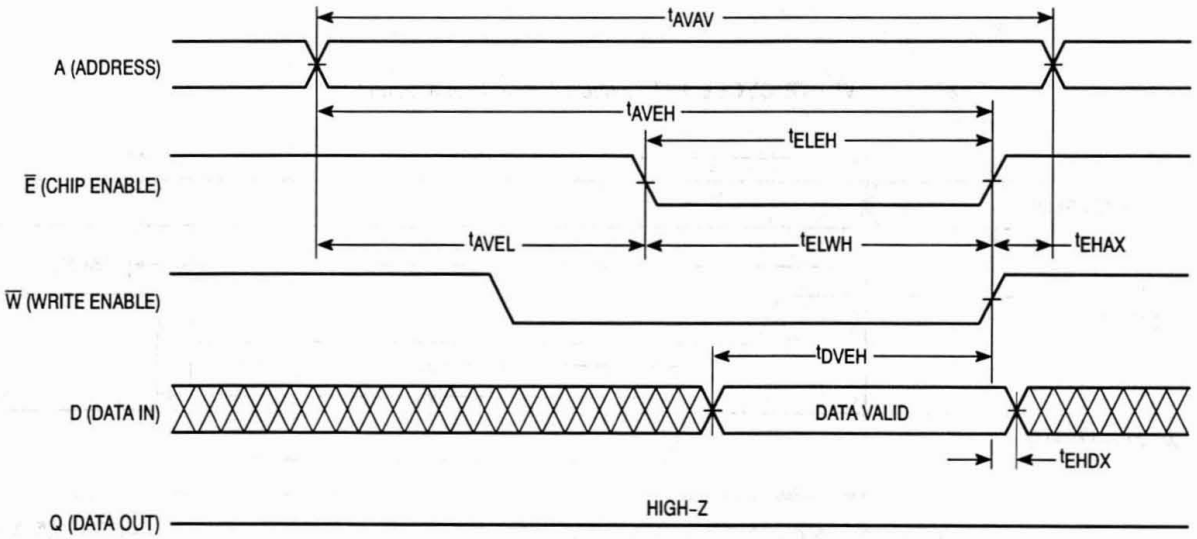


WRITE CYCLE 2 ($\overline{E}$ Controlled; See Notes 1, 2, and 3)

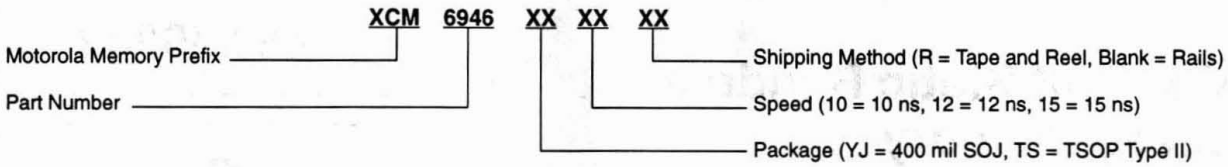
Parameter	Symbol	MCM6946–10		MCM6946–12		MCM6946–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	10	—	12	—	15	—	ns	4
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	9	—	10	—	12	—	ns	
Address Valid to End of Write ($\overline{G}$ High)	t_{AVEH}	8	—	9	—	10	—	ns	
Enable Pulse Width	t_{ELEH}, t_{ELWH}	9	—	10	—	12	—	ns	5, 6
Enable Pulse Width ($\overline{G}$ High)	t_{ELEH}, t_{ELWH}	8	—	9	—	10	—	ns	5, 6
Data Valid to End of Write	t_{DVEH}	5	—	6	—	7	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2 ($\overline{E}$ Controlled; See Notes 1, 2, and 3)



ORDERING INFORMATION
(Order by Full Part Number)


XCM 6946 XX XX XX
Motorola Memory Prefix
Part Number
Shipping Method (R = Tape and Reel, Blank = Rails)
Speed (10 = 10 ns, 12 = 12 ns, 15 = 15 ns)
Package (YJ = 400 mil SOJ, TS = TSOP Type II)

2

Full Commercial Part Numbers —	MCM6946YJ10	MCM6946YJ10R	MCM6946TS10
	MCM6946YJ12	MCM6946YJ12R	MCM6946TS12
	MCM6946YJ15	MCM6946YJ15R	MCM6946TS15
Full Industrial Part Numbers —	SCM6946YJ10A	SCM6946YJ10AR	SCM6946TS10A*
	SCM6946YJ12A	SCM6946YJ12AR	SCM6946TS12A*
	SCM6946YJ15A	SCM6946YJ15AR	SCM6946TS15A*

* Not available in Tape and Reel.

MCM6249

2

1M x 4 Bit Static Random Access Memory

WJ PACKAGE
400 MIL SOJ
CASE 857A–02

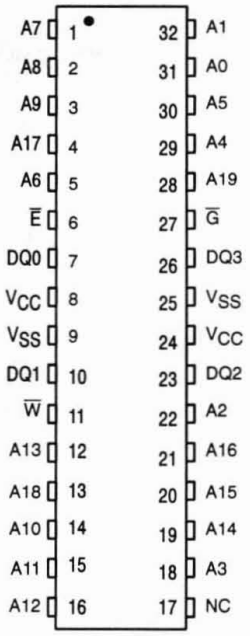
The MCM6249 is a 4,194,304 bit static random access memory organized as 1,048,576 words of 4 bits, fabricated using high–performance silicon–gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6249 is equipped with chip enable ($\overline{E}$) and output enable ($\overline{G}$) pins, allowing for greater system flexibility and eliminating bus contention problems. Either input, when high, will force the outputs into high impedance.

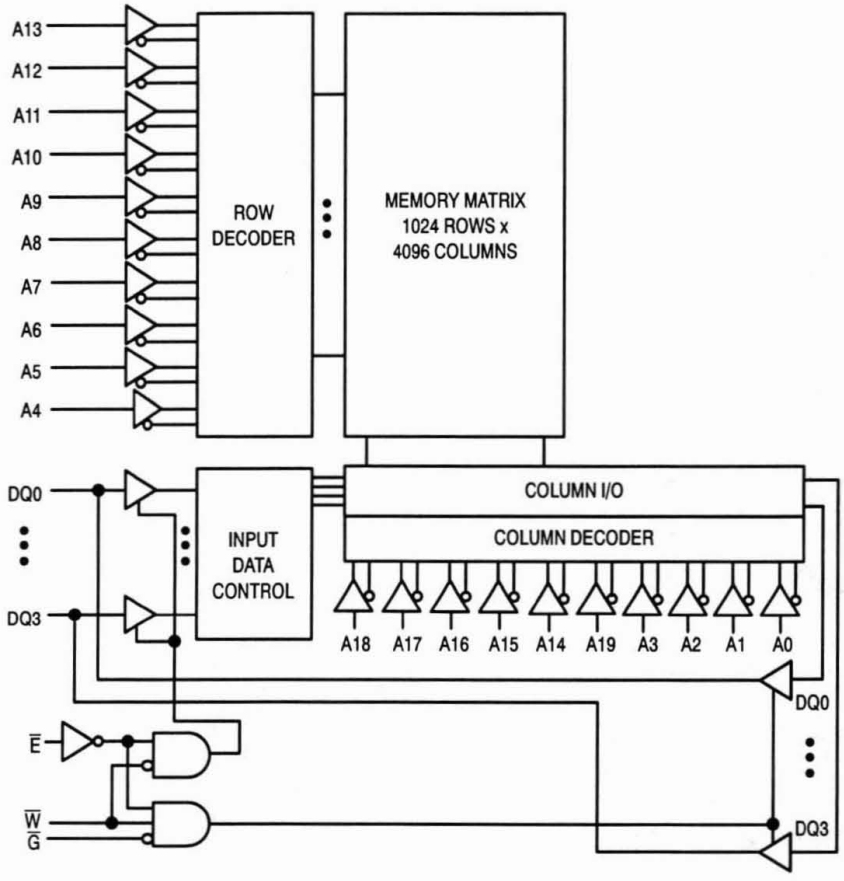
The MCM6249 is available in a 400 mil, 32–lead surface–mount SOJ package.

- Single 5 V ± 10% Power Supply
- Fast Access Time: 20/25/35 ns
- Equal Address and Chip Enable Access Time
- All Inputs and Outputs are TTL Compatible
- Three–State Outputs
- Power Operation: 190/175/160 mA Maximum, Active AC

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A19	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
DQ0 – DQ3	Data Input/Output
NC	No Connection
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

REV 4
5/95

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	Not Selected	High–Z	—	I_{SB1}, I_{SB2}
L	H	H	Output Disabled	High–Z	—	I_{CCA}
L	L	H	Read	D_{out}	Read	I_{CCA}
L	X	L	Write	High–Z	Write	I_{CCA}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns).

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter		Symbol	Min	Typ	Max	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max)	MCM6249–20: t_{AVAV} = 20 ns	I_{CC}	—	175	190	mA
	MCM6249–25: t_{AVAV} = 25 ns		—	160	175	
	MCM6249–35: t_{AVAV} = 35 ns		—	145	160	
AC Standby Current (V_{CC} = max, $\overline{E}$ = V_{IH}, No other restrictions on other inputs)	MCM6249–20: t_{AVAV} = 20 ns	I_{SB1}	—	50	60	mA
	MCM6249–25: t_{AVAV} = 25 ns		—	40	50	
	MCM6249–35: t_{AVAV} = 35 ns		—	35	40	
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V) (V_{CC} = max, f = 0 MHz)		I_{SB2}	—	10	15	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except Clocks and DQs $\overline{E}$, $\overline{G}$, $\overline{W}$	C_{in} C_{ck}	4 5	6 8	pF
Input/Output Capacitance	DQ	$C_{I/O}$	5	8	pF

2

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1a

READ CYCLE TIMING (See Note 1)

Parameter	Symbol	MCM6249–20		MCM6249–25		MCM6249–35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	20	—	25	—	35	—	ns	2, 3
Address Access Time	t_{AVQV}	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	—	20	—	25	—	35	ns	4
Output Enable Access Time	t_{GLQV}	—	6	—	8	—	10	ns	
Output Hold from Address Change	t_{AXQX}	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	5	—	5	—	ns	5, 6, 7
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	5, 6, 7
Enable High to Output High–Z	t_{EHQZ}	0	9	0	10	0	12	ns	5, 6, 7
Output Enable High to Output High–Z	t_{GHQZ}	0	9	0	10	0	12	ns	5, 6, 7
Power Up Time	t_{ELICCH}	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	—	20	—	25	—	35	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low/$\overline{E}$ going high.
5. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1b.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E} \le V_{IL}$, $\overline{G} \le V_{IL}$).

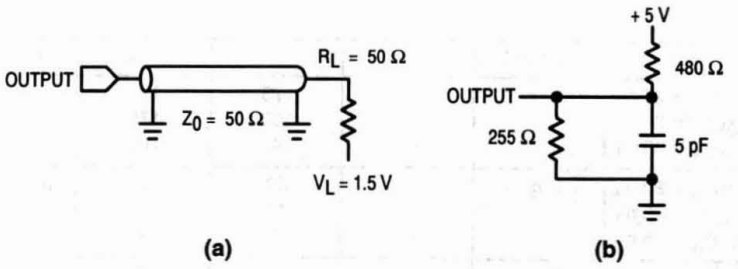
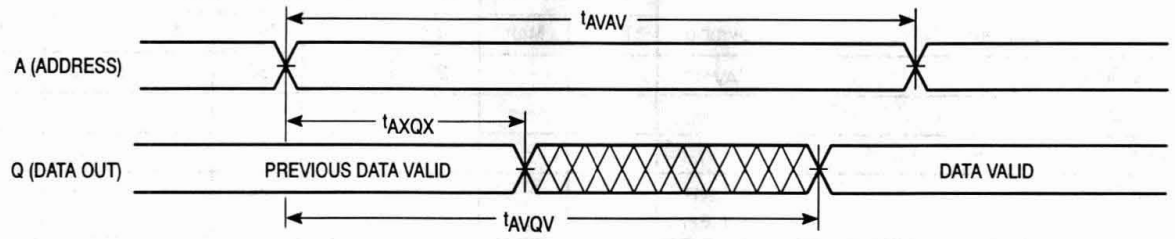


Figure 1. AC Test Loads

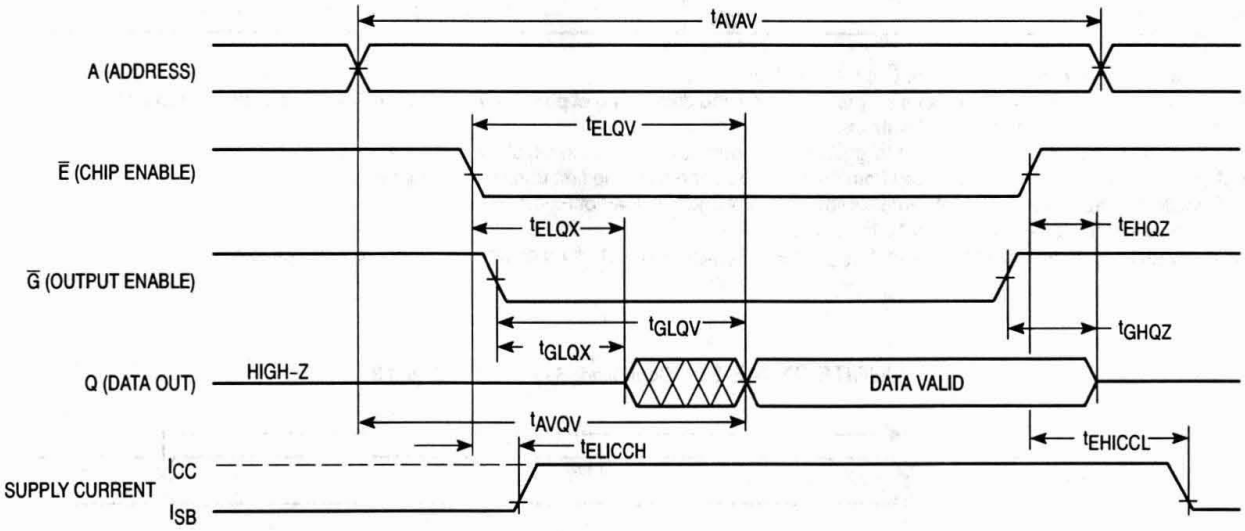
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 8)



READ CYCLE 2 (See Note)



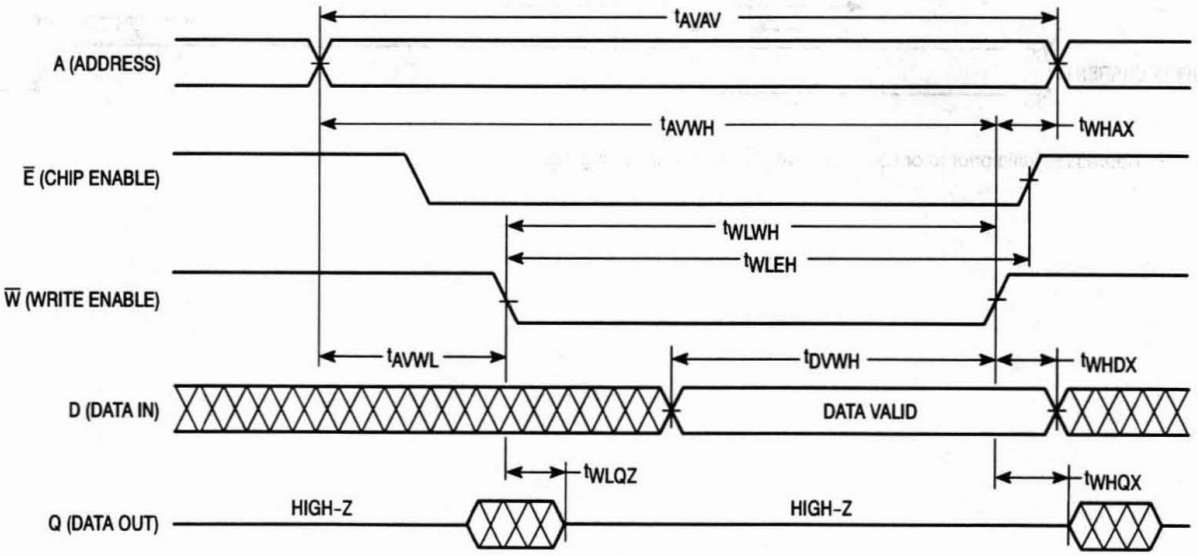
NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low/$\overline{E}$ going high.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	MCM6249–20		MCM6249–25		MCM6249–35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVWH}	10	—	10	—	15	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	9	0	10	0	15	ns	5,6,7
Write High to Output Active	t_{WHQX}	5	—	5	—	5	—	ns	5,6,7
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
4. All write cycle timings are referenced from the last valid address to the first transitioning address.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1b.
6. This parameter is sampled and not 100% tested.
7. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

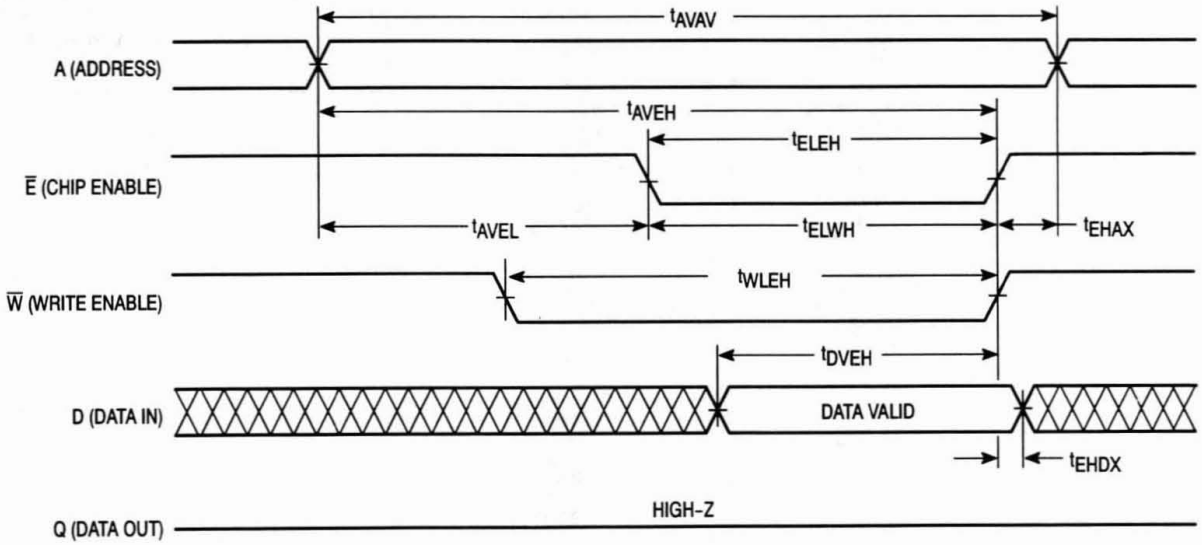


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	MCM6249–20		MCM6249–25		MCM6249–35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	15	—	17	—	20	—	ns	
Enable Pulse Width	t_{ELEH}, t_{ELWH}	15	—	17	—	20	—	ns	5,6
Write Pulse Width	t_{WLEH}	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	10	—	10	—	15	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, and 3)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6249 XX XX XX

- Motorola Memory Prefix
- Part Number
- Shipping Method (R2 = Tape and Reel, Blank = Rails)
- Speed (20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
- Package (WJ = 400 mil SOJ)

Full Part Numbers — MCM6249WJ20 MCM6249WJ20R2
MCM6249WJ25 MCM6249WJ25R2
MCM6249WJ35 MCM6249WJ35R2

MCM6949

2

Product Preview

1M x 4 Bit Static Random Access Memory

YJ PACKAGE
400 MIL SOJ
CASE 857A–02

TS PACKAGE
44 TSOP TYPE II
CASE 924A–01

The MCM6949 is a 4,194,304 bit static random access memory organized as 1,048,576 words of 4 bits. Static design eliminates the need for external clocks or timing strobes.

The MCM6949 is equipped with chip enable ($\overline{E}$) and output enable ($\overline{G}$) pins, allowing for greater system flexibility and eliminating bus contention problems. Either input, when high, will force the outputs into high impedance.

The MCM6949 is available in a 400 mil, 32–lead surface–mount SOJ package and a 44–lead TSOP Type II package.

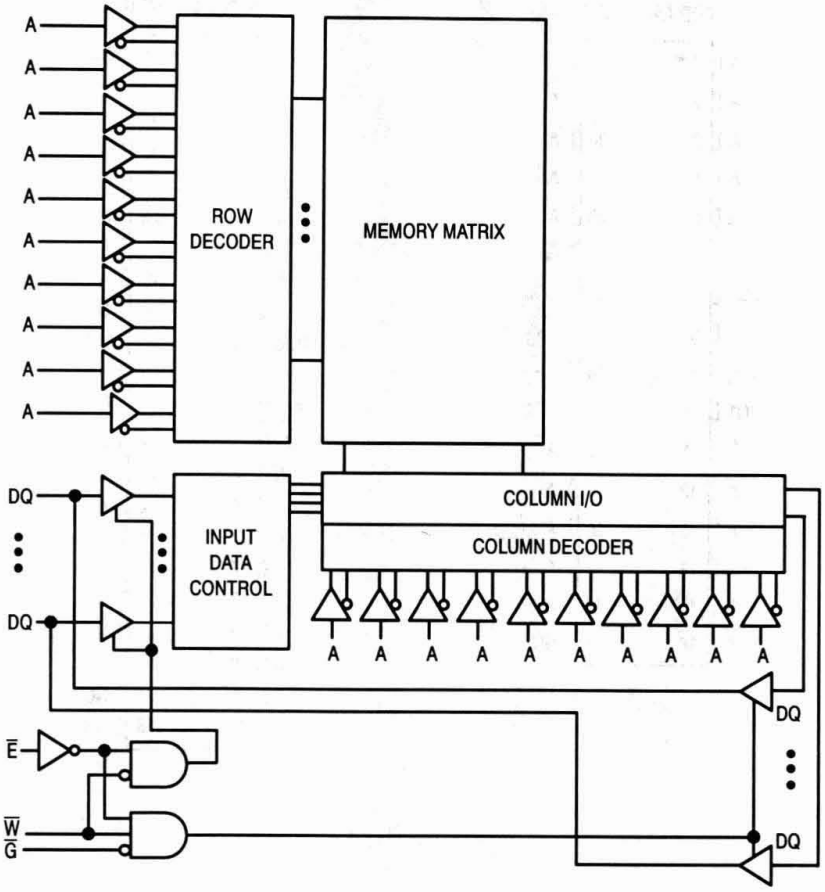
- Single 3.3 V ± 10% Power Supply
- Fast Access Time: 10/12/15 ns
- Equal Address and Chip Enable Access Time
- All Inputs and Outputs are TTL Compatible
- Three–State Outputs
- Power Operation: 165/160/155 mA Maximum, Active AC
- Commercial and Standard Industrial Temperature Option: – 40 to + 85°C

PIN NAMES	
A0 – A19	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
DQ0 – DQ3	Data Input/Output
NC	No Connection
V_{CC}	+ 3.3 V Power Supply
V_{SS}	Ground

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

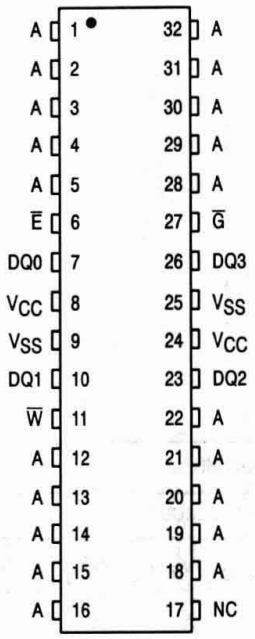
REV 2
3/4/97

BLOCK DIAGRAM

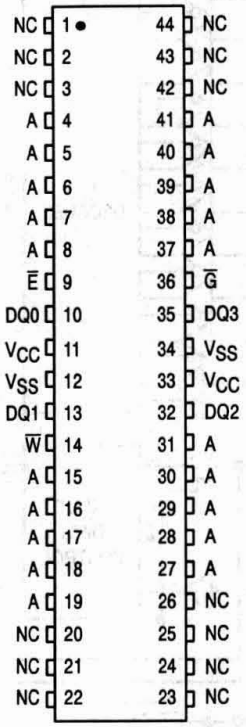


PIN ASSIGNMENTS

400 MIL SOJ


A 1 32 A
A 2 31 A
A 3 30 A
A 4 29 A
A 5 28 A
$\overline{E}$ 6 27 $\overline{G}$
DQ0 7 26 DQ3
V_{CC} 8 25 V_{SS}
V_{SS} 9 24 V_{CC}
DQ1 10 23 DQ2
$\overline{W}$ 11 22 A
A 12 21 A
A 13 20 A
A 14 19 A
A 15 18 A
A 16 17 NC

TSOP TYPE II


NC 1 44 NC
NC 2 43 NC
NC 3 42 NC
A 4 41 A
A 5 40 A
A 6 39 A
A 7 38 A
A 8 37 A
$\overline{E}$ 9 36 $\overline{G}$
DQ0 10 35 DQ3
V_{CC} 11 34 V_{SS}
V_{SS} 12 33 V_{CC}
DQ1 13 32 DQ2
$\overline{W}$ 14 31 A
A 15 30 A
A 16 29 A
A 17 28 A
A 18 27 A
A 19 26 NC
NC 20 25 NC
NC 21 24 NC
NC 22 23 NC

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	Not Selected	High–Z	—	I_{SB1}, I_{SB2}
L	H	H	Output Disabled	High–Z	—	I_{CCA}
L	L	H	Read	D_{out}	Read	I_{CCA}
L	X	L	Write	High–Z	Write	I_{CCA}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating		Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}		V_{CC}	– 0.5 to + 5.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}		V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)		I_{out}	± 20	mA
Power Dissipation		P_D	1.0	W
Temperature Under Bias	Commercial Industrial	T_{bias}	– 10 to + 85 – 45 to + 90	°C
Operating Temperature	Commercial Industrial	T_A	0 to + 70 – 45 to + 85	°C
Storage Temperature — Plastic		T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)
(T_A = – 40 to + 85°C for Industrial Temperature Offering)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns).

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter		Symbol	0 to + 70°C	– 40 to + 85°C	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max)	MCM6949–10: t_{AVAV} = 10 ns MCM6949–12: t_{AVAV} = 12 ns MCM6949–15: t_{AVAV} = 15 ns	I_{CC}	165 160 155	175 170 165	mA
AC Standby Current (V_{CC} = max, $\overline{E}$ = V_{IH}, No other restrictions on other inputs)	MCM6949–10: t_{AVAV} = 10 ns MCM6949–12: t_{AVAV} = 12 ns MCM6949–15: t_{AVAV} = 15 ns	I_{SB1}	50 50 45	55 55 50	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V) (V_{CC} = max, f = 0 MHz)		I_{SB2}	5	5	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except Clocks and DQs $\overline{E}$, $\overline{G}$, $\overline{W}$	C_{in} C_{ck}	4 5	6 8	pF
Input/Output Capacitance	DQ	$C_{I/O}$	5	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)
(T_A = – 40 to + 85°C for Industrial Temperature Offering)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM6949–10		MCM6949–12		MCM6949–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	10	—	12	—	15	—	ns	3
Address Access Time	t_{AVQV}	—	10	—	12	—	15	ns	
Enable Access Time	t_{ELQV}	—	10	—	12	—	15	ns	4
Output Enable Access Time	t_{GLQV}	—	5	—	6	—	7	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	3	—	3	—	3	—	ns	5, 6, 7
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	5, 6, 7
Enable High to Output High–Z	t_{EHQZ}	0	5	0	6	0	7	ns	5, 6, 7
Output Enable High to Output High–Z	t_{GHQZ}	0	5	0	6	0	7	ns	5, 6, 7

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
6. Transition is measured ± 200 mV from steady–state voltage.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E} \le V_{IL}$, $\overline{G} \le V_{IL}$).

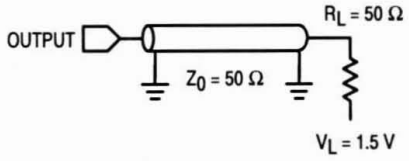
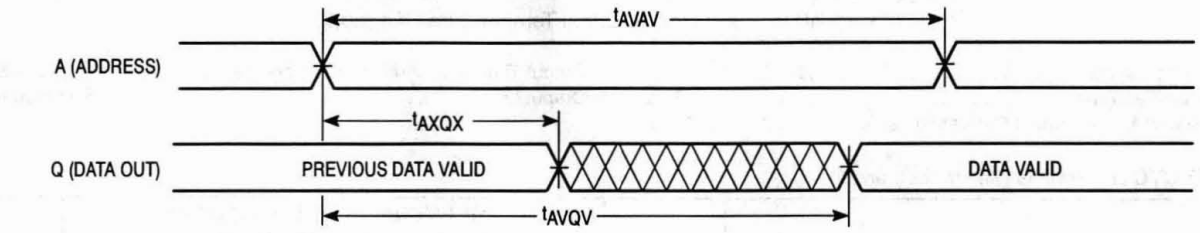


Figure 1. AC Test Load

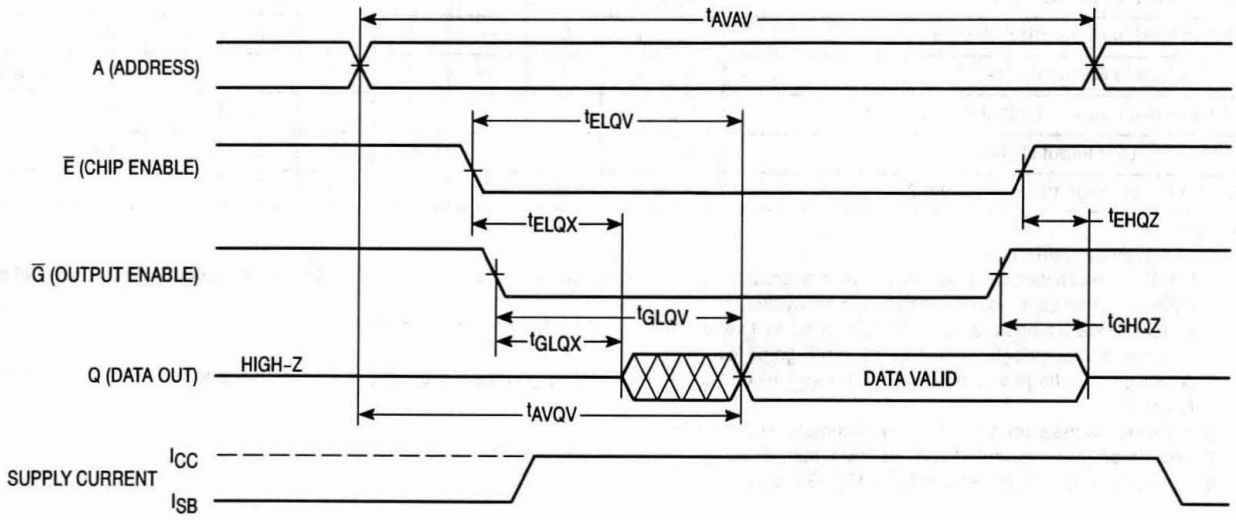
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 8)



READ CYCLE 2 (See Note 4)

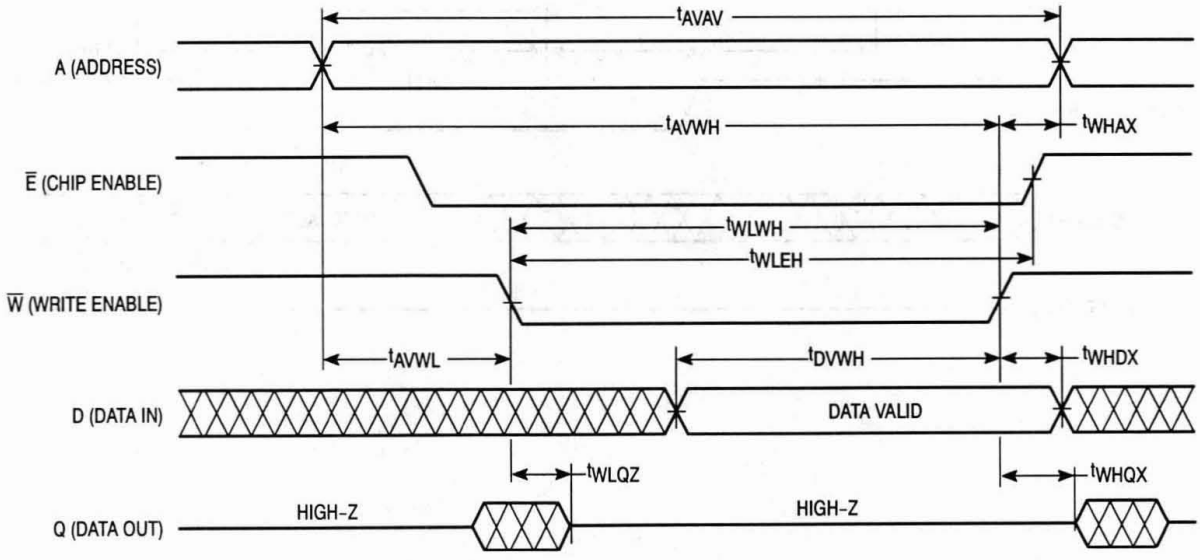


WRITE CYCLE 1 ($\overline{W}$ Controlled; See Notes 1, 2, and 3)

Parameter	Symbol	MCM6949–10		MCM6949–12		MCM6949–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	10	—	12	—	15	—	ns	4
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	9	—	10	—	12	—	ns	
Address Valid to End of Write ($\overline{G}$ High)	t_{AVWH}	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	9	—	10	—	12	—	ns	
Write Pulse Width ($\overline{G}$ High)	t_{WLWH} t_{WLEH}	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	5	—	6	—	7	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	5	0	6	0	7	ns	5, 6, 7
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	5, 6, 7
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
4. All write cycle timings are referenced from the last valid address to the first transitioning address.
5. Transition is measured ± 200 mV from steady–state voltage.
6. This parameter is sampled and not 100% tested.
7. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled; See Notes 1, 2, and 3)

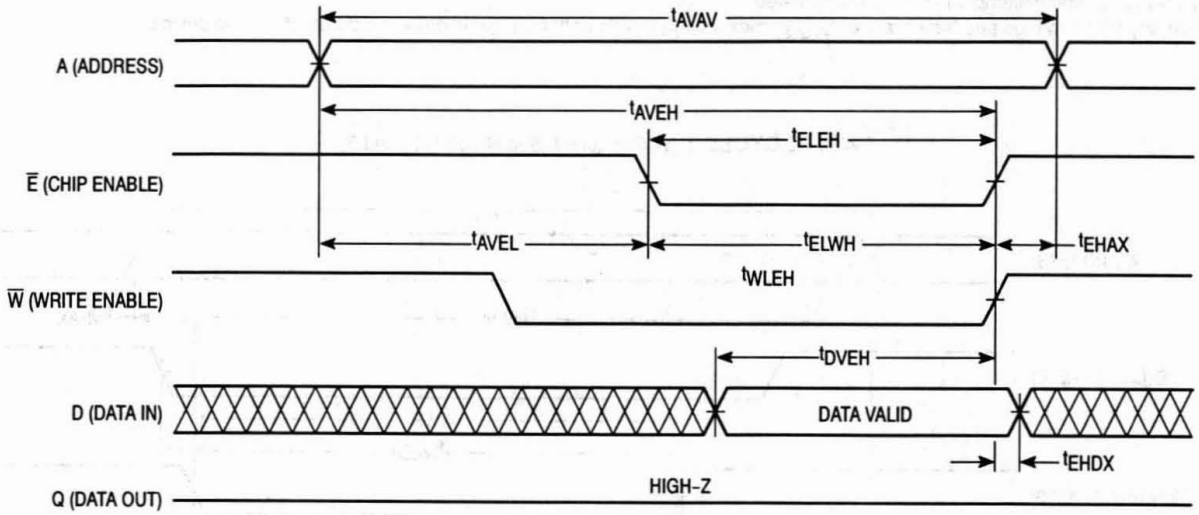


WRITE CYCLE 2 ($\overline{E}$ Controlled; See Notes 1, 2, and 3)

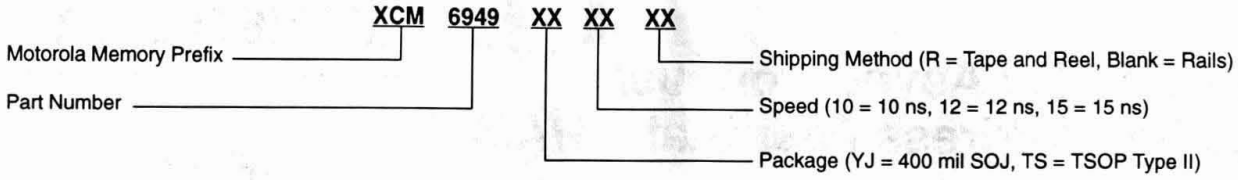
Parameter	Symbol	MCM6949–10		MCM6949–12		MCM6949–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	10	—	12	—	15	—	ns	4
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	9	—	10	—	12	—	ns	
Address Valid to End of Write ($\overline{G}$ High)	t_{AVEH}	8	—	9	—	10	—	ns	
Enable Pulse Width	t_{ELEH}, t_{ELWH}	9	—	10	—	12	—	ns	5, 6
Enable Pulse Width ($\overline{G}$ High)	t_{ELEH}, t_{ELWH}	8	—	9	—	10	—	ns	5, 6
Data Valid to End of Write	t_{DVEH}	5	—	6	—	7	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2 ($\overline{E}$ Controlled; See Notes 1, 2, and 3)



ORDERING INFORMATION
(Order by Full Part Number)


XCM 6949 XX XX XX
Motorola Memory Prefix
Part Number
Shipping Method (R = Tape and Reel, Blank = Rails)
Speed (10 = 10 ns, 12 = 12 ns, 15 = 15 ns)
Package (YJ = 400 mil SOJ, TS = TSOP Type II)

Full Commercial Part Numbers —	MCM6949YJ10	MCM6949YJ10R	MCM6949TS10
	MCM6949YJ12	MCM6949YJ12R	MCM6949TS12
	MCM6949YJ15	MCM6949YJ15R	MCM6949TS15
Full Industrial Part Numbers —	SCM6949YJ10A	SCM6949YJ10AR	SCM6949TS10A*
	SCM6949YJ12A	SCM6949YJ12AR	SCM6949TS12A*
	SCM6949YJ15A	SCM6949YJ15AR	SCM6949TS15A*

* Not available in Tape and Reel.

2

MCM67A618A

64K x 18 Bit Asynchronous/ Latched Address Fast Static RAM

2

The MCM67A618A is a 1,179,648 bit latched address static random access memory organized as 65,536 words of 18 bits. The device integrates a 64K x 18 SRAM core with advanced peripheral circuitry consisting of address and data input latches, active low chip enable, separate upper and lower byte write strobes, and a fast output enable. This device has increased output drive capability supported by multiple power pins.

Address, data in, and chip enable latches are provided. When latch enables (AL for address and chip enables and DL for data in) are high, the address, data in, and chip enable latches are in the transparent state. If latch enables are tied high the device can be used as an asynchronous SRAM. When latch enables are low the address, data in, and chip enable latches are in the latched state. This input latch simplifies read and write cycles by guaranteeing address and data–in hold time in a simple fashion.

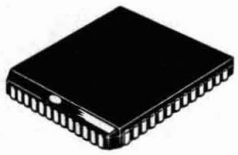
Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits) while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

Six pair of power and ground pins have been utilized and placed on the package for maximum performance.

The MCM67A618A will be available in a 52–pin plastic leaded chip carrier (PLCC).

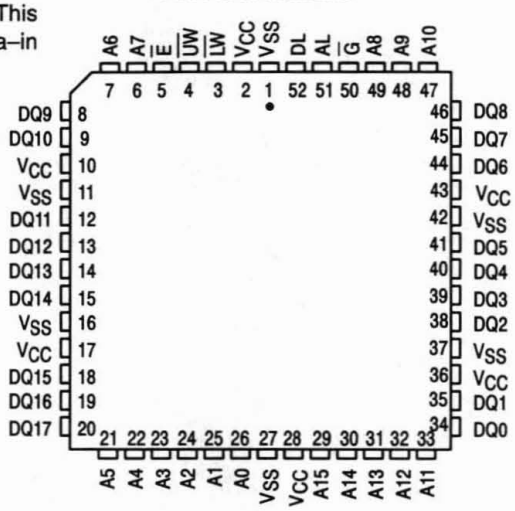
This device is ideally suited for systems that require wide data bus widths, cache memory, and tag RAMs.

- Single 5 V ± 5% Power Supply
- Fast Access Times: 10/12/15 ns Max
- Byte Writeable via Dual Write Enables
- Separate Data Input Latch for Simplified Write Cycles
- Address and Chip Enable Input Latches
- Common Data Inputs and Data Outputs
- Output Enable Controlled Three–State Outputs
- 3.3 V I/O Compatible
- High Board Density 52–Lead PLCC Package



FN PACKAGE
PLASTIC
CASE 778–02

PIN ASSIGNMENT



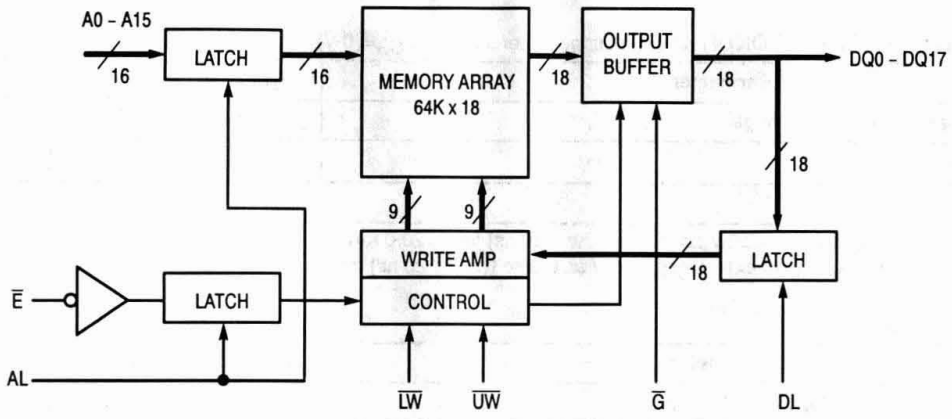
PIN NAMES	
A0 – A15	Address Inputs
AL	Address Latch
DL	Data Latch
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Higher Byte Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

All power supply and ground pins must be connected for proper operation of the device.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

REV 1
10/9/96

BLOCK DIAGRAM



TRUTH TABLE

$\overline{E}$	$\overline{LW}$	$\overline{UW}$	AL*	DL*	$\overline{G}$	Mode	Supply Current	I/O Status
H	X	X	X	X	X	Deselected Cycle	I_{SB}	High–Z
L	X	X	L	X	X	Read or Write Using Latched Addresses	I_{CC}	—
L	X	X	H	X	X	Read or Write Using Unlatched Addresses	I_{CC}	—
L	H	H	X	X	L	Read Cycle	I_{CC}	Data Out
L	H	H	X	X	H	Read Cycle	I_{CC}	High–Z
L	L	L	X	L	X	Write Both Bytes Using Latched Data In	I_{CC}	High–Z
L	L	L	X	H	X	Write Both Bytes Using Unlatched Data In	I_{CC}	High–Z
L	L	H	X	X	X	Write Cycle, Lower Byte	I_{CC}	High–Z
L	H	L	X	X	X	Write Cycle, Lower Byte	I_{CC}	High–Z

*$\overline{E}$ and Addresses satisfy the specified setup and hold times for the falling edge of AL. Data–in satisfies the specified setup and hold times for falling edge of DL.

NOTE: This truth table shows the application of each function. Combinations of these functions are valid.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Standby Current ($\overline{G}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{AVAV} min)	I_{CCA10} I_{CCA12} I_{CCA15}	—	290 280 265	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{AVAV} min)	I_{SB1}	—	95	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V, f = f_{max})	I_{SB2}	—	20	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns
Output Timing Reference Level ..... 1.5 V
Output Load ..... Figure 1a Unless Otherwise Noted

ASYNCHRONOUS READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM67A618A–10		MCM67A618A–12		MCM67A618A–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Times	t_{AVAV}	10	—	12	—	15	—	ns	3
Access Times:								ns	4
Address Valid to Output Valid	t_{AVQV}	—	10	—	12	—	15		
$\overline{E}$ Low to Output Valid	t_{ELQV}	—	10	—	12	—	15		
Output Enable Low to Output Valid	t_{GLQV}	—	5	—	6	—	7		
Output Hold from Address Change	t_{AXQX}	4	—	4	—	4	—	ns	
Output Buffer Control:								ns	5
$\overline{E}$ Low to Output Active	t_{ELQX}	3	—	3	—	3	—		
$\overline{G}$ Low to Output Active	t_{GLQX}	1	—	1	—	1	—		
$\overline{E}$ High to Output High–Z	t_{EHQZ}	2	5	2	6	2	7		
$\overline{G}$ High to Output High–Z	t_{GHQZ}	2	5	2	6	2	7		
Power Up Time	t_{ELICCA}	0	—	0	—	0	—	ns	

NOTES:
1. AL and DL are equal to V_{IH} for all asynchronous cycles.
2. Both Write Enable signals ($\overline{LW}$, $\overline{UW}$) are equal to V_{IH} for all read cycles.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1b. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EHQZ} is less than t_{ELQX} and t_{GHQZ} is less than t_{GLQX} for a given device.

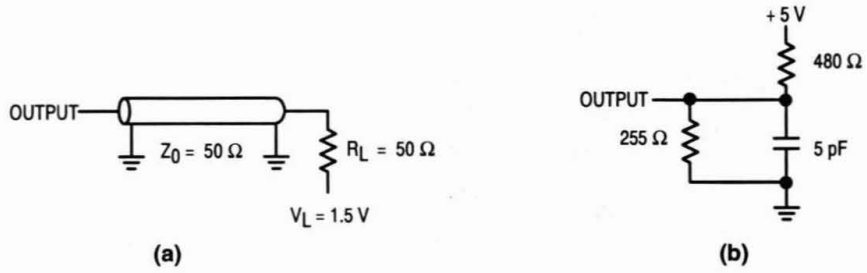
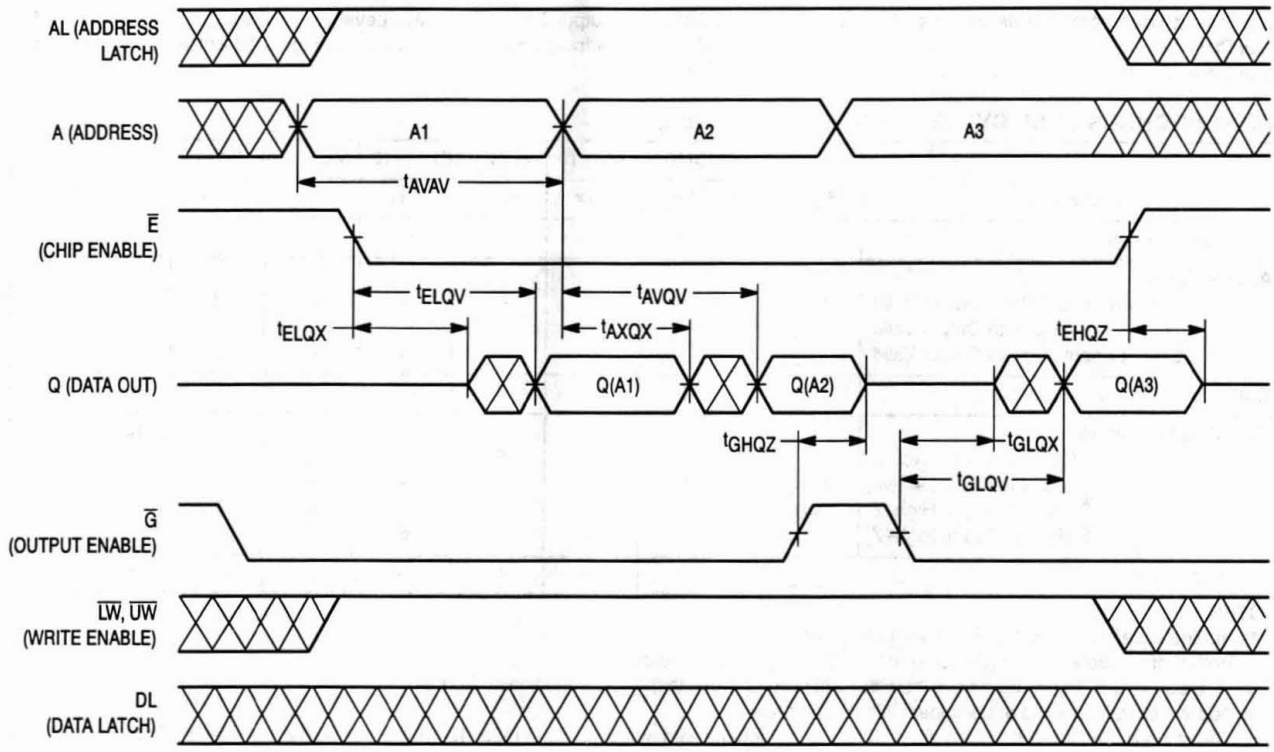


Figure 1. AC Test Loads

ASYNCHRONOUS READ CYCLES

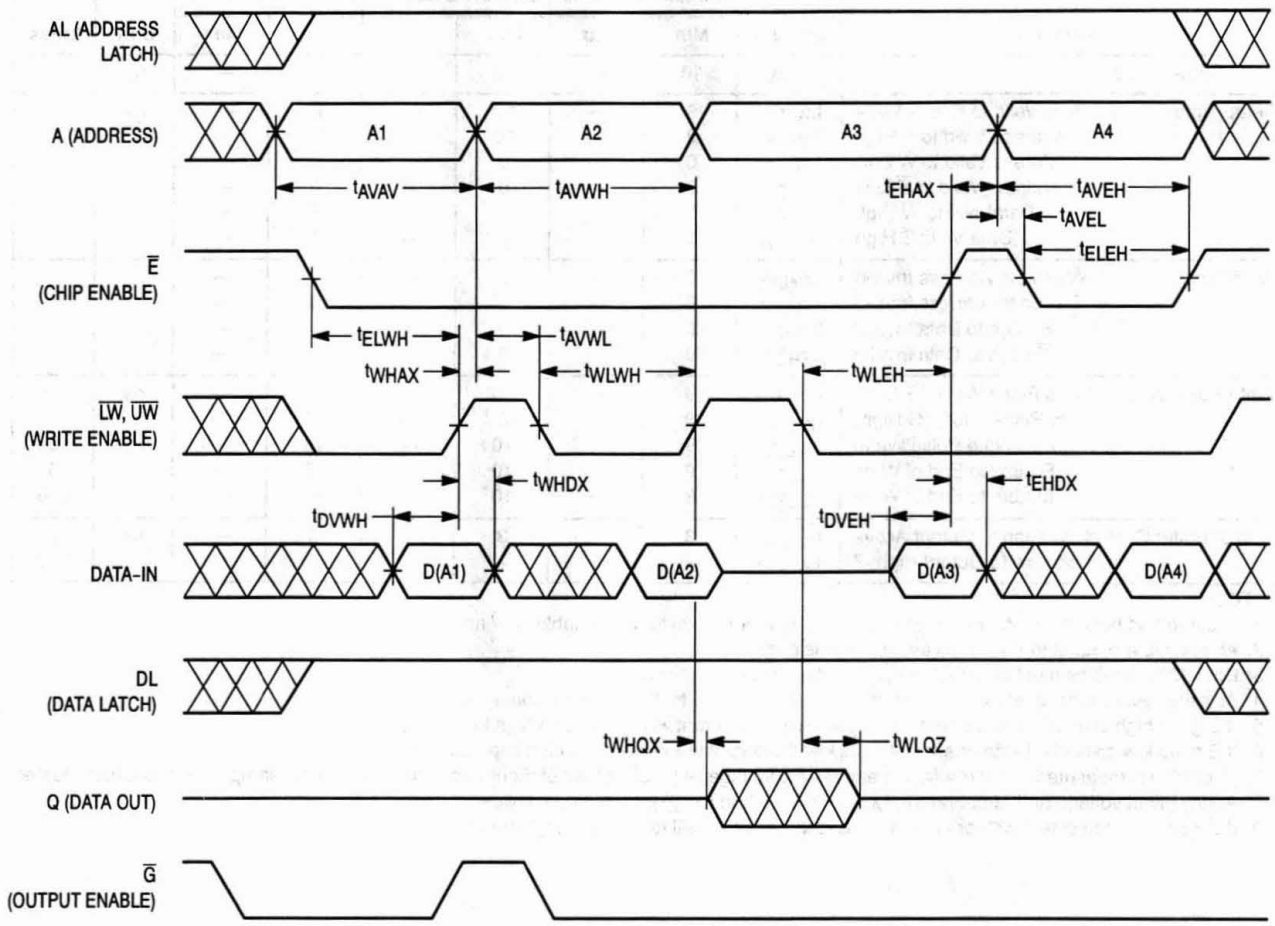


ASYNCHRONOUS WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM67A618A–10		MCM67A618A–12		MCM67A618A–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Times	t_{AVAV}	10	—	12	—	15	—	ns	4
Setup Times: Address Valid to End of Write	t_{AVWH}	9	—	10	—	13	—	ns	
Address Valid to $\overline{E}$ High	t_{AVEH}	9	—	10	—	13	—		
Address Valid to $\overline{W}$ Low	t_{AVWL}	0	—	0	—	0	—		
Address Valid to $\overline{E}$ Low	t_{AVEL}	0	—	0	—	0	—		
DataValid to $\overline{W}$ High	t_{DVWH}	5	—	6	—	7	—		
Data Valid $\overline{E}$ High	t_{DVEH}	5	—	6	—	7	—		
Hold Times: $\overline{W}$ High to Address Invalid	t_{WHAX}	0	—	0	—	0	—	ns	
$\overline{E}$ High to Address Invalid	t_{EHAX}	0	—	0	—	0	—		
$\overline{W}$ High to Data Invalid	t_{WHDX}	0	—	0	—	0	—		
$\overline{E}$ High to Data Invalid	t_{EHDX}	0	—	0	—	0	—		
Write Pulse Width: Write Pulse Width ($\overline{G}$ Low)	t_{WLWH}	9	—	10	—	13	—	ns	
Write Pulse Width ($\overline{G}$ High)	t_{WLWH}	8	—	9	—	12	—		
Write Pulse Width	t_{WLEH}	9	—	10	—	13	—		5
Enable to End of Write	t_{ELWH}	9	—	10	—	13	—		6
Enable to End of Write	t_{ELEH}	9	—	10	—	13	—		5, 6
Output Buffer Control: $\overline{W}$ High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	7
$\overline{W}$ Low to Output High–Z	t_{WLQZ}	—	5	—	6	—	9		7, 8

NOTES:
1. In setup and hold times, W (write) refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. AL and DL are equal to V_{IH} for all asynchronous cycles.
3. Both Write Enables must be equal to V_{IH} for all address transitions.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high the output will remain in a high impedance state.
6. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.
7. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1b. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{WLQZ} is less than t_{WHQX} for a given device.
8. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.

ASYNCHRONOUS WRITE CYCLE

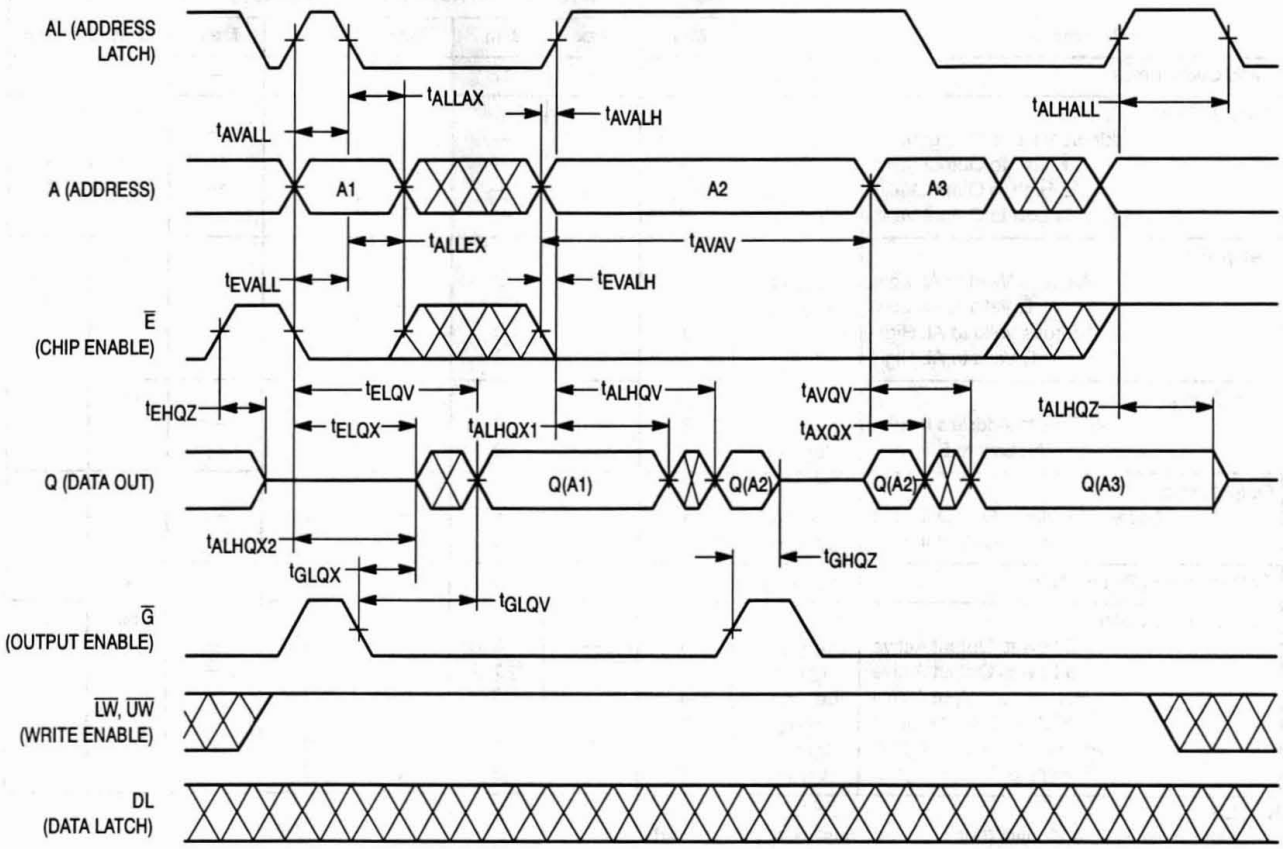


LATCHED READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM67A618A–10		MCM67A618A–12		MCM67A618A–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Times	t_{AVAV}	10	—	12	—	15	—	ns	3
Access Times:								ns	
Address Valid to Output Valid	t_{AVQV}	—	10	—	12	—	15		
$\overline{E}$ Low to Output Valid	t_{ELQV}	—	10	—	12	—	15		3
AL High to Output Valid	t_{ALHQV}	—	10	—	12	—	15		4
Output Enable Low to Output Valid	t_{GLQV}	—	5	—	6	—	7		
Setup Times:								ns	
Address Valid to AL Low	t_{AVALL}	2	—	2	—	2	—		4
$\overline{E}$ Valid to AL Low	t_{EVALL}	2	—	2	—	2	—		4
Address Valid to AL High	t_{AVALH}	0	—	0	—	0	—		
$\overline{E}$ Valid to AL High	t_{EVALH}	0	—	0	—	0	—		
Hold Times:								ns	4
AL Low to Address Invalid	t_{ALLAX}	2	—	2	—	3	—		
AL Low to $\overline{E}$ Invalid	t_{ALLEX}	2	—	2	—	3	—		
Output Hold:								ns	
Address Invalid to Output Invalid	t_{AXQX}	4	—	4	—	4	—		
AL High to Output Invalid	t_{ALHQX1}	4	—	4	—	4	—		
Address Latch Pulse Width	t_{ALHALL}	5	—	5	—	5	—	ns	
Output Buffer Control:								ns	5
$\overline{E}$ Low to Output Active	t_{ELQX}	3	—	3	—	3	—		
$\overline{G}$ Low to Output Active	t_{GLQX}	1	—	1	—	1	—		
AL High to Output Active	t_{ALHQX2}	3	—	3	—	3	—		
$\overline{E}$ High to Output High–Z	t_{EHQZ}	2	5	2	6	2	9		
AL High to Output High–Z	t_{ALHQZ}	2	5	2	6	2	9		
$\overline{G}$ High to Output High–Z	t_{GHQZ}	2	5	2	6	2	7		

NOTES:
1. Both Write Enable Signals ($\overline{LW}$, $\overline{UW}$) are equal to V_{IH} for all read cycles.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. All latched inputs must meet the specified setup and hold times with stable logic levels for ALL falling edges of address latch (AL) and data latch (DL).
5. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1b. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EHQZ} is less than t_{ELQX} and t_{ALHQZ} is less than t_{ALHQX2} and t_{GHQZ} is less than t_{GLQX} for a given device.

LATCHED READ CYCLES

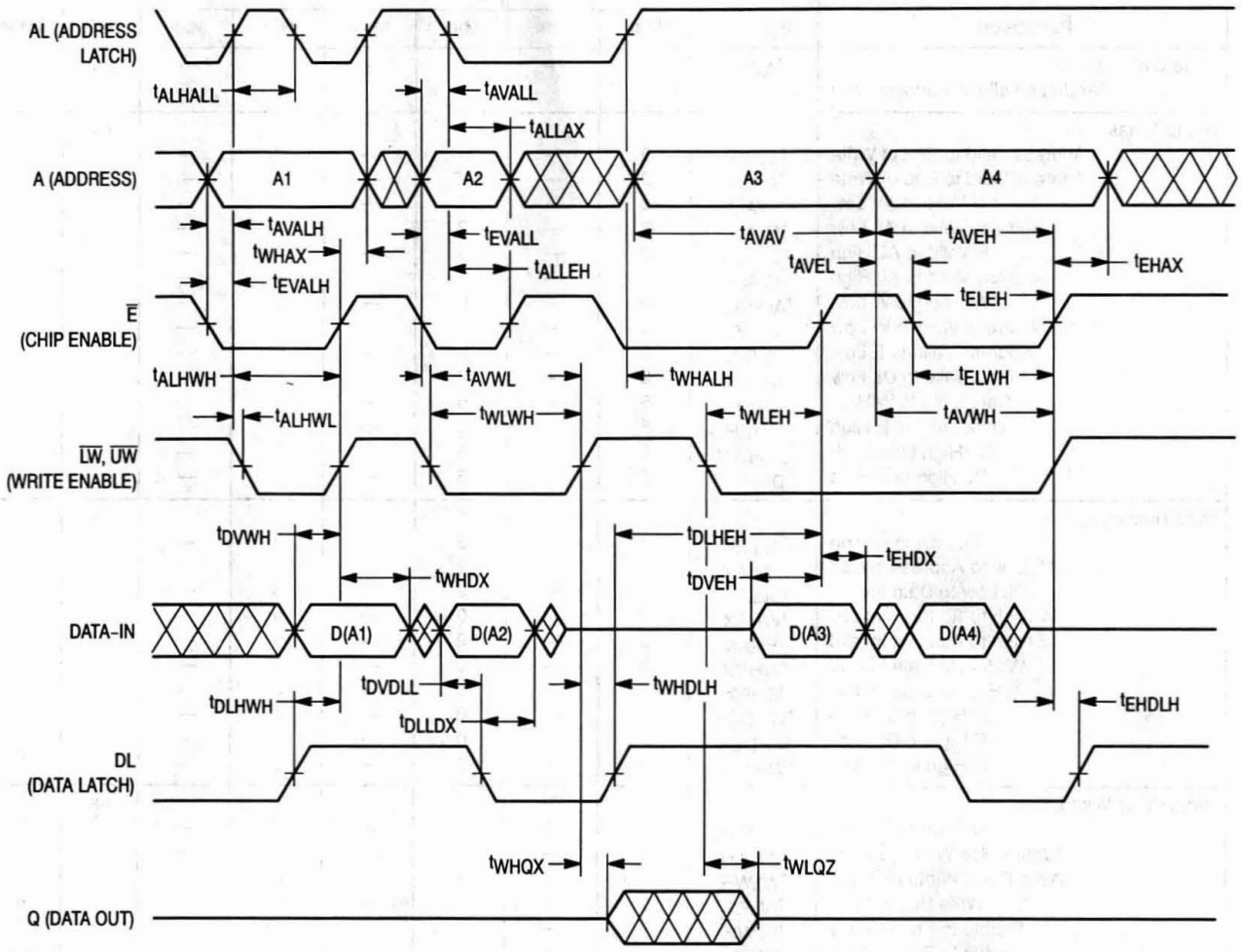


LATCHED WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM67A618A–10		MCM67A618A–12		MCM67A618A–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Times: Address Valid to Address Valid	t_{AVAV}	10	—	12	—	15	—	ns	4
Setup Times:								ns	
Address Valid to End of Write	t_{AVWH}	9	—	10	—	13	—		
Address Valid to End of Write	t_{AVEH}	9	—	10	—	13	—		
$\overline{E}$ Valid to AL Low	t_{EVALL}	2	—	2	—	2	—		
Address Valid to AL Low	t_{AVALL}	2	—	2	—	2	—		
$\overline{E}$ Valid to AL High	t_{EVALH}	0	—	0	—	0	—		
Address Valid to AL High	t_{AVALH}	0	—	0	—	0	—		
AL High to $\overline{W}$ Low	t_{ALHWL}	0	—	0	—	0	—		
Address Valid to $\overline{W}$ Low	t_{AVWL}	0	—	0	—	0	—		
Address Valid to $\overline{E}$ Low	t_{AVEL}	0	—	0	—	0	—		
Data Valid to DL Low	t_{DVDLL}	2	—	2	—	2	—		
Data Valid to $\overline{W}$ High	t_{DVWH}	5	—	6	—	7	—		
Data Valid to $\overline{E}$ High	t_{DVEH}	5	—	6	—	7	—		
DL High to $\overline{W}$ High	t_{DLHWH}	5	—	6	—	7	—		
DL High to $\overline{E}$ High	t_{DLHEH}	5	—	6	—	7	—		
Hold Times:								ns	
AL Low to $\overline{E}$ High	t_{ALLEH}	2	—	2	—	3	—		4
AL Low to Address Invalid	t_{ALLAX}	2	—	2	—	3	—		4
DL Low to Data Invalid	t_{DLLDX}	2	—	2	—	3	—		
$\overline{W}$ High to Address Invalid	t_{WHAX}	0	—	0	—	0	—		
$\overline{E}$ High to Address Invalid	t_{EHAX}	0	—	0	—	0	—		
$\overline{W}$ High to Data Invalid	t_{WHDX}	0	—	0	—	0	—		
$\overline{E}$ High to Data Invalid	t_{EHDX}	0	—	0	—	0	—		
$\overline{W}$ High to DL High	t_{WHDLH}	0	—	0	—	0	—		
$\overline{E}$ High to DL High	t_{EHDLH}	0	—	0	—	0	—		
$\overline{W}$ High to AL High	t_{WHALH}	0	—	0	—	0	—		
Write Pulse Width:								ns	
AL High to $\overline{W}$ High	t_{ALHWH}	9	—	10	—	13	—		5
Write Pulse Width ($\overline{G}$ Low)	t_{WLWH}	9	—	10	—	13	—		
Write Pulse Width ($\overline{G}$ High)	t_{WLWH}	8	—	9	—	12	—		
Write Pulse Width	t_{WLEH}	9	—	10	—	13	—		6
Enable to End of Write	t_{ELWH}	9	—	10	—	13	—		7
Enable to End of Write	t_{ELEH}	9	—	10	—	13	—		6, 7
Address Latch Pulse Width	t_{ALHALL}	5	—	5	—	5	—	ns	4
Output Buffer Control:								ns	
$\overline{W}$ High to Output Active	t_{WHQX}	3	—	3	—	3	—		8
$\overline{W}$ Low to Output High–Z	t_{WLQZ}	—	5	—	6	—	9		8, 9

NOTES:
1. W (write) refers to either one or both byte write enables ($\overline{LW}$, $\overline{UW}$).
2. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
3. Both Write Enables must be equal to V_{IH} for all address transitions.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. All latched inputs must meet the specified setup and hold times with stable logic levels for ALL falling edges of address latch (AL) and data latch (DL).
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high the output will remain in a high impedance state.
7. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.
8. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1b. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{WLQZ} is less than t_{WHQX} for a given device.
9. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.

LATCHED WRITE CYCLES



ORDERING INFORMATION
(Order by Full Part Number)

MCM 67A618A X XX

- Motorola Memory Prefix
- Part Number
- Speed (10 = 10 ns, 12 = 12 ns, 15 = 15 ns)
- Package (FN = PLCC)

Full Part Numbers — MCM67A618AFN10 MCM67A618AFN12 MCM67A618AFN15

MCM6323A

Product Preview

64K x 16 Bit 3.3 V Asynchronous Fast Static RAM

YJ PACKAGE
400 MIL SOJ
CASE 919–01

TS PACKAGE
44–LEAD
TSOP TYPE II
CASE 924A–01

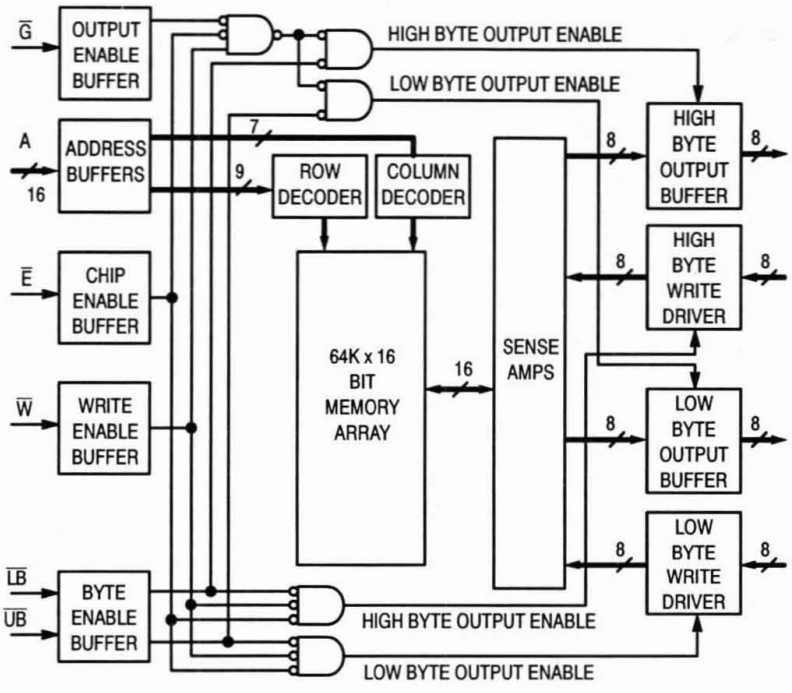
The MCM6323A is a 1,048,576 bit static random access memory organized as 65,536 words of 16 bits. Static design eliminates the need for external clocks or timing strobes; CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6323A is equipped with chip enable ($\overline{E}$), write enable ($\overline{W}$), and output enable ($\overline{G}$) pins, allowing for greater system flexibility and eliminating bus contention problems. Separate byte enable controls ($\overline{LB}$ and $\overline{UB}$) allow individual bytes to be written and read. $\overline{LB}$ controls the lower bits DQ0 to DQ7, while $\overline{UB}$ controls the upper bits DQ8 to DQ15.

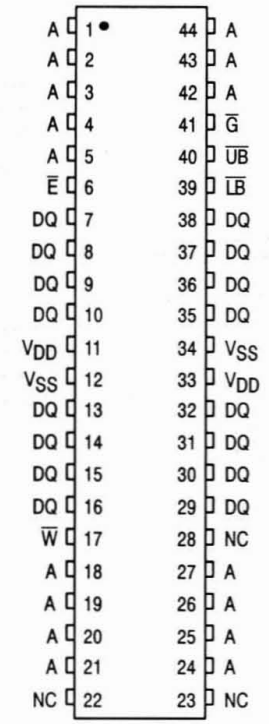
The MCM6323A is available in a 400 mil small–outline J–leaded (SOJ) package and a 44–lead TSOP Type II package in copper leadframe for optimum printed circuit board (PCB) reliability.

- Single 3.3 V ± 0.3 V Power Supply
- Fast Access Time: 10, 12, 15 ns
- Equal Address and Chip Enable Access Time
- All Inputs and Outputs are TTL Compatible
- Data Byte Control
- Fully Static Operation
- Power Operation: 180/160/140 mA Maximum, Active AC
- Industrial Temperature Option: – 40 to + 85°C
  Part Number: SCM6323AYJ10A

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{UB}$	Upper Byte
$\overline{LB}$	Lower Byte
DQ	Data Input/Output
V_{DD}	+ 3.3 V Power Supply
V_{SS}	Ground
NC	No Connection

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

4/1//97

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{LB}$	$\overline{UB}$	Mode	V_{DD} Current	DQ0 – DQ7	DQ8 – DQ15
H	X	X	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	High–Z
L	H	H	X	X	Output Disabled	I_{DDA}	High–Z	High–Z
L	X	X	H	H	Output Disabled	I_{DDA}	High–Z	High–Z
L	L	H	L	H	Low Byte Read	I_{DDA}	D_{out}	High–Z
L	L	H	H	L	High Byte Read	I_{DDA}	High–Z	D_{out}
L	L	H	L	L	Word Read	I_{DDA}	D_{out}	D_{out}
L	X	L	L	H	Low Byte Write	I_{DDA}	D_{in}	High–Z
L	X	L	H	L	High Byte Write	I_{DDA}	High–Z	D_{in}
L	X	L	L	L	Word Write	I_{DDA}	D_{in}	D_{in}

ABSOLUTE MAXIMUM RATINGS (See Notes)

Rating		Symbol	Value	Unit
Supply Voltage		V_{DD}	– 0.5 to + 4.6	V
Voltage on Any Pin		V_{in}	– 0.5 to V_{DD} + 0.5	V
Output Current per Pin		I_{out}	± 20	mA
Package Power Dissipation		P_D	1	W
Temperature Under Bias	Commerial Industrial	T_{bias}	– 10 to + 85 – 45 to + 90	°C
Operating Temperature	Commerial Industrial	T_A	0 to + 70 – 40 to + 85	°C
Storage Temperature		T_{stg}	– 55 to + 150	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. All voltages are referenced to V_{SS}.
3. Power dissipation capability will be dependent upon package characteristics and use environment.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

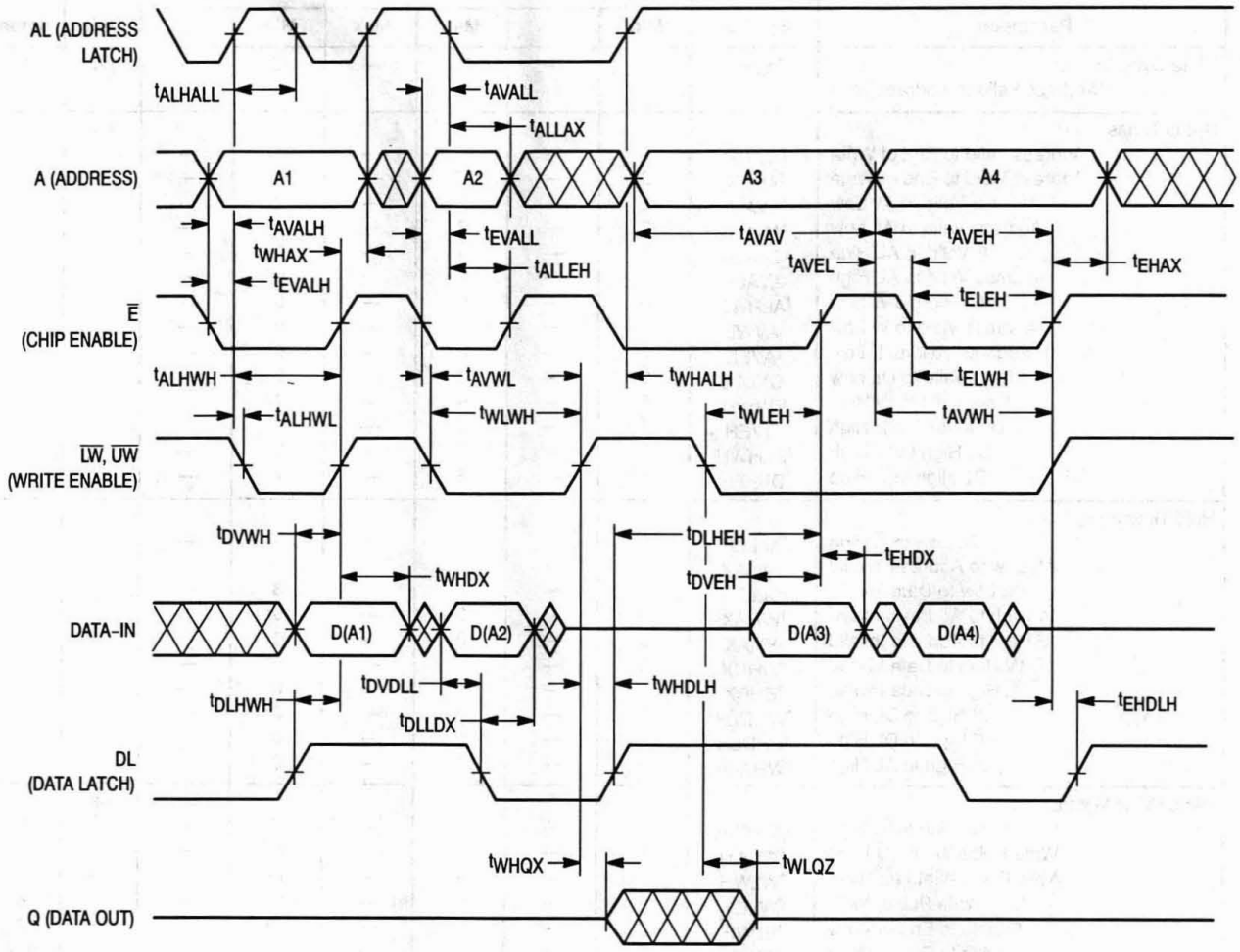
LATCHED WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM67A618A–10		MCM67A618A–12		MCM67A618A–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Times: Address Valid to Address Valid	t_{AVAV}	10	—	12	—	15	—	ns	4
Setup Times:								ns	
Address Valid to End of Write	t_{AVWH}	9	—	10	—	13	—		
Address Valid to End of Write	t_{AVEH}	9	—	10	—	13	—		
$\overline{E}$ Valid to AL Low	t_{EVALL}	2	—	2	—	2	—		
Address Valid to AL Low	t_{AVALL}	2	—	2	—	2	—		
$\overline{E}$ Valid to AL High	t_{EVALH}	0	—	0	—	0	—		
Address Valid to AL High	t_{AVALH}	0	—	0	—	0	—		
AL High to $\overline{W}$ Low	t_{ALHWL}	0	—	0	—	0	—		
Address Valid to $\overline{W}$ Low	t_{AVWL}	0	—	0	—	0	—		
Address Valid to $\overline{E}$ Low	t_{AVEL}	0	—	0	—	0	—		
Data Valid to DL Low	t_{DVDLL}	2	—	2	—	2	—		
Data Valid to $\overline{W}$ High	t_{DVWH}	5	—	6	—	7	—		
Data Valid to $\overline{E}$ High	t_{DVEH}	5	—	6	—	7	—		
DL High to $\overline{W}$ High	t_{DLHWH}	5	—	6	—	7	—		
DL High to $\overline{E}$ High	t_{DLHEH}	5	—	6	—	7	—		
Hold Times:								ns	
AL Low to $\overline{E}$ High	t_{ALLEH}	2	—	2	—	3	—		4
AL Low to Address Invalid	t_{ALLAX}	2	—	2	—	3	—		4
DL Low to Data Invalid	t_{DLLDX}	2	—	2	—	3	—		
$\overline{W}$ High to Address Invalid	t_{WHAX}	0	—	0	—	0	—		
$\overline{E}$ High to Address Invalid	t_{EHAX}	0	—	0	—	0	—		
$\overline{W}$ High to Data Invalid	t_{WHDX}	0	—	0	—	0	—		
$\overline{E}$ High to Data Invalid	t_{EHDX}	0	—	0	—	0	—		
$\overline{W}$ High to DL High	t_{WHDLH}	0	—	0	—	0	—		
$\overline{E}$ High to DL High	t_{EHDLH}	0	—	0	—	0	—		
$\overline{W}$ High to AL High	t_{WHALH}	0	—	0	—	0	—		
Write Pulse Width:								ns	
AL High to $\overline{W}$ High	t_{ALHWH}	9	—	10	—	13	—		5
Write Pulse Width ($\overline{G}$ Low)	t_{WLWH}	9	—	10	—	13	—		
Write Pulse Width ($\overline{G}$ High)	t_{WLWH}	8	—	9	—	12	—		
Write Pulse Width	t_{WLEH}	9	—	10	—	13	—		6
Enable to End of Write	t_{ELWH}	9	—	10	—	13	—		7
Enable to End of Write	t_{ELEH}	9	—	10	—	13	—		6, 7
Address Latch Pulse Width	t_{ALHALL}	5	—	5	—	5	—	ns	4
Output Buffer Control:								ns	
$\overline{W}$ High to Output Active	t_{WHQX}	3	—	3	—	3	—		8
$\overline{W}$ Low to Output High–Z	t_{WLQZ}	—	5	—	6	—	9		8, 9

NOTES:

1. W (write) refers to either one or both byte write enables ($\overline{LW}$, $\overline{UW}$).
2. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
3. Both Write Enables must be equal to V_{IH} for all address transitions.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. All latched inputs must meet the specified setup and hold times with stable logic levels for ALL falling edges of address latch (AL) and data latch (DL).
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high the output will remain in a high impedance state.
7. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.
8. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1b. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{WLQZ} is less than t_{WHQX} for a given device.
9. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.

LATCHED WRITE CYCLES



ORDERING INFORMATION
(Order by Full Part Number)

MCM 67A618A X XX

- Motorola Memory Prefix
- Part Number
- Speed (10 = 10 ns, 12 = 12 ns, 15 = 15 ns)
- Package (FN = PLCC)

Full Part Numbers — MCM67A618AFN10 MCM67A618AFN12 MCM67A618AFN15

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V ± 0.3 V, T_A = 0 to 70°C, Unless Otherwise Noted)
(T_A = – 40 to + 85°C for Industrial Temperature Offering)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{DD} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{DD} + 0.3 V dc; V_{IH} (max) = V_{DD} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{DD})		$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{DD})		$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage	(I_{OL} = + 4.0 mA) (I_{OL} = + 100 µA)	V_{OL}	—	0.4 V_{SS} + 0.2	V
Output High Voltage	(I_{OH} = – 4.0 mA) (I_{OH} = – 100 µA)	V_{OH}	2.4 V_{DD} – 0.2	—	V

POWER SUPPLY CURRENTS (See Note 1)

Parameter		Symbol	6323A–10	6323A–12	6323A–15	Unit	Notes
AC Active Supply Current (I_{out} = 0 mA) (V_{DD} = max, f = f_{max})	Commerical Industrial	I_{DDA}	180 190	160 170	140 150	mA	2
AC Standby Current ($\overline{E}$ = V_{IH}, V_{DD} = max, f = f_{max})	Commerical Industrial	I_{SB1}	45 50	40 45	35 40	mA	2
CMOS Standby Current (V_{DD} = max, f = 0 MHz, $\overline{E}$ ≥ V_{DD} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{DD} – 0.2 V)	Commerical Industrial	I_{SB2}	1 1	1 1	1 1	mA	

NOTES:
1. Typical current = 25°C @ 3.3 V.
2. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V, V_{IL} = 0 V).

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V ± 0.3 V, T_A = 0 to +70°C, Unless Otherwise Noted)
(T_A = – 40 to + 85°C for Industrial Temperature Offering)

Logic Input Timing Measurement Reference Level ..... 1.50 V
Logic Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

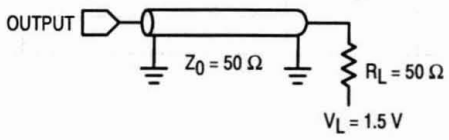
Output Timing Reference Level ..... 1.50 V
Output Load ..... See Figure 1

2

READ CYCLE TIMING (See Notes 1, 2, 7, and 8)

Parameter	Symbol	MCM6323A–10		MCM6323A–12		MCM6323A–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	10	—	12	—	15	—	ns	3
Address Access Time	t_{AVQV}	—	10	—	12	—	15	ns	
Enable Access Time	t_{ELQV}	—	10	—	12	—	15	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	5	—	6	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	3	—	3	—	3	—	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4, 5, 6
Enable High to Output High–Z	t_{EHQZ}	—	4	—	5	—	6	ns	4, 5, 6
Output Enable High to Output High–Z	t_{GHQZ}	—	4	—	5	—	6	ns	4, 5, 6
Byte Enable Access Time	t_{BLQV}	—	4	—	5	—	6	ns	
Byte Enable Low to Output Active	t_{BLQX}	0	—	0	—	0	—	ns	4, 5, 6
Byte High to Output High–Z	t_{BHQZ}	0	5	0	5	0	5	ns	4, 5, 6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For common I/O applications, minimization, or elimination of bus contention conditions is necessary during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} (max) < t_{ELQX} (min), and t_{GHQZ} (max) < t_{GLQX} (min), both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, and $\overline{LB}$ and/or $\overline{UB}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

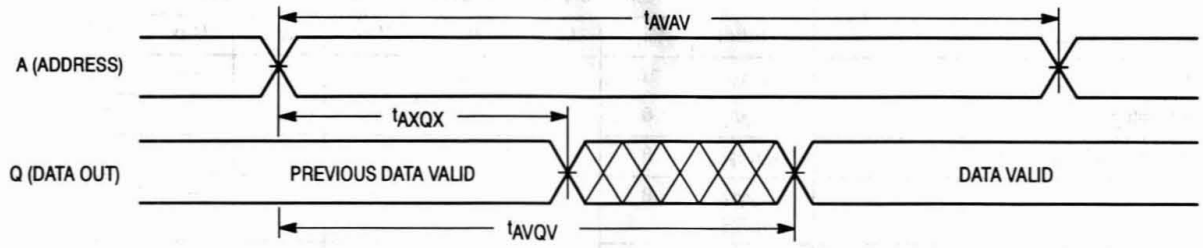


TIMING LIMITS

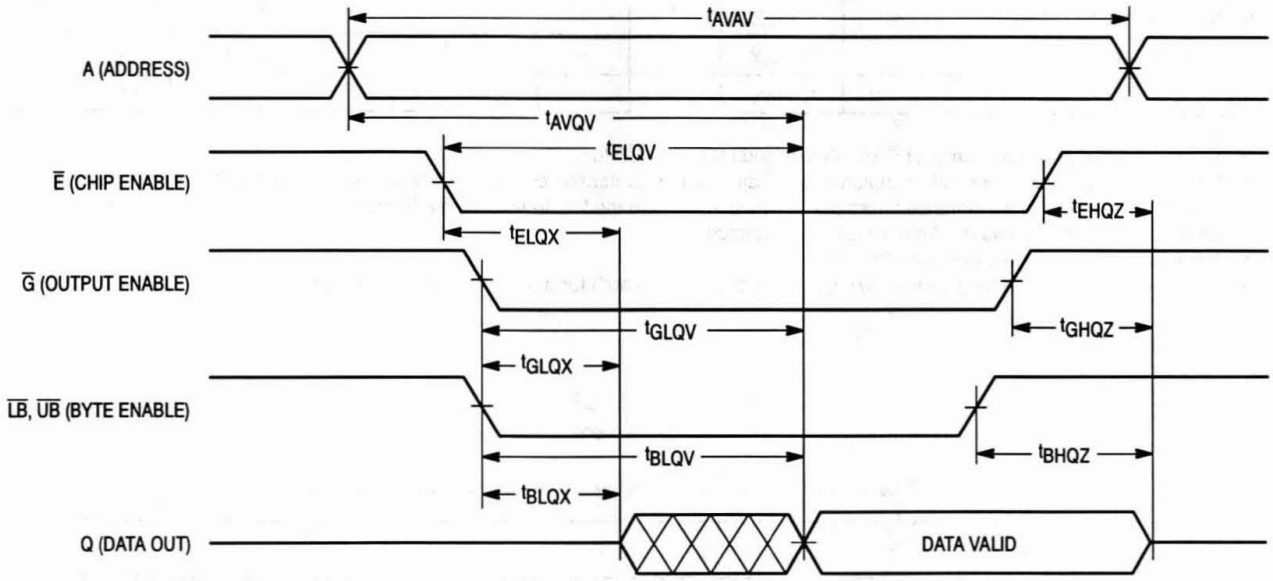
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Figure 1. AC Test Load

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

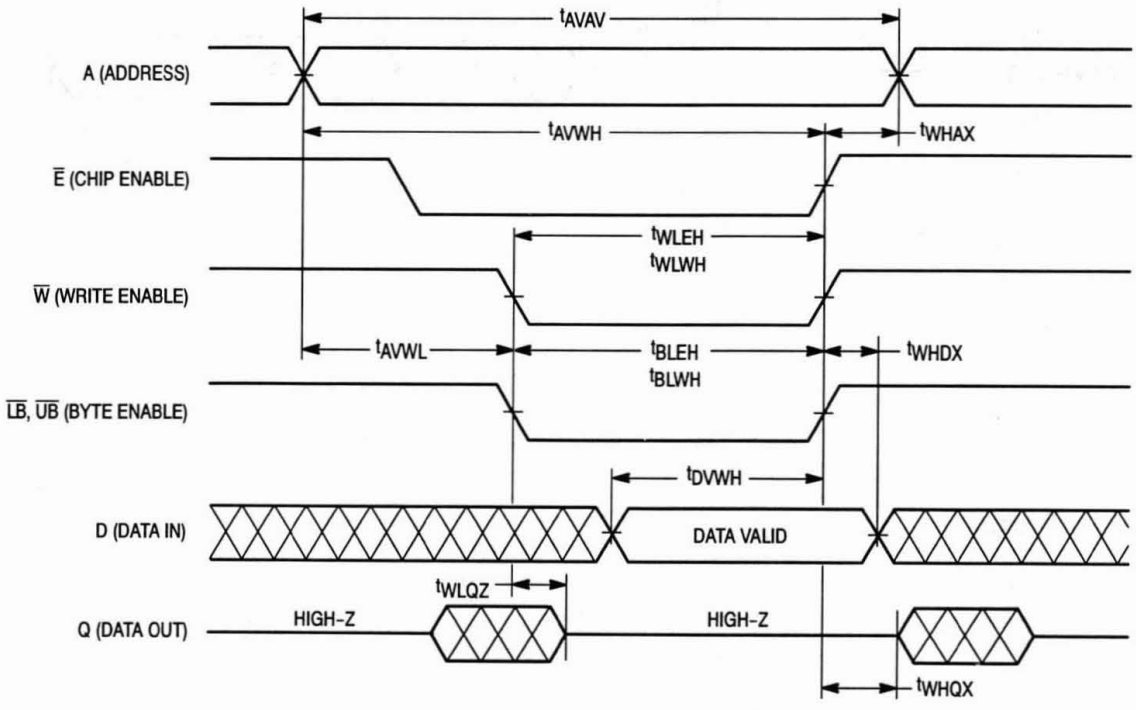


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6323A–10		MCM6323A–12		MCM6323A–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	8	—	9	—	10	—	ns	
Byte Pulse Width	t_{BLWH}, t_{BLEH}	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	4	0	5	0	6	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low, $\overline{W}$ low, and $\overline{LB}$ and/or $\overline{UB}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1
($\overline{W}$ Controlled)

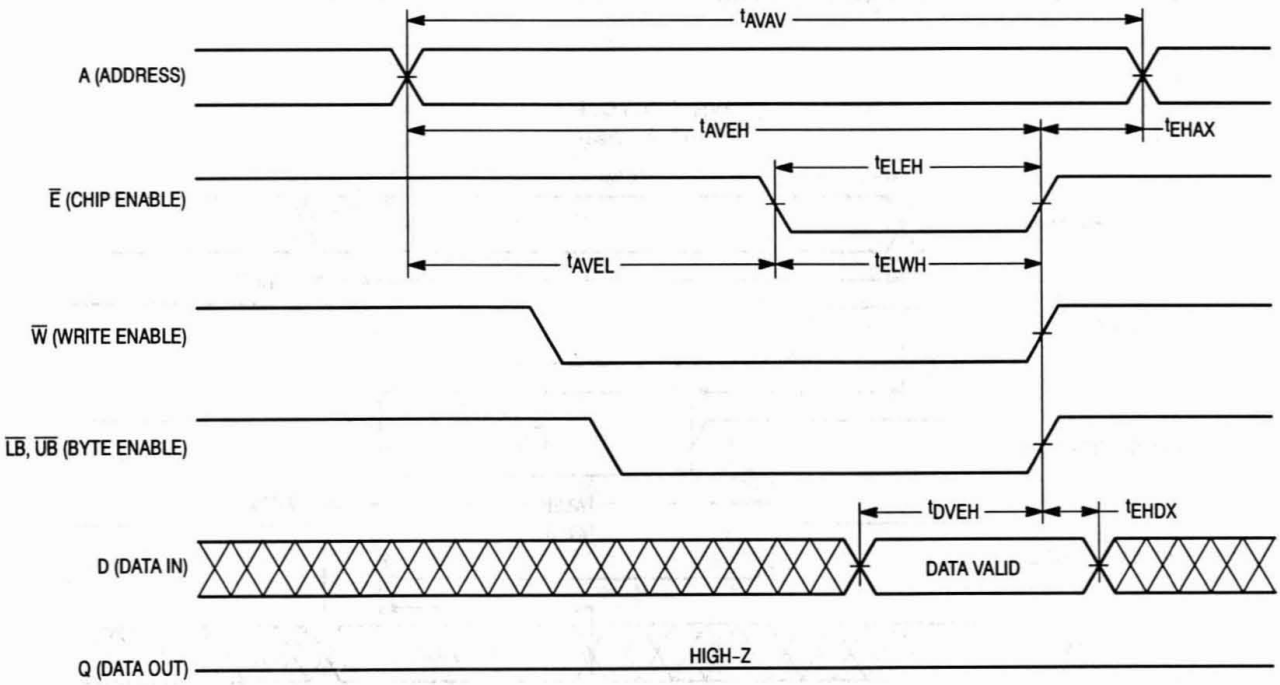


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6323A–10		MCM6323A–12		MCM6323A–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	8	—	9	—	10	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	8	—	9	—	10	—	ns	4, 5
Data Valid to End of Write	t_{DVEH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low, $\overline{W}$ low, and $\overline{LB}$ and/or $\overline{UB}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2
($\overline{E}$ Controlled)

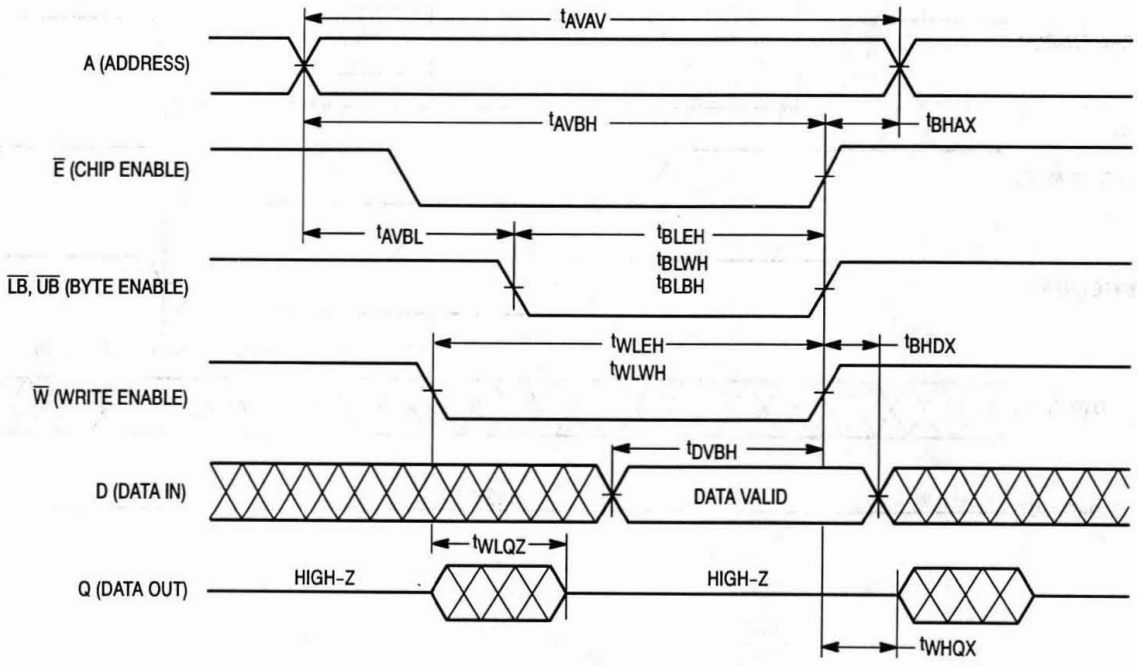


WRITE CYCLE 3 ($\overline{B}$ Controlled, See Notes 1 and 2)

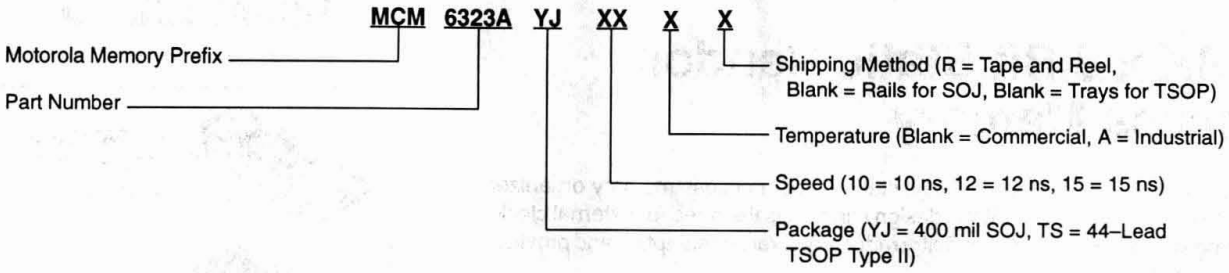
Parameter	Symbol	MCM6323A–10		MCM6323A–12		MCM6323A–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVBL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVBH}	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	8	—	9	—	10	—	ns	
Byte Pulse Width	t_{BLWH}, t_{BLEH}, t_{BLBH}	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVBH}	5	—	6	—	7	—	ns	
Data Hold Time	t_{BHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	4	0	5	0	6	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	4, 5, 6
Write Recovery Time	t_{BHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low, $\overline{W}$ low, and $\overline{LB}$ and/or $\overline{UB}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 3
($\overline{B}$ Controlled)



ORDERING INFORMATION
(Order by Full Part Number)


MCM 6323A YJ XX X X
Motorola Memory Prefix
Part Number
Shipping Method (R = Tape and Reel, Blank = Rails for SOJ, Blank = Trays for TSOP)
Temperature (Blank = Commercial, A = Industrial)
Speed (10 = 10 ns, 12 = 12 ns, 15 = 15 ns)
Package (YJ = 400 mil SOJ, TS = 44–Lead TSOP Type II)

Full Commercial Part Numbers —	MCM6323AYJ10	MCM6323AYJ12	MCM6323AYJ15
	MCM6323AYJ10R	MCM6323AYJ12R	MCM6323AYJ15R
	MCM6323ATS10	MCM6323ATS12	MCM6323ATS15
	MCM6323ATS10R	MCM6323ATS12R	MCM6323ATS15R
Full Industrial Part Numbers —	SCM6323AYJ10A	SCM6323AYJ12A	SCM6323AYJ15A
	SCM6323AYJ10AR	SCM6323AYJ12AR	SCM6323AYJ15AR
	SCM6323ATS10A	SCM6323ATS12A	SCM6323ATS15A
	SCM6323ATS10AR	SCM6323ATS12AR	SCM6323ATS15AR

MCM6226B

128K x 8 Bit Static Random Access Memory

2

The MCM6226B is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits. Static design eliminates the need for external clocks or timing strobes while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6226B is equipped with both chip enable ($\overline{E1}$ and E2) and output enable ($\overline{G}$) pins, allowing for greater system flexibility and eliminating bus contention problems.

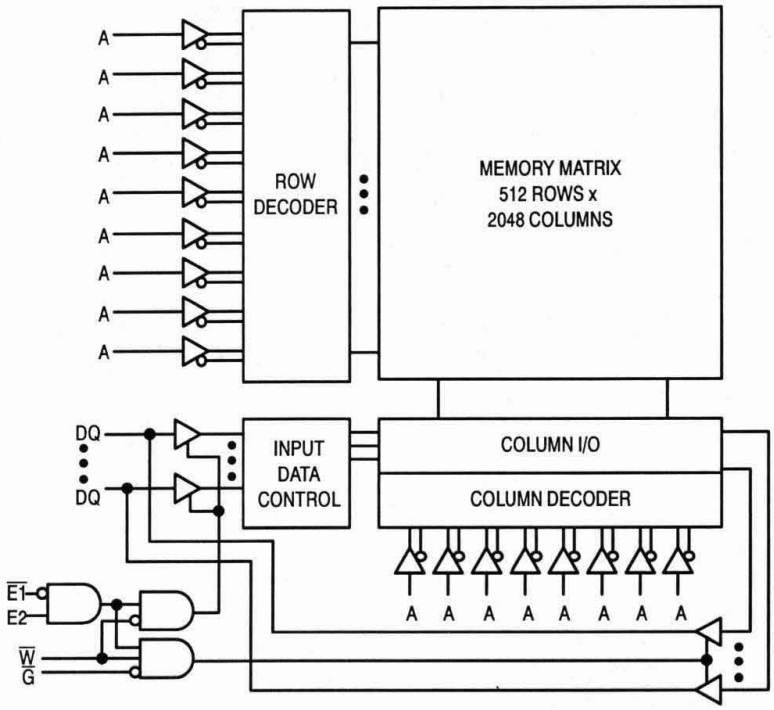
The MCM6226B is available in 300 mil and 400 mil, 32 lead surface–mount SOJ packages.

- Single 5 V ± 10% Power Supply
- Fast Access Times: 15/17/20/25/35 ns
- Equal Address and Chip Enable Access Times
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Low Power Operation: 130/125/120/115/110 mA Maximum, Active AC

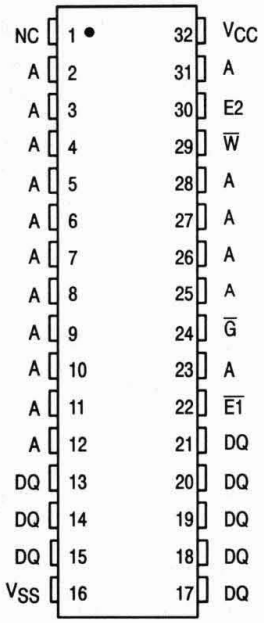
WJ PACKAGE
400 MIL SOJ
CASE 857A–02

J PACKAGE
300 MIL SOJ
CASE 857–02

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

A	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$, E2	Chip Enables
DQ	Data Inputs/Outputs
NC	No Connection
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

REV 3
10/28/96

TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	X	Not Selected	High–Z	—	I_{SB1}, I_{SB2}
X	L	X	X	Not Selected	High–Z	—	I_{SB1}, I_{SB2}
L	H	H	H	Output Disabled	High–Z	—	I_{CCA}
L	H	L	H	Read	D_{out}	Read	I_{CCA}
L	H	X	L	Write	D_{in}	Write	I_{CCA}

H = High, L = Low, X = Don't Care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.1	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns).
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E}$* = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	± 1	µA
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max)	MCM6226B–15: t_{AVAV} = 15 ns	I_{CCA}	—	130	mA
	MCM6226B–17: t_{AVAV} = 17 ns		—	125	
	MCM6226B–20: t_{AVAV} = 20 ns		—	120	
	MCM6226B–25: t_{AVAV} = 25 ns		—	115	
	MCM6226B–35: t_{AVAV} = 35 ns		—	110	
AC Standby Current (V_{CC} = max, $\overline{E}$* = V_{IH}, f ≤ f_{max})	MCM6226B–15: t_{AVAV} = 15 ns	I_{SB1}	—	40	mA
	MCM6226B–17: t_{AVAV} = 17 ns		—	35	
	MCM6226B–20: t_{AVAV} = 20 ns		—	30	
	MCM6226B–25: t_{AVAV} = 25 ns		—	25	
	MCM6226B–35: t_{AVAV} = 35 ns		—	20	
CMOS Standby Current ($\overline{E}$* ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V, V_{CC} = max, f = 0 MHz)		I_{SB2}	—	5	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	—	V

*$\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except Clocks and DQs $\overline{E1}$, E2, $\overline{G}$, and $\overline{W}$	C_{in} C_{ck}	4 5	6 8	pF
I/O Capacitance	DQ	$C_{I/O}$	5	8	pF

2

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1a

READ CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	6226B–15		6226B–17		6226B–20		6226B–25		6226B–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	4
Address Access Time	t_{AVQV}	—	15	—	17	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	—	15	—	17	—	20	—	25	—	35	ns	5
Output Enable Access Time	t_{GLQV}	—	6	—	7	—	7	—	8	—	8	ns	
Output Hold from Address Change	t_{AXQX}	5	—	5	—	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	5	—	5	—	5	—	5	—	ns	6, 7, 8
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	0	—	ns	6, 7, 8
Enable High to Output High–Z	t_{EHQZ}	—	6	—	7	—	7	—	8	—	8	ns	6, 7, 8
Output Enable High to Output High–Z	t_{GHQZ}	—	6	—	7	—	7	—	8	—	8	ns	6, 7, 8

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.
4. All timings are referenced from the last valid address to the first transitioning address.
5. Addresses valid prior to or coincident with $\overline{E}$ going low.
6. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
7. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1b.
8. This parameter is sampled and not 100% tested.
9. Device is continuously selected ($\overline{E} \le V_{IL}$, $\overline{G} \le V_{IL}$).

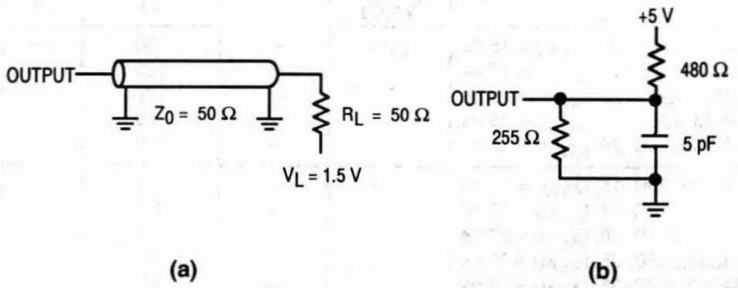
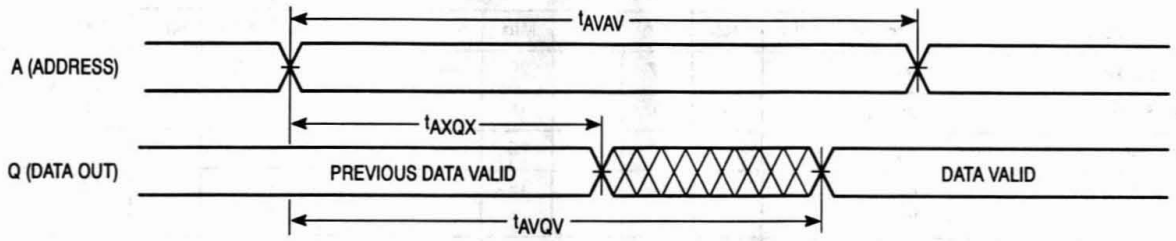


Figure 1. AC Test Loads

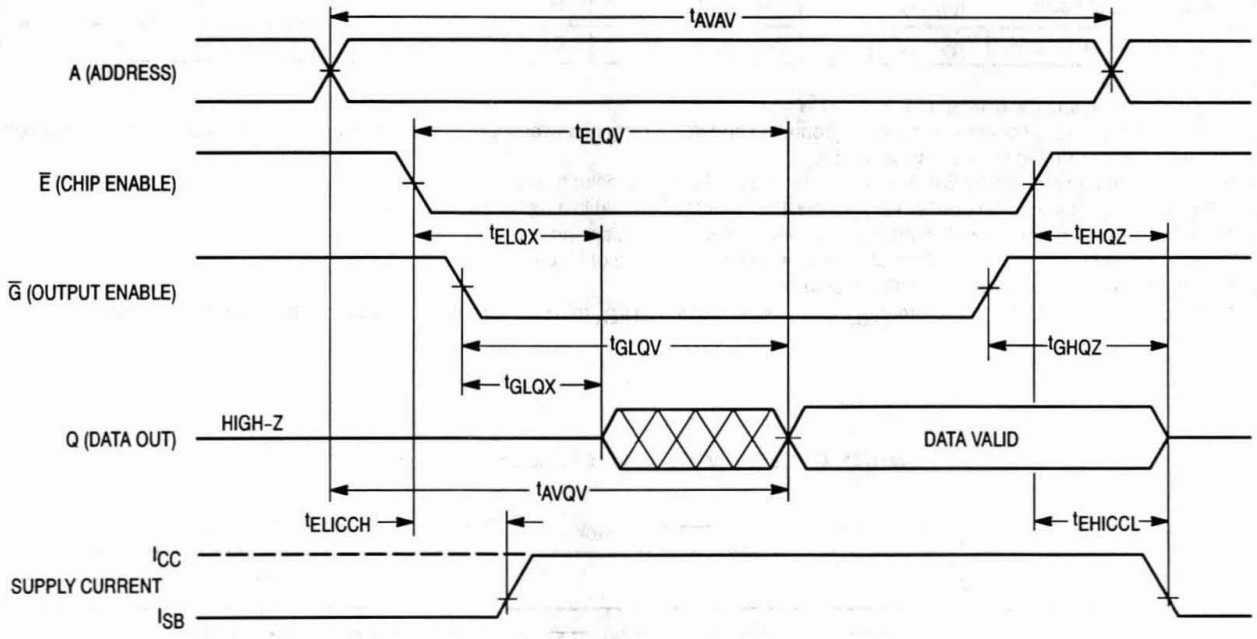
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Notes 1, 2, 3, and 9)



READ CYCLE 2 (See Notes 3 and 5)

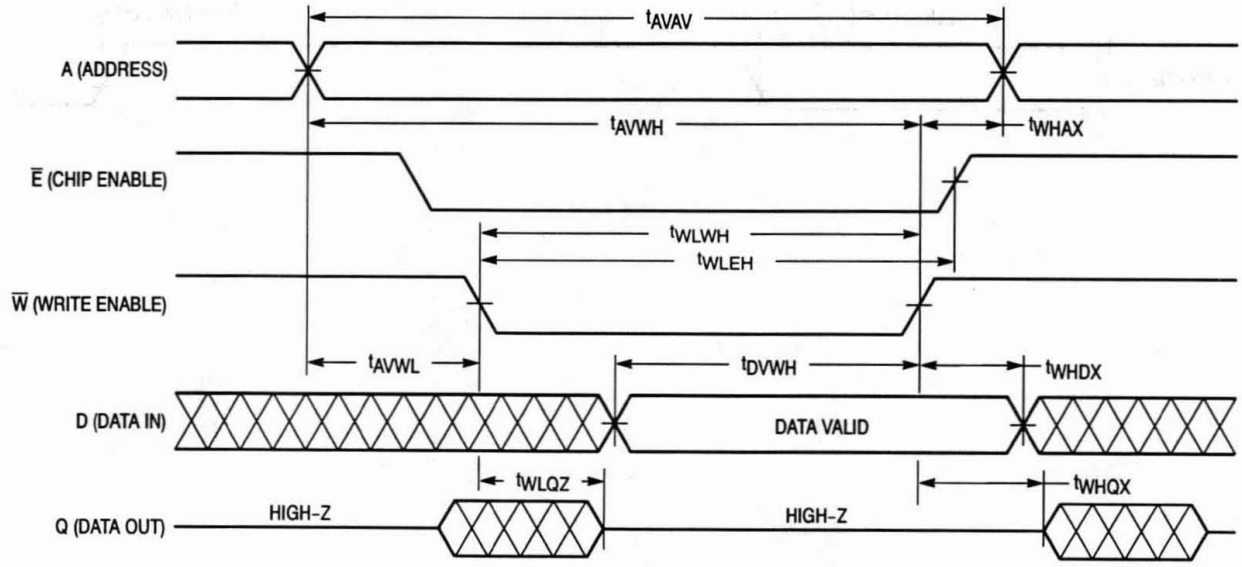


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, 3, and 4)

Parameter	Symbol	6226B–15		6226B–17		6226B–20		6226B–25		6226B–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	5
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	14	—	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVWH}	7	—	8	—	8	—	10	—	11	—	ns	
Data Hold TIme	t_{WHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	—	6	—	7	—	7	—	8	—	8	ns	6, 7, 8
Write High to Output Active	t_{WHQX}	5	—	5	—	5	—	5	—	5	—	ns	6, 7, 8
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.
4. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
5. All timings are referenced from the last valid address to the first transitioning address.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1b.
7. This parameter is sampled and not 100% tested.
8. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled See Notes 1, 2, 3, and 4)

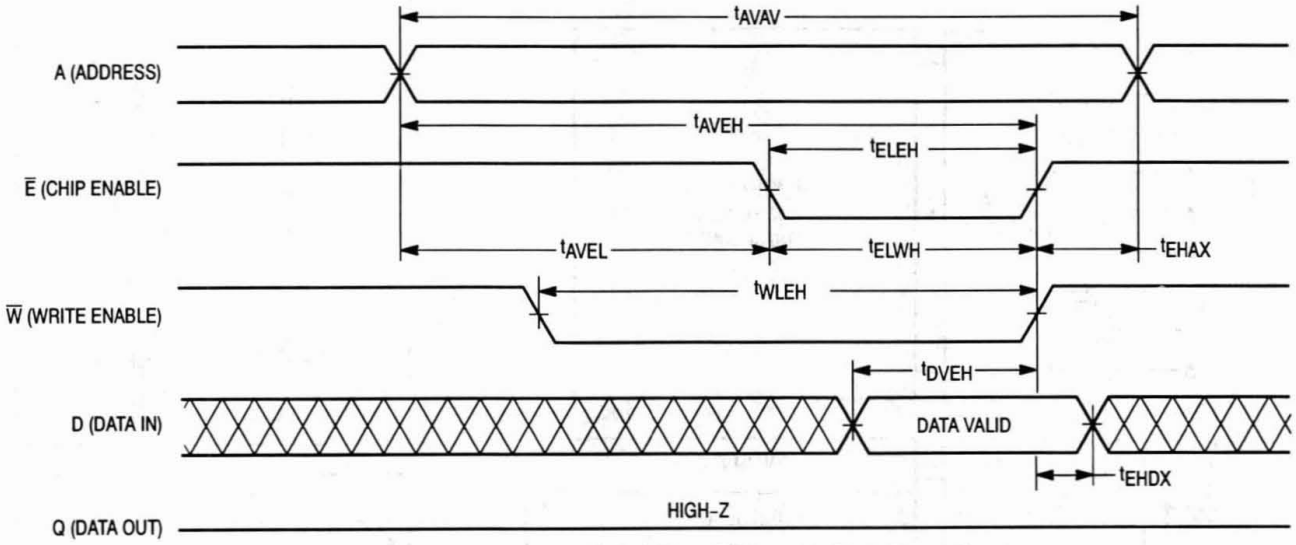


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, 3, and 4)

Parameter	Symbol	6226B–15		6226B–17		6226B–20		6226B–25		6226B–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	5
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	12	—	14	—	15	—	17	—	20	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	10	—	11	—	12	—	15	—	20	—	ns	6, 7
Write Pulse Width	t_{WLEH}	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	7	—	8	—	8	—	10	—	11	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.
4. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
5. All timings are referenced from the last valid address to the first transitioning address.
6. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
7. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high–impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled See Notes 1, 2, 3, and 4)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6226B X XX XX

Motorola Memory Prefix

Part Number

Shipping Method (R2 = Tape and Reel, Blank = Rails)

Speed (15 = 15 ns, 17 = 17 ns, 20 = 20 ns, 25 = 25 ns, 35 = 35 ns)

Package (WJ = 400 mil SOJ, J = 300 mil SOJ)

Full Part Numbers —				
	MCM6226BJ15	MCM6226BJ15R2	MCM6226BWJ15	MCM6226BWJ15R2
	MCM6226BJ17	MCM6226BJ17R2	MCM6226BWJ17	MCM6226BWJ17R2
	MCM6226BJ20	MCM6226BJ20R2	MCM6226BWJ20	MCM6226BWJ20R2
	MCM6226BJ25	MCM6226BJ25R2	MCM6226BWJ25	MCM6226BWJ25R2
	MCM6226BJ35	MCM6226BJ35R2	MCM6226BWJ35	MCM6226BWJ35R2

MCM6226BB

2

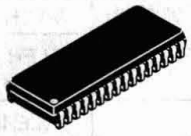
128K x 8 Bit Static Random Access Memory

The MCM6226BB is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits. Static design eliminates the need for external clocks or timing strobes while CMOS circuitry reduces power consumption and provides for greater reliability.

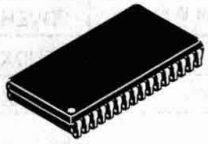
The MCM6226BB is equipped with both chip enable ($\overline{E1}$ and E2) and output enable ($\overline{G}$) pins, allowing for greater system flexibility and eliminating bus contention problems.

The MCM6226BB is available in 300 mil and 400 mil, 32 lead surface–mount SOJ packages.

- Single 5 V ± 10% Power Supply
- Fast Access Times: 15/17/20/25/35 ns
- Equal Address and Chip Enable Access Times
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Low Power Operation: 190/180/165/150/130 mA Maximum, Active AC

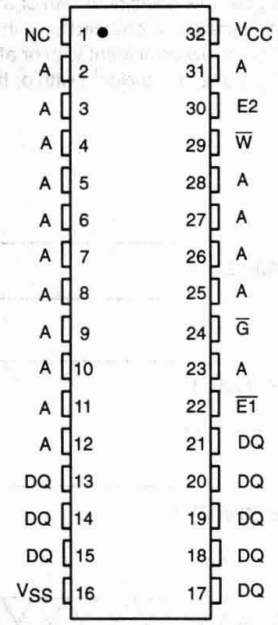


XJ PACKAGE
400 MIL SOJ
CASE 857A–02

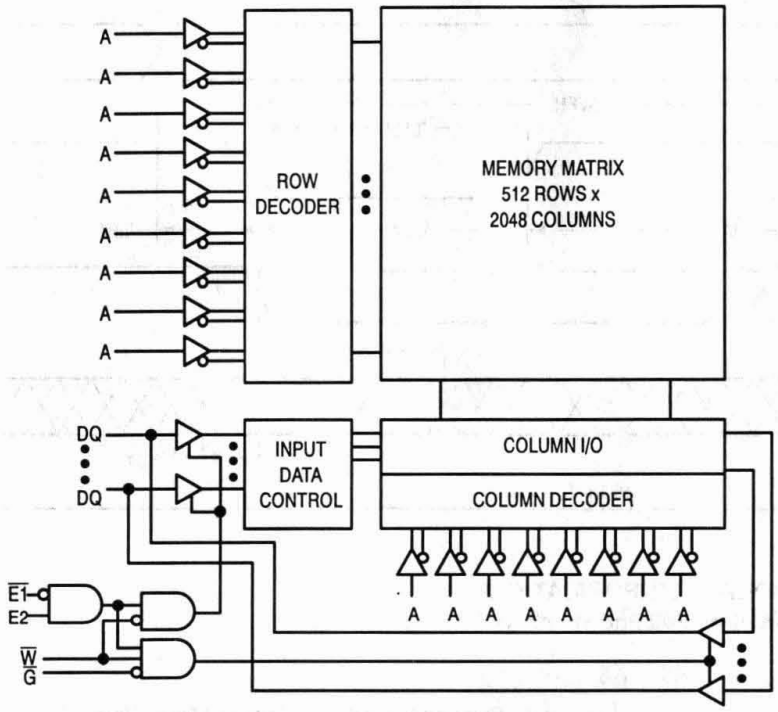


EJ PACKAGE
300 MIL SOJ
CASE 857–02

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$, E2	Chip Enables
DQ	Data Inputs/Outputs
NC	No Connection
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

REV 2
10/31/96

TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	X	Not Selected	High–Z	—	I_{SB1}, I_{SB2}
X	L	X	X	Not Selected	High–Z	—	I_{SB1}, I_{SB2}
L	H	H	H	Output Disabled	High–Z	—	I_{CCA}
L	H	L	H	Read	D_{out}	Read	I_{CCA}
L	H	X	L	Write	D_{in}	Write	I_{CCA}

H = High, L = Low, X = Don't Care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns).
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E}$* = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	± 1	µA
AC Active Supply Current (I_{out} = 0 mA, all inputs = V_{IL} or V_{IH}, V_{IL} = 0, V_{IH} ≥ 3 V, cycle time ≥ t_{AVAV} min, V_{CC} = max)	MCM6226BB–15: t_{AVAV} = 15 ns MCM6226BB–17: t_{AVAV} = 17 ns MCM6226BB–20: t_{AVAV} = 20 ns MCM6226BB–25: t_{AVAV} = 25 ns MCM6226BB–35: t_{AVAV} = 35 ns	I_{CCA}	— — — — —	195 180 165 150 130	mA
AC Standby Current (V_{CC} = max, $\overline{E}$* = V_{IH}, f = f_{max})	MCM6226BB–15: t_{AVAV} = 15 ns MCM6226BB–17: t_{AVAV} = 17 ns MCM6226BB–20: t_{AVAV} = 20 ns MCM6226BB–25: t_{AVAV} = 25 ns MCM6226BB–35: t_{AVAV} = 35 ns	I_{SB1}	— — — — —	45 40 35 30 25	mA
CMOS Standby Current ($\overline{E}$* ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V, V_{CC} = max, f = 0 MHz)		I_{SB2}	—	5	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	—	V

*$\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except Clocks and DQs $\overline{E1}$, E2, $\overline{G}$, and $\overline{W}$	C_{in} C_{ck}	4 5	6 8	pF
I/O Capacitance	DQ	$C_{I/O}$	5	8	pF

2

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1a

READ CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	6226BB–15		6226BB–17		6226BB–20		6226BB–25		6226BB–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	4
Address Access Time	t_{AVQV}	—	15	—	17	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	—	15	—	17	—	20	—	25	—	35	ns	5
Output Enable Access Time	t_{GLQV}	—	6	—	7	—	7	—	8	—	8	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	5	—	5	—	5	—	5	—	ns	6, 7, 8
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	0	—	ns	6, 7, 8
Enable High to Output High–Z	t_{EHQZ}	—	6	—	7	—	7	—	8	—	8	ns	6, 7, 8
Output Enable High to Output High–Z	t_{GHQZ}	—	6	—	7	—	7	—	8	—	8	ns	6, 7, 8

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.
4. All timings are referenced from the last valid address to the first transitioning address.
5. Addresses valid prior to or coincident with $\overline{E}$ going low.
6. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
7. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1b.
8. This parameter is sampled and not 100% tested.
9. Device is continuously selected ($\overline{E} \le V_{IL}$, $\overline{G} \le V_{IL}$).

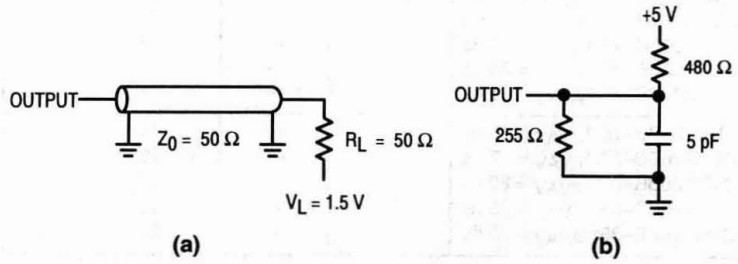
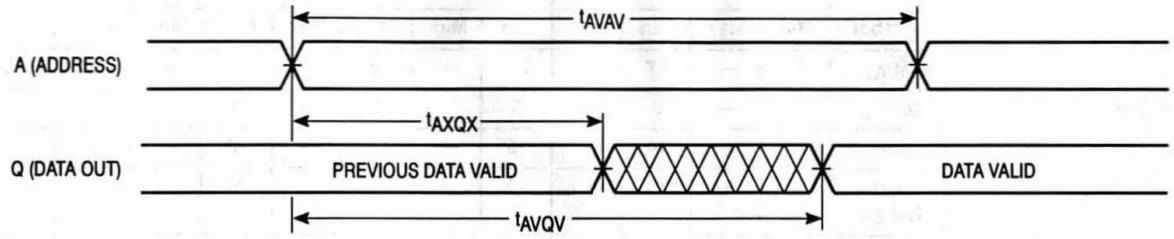


Figure 1. AC Test Loads

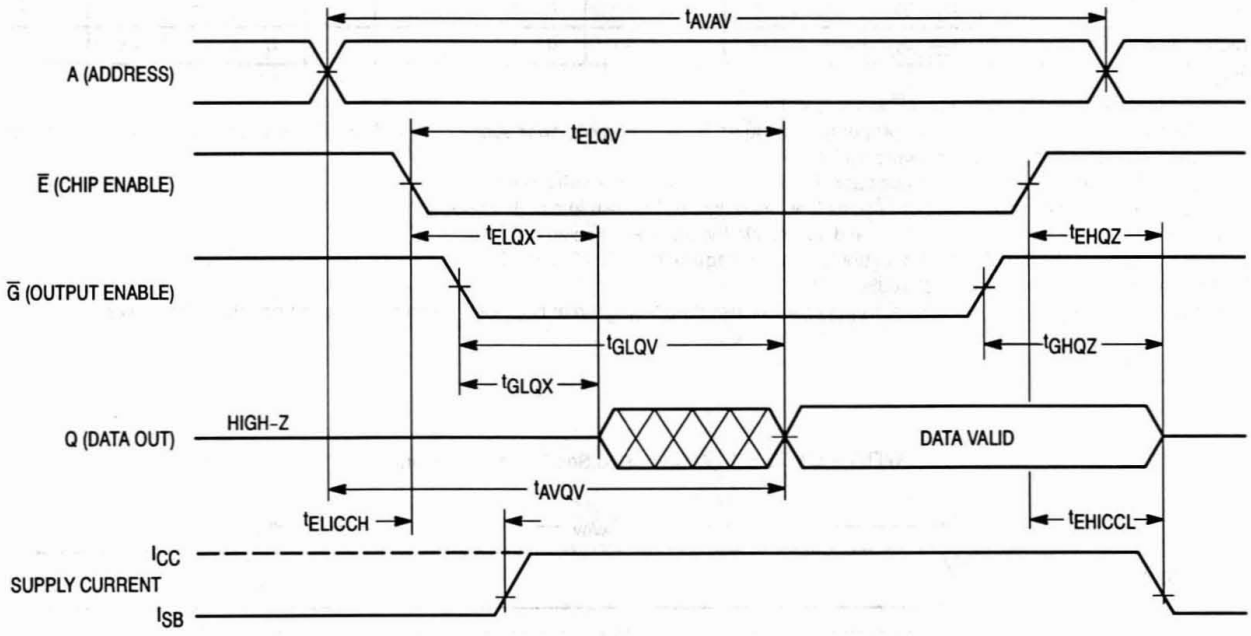
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Notes 1, 2, 3, and 9)



READ CYCLE 2 (See Notes 3 and 5)

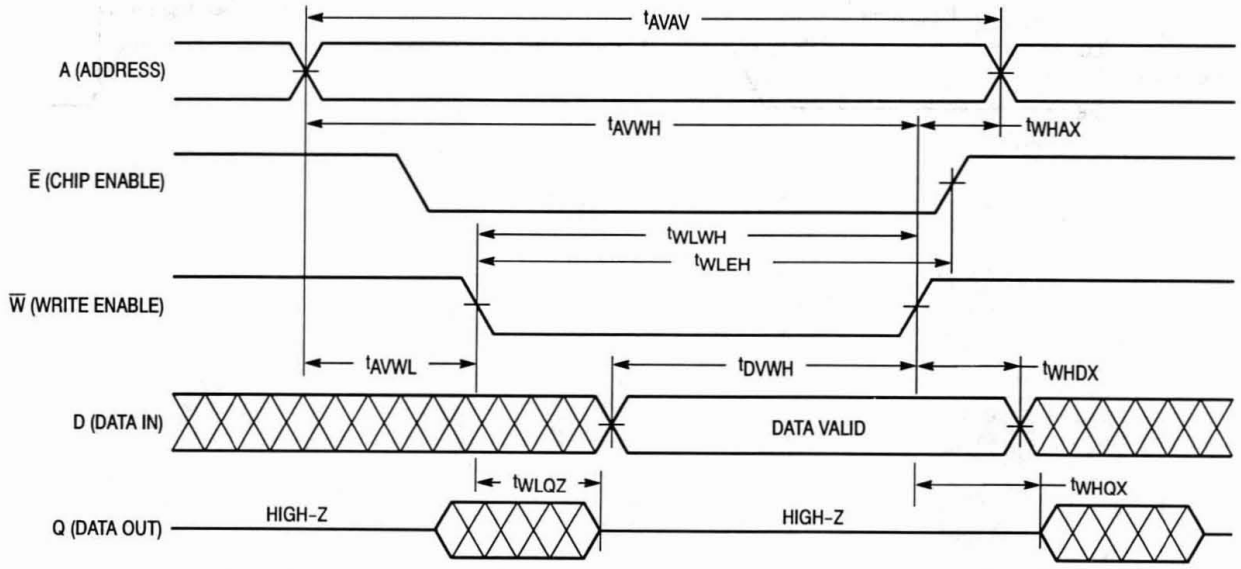


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, 3, and 4)

Parameter	Symbol	6226BB–15		6226BB–17		6226BB–20		6226BB–25		6226BB–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	5
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	14	—	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVWH}	7	—	8	—	9	—	10	—	11	—	ns	
Data Hold TIme	t_{WHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	—	6	—	7	—	7	—	8	—	8	ns	6, 7, 8
Write High to Output Active	t_{WHQX}	5	—	5	—	5	—	5	—	5	—	ns	6, 7, 8
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.
4. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
5. All timings are referenced from the last valid address to the first transitioning address.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1b.
7. This parameter is sampled and not 100% tested.
8. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled See Notes 1, 2, 3, and 4)

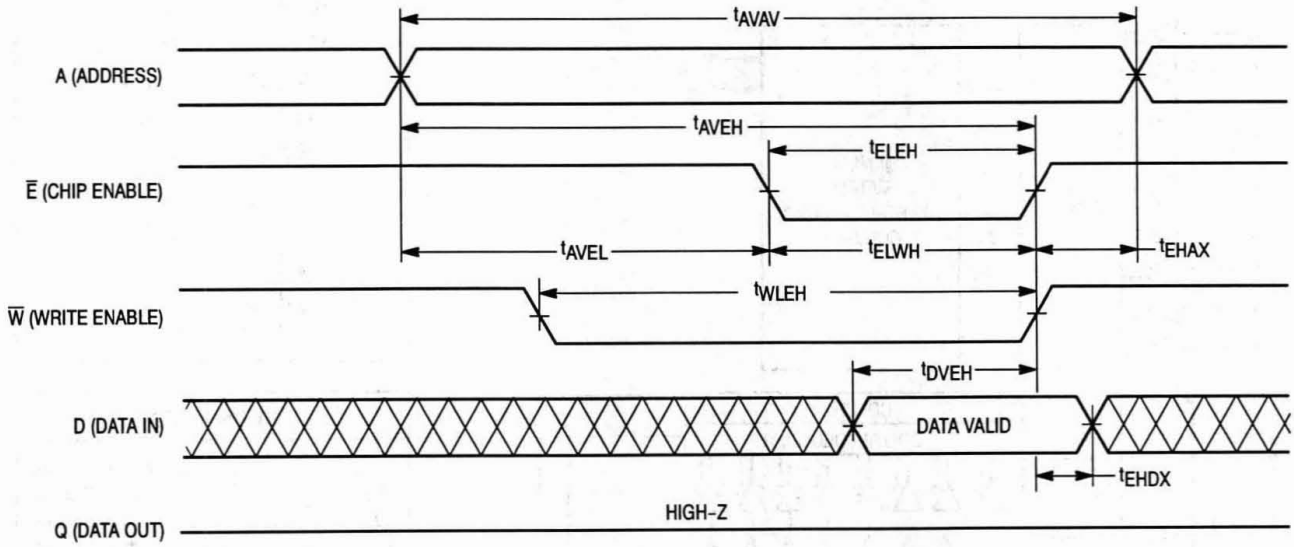


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, 3, and 4)

Parameter	Symbol	6226BB–15		6226BB–17		6226BB–20		6226BB–25		6226BB–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	5
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	12	—	14	—	15	—	17	—	20	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	12	—	14	—	15	—	17	—	20	—	ns	6, 7
Write Pulse Width	t_{WLEH}	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	7	—	8	—	9	—	10	—	11	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.
4. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
5. All timings are referenced from the last valid address to the first transitioning address.
6. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
7. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high–impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled See Notes 1, 2, 3, and 4)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6226BB XX XX XX

- Motorola Memory Prefix
- Part Number
- Shipping Method (R2 = Tape and Reel, Blank = Rails)
- Speed (15 = 15 ns, 17 = 17 ns, 20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
- Package (XJ = 400 mil SOJ, EJ = 300 mil SOJ)

Full Part Numbers —

MCM6226BBXJ15	MCM6226BBXJ15R2	MCM6226BBEJ15	MCM6226BBEJ15R2
MCM6226BBXJ17	MCM6226BBXJ17R2	MCM6226BBEJ17	MCM6226BBEJ17R2
MCM6226BBXJ20	MCM6226BBXJ20R2	MCM6226BBEJ20	MCM6226BBEJ20R2
MCM6226BBXJ25	MCM6226BBXJ25R2	MCM6226BBEJ25	MCM6226BBEJ25R2
MCM6226BBXJ35	MCM6226BBXJ35R2	MCM6226BBEJ35	MCM6226BBEJ35R2

MCM6726B

2

128K x 8 Bit Fast Static Random Access Memory

The MCM6726B is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits. Static design eliminates the need for external clocks or timing strobes.

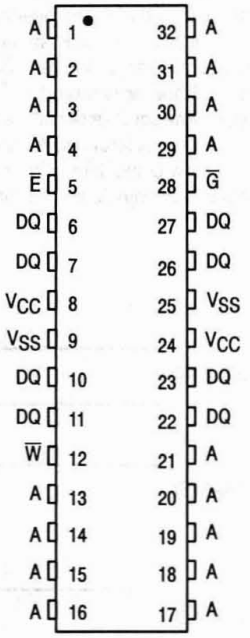
Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small–outline J–leaded package.

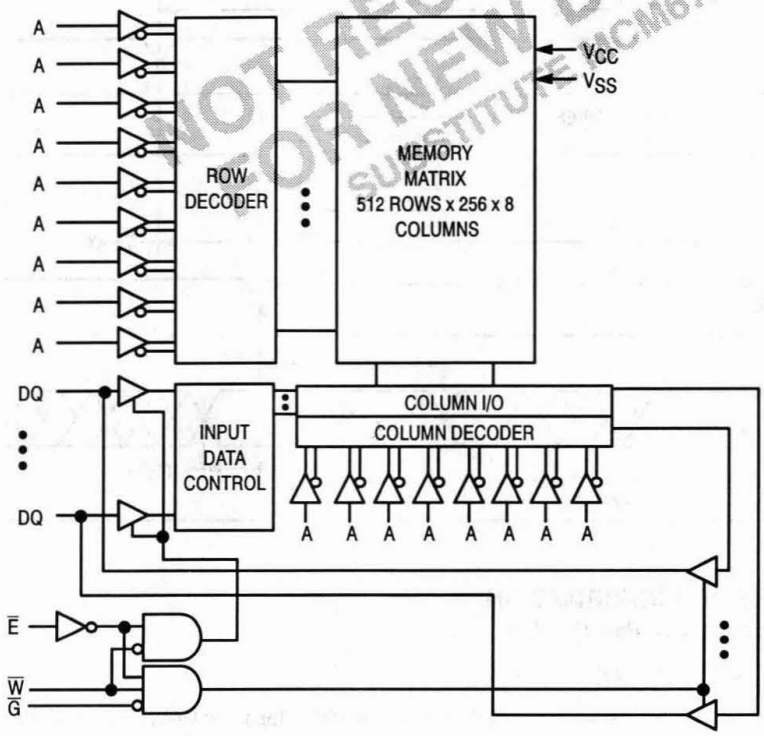
- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 8, 10, 12 ns
- Center Power and I/O Pins for Reduced Noise

WJ PACKAGE
400 MIL SOJ
CASE 857A–02

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

NOT RECOMMENDED FOR NEW DESIGNS
SUBSTITUTE MCM6726D

REV 4
4/7/97

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	H	Output Disabled	I_{CCA}	High–Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High–Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	1.2	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

2

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = –0.5 V dc; V_{IL} (min) = –2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	6726B–8	6726B–10	6726B–12	Unit	Notes
AC Active Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	I_{CCA}	195	175	165	mA	1, 2, 3
Active Quiescent Current ($\overline{E}$ = V_{IL}, V_{CC} = max, f = 0 MHz)	I_{CC2}	100	100	100	mA	
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	60	60	60	mA	1, 2, 3
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	20	mA	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
2. All addresses transition simultaneously low (LSB) and then high (MSB).
3. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

2

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

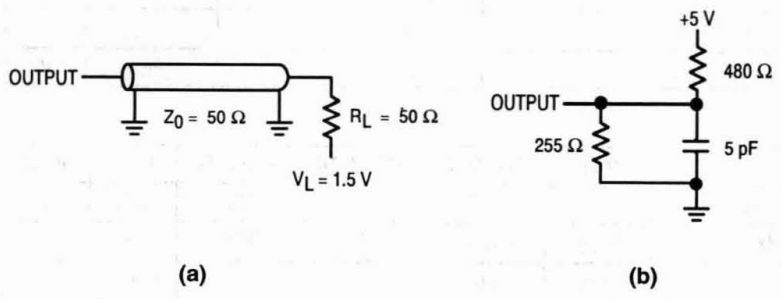
Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1a

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	6726B–8		6726B–10		6726B–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Access Time	t_{AVQV}	—	8	—	10	—	12	ns	
Enable Access Time	t_{ELQV}	—	8	—	10	—	12	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	5	—	6	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	3	—	3	—	3	—	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	—	4	—	5	—	6	ns	4,5,6
Output Enable High to Output High–Z	t_{GHQZ}	—	4	—	5	—	6	ns	4,5,6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1b.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.



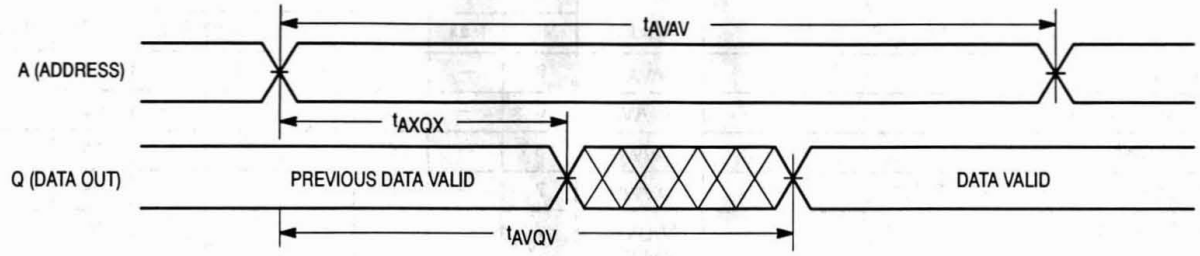
(a) (b)

Figure 1. AC Test Loads

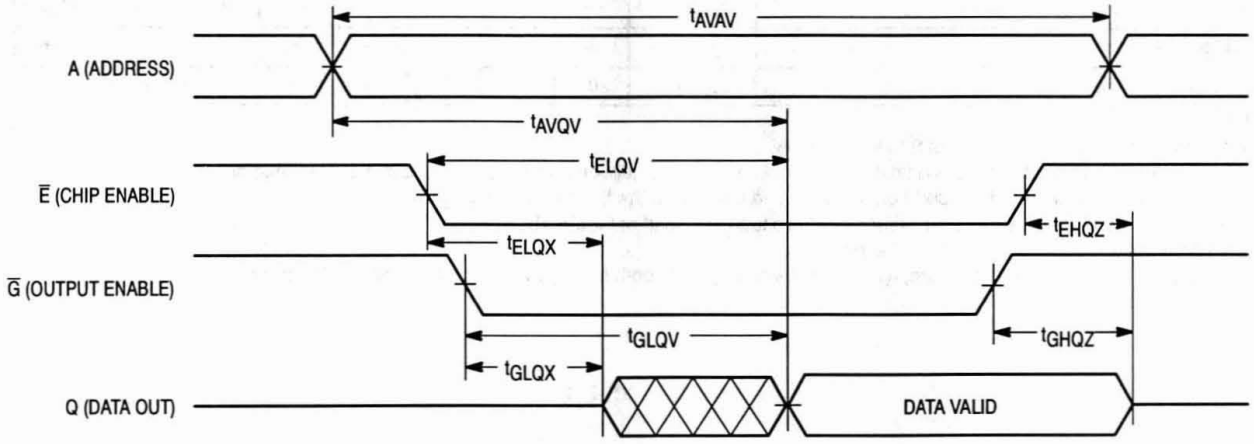
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

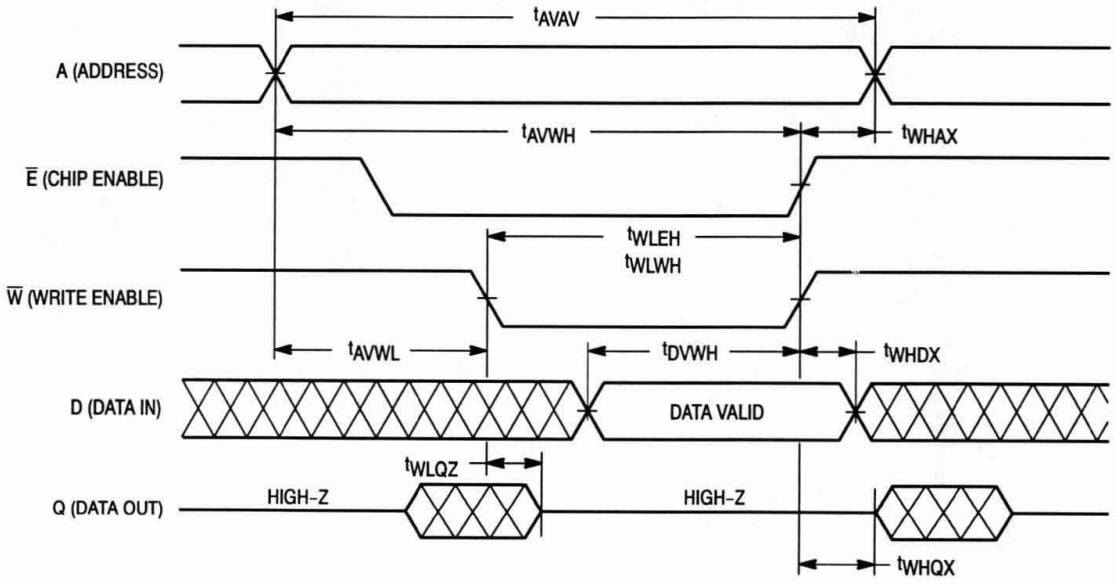


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6726B–8		6726B–10		6726B–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	8	—	9	—	10	—	ns	
Address Valid to End of Write, $\overline{G}$ High	t_{AVWH}	7	—	8	—	9	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	8	—	9	—	10	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	7	—	8	—	9	—	ns	
Data Valid to End of Write	t_{DVWH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	—	4	—	5	—	6	ns	4,5,6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage with load of Figure 1b.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

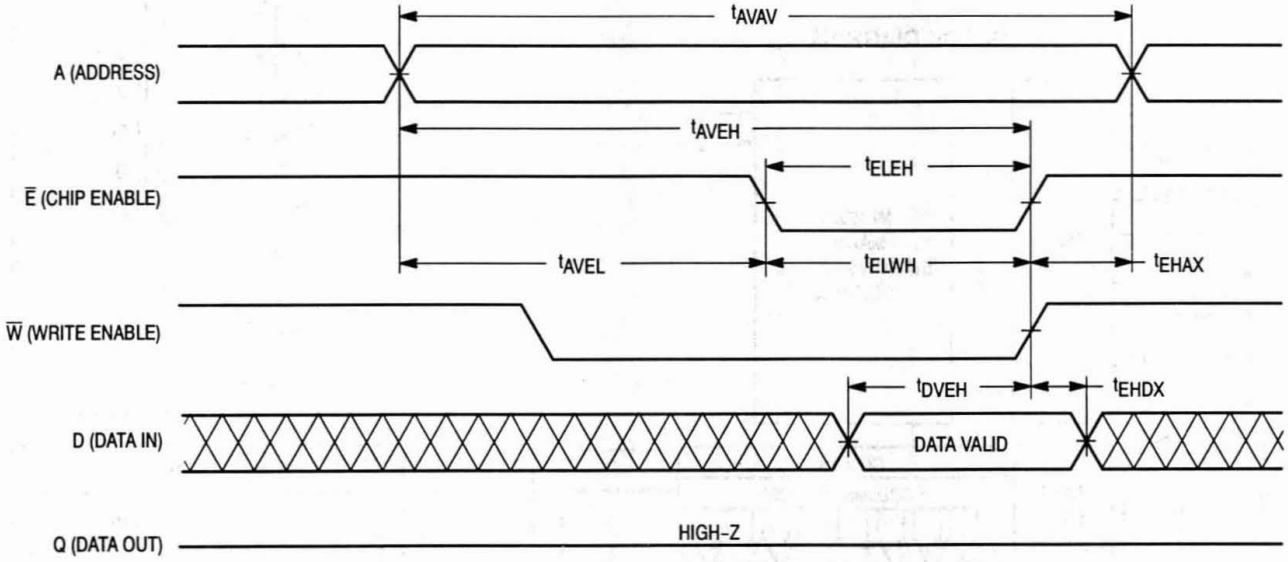


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6726B–8		6726B–10		6726B–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	7	—	8	—	9	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	7	—	8	—	9	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6726B WJ XX X

- MCM — Motorola Memory Prefix
- 6726B — Part Number
- WJ — Package (WJ = 400 mil SOJ)
- XX — Speed (8 = 8 ns, 10 = 10 ns, 12 = 12 ns)
- X — Shipping Method (R = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6726BWJ8, MCM6726BWJ8R, MCM6726BWJ10, MCM6726BWJ10R, MCM6726BWJ12, MCM6726BWJ12R

MCM6726C

128K x 8 Bit Fast Static Random Access Memory

2

The MCM6726C is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits. Static design eliminates the need for external clocks or timing strobes.

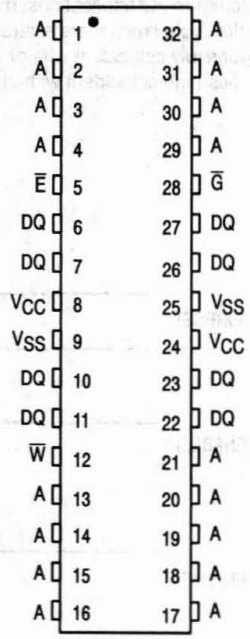
Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small–outline J–leaded package.

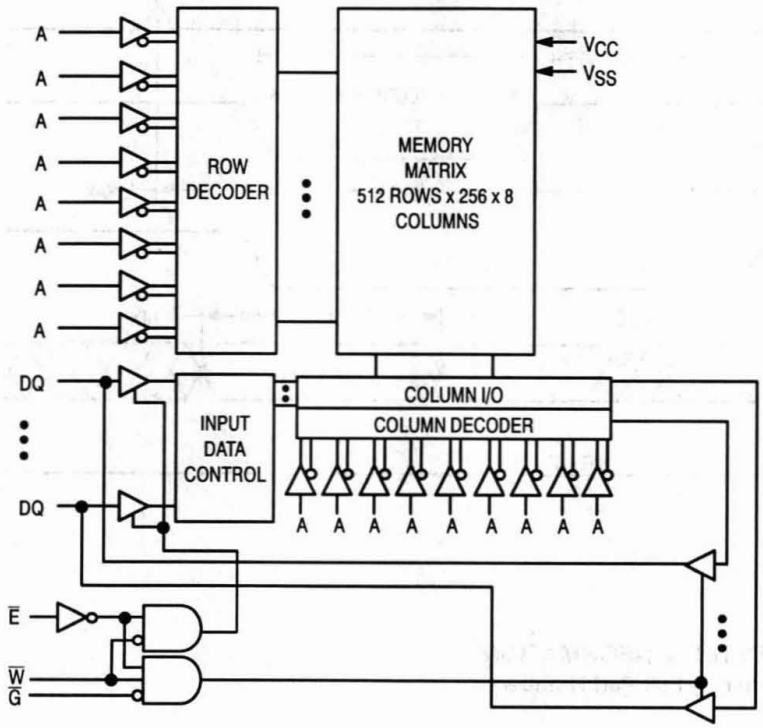
- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 6, 7 ns
- Center Power and I/O Pins for Reduced Noise

WJ PACKAGE
400 MIL SOJ
CASE 857A–02

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

REV 3
3/7/97

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	H	Output Disabled	I_{CCA}	High–Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High–Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	1.5	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = –0.5 V dc; V_{IL} (min) = –2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	MCM6726C–6	MCM6726C–7	Unit	Notes
AC Active Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	I_{CCA}	250	220	mA	1, 2, 3
Active Quiescent Current ($\overline{E}$ = V_{IL}, V_{CC} = max, f = 0 MHz)	I_{CC2}	100	100	mA	
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	100	100	mA	1, 2, 3
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V)	I_{SB2}	60	60	mA	

NOTES:
1. Reference AC Operating Conditions and Characterisitics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3 V, V_{IH} = 3 V).
2. All addresses transition simultaneously low (LSB) and then high (MSB).
3. Data States are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

2

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1a

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM6726C–6		MCM6726C–7		Unit	Notes
		Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	6	—	7	—	ns	3
Address Access Time	t_{AVQV}	—	6	—	7	ns	
Enable Access Time	t_{ELQV}	—	6	—	7	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	4	ns	
Output Hold from Address Change	t_{AXQX}	2	—	2	—	ns	
Enable Low to Output Active	t_{ELQX}	3	—	3	—	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	—	3	—	3.5	ns	4,5,6
Output Enable High to Output High–Z	t_{GHQZ}	—	3	—	3.5	ns	4,5,6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1b.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

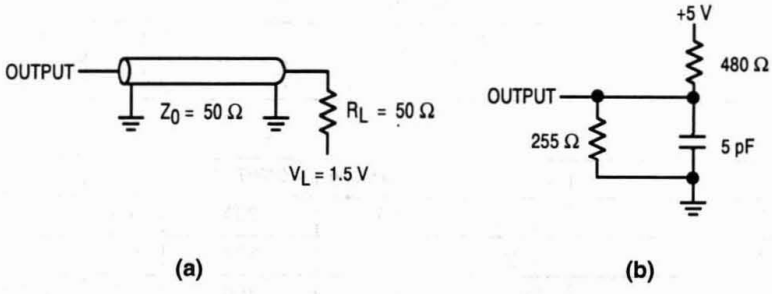
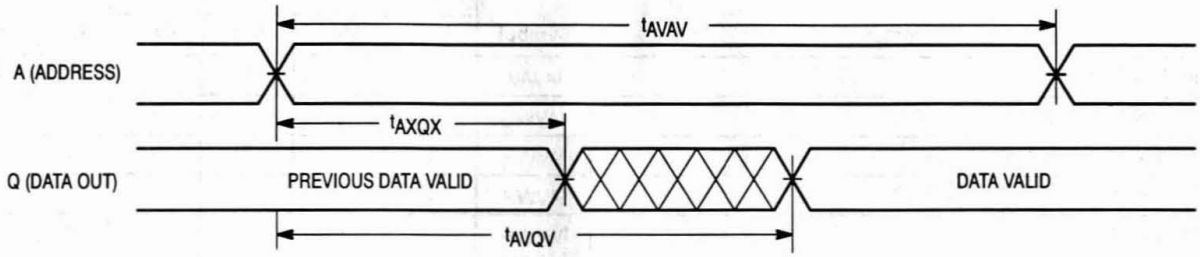


Figure 1. AC Test Loads

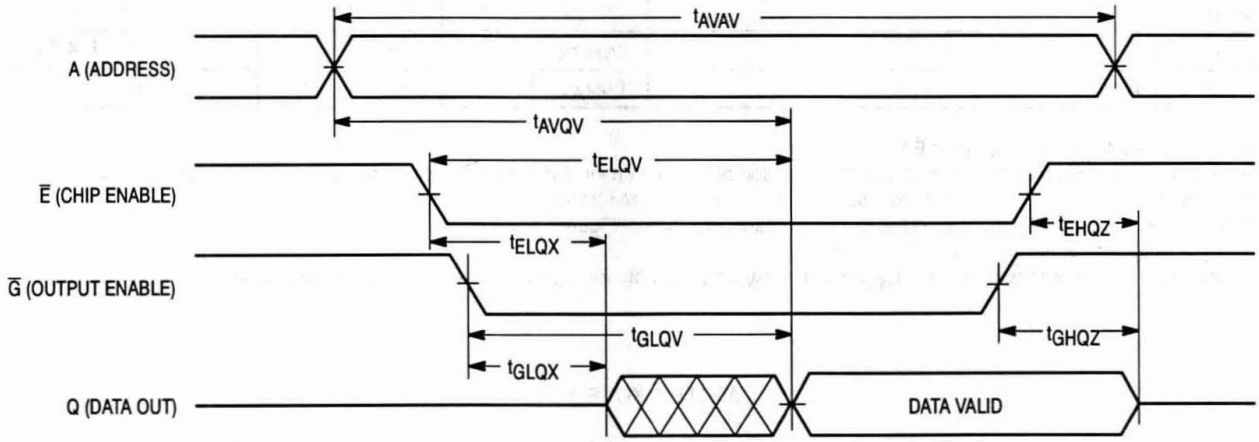
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

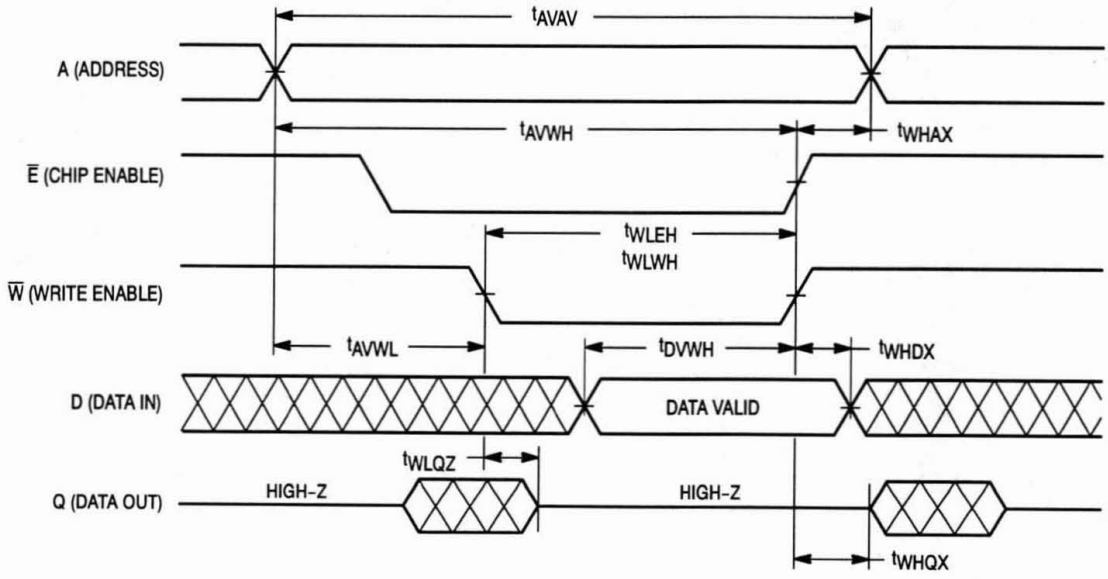


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6726C–6		MCM6726C–7		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	6	—	7	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	6	—	7	—	ns	
Address Valid to End of Write, $\overline{G}$ High	t_{AVWH}	6	—	7	—	ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	6	—	7	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH} t_{WLEH}	6	—	7	—	ns	
Data Valid to End of Write	t_{DVWH}	3	—	3.5	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	—	3.5	—	3.5	ns	4,5,6
Write High to Output Active	t_{WHQX}	3	—	3	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	1	—	1	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage with load of Figure 1b.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

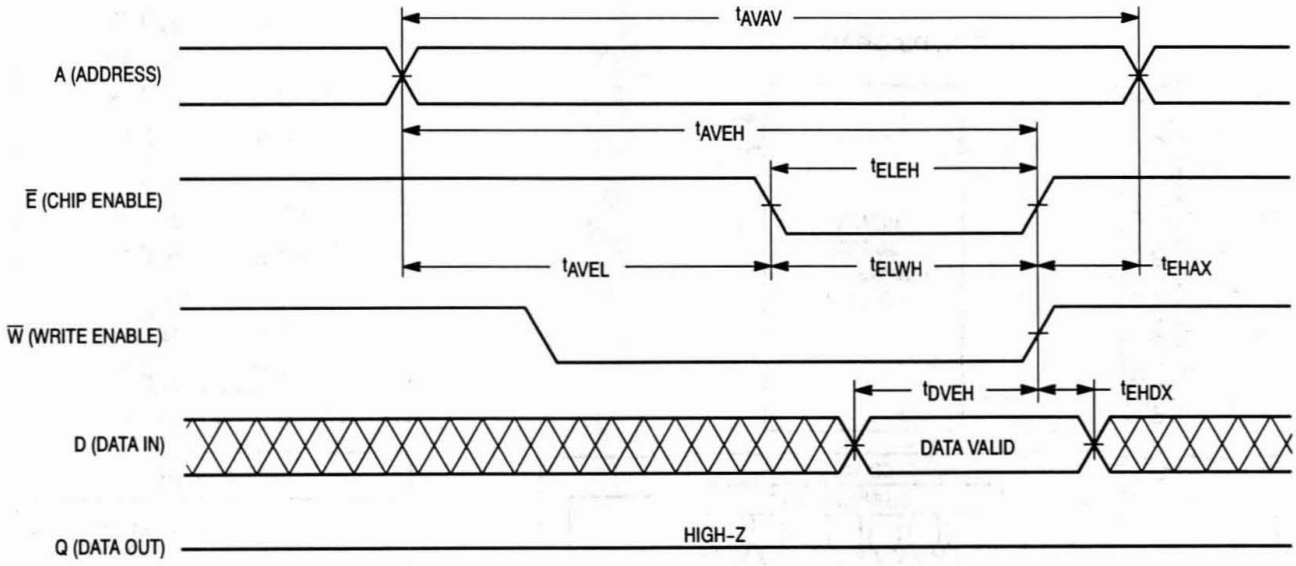


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6726C–6		MCM6726C–7		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	6	—	7	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	6	—	7	—	ns	
Enable to End of Write	t_{ELEH} t_{ELWH}	5	—	6	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	3	—	3.5	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6726C WJ X X

- MCM — Motorola Memory Prefix
- 6726C — Part Number
- WJ — Package (WJ = 400 mil SOJ)
- X — Speed (6 = 6 ns, 7 = 7 ns)
- X — Shipping Method (R = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6726CWJ6, MCM6726CWJ7, MCM6726CWJ6R, MCM6726CWJ7R

MCM6726D

2

128K x 8 Bit Fast Static Random Access Memory

WJ PACKAGE
400 MIL SOJ
CASE 857A–02

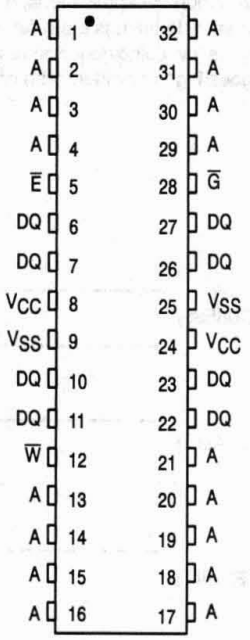
The MCM6726D is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

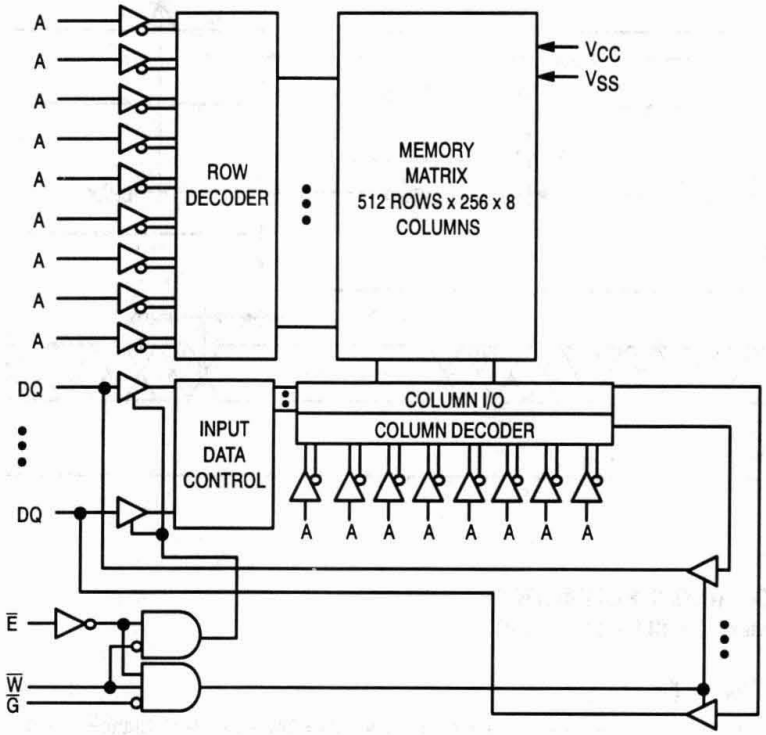
This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small–outline J–leaded package.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 8, 10, 12 ns
- Center Power and I/O Pins for Reduced Noise

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

10/9/96

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	H	Output Disabled	I_{CCA}	High–Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High–Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	1.2	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

*V_{IL} (min) = –0.5 V dc; V_{IL} (min) = –2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	6726D–8	6726D–10	6726D–12	Unit	Notes
AC Active Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	I_{CCA}	195	175	165	mA	1, 2, 3
Active Quiescent Current ($\overline{E}$ = V_{IL}, V_{CC} = max, f = 0 MHz)	I_{CC2}	100	100	100	mA	
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	60	60	60	mA	1, 2, 3
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	20	mA	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
2. All addresses transition simultaneously low (LSB) and then high (MSB).
3. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

2

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1a

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	6726D–8		6726D–10		6726D–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Access Time	t_{AVQV}	—	8	—	10	—	12	ns	
Enable Access Time	t_{ELQV}	—	8	—	10	—	12	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	5	—	6	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	3	—	3	—	3	—	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	—	4	—	5	—	6	ns	4,5,6
Output Enable High to Output High–Z	t_{GHQZ}	—	4	—	5	—	6	ns	4,5,6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1b.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

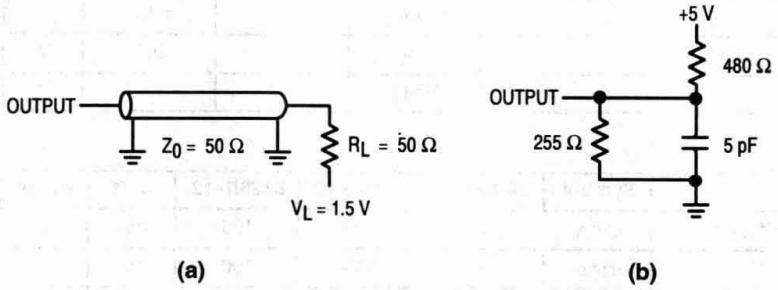
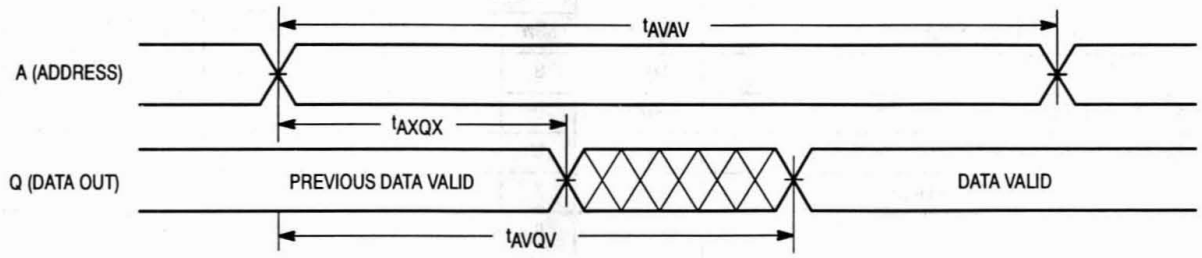


Figure 1. AC Test Loads

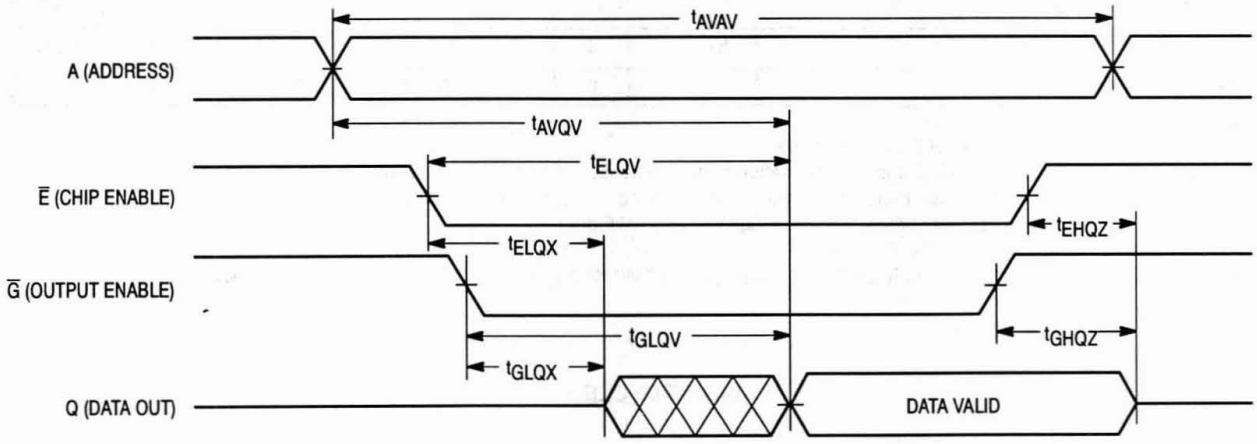
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

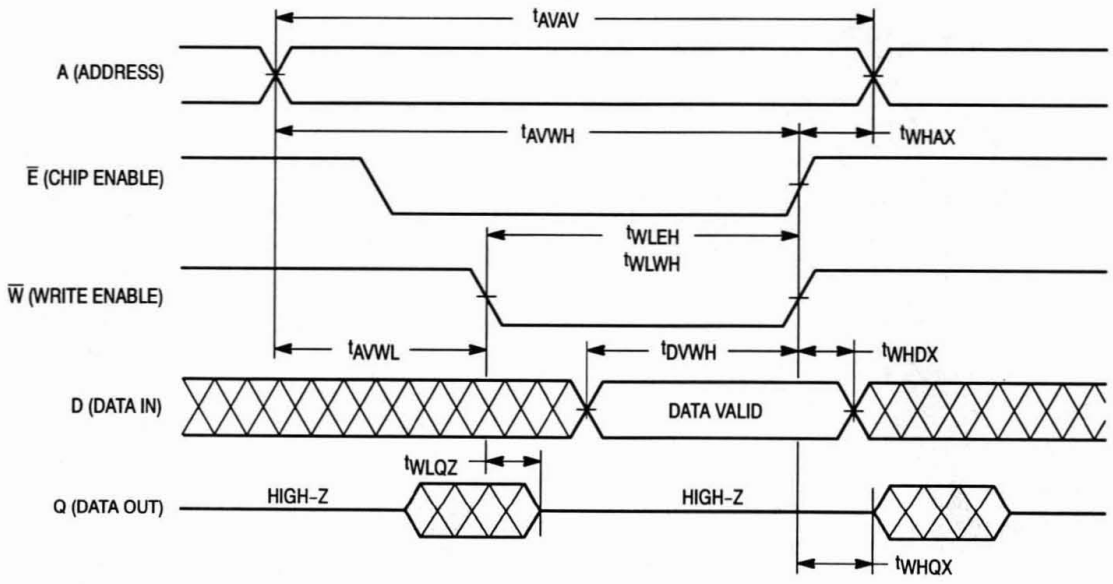


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6726D–8		6726D–10		6726D–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	8	—	9	—	10	—	ns	
Address Valid to End of Write, $\overline{G}$ High	t_{AVWH}	7	—	8	—	9	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	8	—	9	—	10	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	7	—	8	—	9	—	ns	
Data Valid to End of Write	t_{DVWH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	—	4	—	5	—	6	ns	4,5,6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage with load of Figure 1b.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

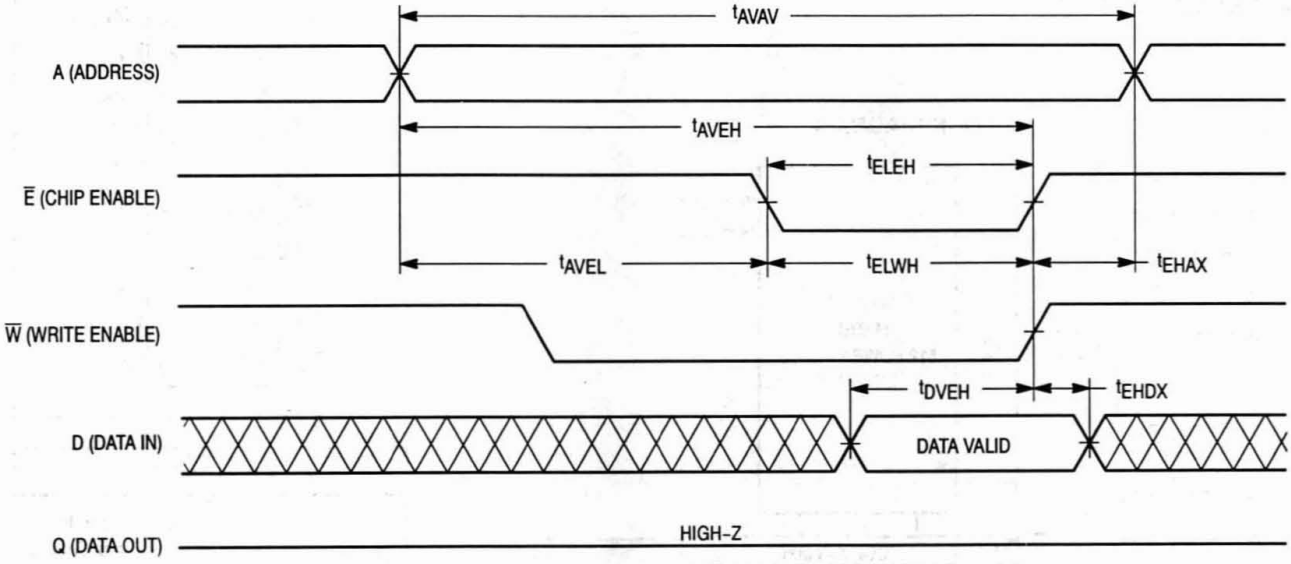


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6726D–8		6726D–10		6726D–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	7	—	8	—	9	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	7	—	8	—	9	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6726D WJ XX X

- Motorola Memory Prefix
- Part Number
- Shipping Method (R = Tape and Reel, Blank = Rails)
- Speed (8 = 8 ns, 10 = 10 ns, 12 = 12 ns)
- Package (WJ = 400 mil SOJ)

Full Part Numbers — MCM6726DWJ8, MCM6726DWJ8R, MCM6726DWJ10, MCM6726DWJ10R, MCM6726DWJ12, MCM6726DWJ12R

MCM6926

2

Advance Information

128K x 8 Bit Fast Static Random Access Memory

WJ PACKAGE
400 MIL SOJ
CASE 857A–02

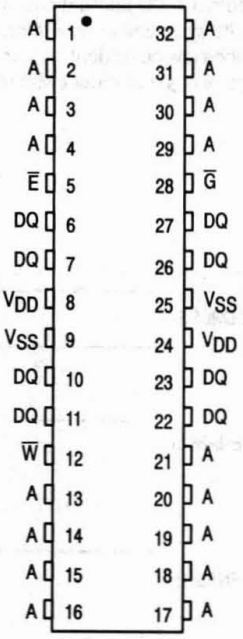
The MCM6926 is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

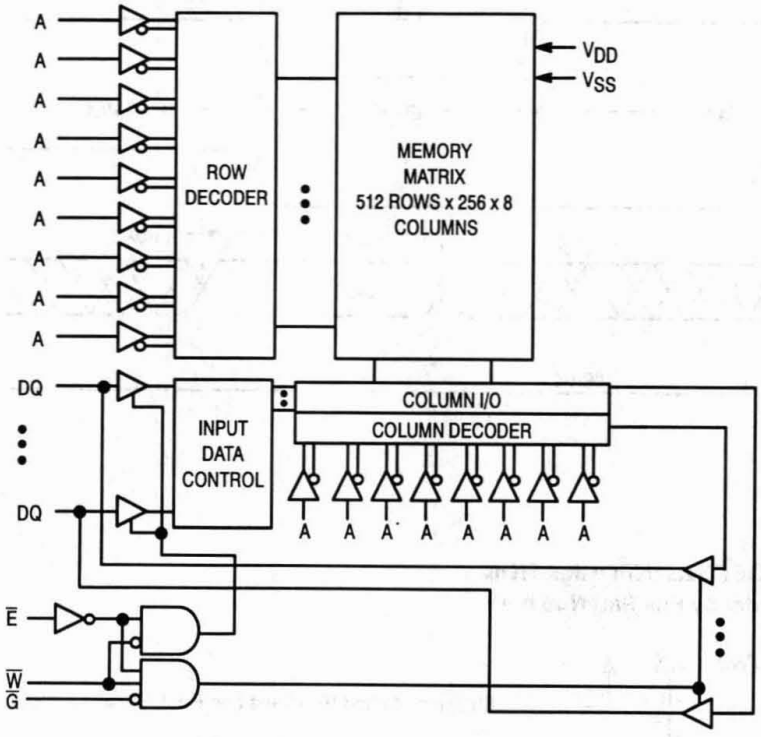
This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small–outline J–leaded package.

- Single 3.3 V Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 8, 10, 12, 15 ns
- Center Power and I/O Pins for Reduced Noise
- Fully 3.3 V BiCMOS

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ	Data Input/Output
V_{DD}	+ 3.3 V Power Supply
V_{SS}	Ground

This document contains information on a new product. Motorola reserves the right to change or discontinue this product without notice.

REV 4
2/25/97

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{DD} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	H	Output Disabled	I_{DDA}	High–Z	—
L	L	H	Read	I_{DDA}	D_{out}	Read Cycle
L	X	L	Write	I_{DDA}	High–Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{DD}	V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	0.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{DD}	3.135	3.3	3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{DD} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = –0.5 V dc; V_{IL} (min) = –2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{DD} + 0.3 V dc; V_{IH} (max) = V_{DD} + 2 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{DD})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{DD})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS (See Note 1)

Parameter	Symbol	6926–8		6926–10		6926–12		6926–15		Unit	Notes
		Typ	Max	Typ	Max	Typ	Max	Typ	Max		
AC Active Supply Current (I_{out} = 0 mA) (V_{DD} = max, f = f_{max})	I_{DDA}	—	150	—	130	—	120	—	110	mA	2, 3, 4
Active Quiescent Current ($\overline{E}$ = V_{IL}, V_{DD} = max, f = 0 MHz)	I_{DD2}	—	80	—	80	—	80	—	80	mA	
AC Standby Current ($\overline{E}$ = V_{IH}, V_{DD} = max, f = f_{max})	I_{SB1}	—	50	—	45	—	40	—	35	mA	2, 3, 4
CMOS Standby Current (V_{DD} = max, f = 0 MHz, $\overline{E} \geq V_{DD} - 0.2$ V, $V_{in} \leq V_{SS} + 0.2$ V, or $\geq V_{DD} - 0.2$ V)	I_{SB2}	—	20	—	20	—	20	—	20	mA	

NOTES:
1. Typical current = 25°C @ 3.3 V.
2. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
3. All address transition simultaneously low (LSB) and then high (MSB).
4. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_A = 0 to +70°C, Unless Otherwise Noted)

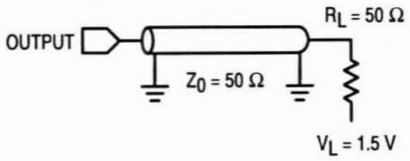
Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	6926–8		6926–10		6926–12		6926–15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	3
Address Access Time	t_{AVQV}	—	8	—	10	—	12	—	15	ns	
Enable Access Time	t_{ELQV}	—	8	—	10	—	12	—	15	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	5	—	6	—	7	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	3	—	3	—	3	—	3	—	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	—	4	—	5	—	6	—	7	ns	4,5,6
Output Enable High to Output High–Z	t_{GHQZ}	—	4	—	5	—	6	—	7	ns	4,5,6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

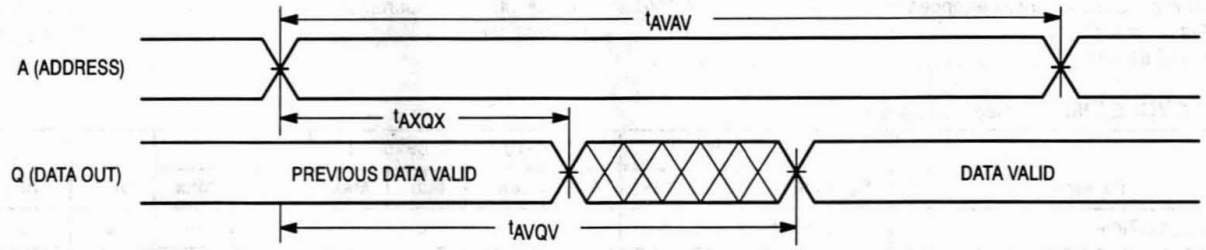


TIMING LIMITS

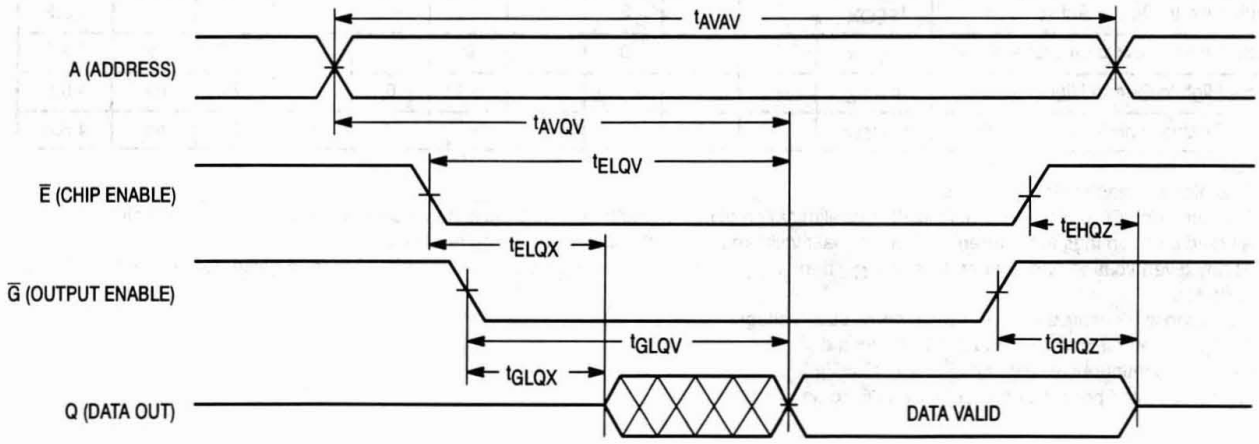
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Figure 1. AC Test Load

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

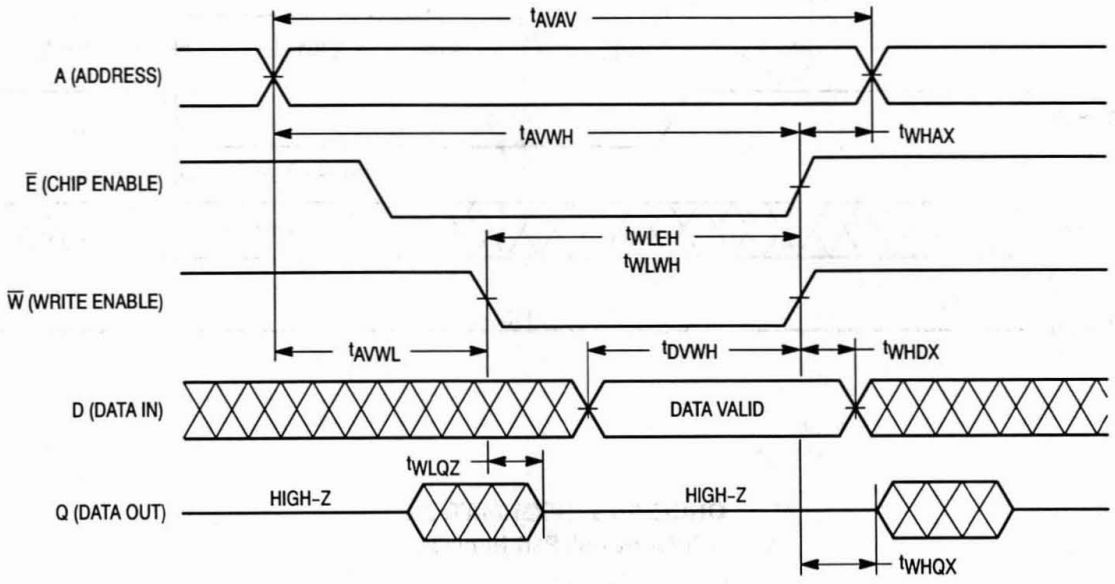


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6926–8		6926–10		6926–12		6926–15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	8	—	9	—	10	—	12	—	ns	
Address Valid to End of Write, $\overline{G}$ High	t_{AVWH}	7	—	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	8	—	9	—	10	—	12	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	7	—	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	4	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	—	4	—	5	—	6	—	7	ns	4,5,6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	3	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

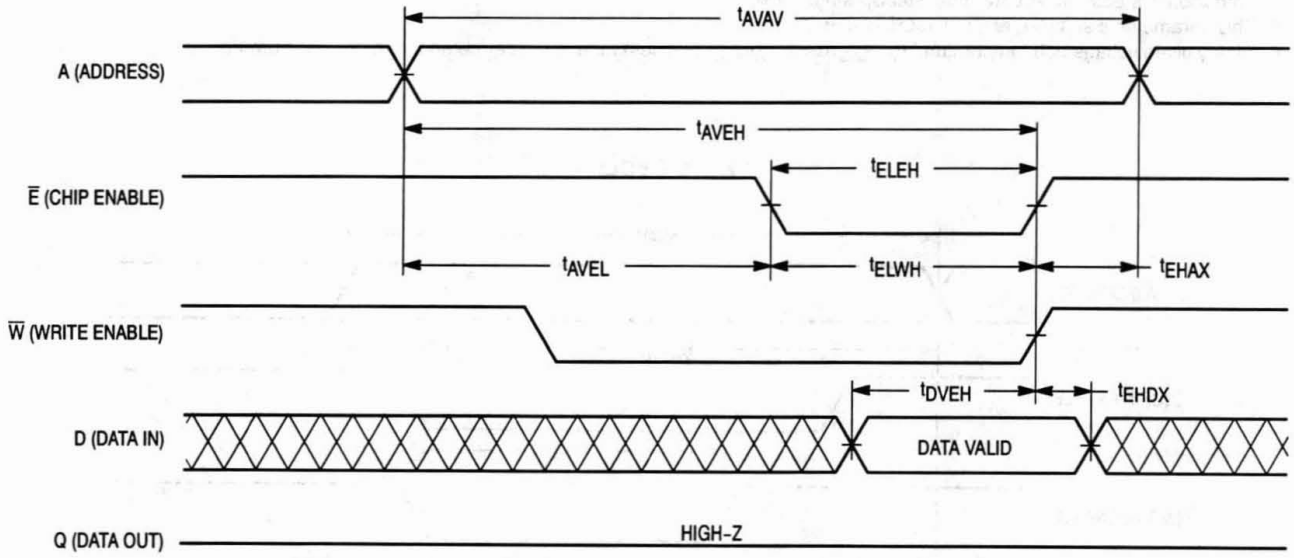


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6926–8		6926–10		6926–12		6926–15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	7	—	8	—	9	—	10	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	7	—	8	—	9	—	10	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	4	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6926 WJ XX X

- MCM — Motorola Memory Prefix
- 6926 — Part Number
- WJ — Package (WJ = 400 mil SOJ)
- XX — Speed (8 = 8 ns, 10 = 10 ns, 12 = 12 ns, 15 = 15 ns)
- X — Shipping Method (R = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6926WJ8, MCM6926WJ8R, MCM6926WJ10, MCM6926WJ10R, MCM6926WJ12, MCM6926WJ12R, MCM6926WJ15, MCM6926WJ15R

MCM6926A

Advance Information

128K x 8 Bit Fast Static Random Access Memory

WJ PACKAGE
400 MIL SOJ
CASE 857A–02

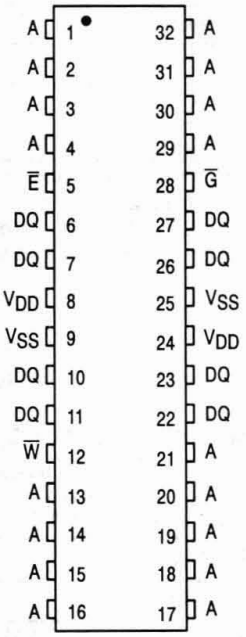
The MCM6926A is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

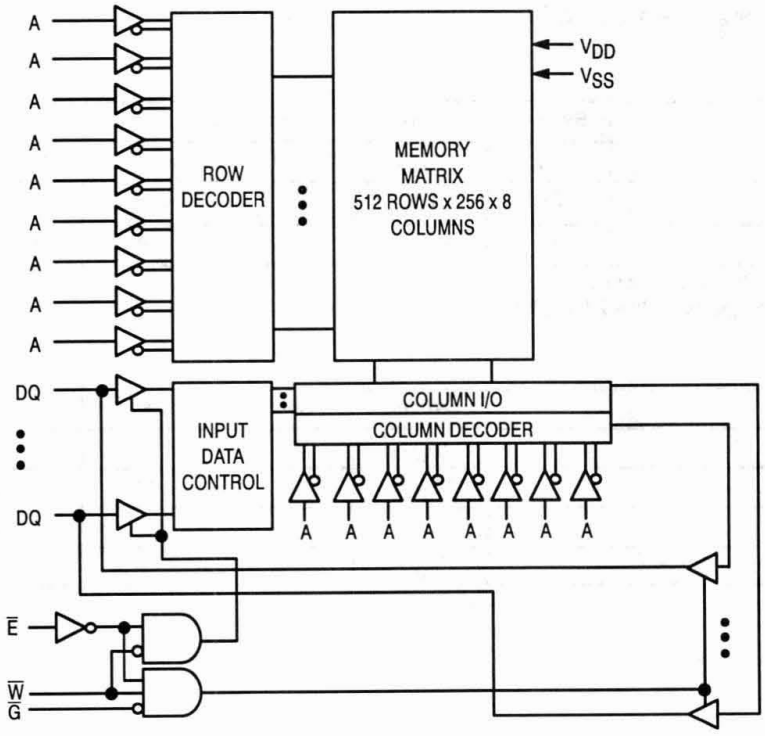
This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small–outline J–leaded package.

- Single 3.3 V Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 8, 10, 12, 15 ns
- Center Power and I/O Pins for Reduced Noise
- Fully 3.3 V BiCMOS

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ	Data Input/Output
V_{DD}	+ 3.3 V Power Supply
V_{SS}	Ground

This document contains information on a new product. Motorola reserves the right to change or discontinue this product without notice.

REV 1
2/25/97

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{DD} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	H	Output Disabled	I_{DDA}	High–Z	—
L	L	H	Read	I_{DDA}	D_{out}	Read Cycle
L	X	L	Write	I_{DDA}	High–Z	Write Cycle

2

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{DD}	V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	0.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{DD}	3.135	3.3	3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{DD} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{DD} + 0.3 V dc; V_{IH} (max) = V_{DD} + 2 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{DD})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{DD})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS (See Note 1)

Parameter	Symbol	6926A–8		6926A–10		6926A–12		6926A–15		Unit	Notes
		Typ	Max	Typ	Max	Typ	Max	Typ	Max		
AC Active Supply Current (I_{out} = 0 mA) (V_{DD} = max, f = f_{max})	I_{DDA}	—	150	—	130	—	120	—	110	mA	2, 3, 4
Active Quiescent Current ($\overline{E}$ = V_{IL}, V_{DD} = max, f = 0 MHz)	I_{DD2}	—	80	—	80	—	80	—	80	mA	
AC Standby Current ($\overline{E}$ = V_{IH}, V_{DD} = max, f = f_{max})	I_{SB1}	—	50	—	45	—	40	—	35	mA	2, 3, 4
CMOS Standby Current (V_{DD} = max, f = 0 MHz, $\overline{E} \geq V_{DD} - 0.2$ V, $V_{in} \leq V_{SS} + 0.2$ V, or $\geq V_{DD} - 0.2$ V)	I_{SB2}	—	20	—	20	—	20	—	20	mA	

NOTES:
1. Typical current = 25°C @ 3.3 V.
2. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
3. All address transition simultaneously low (LSB) and then high (MSB).
4. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_A = 0 to +70°C, Unless Otherwise Noted)

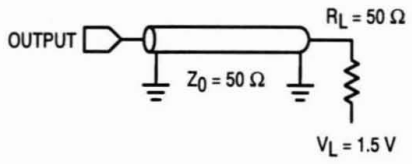
Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	6926A–8		6926A–10		6926A–12		6926A–15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	3
Address Access Time	t_{AVQV}	—	8	—	10	—	12	—	15	ns	
Enable Access Time	t_{ELQV}	—	8	—	10	—	12	—	15	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	5	—	6	—	7	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	3	—	3	—	3	—	3	—	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	ns	4, 5, 6
Enable High to Output High–Z	t_{EHQZ}	—	4	—	5	—	6	—	7	ns	4, 5, 6
Output Enable High to Output High–Z	t_{GHQZ}	—	4	—	5	—	6	—	7	ns	4, 5, 6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

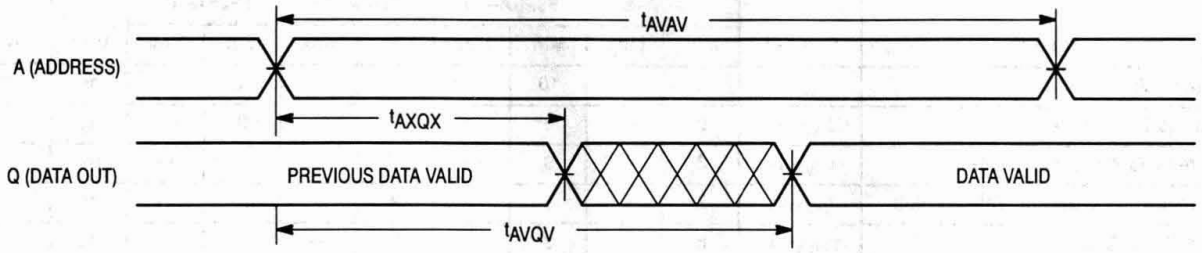


TIMING LIMITS

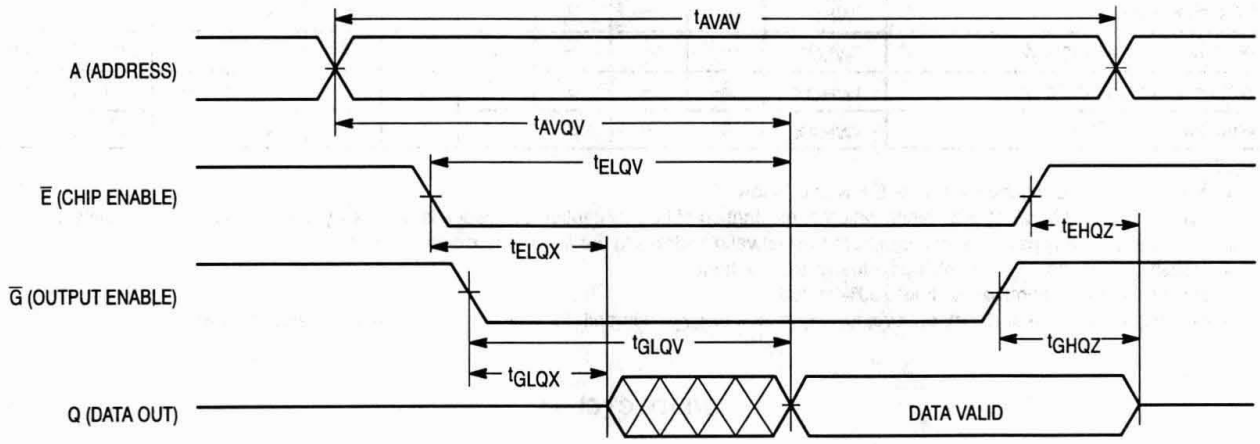
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Figure 1. AC Test Load

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

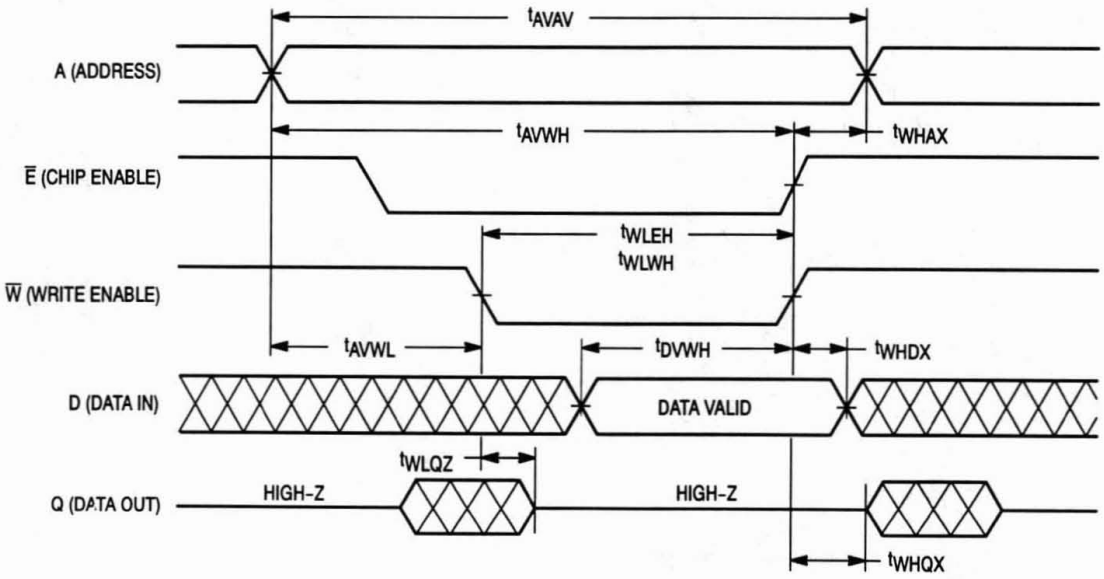


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6926A–8		6926A–10		6926A–12		6926A–15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	8	—	9	—	10	—	12	—	ns	
Address Valid to End of Write, $\overline{G}$ High	t_{AVWH}	7	—	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	8	—	9	—	10	—	12	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	7	—	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	4	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	—	4	—	5	—	6	—	7	ns	4,5,6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	3	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

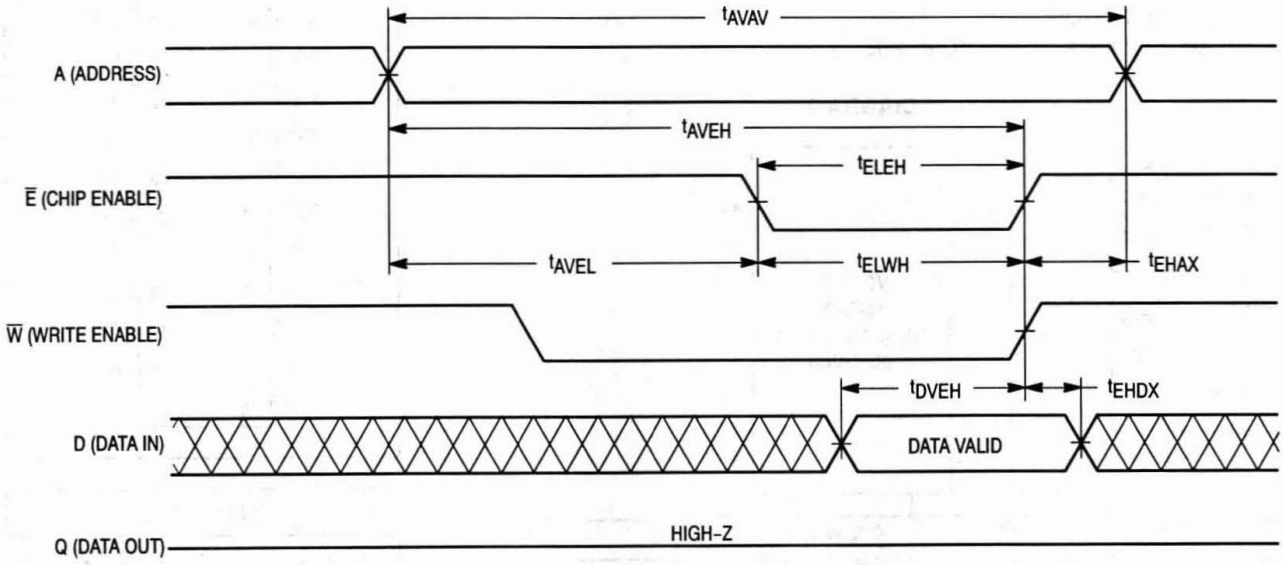


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6926A–8		6926A–10		6926A–12		6926A–15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	7	—	8	—	9	—	10	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	7	—	8	—	9	—	10	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	4	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6926A WJ XX X

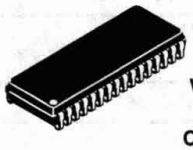
- Motorola Memory Prefix
- Part Number
- Shipping Method (R = Tape and Reel, Blank = Rails)
- Speed (8 = 8 ns, 10 = 10 ns, 12 = 12 ns, 15 = 15 ns)
- Package (WJ = 400 mil SOJ)

Full Part Numbers — MCM6926AWJ8, MCM6926AWJ8R, MCM6926AWJ10, MCM6926AWJ10R, MCM6926AWJ12, MCM6926AWJ12R, MCM6926AWJ15, MCM6926AWJ15R

MCM6926–C

2

128K x 8 Bit Fast Static Random Access Memory



WJ PACKAGE
400 MIL SOJ
CASE 857A–02

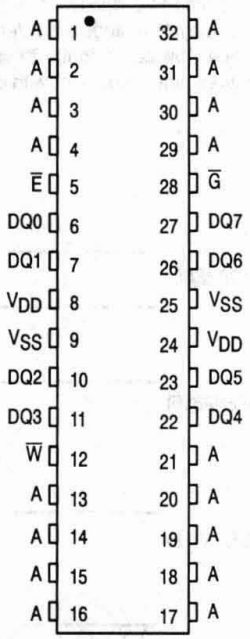
The MCM6926WJssC is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits. This device is fabricated using high performance silicon–gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

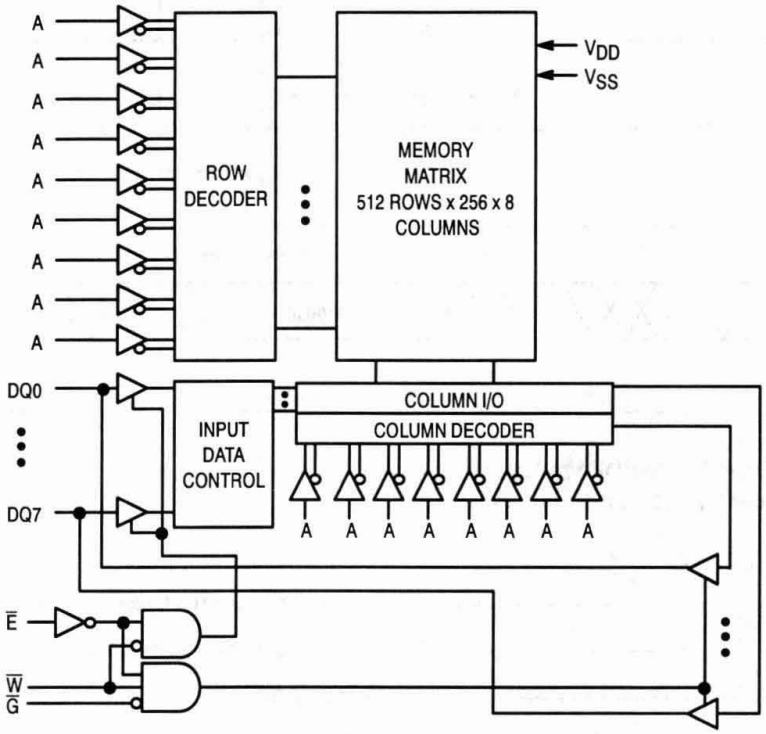
This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small–outline J–leaded package.

- Single 3.3 V Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 8, 10, 12, 15 ns
- Center Power and I/O Pins for Reduced Noise
- Fully 3.3 V BiCMOS
- Industrial Temperature (– 40°C to + 85°C)

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A16	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0 – DQ7	Data Input/Output
V_{DD}	+ 3.3 V Power Supply
V_{SS}	Ground

REV 1
2/25/97

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{DD} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	H	Output Disabled	I_{DDA}	High–Z	—
L	L	H	Read	I_{DDA}	D_{out}	Read Cycle
L	X	L	Write	I_{DDA}	High–Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{DD}	V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	0.6	W
Temperature Under Bias	T_{bias}	– 40 to + 85	°C
Operating Temperature	T_A	– 40 to + 85	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_A = – 40 to + 85°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{DD}	3.135	3.3	3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{DD} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = –0.5 V dc; V_{IL} (min) = –2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{DD} + 0.3 V dc; V_{IH} (max) = V_{DD} + 2 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{DD})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{DD})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS (See Note 1)

Parameter	Symbol	6926–8		6926–10		6926–12		6926–15		Unit	Notes
		Typ	Max	Typ	Max	Typ	Max	Typ	Max		
AC Active Supply Current (I_{out} = 0 mA) (V_{DD} = max, f = f_{max})	I_{DDA}	—	150	—	130	—	120	—	110	mA	2, 3, 4
Active Quiescent Current ($\overline{E}$ = V_{IL}, V_{DD} = max, f = 0 MHz)	I_{DD2}	—	80	—	80	—	80	—	80	mA	
AC Standby Current ($\overline{E}$ = V_{IH}, V_{DD} = max, f = f_{max})	I_{SB1}	—	50	—	45	—	40	—	35	mA	2, 3, 4
CMOS Standby Current (V_{DD} = max, f = 0 MHz, $\overline{E} \geq V_{DD} - 0.2$ V, $V_{in} \leq V_{SS} + 0.2$ V, or $\geq V_{DD} - 0.2$ V)	I_{SB2}	—	20	—	20	—	20	—	20	mA	

NOTES:
1. Typical current = 25°C @ 3.3 V.
2. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
3. All address transition simultaneously low (LSB) and then high (MSB).
4. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_A = – 40 to +85°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	6926–8		6926–10		6926–12		6926–15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	3
Address Access Time	t_{AVQV}	—	8	—	10	—	12	—	15	ns	
Enable Access Time	t_{ELQV}	—	8	—	10	—	12	—	15	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	5	—	6	—	7	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	3	—	3	—	3	—	3	—	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	—	4	0	5	0	6	0	7	ns	4,5,6
Output Enable High to Output High–Z	t_{GHQZ}	—	4	0	5	0	6	0	7	ns	4,5,6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

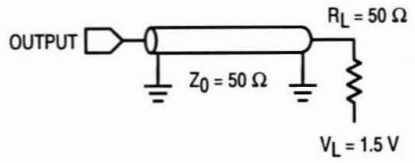
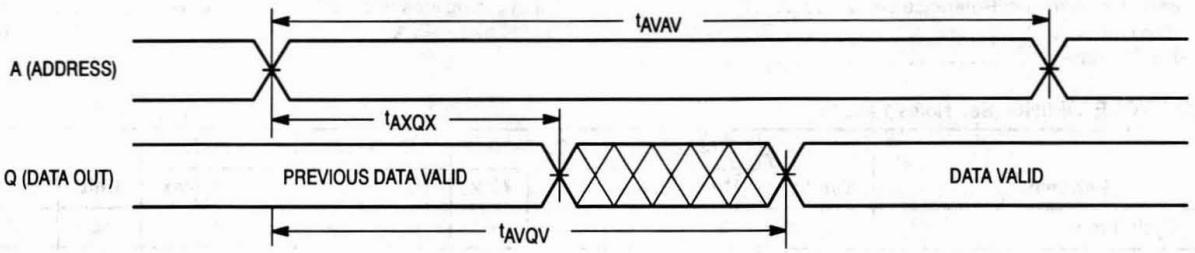


Figure 1. AC Test Load

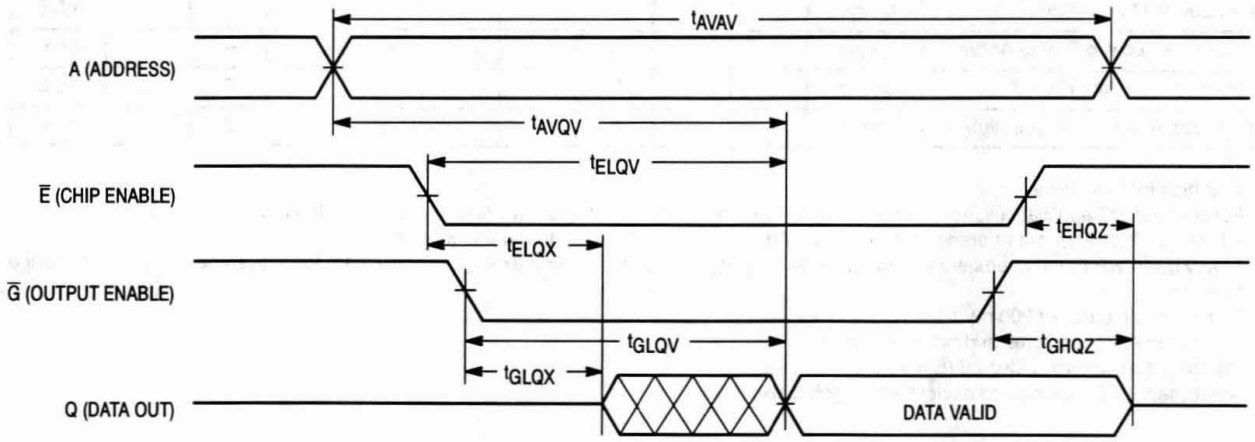
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

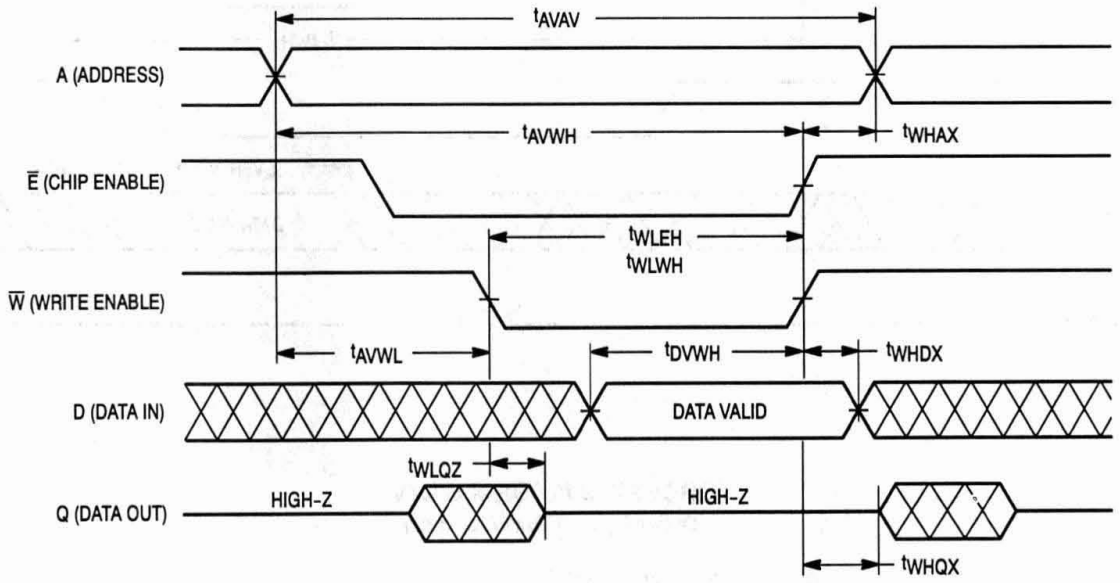


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6926–8		6926–10		6926–12		6926–15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	8	—	9	—	10	—	12	—	ns	
Address Valid to End of Write, $\overline{G}$ High	t_{AVWH}	7	—	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	8	—	9	—	10	—	12	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	7	—	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	4	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	4	0	5	0	6	0	7	ns	4,5,6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	3	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

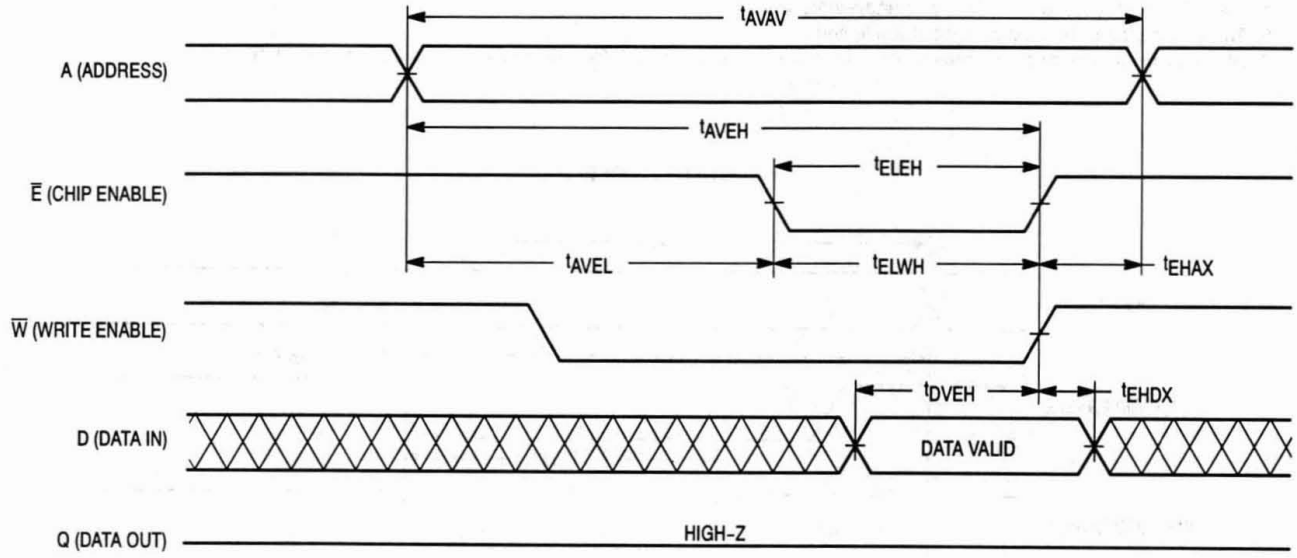


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6926–8		6926–10		6926–12		6926–15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	7	—	8	—	9	—	10	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	7	—	8	—	9	—	10	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	4	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

SCM 6926 WJ XX X X

- SCM — Motorola Memory Prefix
- 6926 — Part Number
- WJ — Package (WJ = 400 mil SOJ)
- XX — Speed (8 = 8 ns, 10 = 10 ns, 12 = 12 ns, 15 = 15 ns)
- X — Shipping Method (R = Tape and Reel, Blank = Rails)
- X — C = Industrial Temperature

Full Part Numbers — SCM6926WJ8C, SCM6926WJ8RC, SCM6926WJ10C, SCM6926WJ10RC, SCM6926WJ12C, SCM6926WJ12RC, SCM6926WJ15C, SCM6926WJ15RC

MCM6229B

256K x 4 Bit Static Random Access Memory

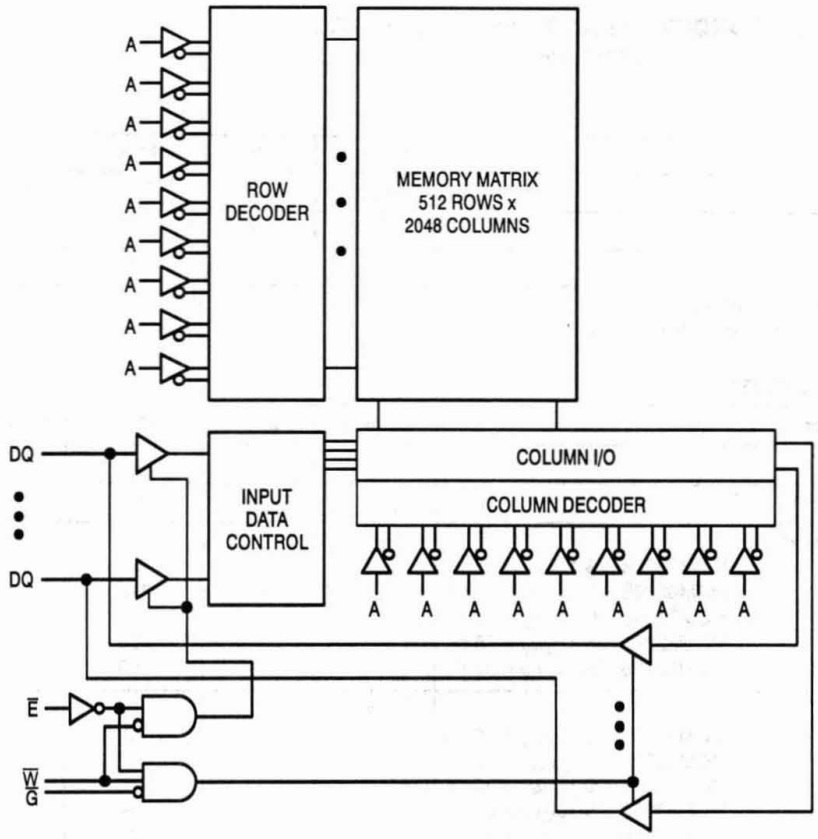
The MCM6229B is a 1,048,576 bit static random access memory organized as 262,144 words of 4 bits. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6229B is equipped with both chip enable ($\overline{E}$) and output enable ($\overline{G}$) pins, allowing for greater system flexibility and eliminating bus contention problems. Either input, when high, will force the outputs to high impedance.

The MCM6229B is available in 300 mil and 400 mil, 28–lead surface–mount SOJ packages.

- Single 5 V ± 10% Power Supply
- Fast Access Times: 15/17/20/25/35 ns
- Equal Address and Chip Enable Access Times
- All Inputs and Outputs are TTL Compatible
- Three–State Outputs
- Low Power Operation: 120/115/110/105/100 mA Maximum, Active AC

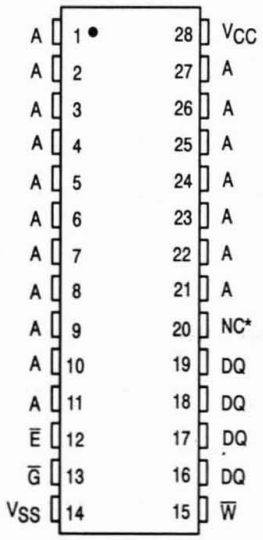
BLOCK DIAGRAM



J PACKAGE
300 MIL SOJ
CASE 810B–03

WJ PACKAGE
400 MIL SOJ
CASE 810–03

PIN ASSIGNMENT



PIN NAMES

A	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
DQ	Data Inputs/Outputs
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC*	No Connection

*If not used for no connect, then do not exceed voltages of – 0.5 to V_{CC} + 0.5 V. This pin is used for manufacturing diagnostics.

REV 3
10/9/96

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	Not Selected	High–Z	—	I_{SB1}, I_{SB2}
L	H	H	Output Disabled	High–Z	—	I_{CCA}
L	L	H	Read	D_{out}	Read	I_{CCA}
L	X	L	Write	D_{in}	Write	I_{CCA}

H = High, L = Low, X = Don't Care

2

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns).
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1	µA
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max)	I_{CCA}			mA
MCM6229B–15: t_{AVAV} = 15 ns		—	120	
MCM6229B–17: t_{AVAV} = 17 ns		—	115	
MCM6229B–20: t_{AVAV} = 20 ns		—	110	
MCM6229B–25: t_{AVAV} = 25 ns		—	105	
MCM6229B–35: t_{AVAV} = 35 ns		—	100	
AC Standby Current (V_{CC} = max, $\overline{E}$ = V_{IH}, f ≤ f_{max})	I_{SB1}			mA
MCM6229B–15: t_{AVAV} = 15 ns		—	40	
MCM6229B–17: t_{AVAV} = 17 ns		—	35	
MCM6229B–20: t_{AVAV} = 20 ns		—	30	
MCM6229B–25: t_{AVAV} = 25 ns		—	25	
MCM6229B–35: t_{AVAV} = 35 ns		—	20	
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V, V_{CC} = max, f = 0 MHz)	I_{SB2}	—	5	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs except Clocks & DQs $\overline{E}$, $\overline{G}$, and $\overline{W}$	C_{in} C_{ck}	4 5	6 8	pF
Input/Output Capacitance	DQ	$C_{I/O}$	5	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1a

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	6229B–15		6229B–17		6229B–20		6229B–25		6229B–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	2, 3
Address Access Time	t_{AVQV}	—	15	—	17	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	—	15	—	17	—	20	—	25	—	35	ns	4
Output Enable Access Time	t_{GLQV}	—	6	—	7	—	7	—	8	—	8	ns	
Output Hold from Address Change	t_{AXQX}	5	—	5	—	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	5	—	5	—	5	—	5	—	ns	5, 6 ,7
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	0	—	ns	5, 6, 7
Enable High to Output High–Z	t_{EHQZ}	—	6	—	7	—	7	—	8	—	8	ns	5, 6, 7
Output Enable High to Output High–Z	t_{GHQZ}	—	6	—	7	—	7	—	8	—	8	ns	5, 6, 7

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1b.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E} \le V_{IL}$, $\overline{G} \le V_{IL}$).

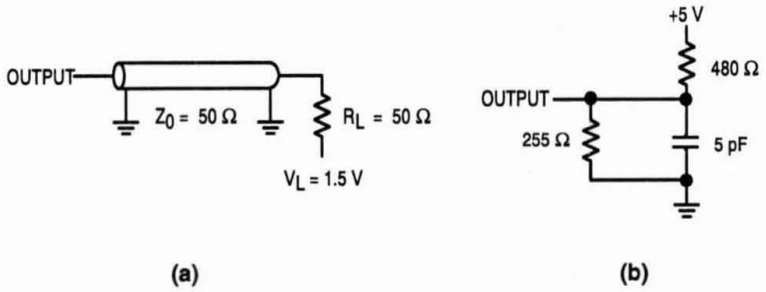
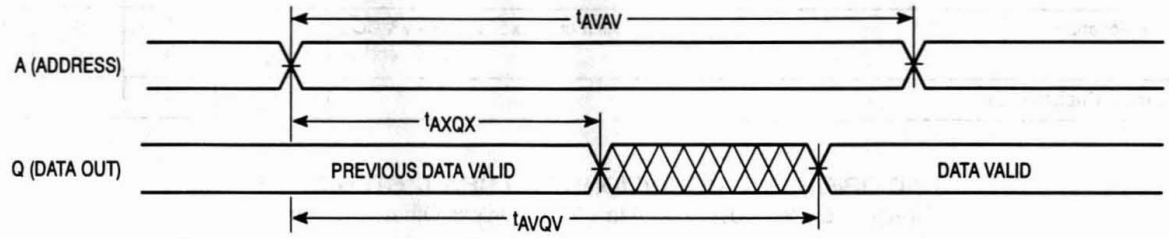


Figure 1. AC Test Loads

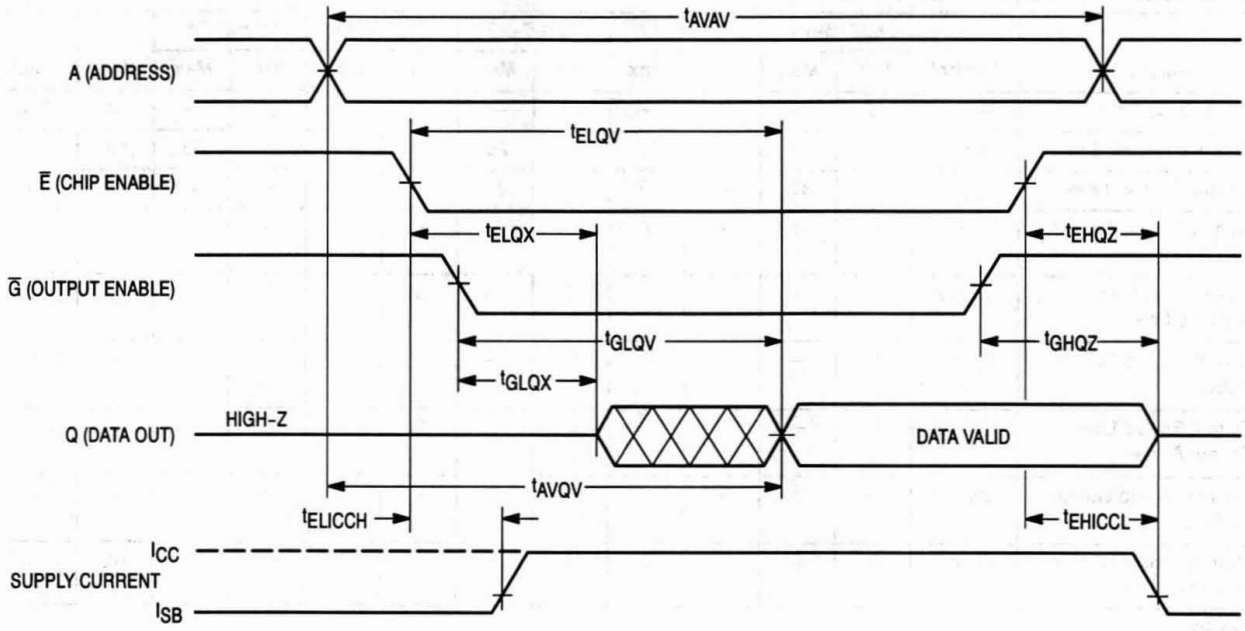
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Notes 1, 2, and 8)



READ CYCLE 2 (See Note 8)

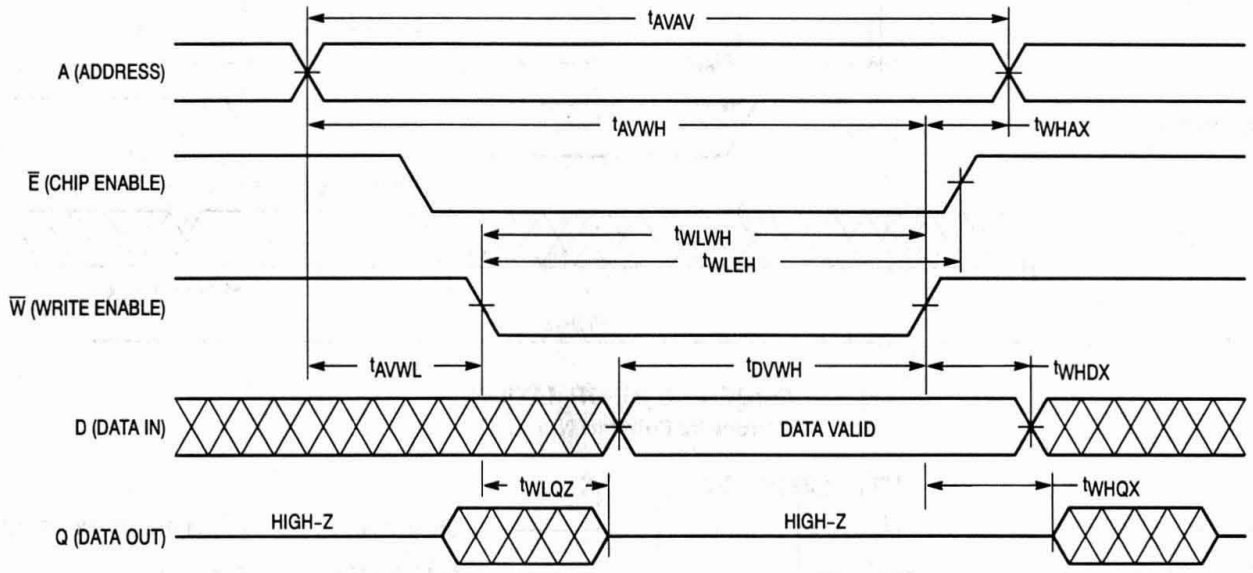


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	6229B–15		6229B–17		6229B–20		6229B–25		6229B–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	14	—	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVWH}	7	—	8	—	8	—	10	—	11	—	ns	
Data Hold TIme	t_{WHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	—	6	—	7	—	7	—	8	—	8	ns	5, 6, 7
Write High to Output Active	t_{WHQX}	5	—	5	—	5	—	5	—	5	—	ns	5, 6, 7
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1b.
6. This parameter is sampled and not 100% tested.
7. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled See Notes 1, 2, and 3)

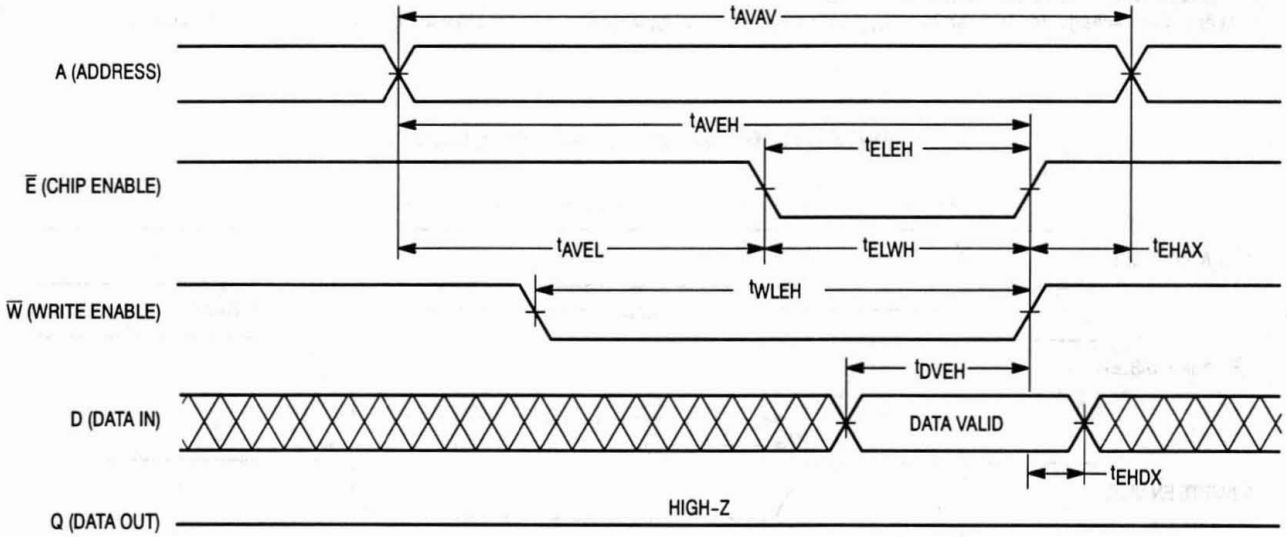


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	6229B–15		6229B–17		6229B–20		6229B–25		6229B–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	12	—	14	—	15	—	17	—	20	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	10	—	11	—	12	—	15	—	20	—	ns	5, 6
Write Pulse Width	t_{WLEH}	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	7	—	8	—	8	—	10	—	11	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high–impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled See Notes 1, 2, and 3)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6229B XX XX XX

- Motorola Memory Prefix
- Part Number
- Shipping Method (R2 = Tape and Reel, Blank = Rails)
- Speed (15 = 15 ns, 17 = 17 ns, 20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
- Package (J = 300 mil SOJ, WJ = 400 mil SOJ)

Full Part Numbers —

MCM6229BJ15	MCM6229BJ15R2	MCM6229BWJ15	MCM6229BWJ15R2
MCM6229BJ17	MCM6229BJ17R2	MCM6229BWJ17	MCM6229BWJ17R2
MCM6229BJ20	MCM6229BJ20R2	MCM6229BWJ20	MCM6229BWJ20R2
MCM6229BJ25	MCM6229BJ25R2	MCM6229BWJ25	MCM6229BWJ25R2
MCM6229BJ35	MCM6229BJ35R2	MCM6229BWJ35	MCM6229BWJ35R2

MCM6229BB

Product Preview

256K x 4 Bit Static Random Access Memory

XJ PACKAGE
400 MIL SOJ
CASE 810–03

EJ PACKAGE
300 MIL SOJ
CASE 810B–03

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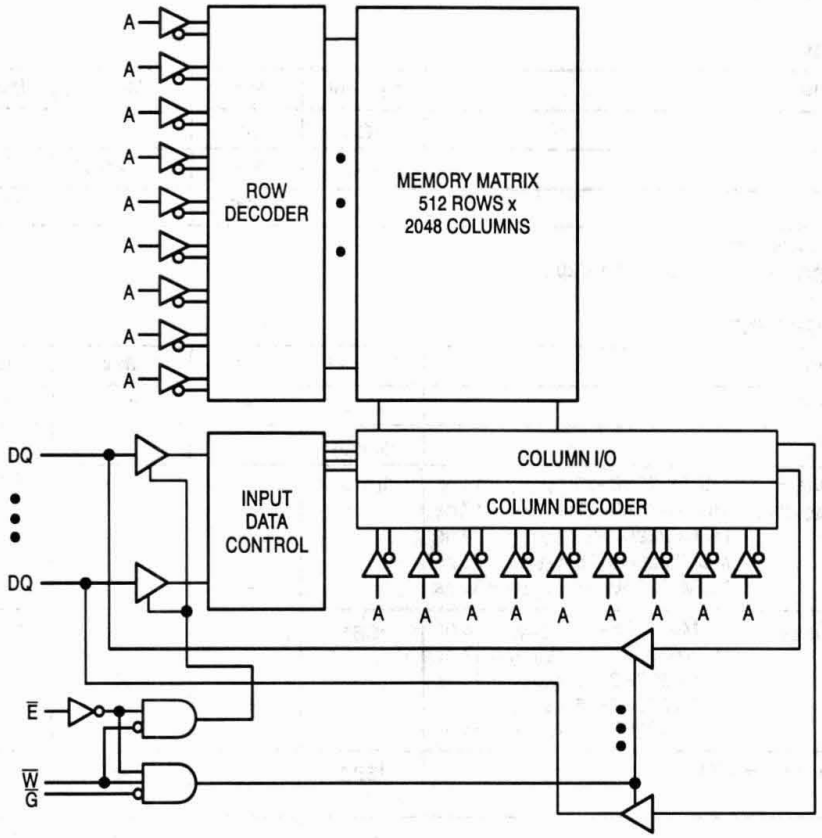
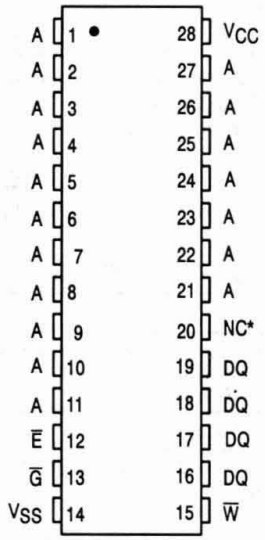
The MCM6229BB is available in 300 mil and 400 mil, 28 lead surface–mount SOJ packages.

- Single 5 V ± 10% Power Supply
- Fast Access Times: 15/17/20/25/35 ns
- Equal Address and Chip Enable Access Times
- All Inputs and Outputs are TTL Compatible and LVTTL Compatible
- Three State Outputs
- Low Power Operation: 155/150/135/130/110 mA Maximum, Active AC

BLOCK DIAGRAM



PIN ASSIGNMENTS



PIN NAMES

A	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
DQ	Data Inputs/Outputs
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC*	No Connection

*If not used for no connect, then do not exceed voltages of – 0.5 to V_{CC} + 0.5 V. This pin is used for manufacturing diagnostics.

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

11/7/96

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	Not Selected	High–Z	—	I_{SB1}, I_{SB2}
L	H	H	Output Disabled	High–Z	—	I_{CCA}
L	L	H	Read	D_{out}	Read	I_{CCA}
L	X	L	Write	D_{in}	Write	I_{CCA}

H = High, L = Low, X = Don't Care

2

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns).
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	± 1	µA
AC Active Supply Current (I_{out} = 0 mA, all inputs = V_{IL} or V_{IH}, V_{IL} = 0, V_{IH} ≥ 3 V, cycle time ≥ t_{AVAV} min, V_{CC} = max)	MCM6229BB–15: t_{AVAV} = 15 ns	I_{CCA}	—	155	mA
	MCM6229BB–17: t_{AVAV} = 17 ns		—	150	
	MCM6229BB–20: t_{AVAV} = 20 ns		—	135	
	MCM6229BB–25: t_{AVAV} = 25 ns		—	130	
	MCM6229BB–35: t_{AVAV} = 35 ns		—	110	
AC Standby Current (V_{CC} = max, $\overline{E}$ = V_{IH}, f = f_{max})	MCM6229BB–15: t_{AVAV} = 15 ns	I_{SB1}	—	45	mA
	MCM6229BB–17: t_{AVAV} = 17 ns		—	40	
	MCM6229BB–20: t_{AVAV} = 20 ns		—	35	
	MCM6229BB–25: t_{AVAV} = 25 ns		—	30	
	MCM6229BB–35: t_{AVAV} = 35 ns		—	25	
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V, V_{CC} = max, f = 0 MHz)		I_{SB2}	—	5	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except Clocks and DQs	C_{in}	4	6	pF
	$\overline{E}$, $\overline{G}$, and $\overline{W}$	C_{ck}	5	8	
I/O Capacitance	DQ	$C_{I/O}$	5	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1a

READ CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	6229BB–15		6229BB–17		6229BB–20		6229BB–25		6229BB–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	3
Address Access Time	t_{AVQV}	—	15	—	17	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	—	15	—	17	—	20	—	25	—	35	ns	4
Output Enable Access Time	t_{GLQV}	—	6	—	7	—	7	—	8	—	8	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	5	—	5	—	5	—	5	—	ns	5, 6, 7
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	0	—	ns	5, 6, 7
Enable High to Output High–Z	t_{EHQZ}	0	6	0	7	0	7	0	8	0	8	ns	5, 6, 7
Output Enable High to Output High–Z	t_{GHQZ}	0	6	0	7	0	7	0	8	0	8	ns	5, 6, 7

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1b.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E} \le V_{IL}$, $\overline{G} \le V_{IL}$).

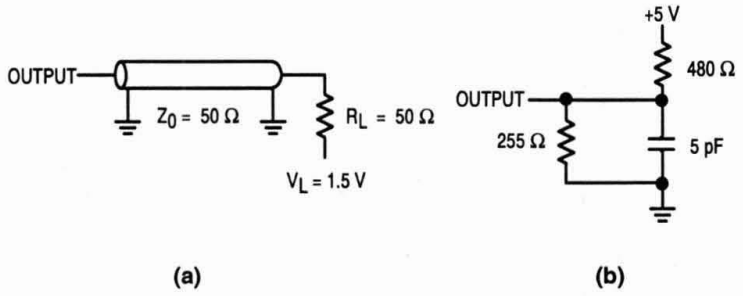
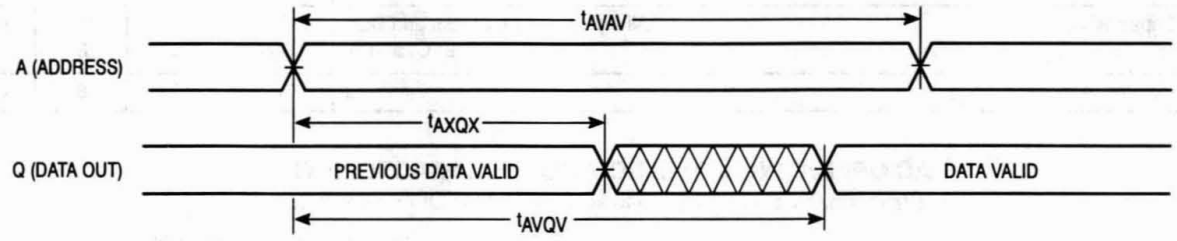


Figure 1. AC Test Loads

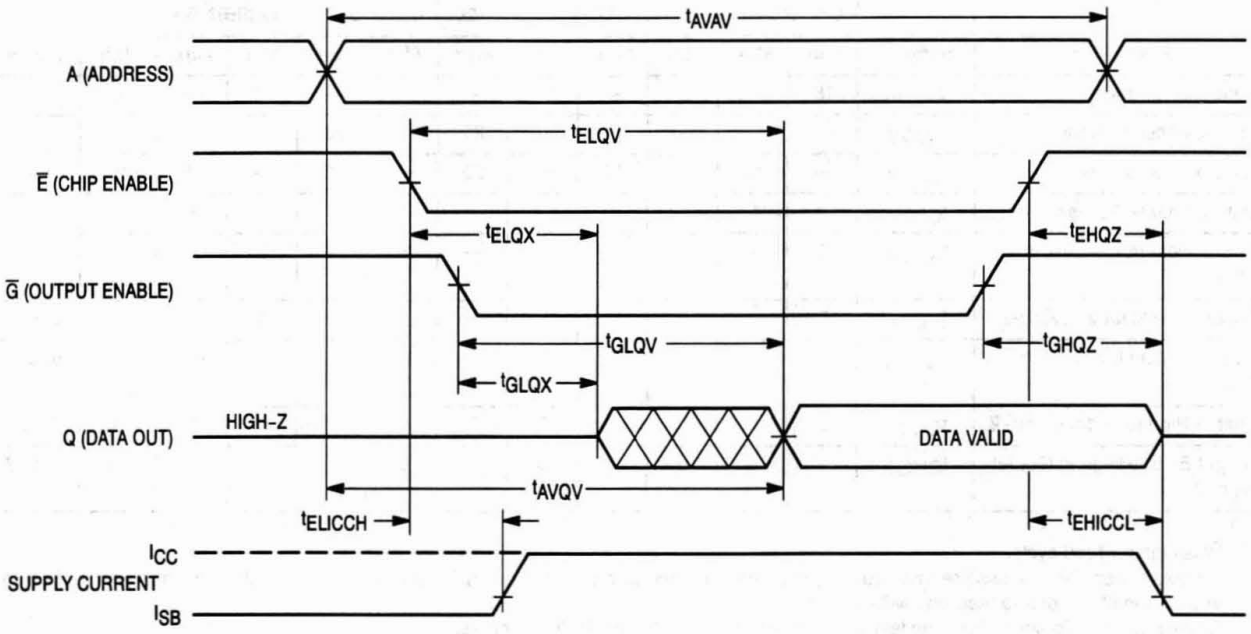
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Notes 1, 2, 3, and 9)



READ CYCLE 2 (See Notes 3 and 5)

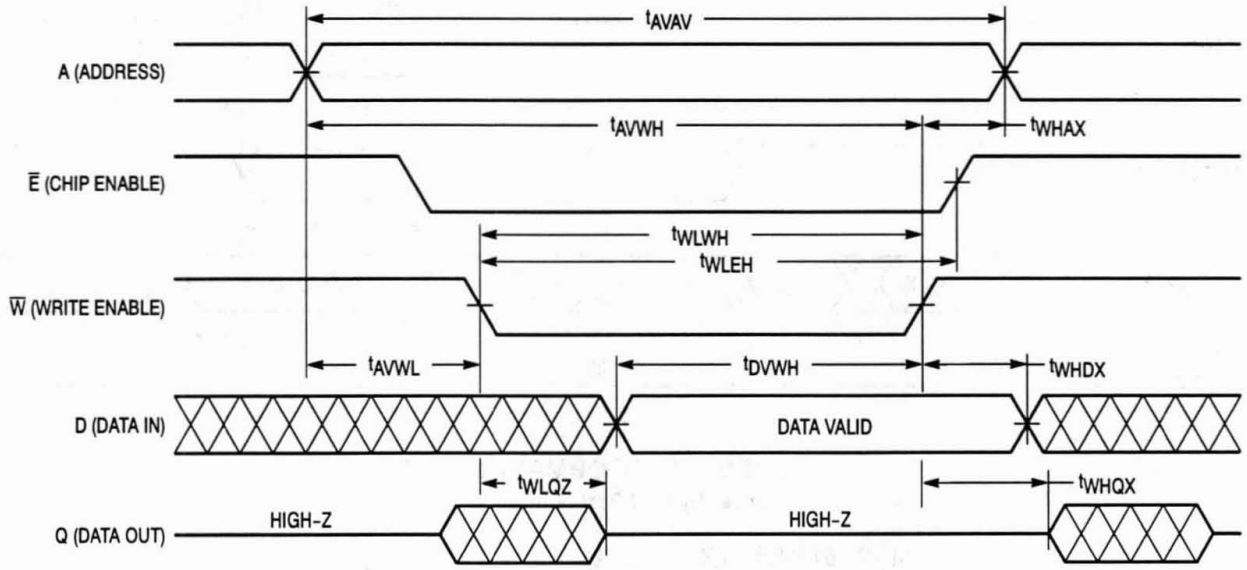


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, 3, and 4)

Parameter	Symbol	6229BB–15		6229BB–17		6229BB–20		6229BB–25		6229BB–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	14	—	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVWH}	7	—	8	—	9	—	10	—	11	—	ns	
Data Hold TIme	t_{WHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	—	6	—	7	—	7	—	8	—	8	ns	5, 6, 7
Write High to Output Active	t_{WHQX}	5	—	5	—	5	—	5	—	5	—	ns	5, 6, 7
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1b.
6. This parameter is sampled and not 100% tested.
7. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled See Notes 1, 2, 3, and 4)

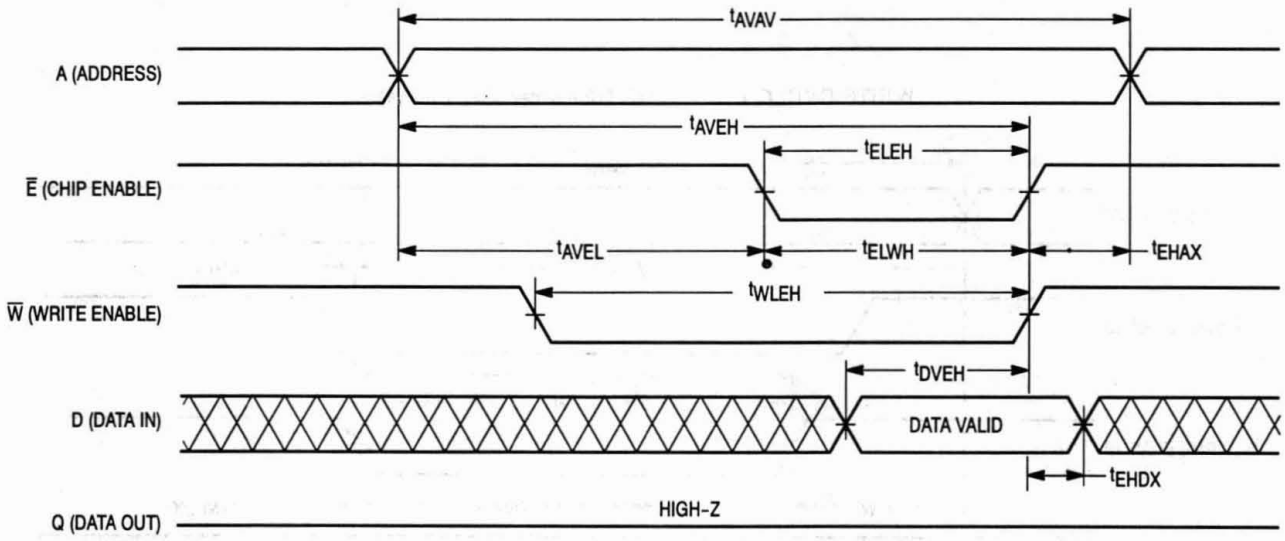


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	6229BB–15		6229BB–17		6229BB–20		6229BB–25		6229BB–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	12	—	14	—	15	—	17	—	20	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	12	—	14	—	15	—	17	—	20	—	ns	5, 6
Write Pulse Width	t_{WLEH}	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	7	—	8	—	9	—	10	—	11	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high–impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled See Notes 1, 2, 3, and 4)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6229BB XX XX XX

- MCM — Motorola Memory Prefix
- 6229BB — Part Number
- XX — Package (XJ = 400 mil SOJ, EJ = 300 mil SOJ)
- XX — Speed (15 = 15 ns, 17 = 17 ns, 20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
- XX — Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers —

MCM6229BBXJ15	MCM6229BBXJ15R2	MCM6229BBEJ15	MCM6229BBEJ15R2
MCM6229BBXJ17	MCM6229BBXJ17R2	MCM6229BBEJ17	MCM6229BBEJ17R2
MCM6229BBXJ20	MCM6229BBXJ20R2	MCM6229BBEJ20	MCM6229BBEJ20R2
MCM6229BBXJ25	MCM6229BBXJ25R2	MCM6229BBEJ25	MCM6229BBEJ25R2
MCM6229BBXJ35	MCM6229BBXJ35R2	MCM6229BBEJ35	MCM6229BBEJ35R2

MCM6729B

256K x 4 Bit Fast Static Random Access Memory

The MCM6729B is a 1,048,576 bit static random access memory organized as 262,144 words of 4 bits. Static design eliminates the need for external clocks or timing strobes.

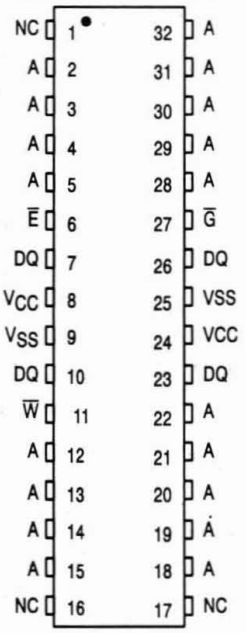
Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small–outline J–leaded package.

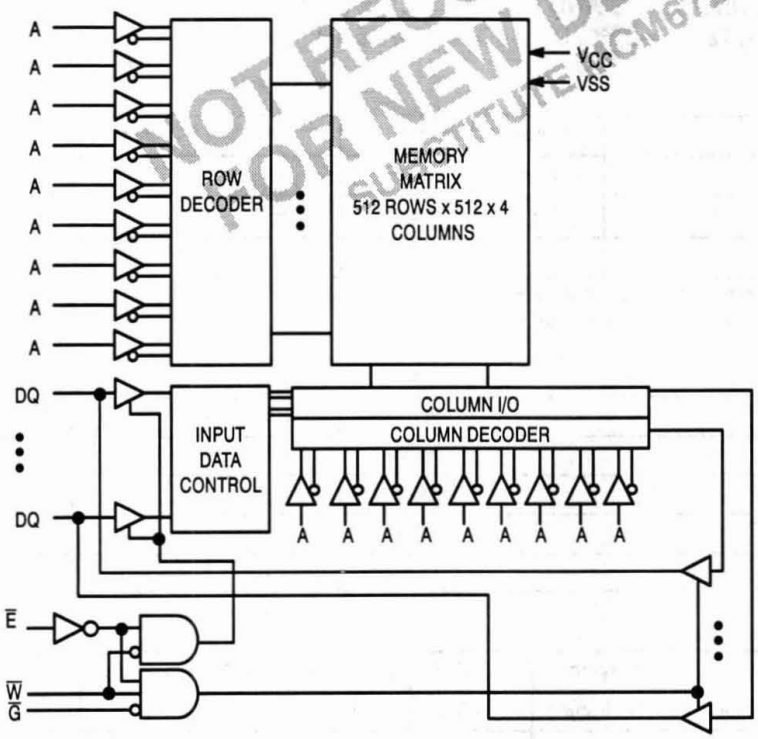
- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 8, 10, 12 ns
- Center Power and I/O Pins for Reduced Noise

WJ PACKAGE
400 MIL SOJ
CASE 857A–02

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

NOT RECOMMENDED FOR NEW DESIGNS
SUBSTITUTE MCM6729D

REV 4
4/7/97

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	H	Output Disabled	I_{CCA}	High–Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High–Z	Write Cycle

2

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	±30	mA
Power Dissipation	P_D	1.2	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	6729B–8	6729B–10	6729B–12	Unit	Notes
AC Active Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	I_{CCA}	195	165	155	mA	1, 2, 3
Active Quiescent Current ($\overline{E}$ = V_{IL}, V_{CC} = max, f = 0 MHz)	I_{CC2}	90	90	90	mA	
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	60	60	60	mA	1, 2, 3
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	20	mA	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
2. All addresses transition simultaneously low (LSB) and then high (MSB).
3. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

2

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1a

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	6729B–8		6729B–10		6729B–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Access Time	t_{AVQV}	—	8	—	10	—	12	ns	
Enable Access Time	t_{ELQV}	—	8	—	10	—	12	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	5	—	6	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	3	—	3	—	3	—	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	—	4	—	5	—	6	ns	4,5,6
Output Enable High to Output High–Z	t_{GHQZ}	—	4	—	5	—	6	ns	4,5,6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} (max) < t_{ELQX} (min), and t_{GHQZ} (max) < t_{GLQX} (min), both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1b.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

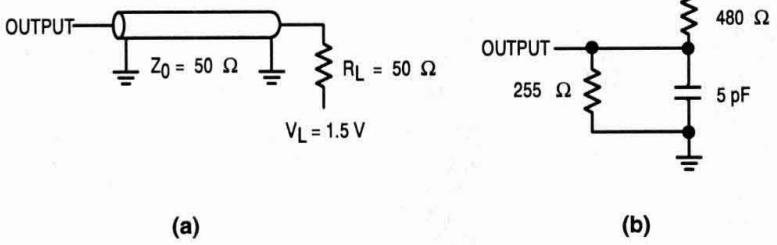
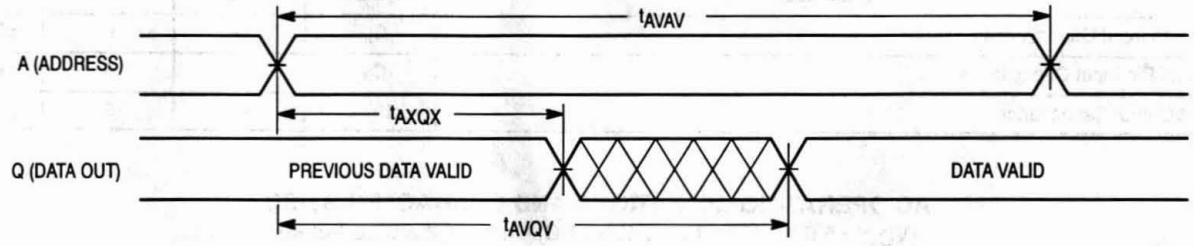


Figure 1. AC Test Loads

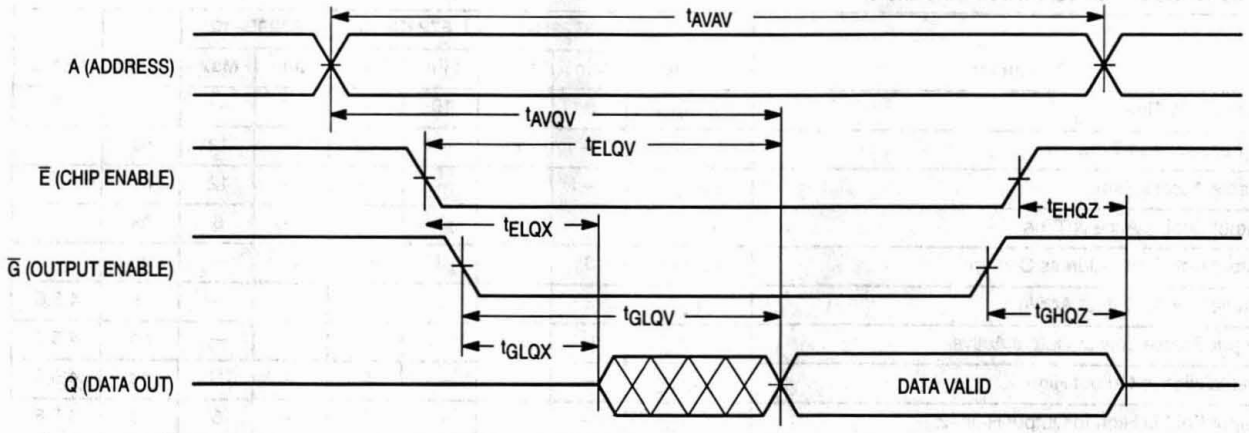
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

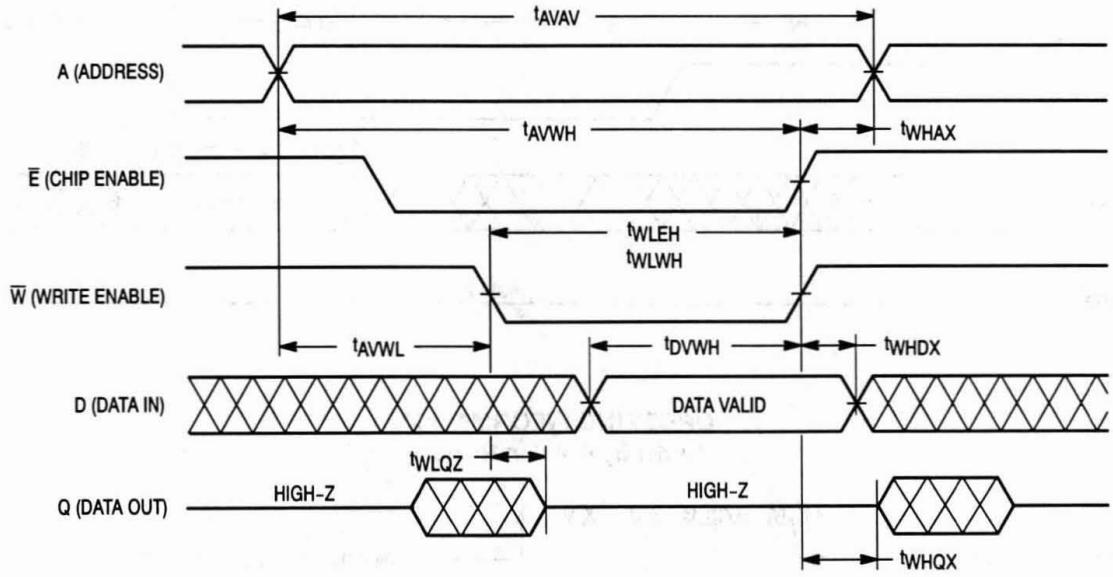


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6729B–8		6729B–10		6729B–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	8	—	9	—	10	—	ns	
Address Valid to End of Write, $\overline{G}$ High	t_{AVWH}	7	—	8	—	9	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	8	—	9	—	10	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	7	—	8	—	9	—	ns	
Data Valid to End of Write	t_{DVWH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	—	4	—	5	—	6	ns	4,5,6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage with load of Figure 1b.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

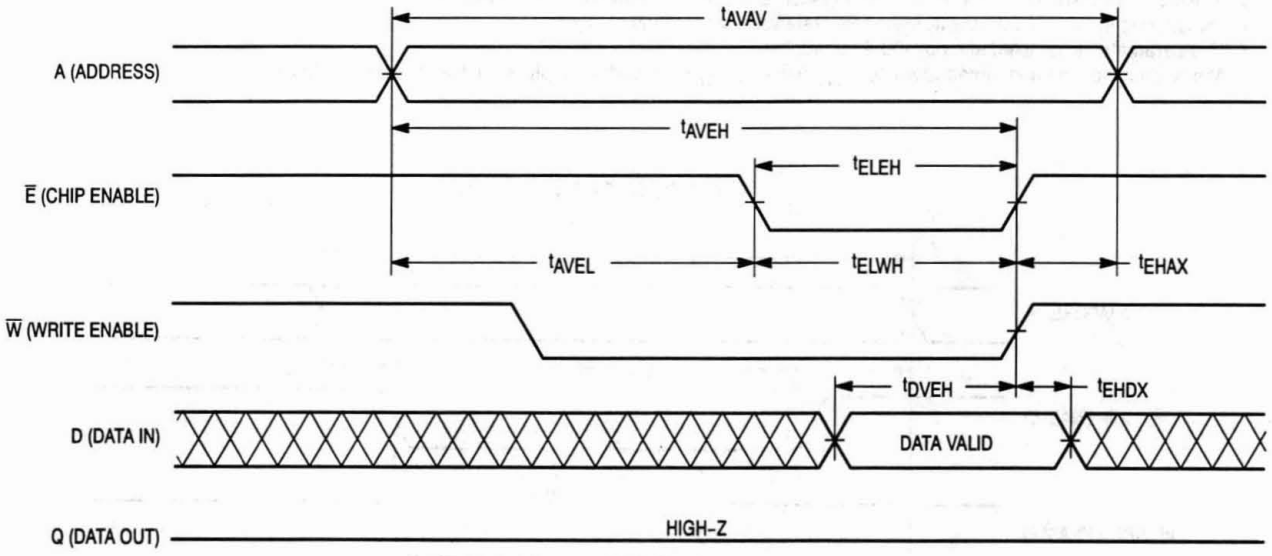


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6729B–8		6729B–10		6729B–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	7	—	8	—	9	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	7	—	8	—	9	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6729B WJ XX X

- MCM — Motorola Memory Prefix
- 6729B — Part Number
- WJ — Package (WJ = 400 mil SOJ)
- XX — Speed (8 = 8 ns, 10 = 10 ns, 12 = 12 ns)
- X — Shipping Method (R = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6729BWJ8, MCM6729BWJ8R, MCM6729BWJ10, MCM6729BWJ10R, MCM6729BWJ12, MCM6729BWJ12R

MCM6729C

256K x 4 Bit Fast Static Random Access Memory

WJ PACKAGE
400 MIL SOJ
CASE 857A–01

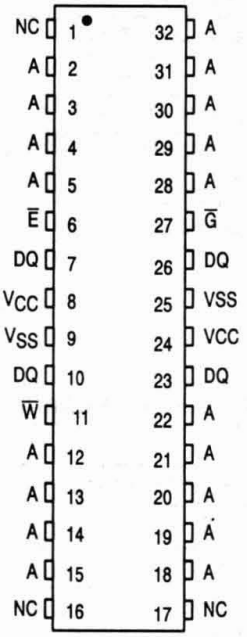
The MCM6729C is a 1,048,576 bit static random access memory organized as 262,144 words of 4 bits. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

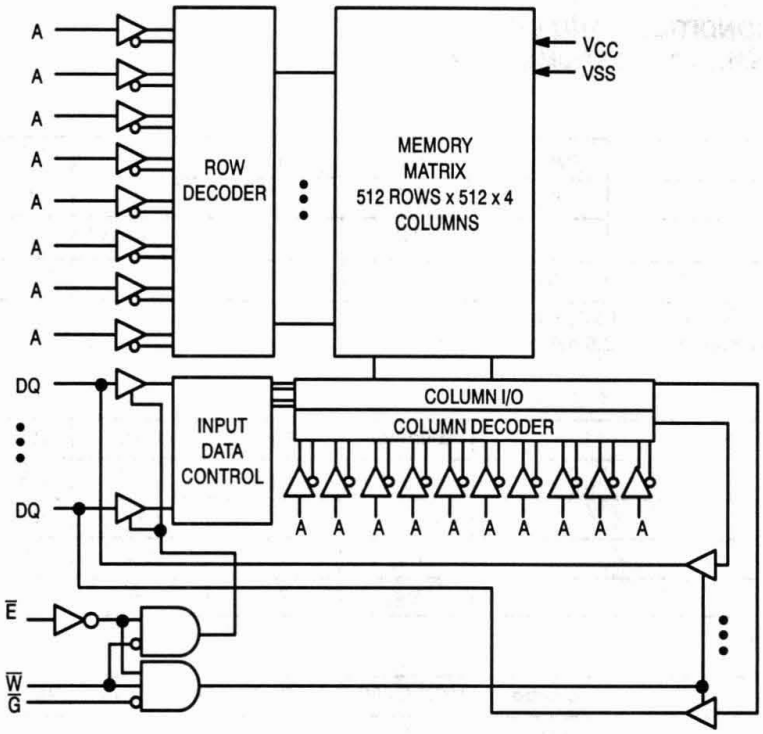
This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small–outline J–leaded package.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 6, 7 ns
- Center Power and I/O Pins for Reduced Noise

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

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TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	H	Output Disabled	I_{CCA}	High–Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High–Z	Write Cycle

2

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	±30	mA
Power Dissipation	P_D	1.5	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	MCM6729C–6	MCM6729C–7	Unit	Notes
AC Active Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	I_{CCA}	250	220	mA	1, 2, 3
Active Quiescent Current ($\overline{E}$ = V_{IL}, V_{CC} = max, f = 0 MHz)	I_{CC2}	100	100	mA	
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	100	100	mA	1, 2, 3
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V)	I_{SB2}	60	60	mA	

NOTES:
1. Reference AC Operating Conditions and Characterisitics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3 V, V_{IH} = 3 V).
2. All addresses transition simultaneously low (LSB) and then high (MSB).
3. Data States are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1a

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM6729C–6		MCM6729C–7		Unit	Notes
		Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	6	—	7	—	ns	3
Address Access Time	t_{AVQV}	—	6	—	7	ns	
Enable Access Time	t_{ELQV}	—	6	—	7	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	4	ns	
Output Hold from Address Change	t_{AXQX}	2	—	2	—	ns	
Enable Low to Output Active	t_{ELQX}	3	—	3	—	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	—	3	—	3.5	ns	4,5,6
Output Enable High to Output High–Z	t_{GHQZ}	—	3	—	3.5	ns	4,5,6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} (max) < t_{ELQX} (min), and t_{GHQZ} (max) < t_{GLQX} (min), both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1b.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

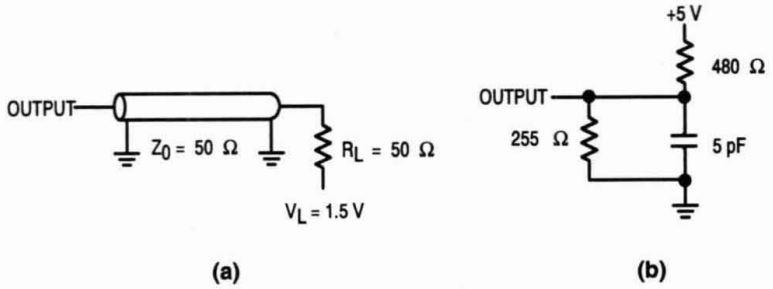
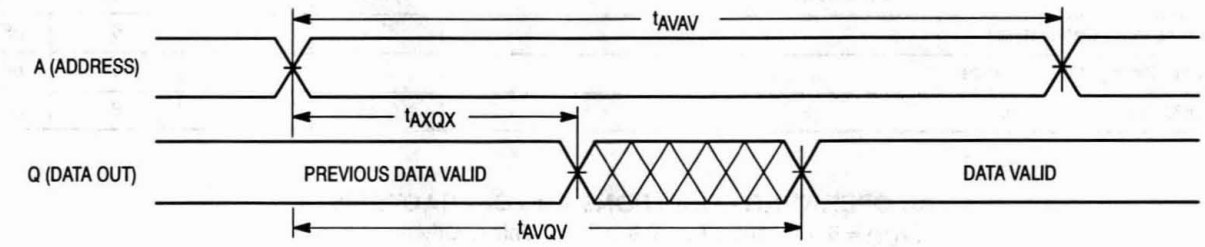


Figure 1. AC Test Loads

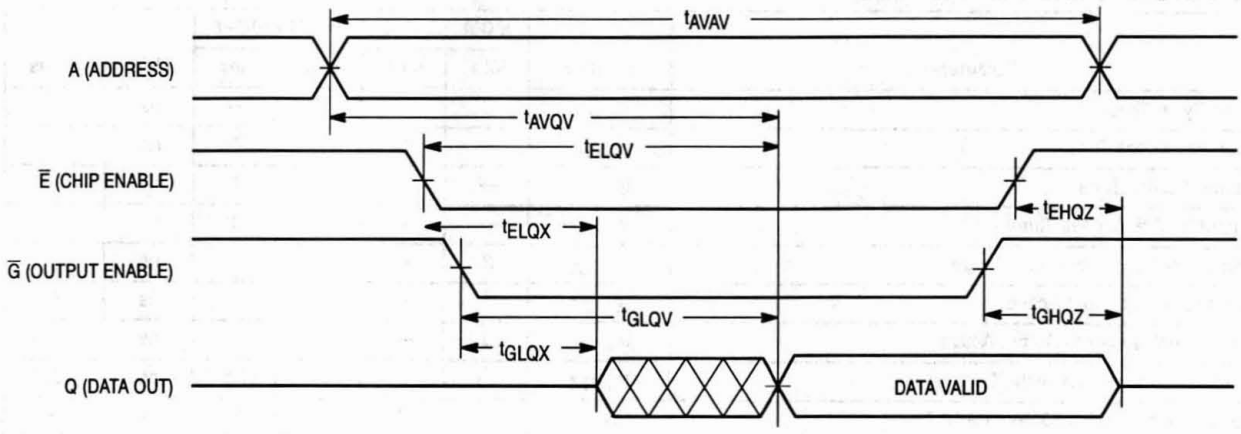
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

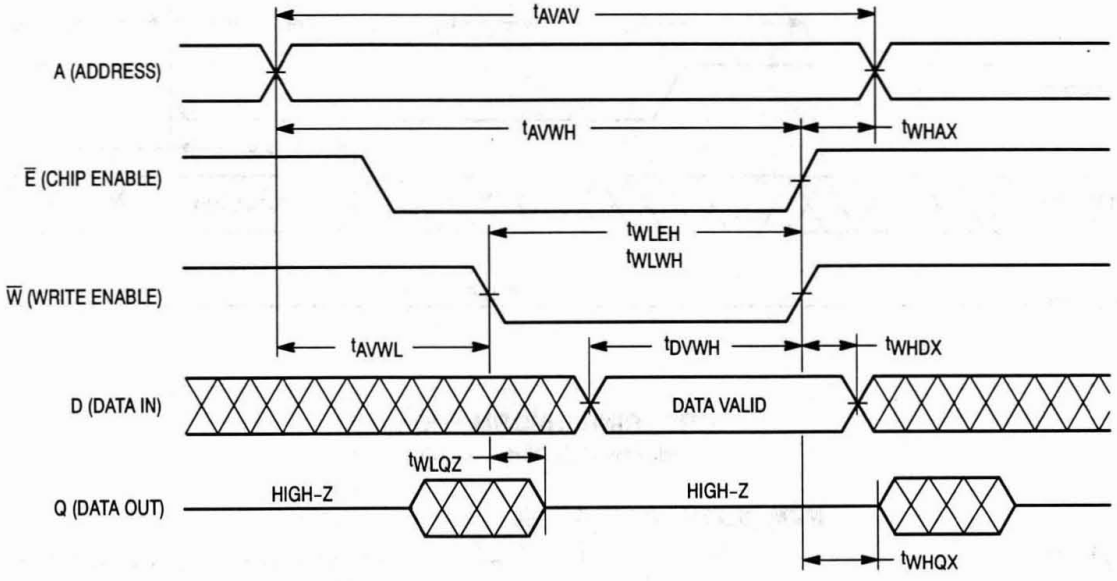


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6729C–6		MCM6729C–7		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	6	—	7	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	6	—	7	—	ns	
Address Valid to End of Write, $\overline{G}$ High	t_{AVWH}	6	—	7	—	ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	6	—	7	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH} t_{WLEH}	6	—	7	—	ns	
Data Valid to End of Write	t_{DVWH}	3	—	3.5	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	—	3.5	—	3.5	ns	4,5,6
Write High to Output Active	t_{WHQX}	3	—	3	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	1	—	1	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage with load of Figure 1b.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

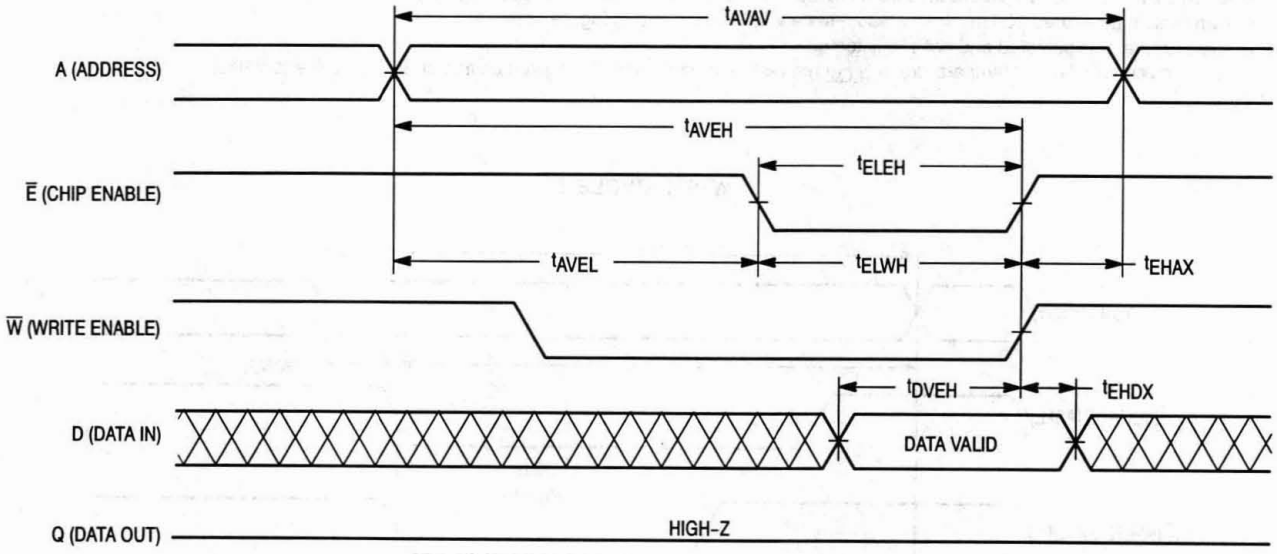


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6729C–6		MCM6729C–7		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	6	—	7	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	6	—	7	—	ns	
Enable to End of Write	t_{ELEH} t_{ELWH}	5	—	6	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	3	—	3.5	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6729C WJ X X

- MCM — Motorola Memory Prefix
- 6729C — Part Number
- WJ — Package (WJ = 400 mil SOJ)
- X — Speed (6 = 6 ns, 7 = 7 ns)
- X — Shipping Method (R = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6729CWJ6 MCM6729CWJ7
MCM6729CWJ6R MCM6729CWJ7R

MCM6729D

256K x 4 Bit Fast Static Random Access Memory

WJ PACKAGE
400 MIL SOJ
CASE 857A–02

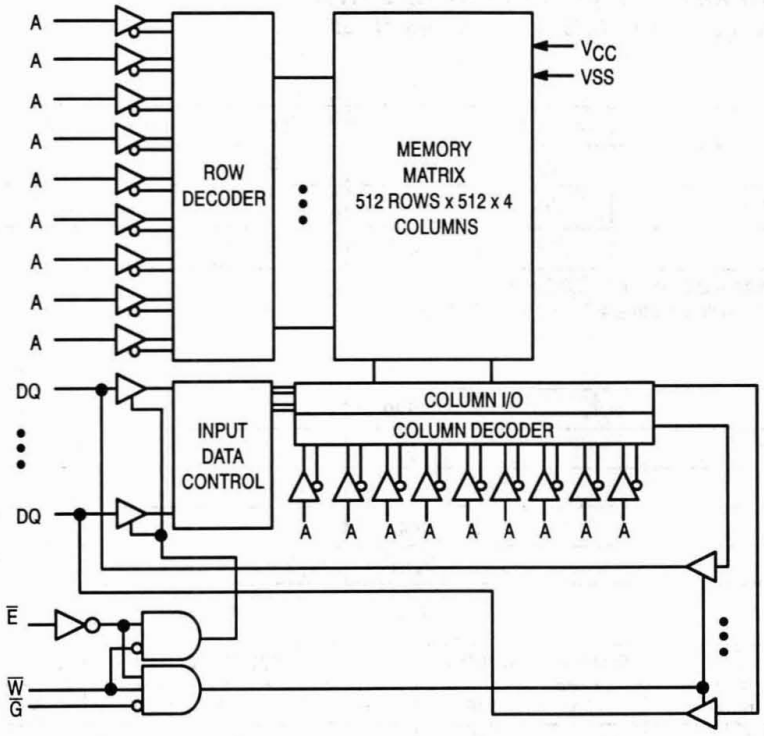
The MCM6729D is a 1,048,576 bit static random access memory organized as 262,144 words of 4 bits. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

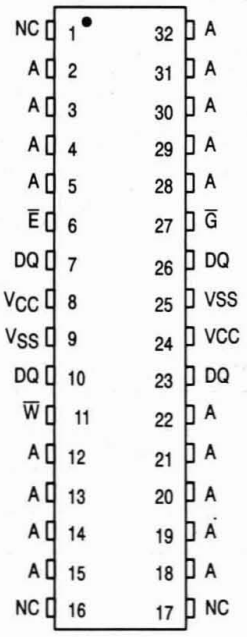
This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small–outline J–leaded package.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 8, 10, 12 ns
- Center Power and I/O Pins for Reduced Noise

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

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TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	H	Output Disabled	I_{CCA}	High–Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High–Z	Write Cycle

2

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	±30	mA
Power Dissipation	P_D	1.2	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	6729D–8	6729D–10	6729D–12	Unit	Notes
AC Active Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	I_{CCA}	195	165	155	mA	1, 2, 3
Active Quiescent Current ($\overline{E}$ = V_{IL}, V_{CC} = max, f = 0 MHz)	I_{CC2}	90	90	90	mA	
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	60	60	60	mA	1, 2, 3
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	20	mA	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
2. All addresses transition simultaneously low (LSB) and then high (MSB).
3. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

2

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1a

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	6729D–8		6729D–10		6729D–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Access Time	t_{AVQV}	—	8	—	10	—	12	ns	
Enable Access Time	t_{ELQV}	—	8	—	10	—	12	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	5	—	6	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	3	—	3	—	3	—	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	—	4	—	5	—	6	ns	4,5,6
Output Enable High to Output High–Z	t_{GHQZ}	—	4	—	5	—	6	ns	4,5,6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} (max) < t_{ELQX} (min), and t_{GHQZ} (max) < t_{GLQX} (min), both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1b.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

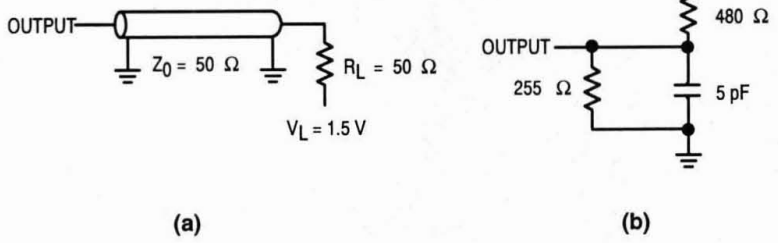
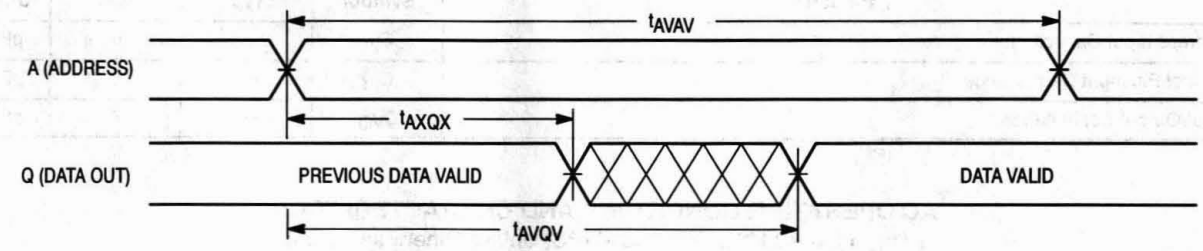


Figure 1. AC Test Loads

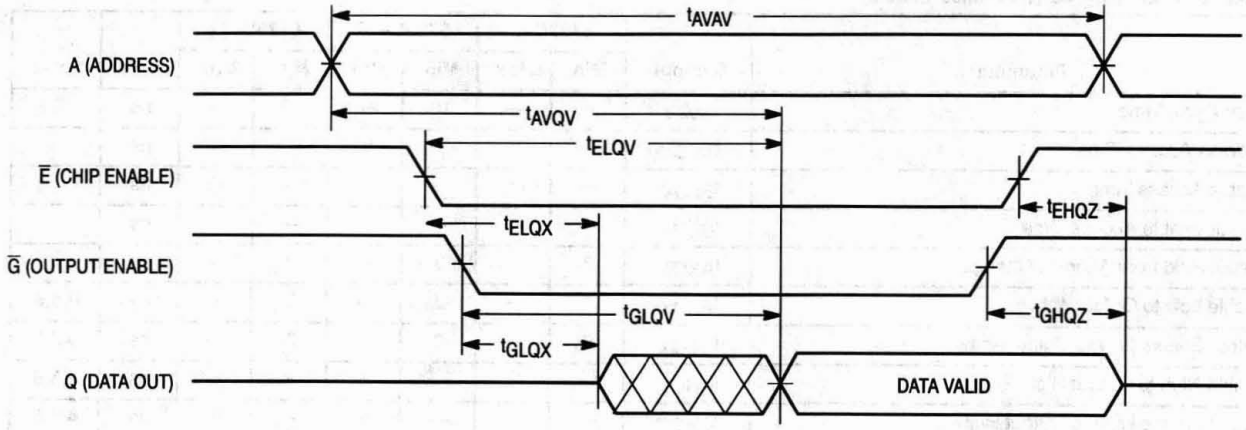
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

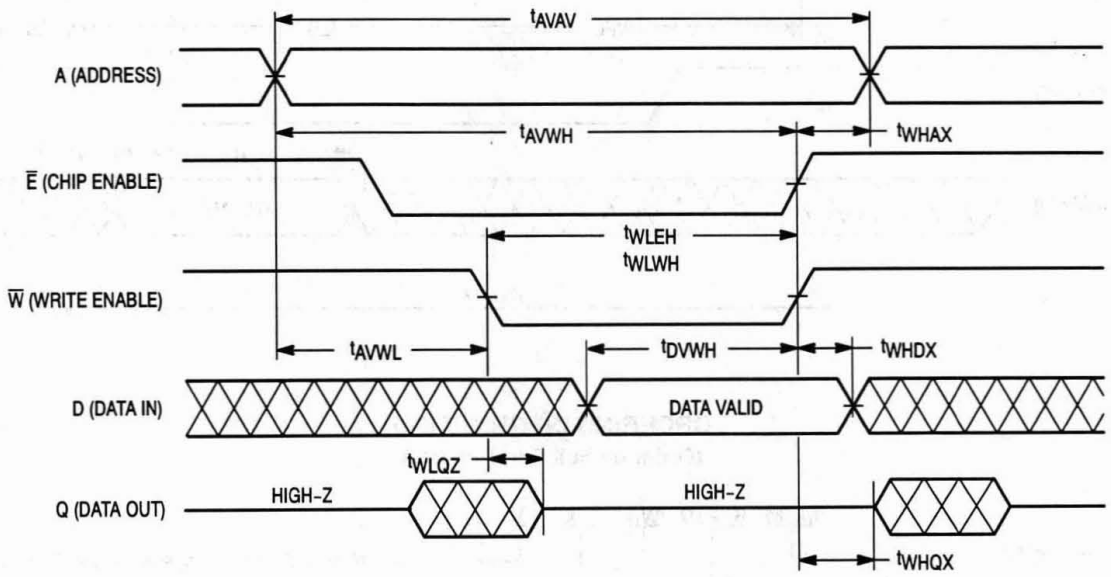


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6729D–8		6729D–10		6729D–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	8	—	9	—	10	—	ns	
Address Valid to End of Write, $\overline{G}$ High	t_{AVWH}	7	—	8	—	9	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	8	—	9	—	10	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	7	—	8	—	9	—	ns	
Data Valid to End of Write	t_{DVWH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	—	4	—	5	—	6	ns	4,5,6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage with load of Figure 1b.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

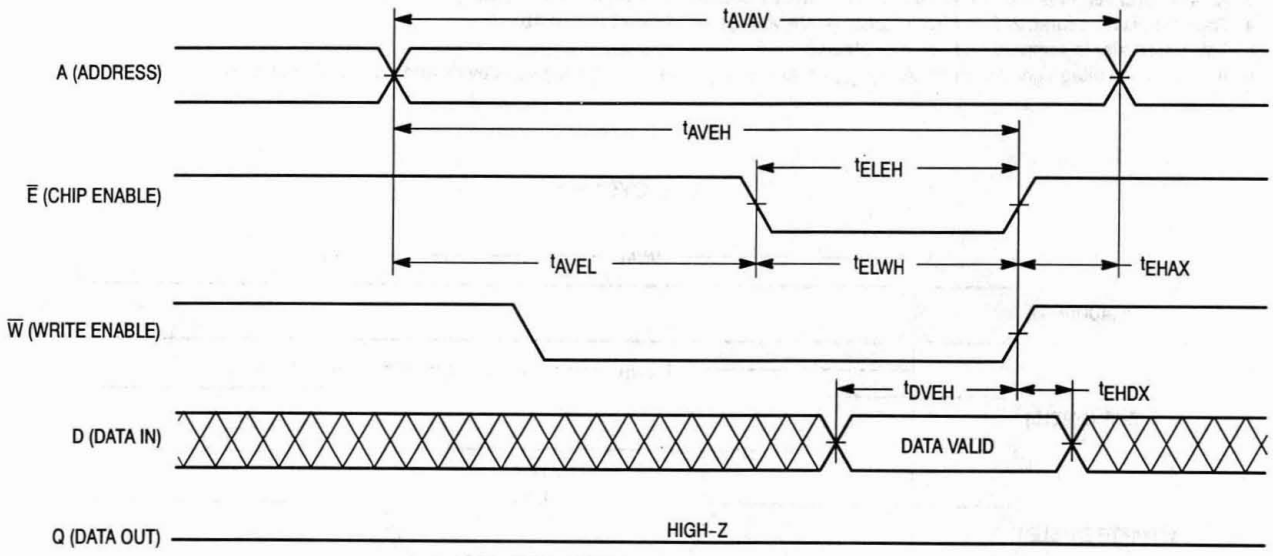


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6729D–8		6729D–10		6729D–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	7	—	8	—	9	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	7	—	8	—	9	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6729D WJ XX X

- MCM — Motorola Memory Prefix
- 6729D — Part Number
- WJ — Package (WJ = 400 mil SOJ)
- XX — Speed (8 = 8 ns, 10 = 10 ns, 12 = 12 ns)
- X — Shipping Method (R = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6729DWJ8, MCM6729DWJ8R, MCM6729DWJ10, MCM6729DWJ10R, MCM6729DWJ12, MCM6729DWJ12R

MCM6929

2

Advance Information

256K x 4 Bit Fast Static Random Access Memory

WJ PACKAGE
400 MIL SOJ
CASE 857A–02

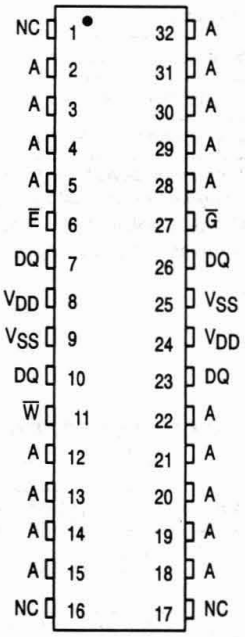
The MCM6929 is a 1,048,576 bit static random access memory organized as 262,144 words of 4 bits. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

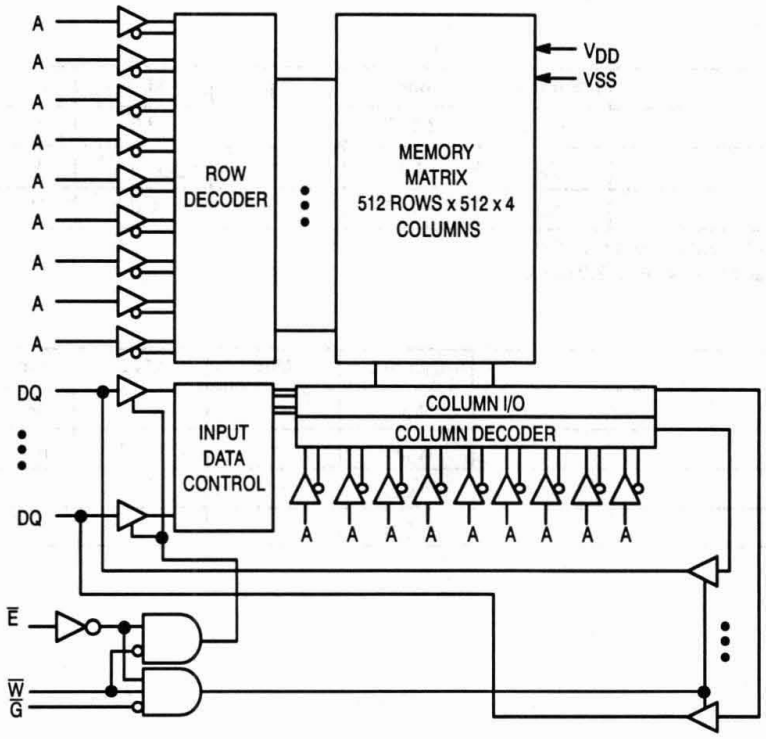
This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small–outline J–leaded package.

- Single 3.3 V Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 8, 10, 12, 15 ns
- Center Power and I/O Pins for Reduced Noise
- Fully 3.3 V BiCMOS

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ	Data Input/Output
V_{DD}	+ 3.3 V Power Supply
V_{SS}	Ground
NC	No Connection

This document contains information on a new product. Motorola reserves the right to change or discontinue this product without notice.

REV 4
2/26/97

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{DD} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	H	Output Disabled	I_{DDA}	High–Z	—
L	L	H	Read	I_{DDA}	D_{out}	Read Cycle
L	X	L	Write	I_{DDA}	High–Z	Write Cycle

2

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{DD}	V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	0.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V +10%, – 5% T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{DD}	3.135	3.3	3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{DD} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = –0.5 V dc; V_{IL} (min) = –2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{DD} + 0.3 V dc; V_{IH} (max) = V_{DD} + 2 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{DD})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{DD})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS (See Note 1)

Parameter	Symbol	6929–8		6929–10		6929–12		6929–15		Unit	Notes
		Typ	Max	Typ	Max	Typ	Max	Typ	Max		
AC Active Supply Current (I_{out} = 0 mA) (V_{DD} = max, f = f_{max})	I_{DDA}	—	150	—	130	—	120	—	110	mA	2, 3, 4
Active Quiescent Current ($\overline{E}$ = V_{IL}, V_{DD} = max, f = 0 MHz)	I_{DD2}	—	80	—	80	—	80	—	80	mA	
AC Standby Current ($\overline{E}$ = V_{IH}, V_{DD} = max, f = f_{max})	I_{SB1}	—	50	—	45	—	40	—	35	mA	2, 3, 4
CMOS Standby Current (V_{DD} = max, f = 0 MHz, $\overline{E} \geq V_{DD} - 0.2$ V, $V_{in} \leq V_{SS} + 0.2$ V, or $\geq V_{DD} - 0.2$ V)	I_{SB2}	—	20	—	20	—	20	—	20	mA	

NOTES:
1. Typical current = 25°C @ 3.3 V.
2. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
3. All addresses transition simultaneously low (LSB) and then high (MSB).
4. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_A = 0 to +70°C, Unless Otherwise Noted)

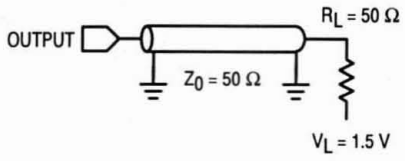
Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	6929–8		6929–10		6929–12		6929–15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	3
Address Access Time	t_{AVQV}	—	8	—	10	—	12	—	15	ns	
Enable Access Time	t_{ELQV}	—	8	—	10	—	12	—	15	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	5	—	6	—	7	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	3	—	3	—	3	—	3	—	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	—	4	—	5	—	6	—	7	ns	4,5,6
Output Enable High to Output High–Z	t_{GHQZ}	—	4	—	5	—	6	—	7	ns	4,5,6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

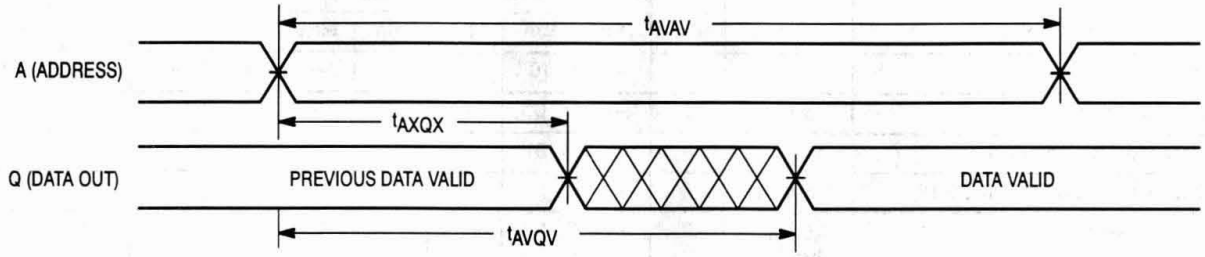


TIMING LIMITS

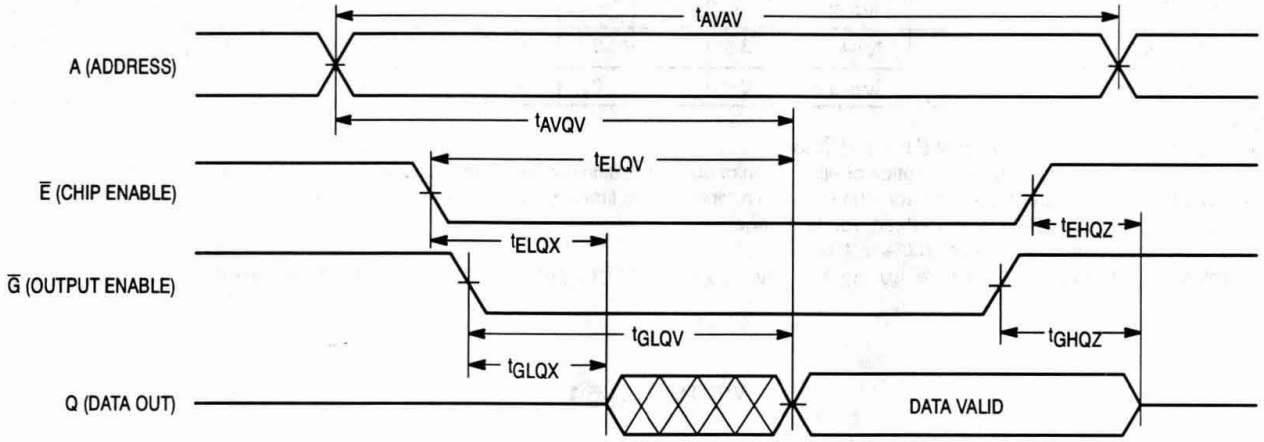
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Figure 1. AC Test Load

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

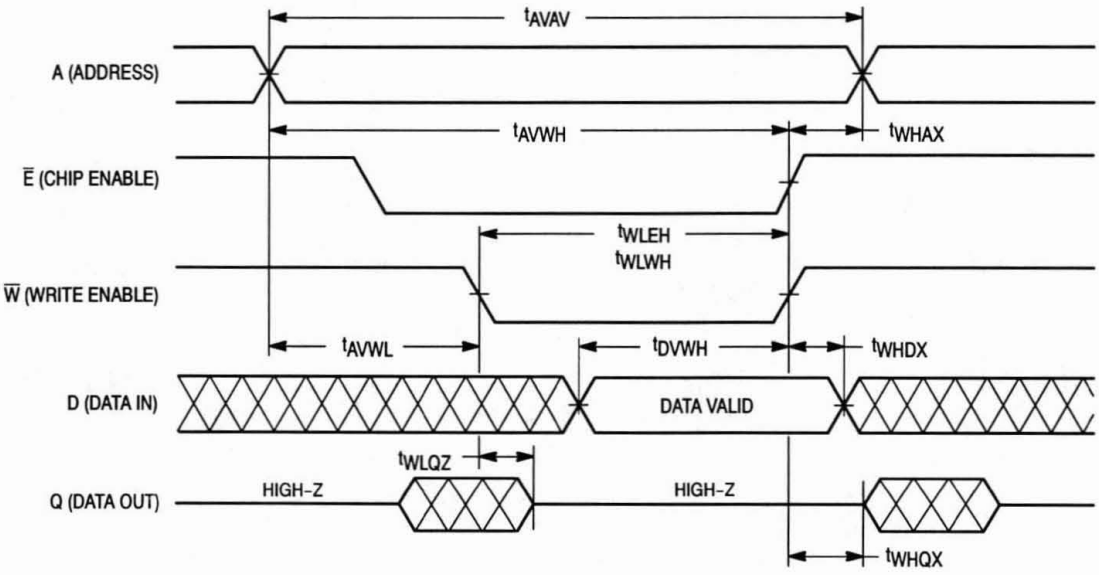


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6929–8		6929–10		6929–12		6929–15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	8	—	9	—	10	—	12	—	ns	
Address Valid to End of Write, $\overline{G}$ High	t_{AVWH}	7	—	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	8	—	9	—	10	—	12	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	7	—	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	4	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	—	4	—	5	—	6	—	7	ns	4,5,6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	3	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

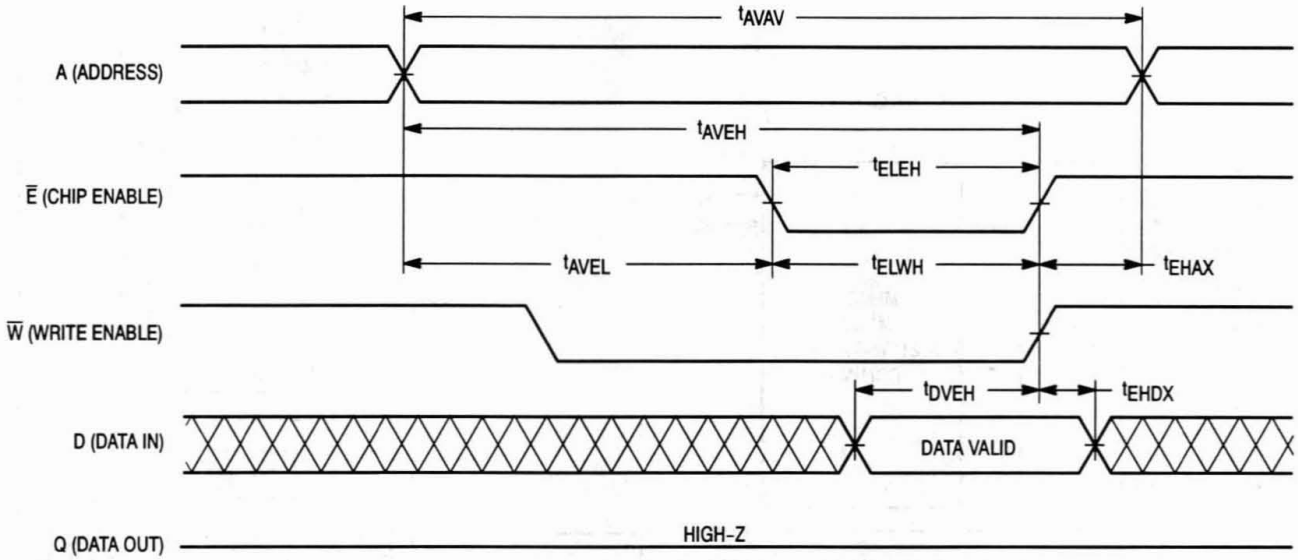


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6929–8		6929–10		6929–12		6929–15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	7	—	8	—	9	—	10	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	7	—	8	—	9	—	10	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	4	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6929 WJ XX X

- Motorola Memory Prefix — MCM
- Part Number — 6929
- Package (WJ = 400 mil SOJ) — WJ
- Speed (8 = 8 ns, 10 = 10 ns, 12 = 12 ns, 15 = 15 ns) — XX
- Shipping Method (R = Tape and Reel, Blank = Rails) — X

Full Part Numbers — MCM6929WJ8, MCM6929WJ8R, MCM6929WJ10, MCM6929WJ10R, MCM6929WJ12, MCM6929WJ12R, MCM6929WJ15, MCM6929WJ15R

MCM6929A

2

Advance Information

256K x 4 Bit Fast Static Random Access Memory

WJ PACKAGE
400 MIL SOJ
CASE 857A–02

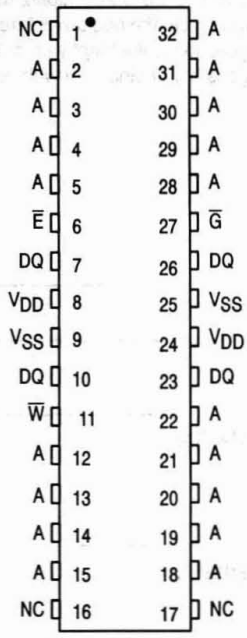
The MCM6929A is a 1,048,576 bit static random access memory organized as 262,144 words of 4 bits. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

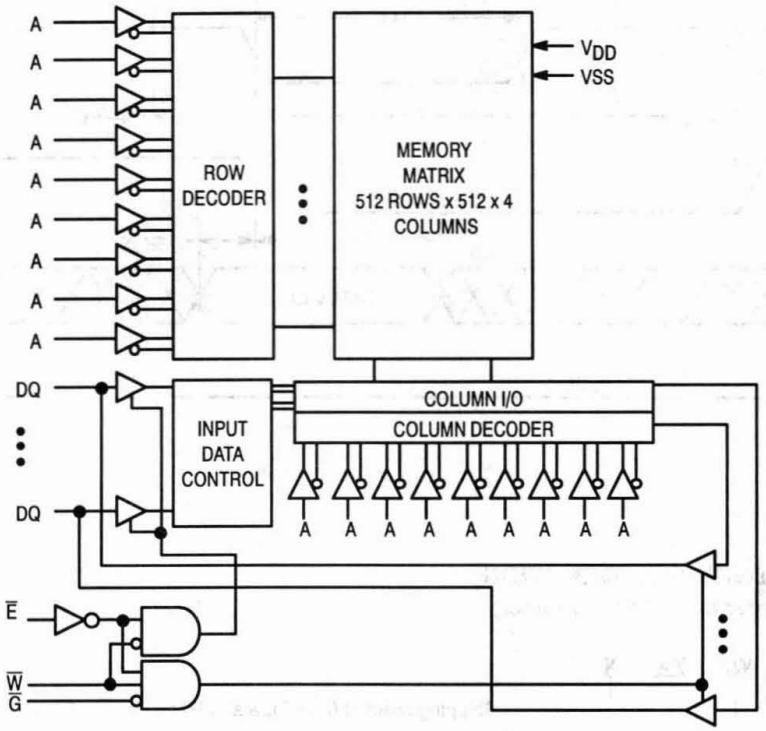
This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small–outline J–leaded package.

- Single 3.3 V Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 8, 10, 12, 15 ns
- Center Power and I/O Pins for Reduced Noise
- Fully 3.3 V BiCMOS

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ	Data Input/Output
V_{DD}	+ 3.3 V Power Supply
V_{SS}	Ground
NC	No Connection

This document contains information on a new product. Motorola reserves the right to change or discontinue this product without notice.

REV1
2/26/97

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{DD} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	H	Output Disabled	I_{DDA}	High–Z	—
L	L	H	Read	I_{DDA}	D_{out}	Read Cycle
L	X	L	Write	I_{DDA}	High–Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{DD}	V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	0.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V +10%, – 5% T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{DD}	3.135	3.3	3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{DD} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = –0.5 V dc; V_{IL} (min) = –2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{DD} + 0.3 V dc; V_{IH} (max) = V_{DD} + 2 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{DD})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{DD})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS (See Note 1)

Parameter	Symbol	6929A–8		6929A–10		6929A–12		6929A–15		Unit	Notes
		Typ	Max	Typ	Max	Typ	Max	Typ	Max		
AC Active Supply Current (I_{out} = 0 mA) (V_{DD} = max, f = f_{max})	I_{DDA}	—	150	—	130	—	120	—	110	mA	2, 3, 4
Active Quiescent Current ($\overline{E}$ = V_{IL}, V_{DD} = max, f = 0 MHz)	I_{DD2}	—	80	—	80	—	80	—	80	mA	
AC Standby Current ($\overline{E}$ = V_{IH}, V_{DD} = max, f = f_{max})	I_{SB1}	—	50	—	45	—	40	—	35	mA	2, 3, 4
CMOS Standby Current (V_{DD} = max, f = 0 MHz, $\overline{E} \geq V_{DD} - 0.2$ V, $V_{in} \leq V_{SS} + 0.2$ V, or $\geq V_{DD} - 0.2$ V)	I_{SB2}	—	20	—	20	—	20	—	20	mA	

NOTES:
1. Typical current = 25°C @ 3.3 V.
2. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
3. All addresses transition simultaneously low (LSB) and then high (MSB).
4. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	6929A–8		6929A–10		6929A–12		6929A–15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	3
Address Access Time	t_{AVQV}	—	8	—	10	—	12	—	15	ns	
Enable Access Time	t_{ELQV}	—	8	—	10	—	12	—	15	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	5	—	6	—	7	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	3	—	3	—	3	—	3	—	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	—	4	—	5	—	6	—	7	ns	4,5,6
Output Enable High to Output High–Z	t_{GHQZ}	—	4	—	5	—	6	—	7	ns	4,5,6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

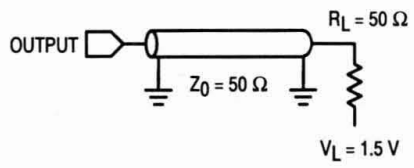
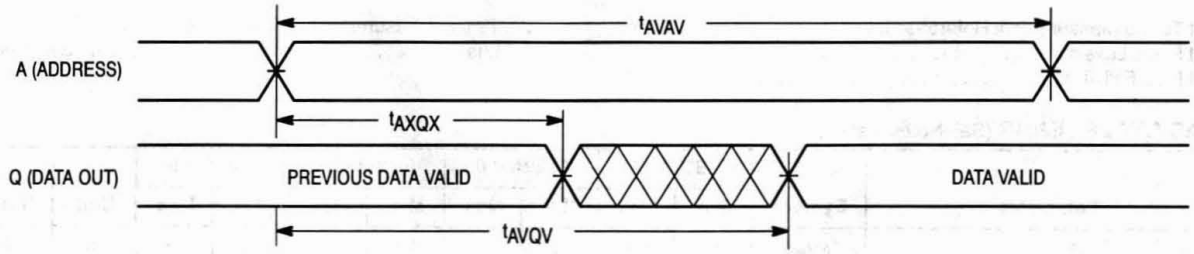


Figure 1. AC Test Load

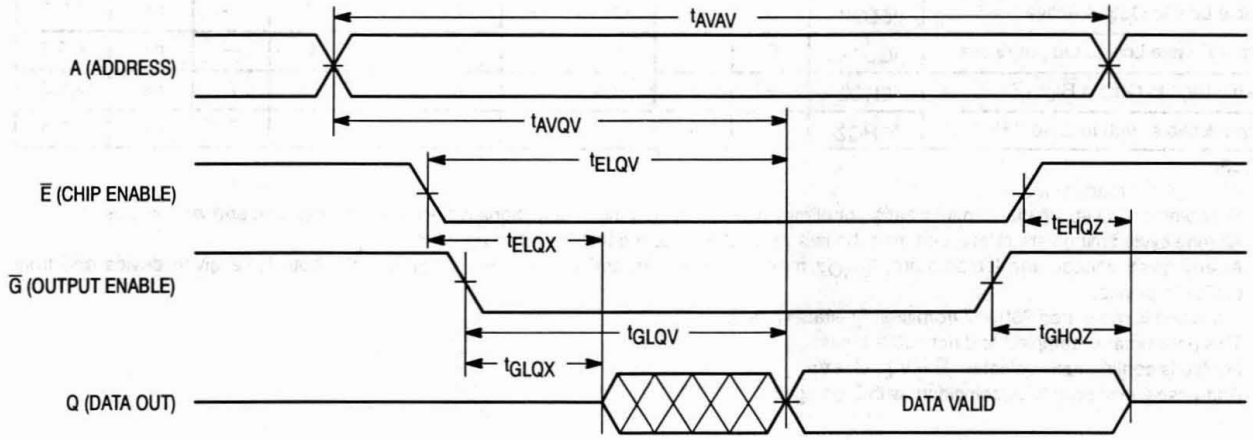
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

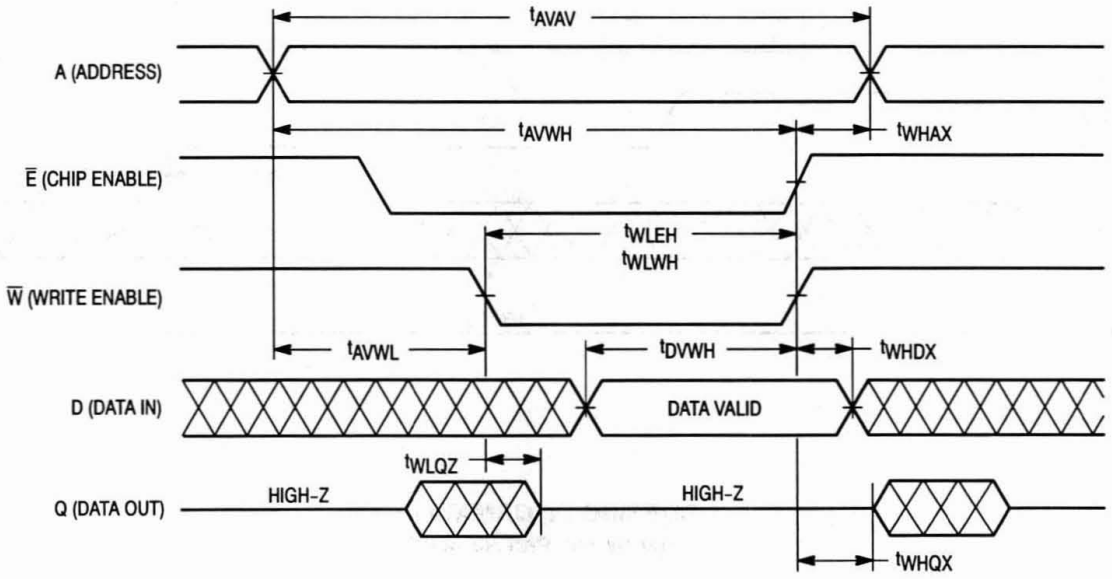


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6929A–8		6929A–10		6929A–12		6929A–15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	8	—	9	—	10	—	12	—	ns	
Address Valid to End of Write, $\overline{G}$ High	t_{AVWH}	7	—	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	8	—	9	—	10	—	12	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	7	—	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	4	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	—	4	—	5	—	6	—	7	ns	4,5,6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	3	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

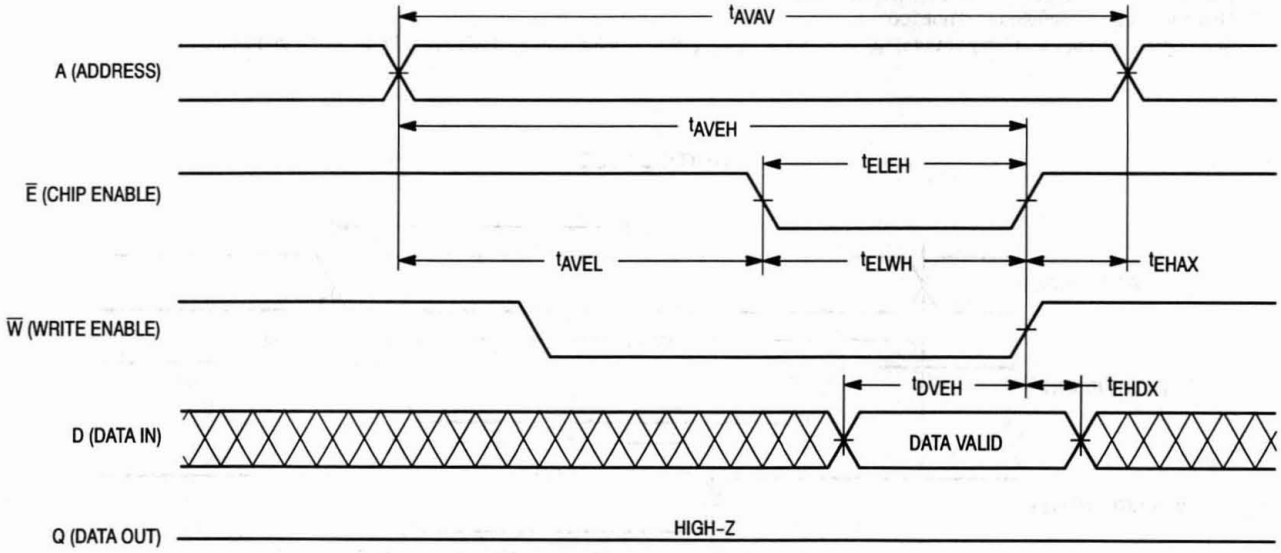


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6929A–8		6929A–10		6929A–12		6929A–15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	7	—	8	—	9	—	10	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	7	—	8	—	9	—	10	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	4	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6929A WJ XX X

- MCM — Motorola Memory Prefix
- 6929A — Part Number
- WJ — Package (WJ = 400 mil SOJ)
- XX — Speed (8 = 8 ns, 10 = 10 ns, 12 = 12 ns, 15 = 15 ns)
- X — Shipping Method (R = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6929AWJ8, MCM6929AWJ8R, MCM6929AWJ10, MCM6929AWJ10R, MCM6929AWJ12, MCM6929AWJ12R, MCM6929AWJ15, MCM6929AWJ15R

MCM6929–C

256K x 4 Bit Fast Static Random Access Memory

WJ PACKAGE
400 MIL SOJ
CASE 857A–02

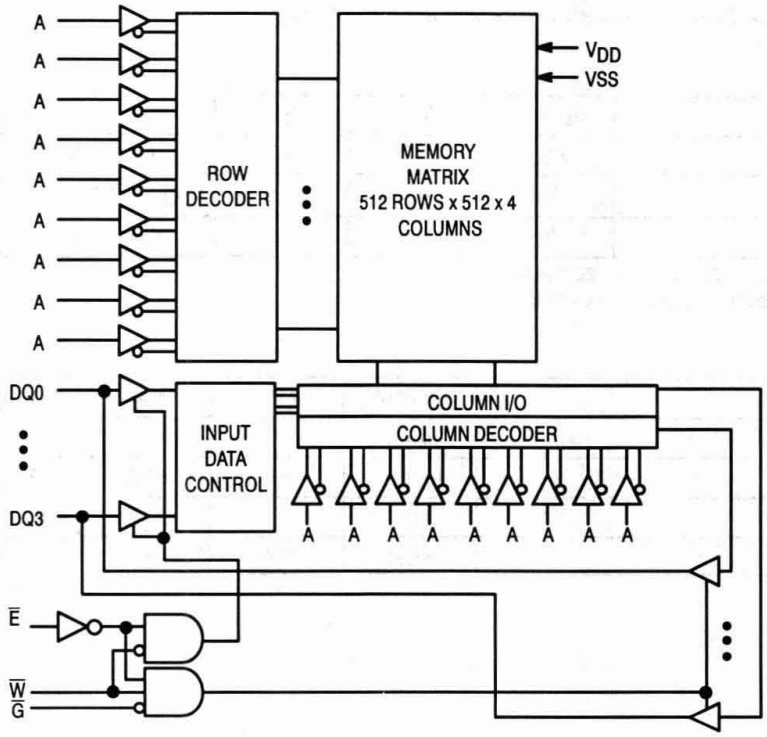
The MCM6929WJssC is a 1,048,576 bit static random access memory organized as 262,144 words of 4 bits. This device is fabricated using high performance silicon–gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

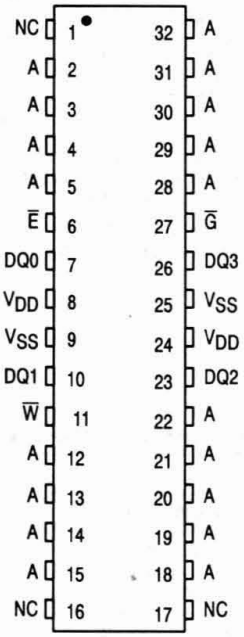
This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small–outline J–leaded package.

- Single 3.3 V Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 8, 10, 12, 15 ns
- Center Power and I/O Pins for Reduced Noise
- Fully 3.3 V BiCMOS
- Industrial Temperature (– 40°C to + 85°C)

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

A0 – A17	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0 – DQ3	Data Input/Output
V_{DD}	+ 3.3 V Power Supply
V_{SS}	Ground
NC	No Connection

REV 1
2/26/97

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{DD} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	H	Output Disabled	I_{DDA}	High–Z	—
L	L	H	Read	I_{DDA}	D_{out}	Read Cycle
L	X	L	Write	I_{DDA}	High–Z	Write Cycle

2

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{DD}	V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	0.6	W
Temperature Under Bias	T_{bias}	– 40 to + 85	°C
Operating Temperature	T_A	– 40 to + 85	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V +10%, – 5% T_A = – 40 to + 85°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{DD}	3.135	3.3	3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{DD} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = –0.5 V dc; V_{IL} (min) = –2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{DD} + 0.3 V dc; V_{IH} (max) = V_{DD} + 2 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{DD})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{DD})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS (See Note 1)

Parameter	Symbol	6929–8		6929–10		6929–12		6929–15		Unit	Notes
		Typ	Max	Typ	Max	Typ	Max	Typ	Max		
AC Active Supply Current (I_{out} = 0 mA) (V_{DD} = max, f = f_{max})	I_{DDA}	—	150	—	130	—	120	—	110	mA	2, 3, 4
Active Quiescent Current ($\overline{E}$ = V_{IL}, V_{DD} = max, f = 0 MHz)	I_{DD2}	—	80	—	80	—	80	—	80	mA	
AC Standby Current ($\overline{E}$ = V_{IH}, V_{DD} = max, f = f_{max})	I_{SB1}	—	50	—	45	—	40	—	35	mA	2, 3, 4
CMOS Standby Current (V_{DD} = max, f = 0 MHz, $\overline{E} \geq V_{DD} - 0.2$ V, $V_{in} \leq V_{SS} + 0.2$ V, or $\geq V_{DD} - 0.2$ V)	I_{SB2}	—	20	—	20	—	20	—	20	mA	

NOTES:
1. Typical current = 25°C @ 3.3 V.
2. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
3. All addresses transition simultaneously low (LSB) and then high (MSB).
4. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_A = – 40 to + 85°C, Unless Otherwise Noted)

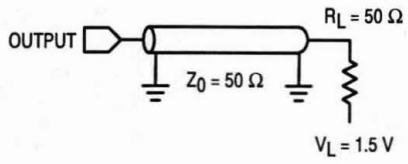
Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	6929–8		6929–10		6929–12		6929–15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	3
Address Access Time	t_{AVQV}	—	8	—	10	—	12	—	15	ns	
Enable Access Time	t_{ELQV}	—	8	—	10	—	12	—	15	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	5	—	6	—	7	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	3	—	3	—	3	—	3	—	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	—	4	0	5	0	6	0	7	ns	4,5,6
Output Enable High to Output High–Z	t_{GHQZ}	—	4	0	5	0	6	0	7	ns	4,5,6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

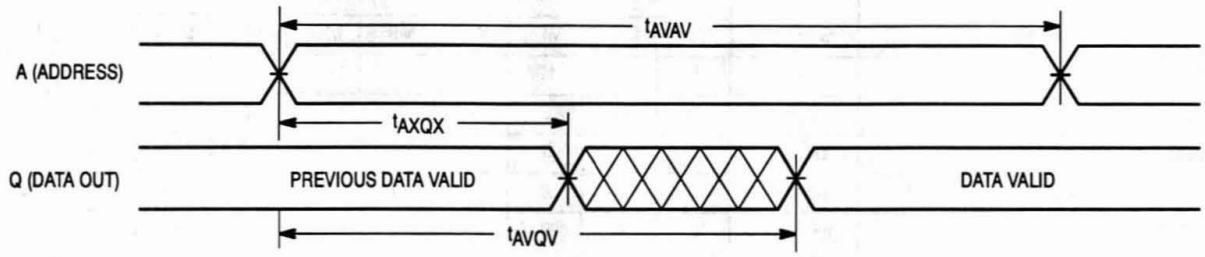


TIMING LIMITS

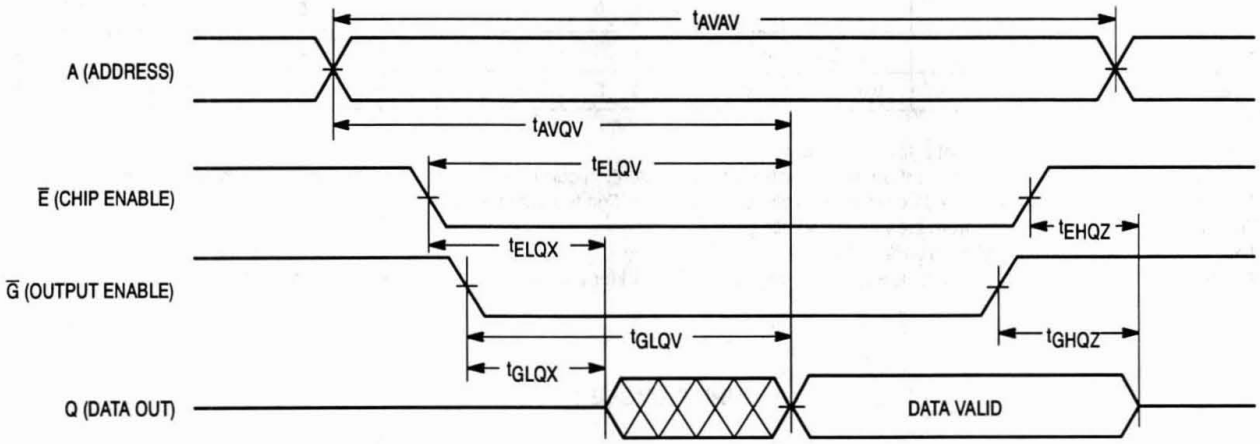
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Figure 1. AC Test Load

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

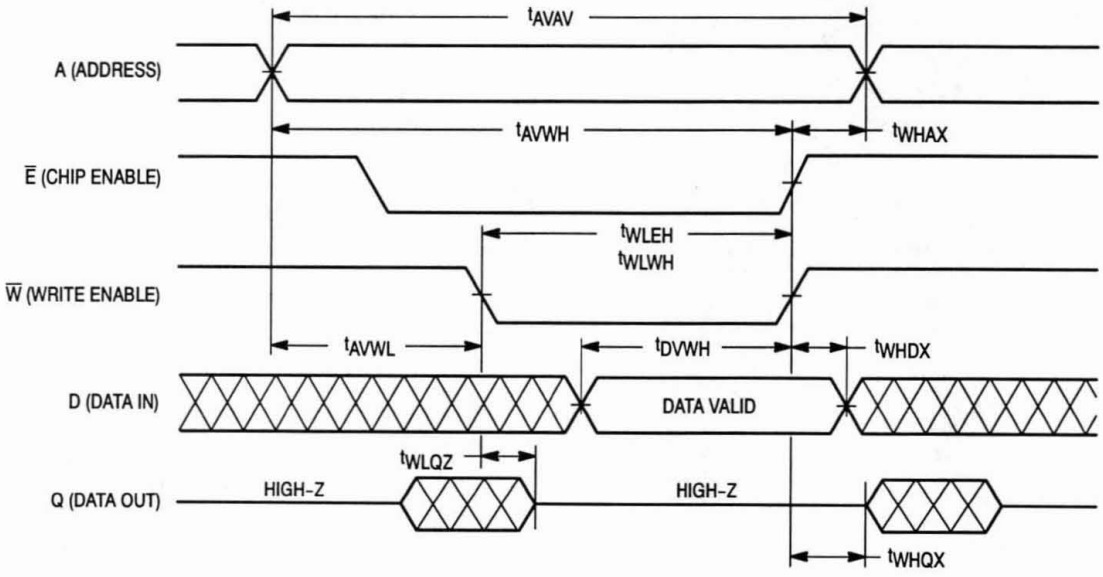


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6929–8		6929–10		6929–12		6929–15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	8	—	9	—	10	—	12	—	ns	
Address Valid to End of Write, $\overline{G}$ High	t_{AVWH}	7	—	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	8	—	9	—	10	—	12	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	7	—	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	4	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	4	0	5	0	6	0	7	ns	4,5,6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	3	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

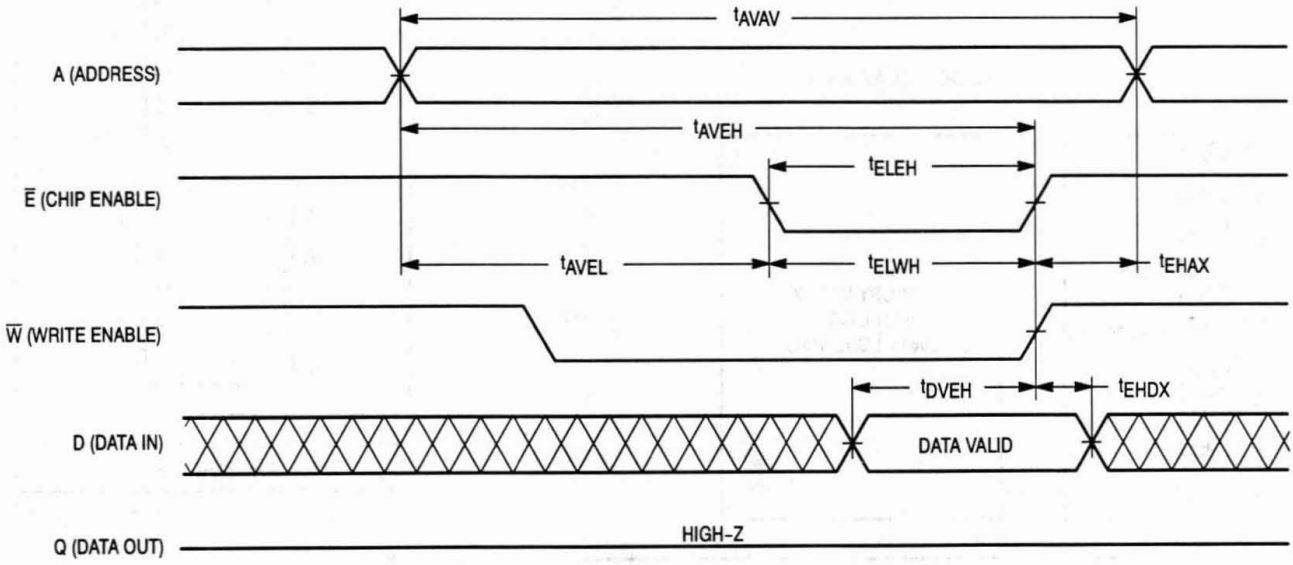


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6929–8		6929–10		6929–12		6929–15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	7	—	8	—	9	—	10	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	7	—	8	—	9	—	10	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	4	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

SCM 6929 WJ XX X X

- SCM — Motorola Memory Prefix
- 6929 — Part Number
- WJ — Package (WJ = 400 mil SOJ)
- XX — Speed (8 = 8 ns, 10 = 10 ns, 12 = 12 ns, 15 = 15 ns)
- X — Shipping Method (R = Tape and Reel, Blank = Rails)
- X — C = Industrial Temperature

Full Part Numbers — SCM6929WJ8C, SCM6929WJ8RC, SCM6929WJ10C, SCM6929WJ10RC, SCM6929WJ12C, SCM6929WJ12RC, SCM6929WJ15C, SCM6929WJ15RC

MCM6227B

2

1M x 1 Bit Static Random Access Memory

The MCM6227B is a 1,048,576 bit static random–access memory organized as 1,048,576 words of 1 bit. Static design eliminates the need for external clocks or timing strobes while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6227B is each equipped with a chip enable ($\overline{E}$) pin. This feature provides reduced system power requirements without degrading access time performance.

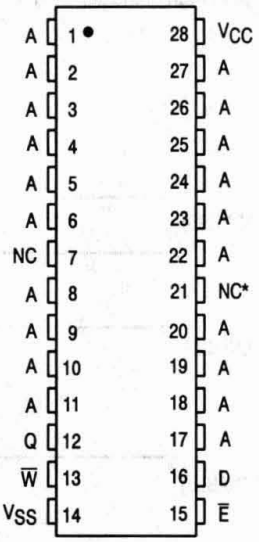
The MCM6227B is available in 300 mil and 400 mil, 28–lead surface–mount SOJ packages.

- Single 5 V ± 10% Power Supply
- Fast Access Times: 15/17/20/25/35 ns
- Equal Address and Chip Enable Access Times
- Input and Output are TTL Compatible
- Three–State Output
- Low Power Operation: 115/110/105/100/95 mA Maximum, Active AC

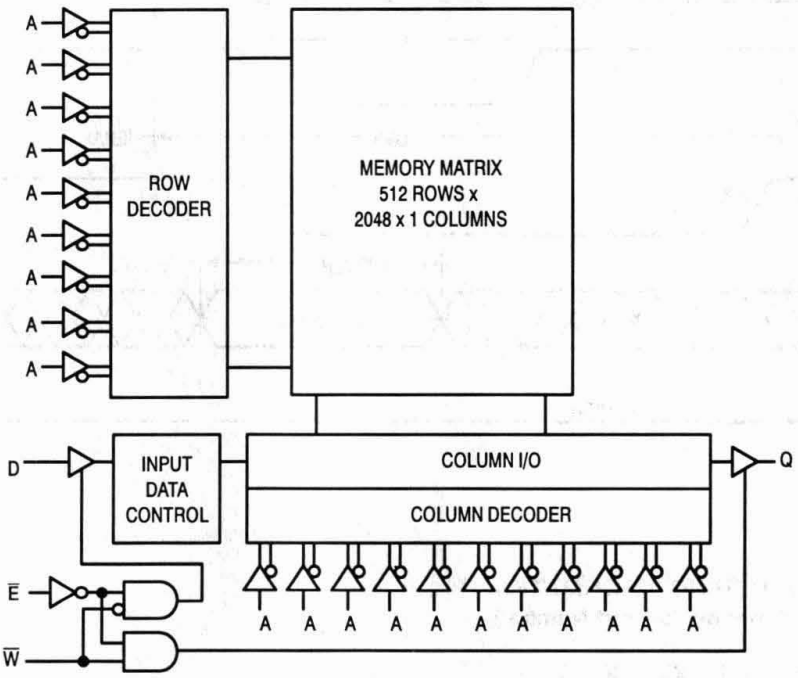
J PACKAGE
300 MIL SOJ
CASE 810B–03

WJ PACKAGE
400 MIL SOJ
CASE 810–03

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A	Address Inputs
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D	Data Input
Q	Data Output
NC	No Connection
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

*If not used for no connect, then do not exceed voltages of – 0.5 to V_{CC} + 0.5 V. This pin is used for manufacturing diagnostics.

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TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	Not Selected	High–Z	—	I_{SB1}, I_{SB2}
L	H	Read	D_{out}	Read	I_{CCA}
L	L	Write	High–Z	Write	I_{CCA}

H = High, L = Low, X = Don't Care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	1.1	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} +0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns).
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1	µA
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max)	I_{CCA}			mA
MCM6227B–15: t_{AVAV} = 15 ns		—	115	
MCM6227B–17: t_{AVAV} = 17 ns		—	110	
MCM6227B–20: t_{AVAV} = 20 ns		—	105	
MCM6227B–25: t_{AVAV} = 25 ns		—	100	
MCM6227B–35: t_{AVAV} = 35 ns		—	95	
AC Standby Current (V_{CC} = max, $\overline{E}$ = V_{IH}, f ≤ f_{max})	I_{SB1}			mA
MCM6227B–15: t_{AVAV} = 15 ns		—	40	
MCM6227B–17: t_{AVAV} = 17 ns		—	35	
MCM6227B–20: t_{AVAV} = 20 ns		—	30	
MCM6227B–25: t_{AVAV} = 25 ns		—	25	
MCM6227B–35: t_{AVAV} = 35 ns		—	20	
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V, V_{CC} = max, f = 0 MHz)	I_{SB2}	—	5	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except Clocks and D, Q $\overline{E}$ and $\overline{W}$	C_{in}	4 5	6 8	pF
Input and Output Capacitance	D, Q	C_{in}, C_{out}	5	8	pF

2

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1a

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	6227B–15		6227B–17		6227B–20		6227B–25		6227B–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	2, 3
Address Access Time	t_{AVQV}	—	15	—	17	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	—	15	—	17	—	20	—	25	—	35	ns	4
Output Hold from Address Change	t_{AXQX}	5	—	5	—	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	5	—	5	—	5	—	5	—	ns	5, 6, 7
Enable High to Output High–Z	t_{EHQZ}	—	6	—	7	—	7	—	8	—	8	ns	5, 6, 7

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1b.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E} \le V_{IL}$).

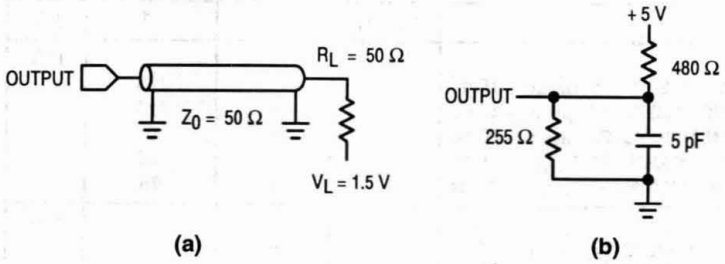
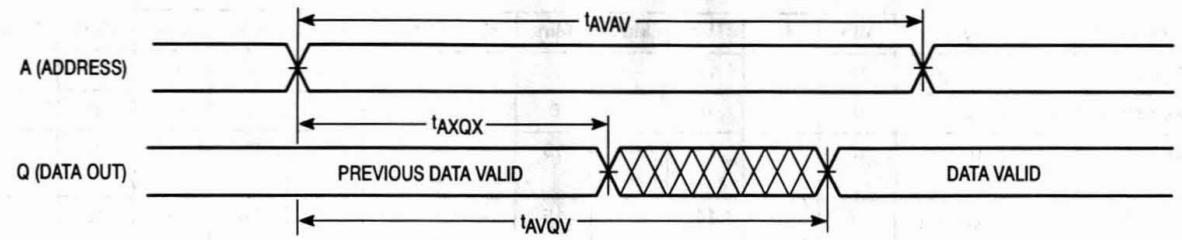


Figure 1. AC Test Loads

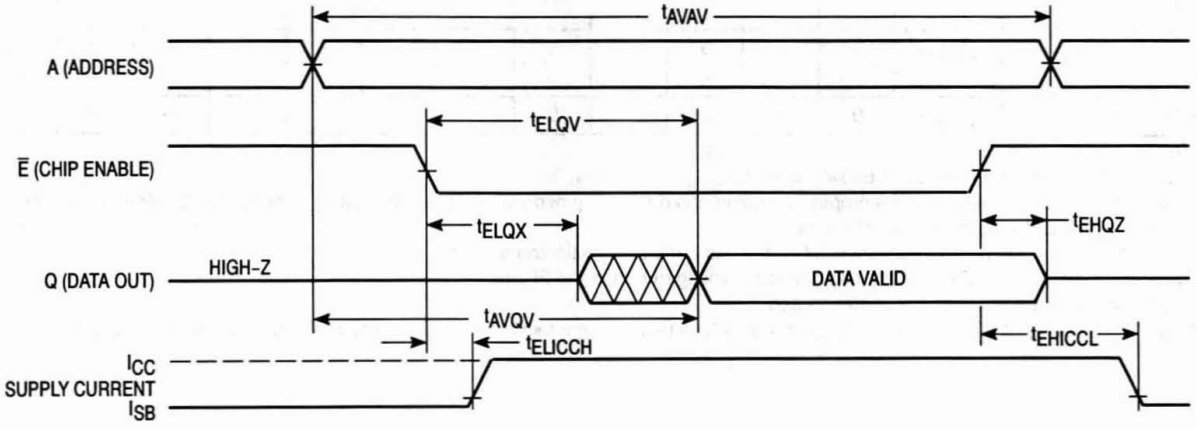
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Notes 1, 2, and 8)



READ CYCLE 2 (See Note 4)

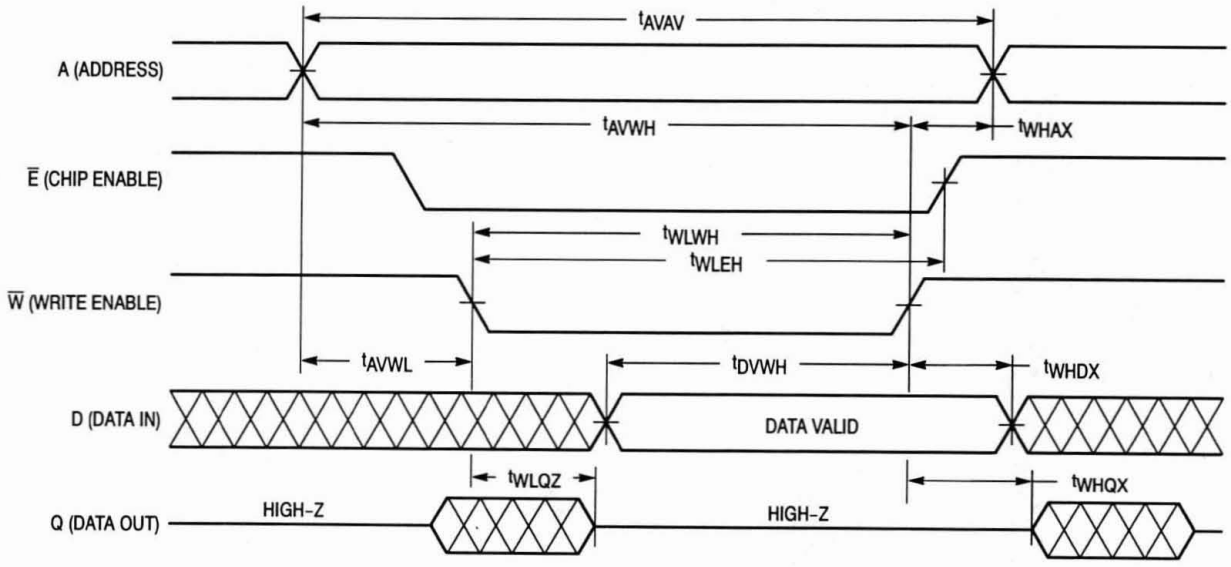


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6227B–15		6227B–17		6227B–20		6227B–25		6227B–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	14	—	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVWH}	7	—	8	—	8	—	10	—	11	—	ns	
Data Hold TIme	t_{WHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	—	6	—	7	—	7	—	8	—	8	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	5	—	5	—	5	—	5	—	5	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1b.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled See Notes 1 and 2)

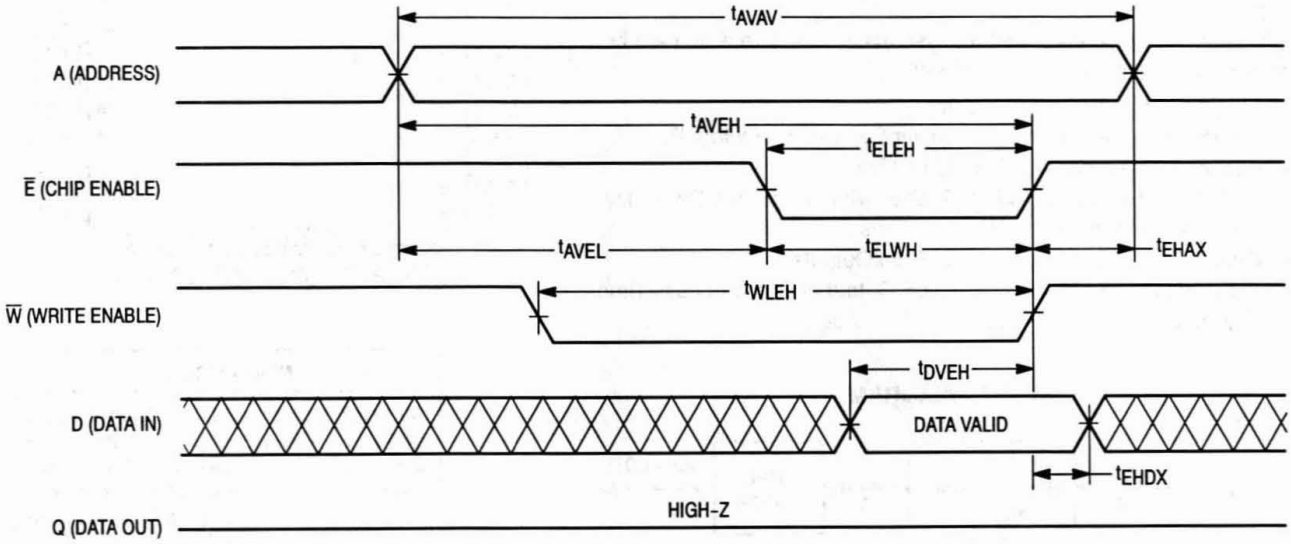


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6227B–15		6227B–17		6227B–20		6227B–25		6227B–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	12	—	14	—	15	—	17	—	20	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	10	—	11	—	12	—	15	—	20	—	ns	4, 5
Write Pulse Width	t_{WLEH}	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	7	—	8	—	8	—	10	—	11	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high–impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled See Notes 1 and 2)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6227B XX XX XX

- Motorola Memory Prefix
- Part Number
- Shipping Method (R2 = Tape and Reel, Blank = Rails)
- Speed (15 = 15 ns, 17 = 17 ns, 20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
- Package (J = 300 mil SOJ, WJ = 400 mil SOJ)

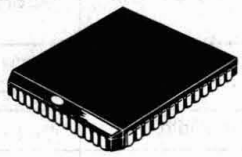
Full Part Numbers —

MCM6227BJ15	MCM6227BJ15R2	MCM6227BWJ15	MCM6227BWJ15R2
MCM6227BJ17	MCM6227BJ17R2	MCM6227BWJ17	MCM6227BWJ17R2
MCM6227BJ20	MCM6227BJ20R2	MCM6227BWJ20	MCM6227BWJ20R2
MCM6227BJ25	MCM6227BJ25R2	MCM6227BWJ25	MCM6227BWJ25R2
MCM6227BJ35	MCM6227BJ35R2	MCM6227BWJ35	MCM6227BWJ35R2

MCM62996

2

16K x 16 Bit Asynchronous Fast Static RAM



FN PACKAGE
52–LEAD PLCC
CASE 778–02

The MCM62996 is a 262,144 bit static random access memory organized as 16,384 words of 16 bits. The device integrates a 16K x 16 SRAM core with active high and active low chip enables, separate upper and lower byte write strobes, and a fast output enable. This device has increased output drive capability supported by multiple power pins. In addition, the output levels can be either 3.3 V or 5 V TTL compatible by choice of the appropriate output bus power supply.

Dual write strobes ($\overline{BWL}$ and $\overline{BWH}$) are provided to allow individually writeable bytes. $\overline{BWL}$ controls DQ0 – DQ7 (the lower bits), while $\overline{BWH}$ controls DQ8 – DQ15 (the upper bits).

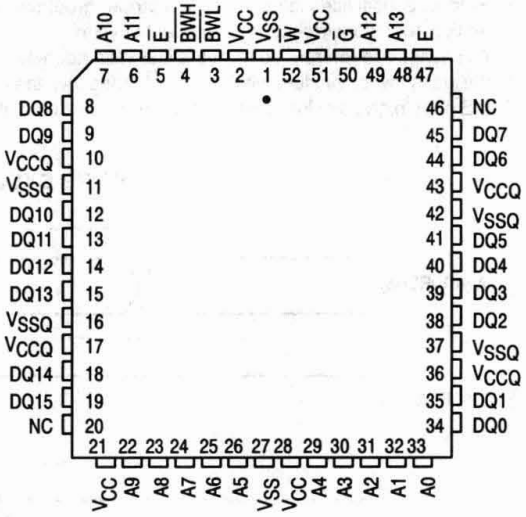
Additional power supply pins have been utilized and placed on the package for maximum performance. In addition, the output buffer power pins are electrically isolated from the other two and supply power only to the output buffers. This allows connecting the output buffers to 3.3 V instead of 5.0 V if desired. If 3.3 V output levels are chosen, the output buffer impedance in the "high" state is approximately equal to the impedance in the "low" state thereby allowing simplified transmission line terminations.

The MCM62996 will be available in a 52–pin plastic leaded chip carrier PLCC.

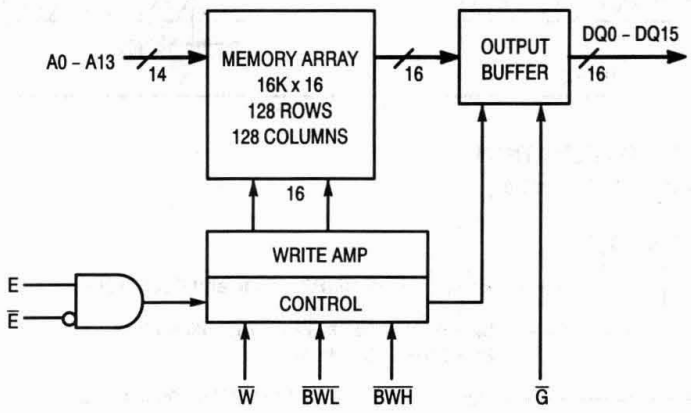
This device is ideally suited for systems that require wide data bus widths, cache memory, and tag RAMs.

- Single 5 V ± 10% Power Supply
- Choice of 5 V or 3.3 V ± 10% Power Supplies for Output Buffers
- Fast Access Times: 12/15/20/25 ns Max
- Byte Writeable via Dual Write Strobes with Abort Write Capability
- Common Data Inputs and Data Outputs
- Output Enable Controlled Three State Outputs
- High Output Drive Capability: 85 pF/Output at Rated Access Time
- High Board Density 52–Lead PLCC Package

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A13	Address Inputs
$\overline{W}$	Write Enable
$\overline{BWL}$	Byte Write Strobe Low
$\overline{BWH}$	Byte Write Strobe High
E	Active High Chip Enable
$\overline{E}$	Active Low Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ15	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

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TRUTH TABLE (See Notes)

$\overline{E}$	$\overline{W}$	$\overline{BWL}$	$\overline{BWH}$	$\overline{G}$	Mode	Supply Current	I/O Status
F	X	X	X	X	Deselected Cycle	I_{SB}	High–Z
T	H	X	X	H	Read Cycle	I_{CC}	High–Z
T	H	X	X	L	Read Cycle	I_{CC}	Data Out
T	L	L	L	X	Write Cycle All Bits	I_{CC}	High–Z
T	L	H	H	X	Aborted Write Cycle	I_{CC}	High–Z
T	L	L	H	X	Write Cycle Lower 8 Bits	I_{CC}	High–Z
T	L	H	L	X	Write Cycle Upper 8 Bits	I_{CC}	High–Z

NOTE: True (T) is E = 1 and $\overline{E}$ = 0. E, $\overline{E}$, and addresses satisfy the specified setup and hold times for the falling edge of LE. Data–in satisfies the specified setup and hold times for falling edge of DL.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC} and V_{CCQ}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = V_{CCQ} = 5.0$ V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to $V_{SS} = V_{SSQ} = 0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}*	4.5	5.0	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible)	V_{CCQ}	4.5 3.0	5.0 3.3	5.5 3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL}(min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 1.0	µA
Output Leakage Current ($\overline{G} = V_{IH}$)	$I_{lkg(O)}$	—	—	± 1.0	µA
AC Supply Current (I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and $V_{IH} \geq$ 3.0 V, Cycle Time ≥ t_{AVAV} min)	I_{CCA12} I_{CCA15} I_{CCA20} I_{CCA25}	— — — —	295 275 265 255	350 330 320 310	mA
Standby Current (E = V_{IL}, $\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0 V and $V_{IH} \geq$ 3.0 V, Cycle Time ≥ t_{AVAV} min)	I_{SB}	—	40	50	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ15)	C_{in}	4	6	pF
Input/Output Capacitance (DQ0 – DQ15)	C_{out}	8	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 3.3 V or 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

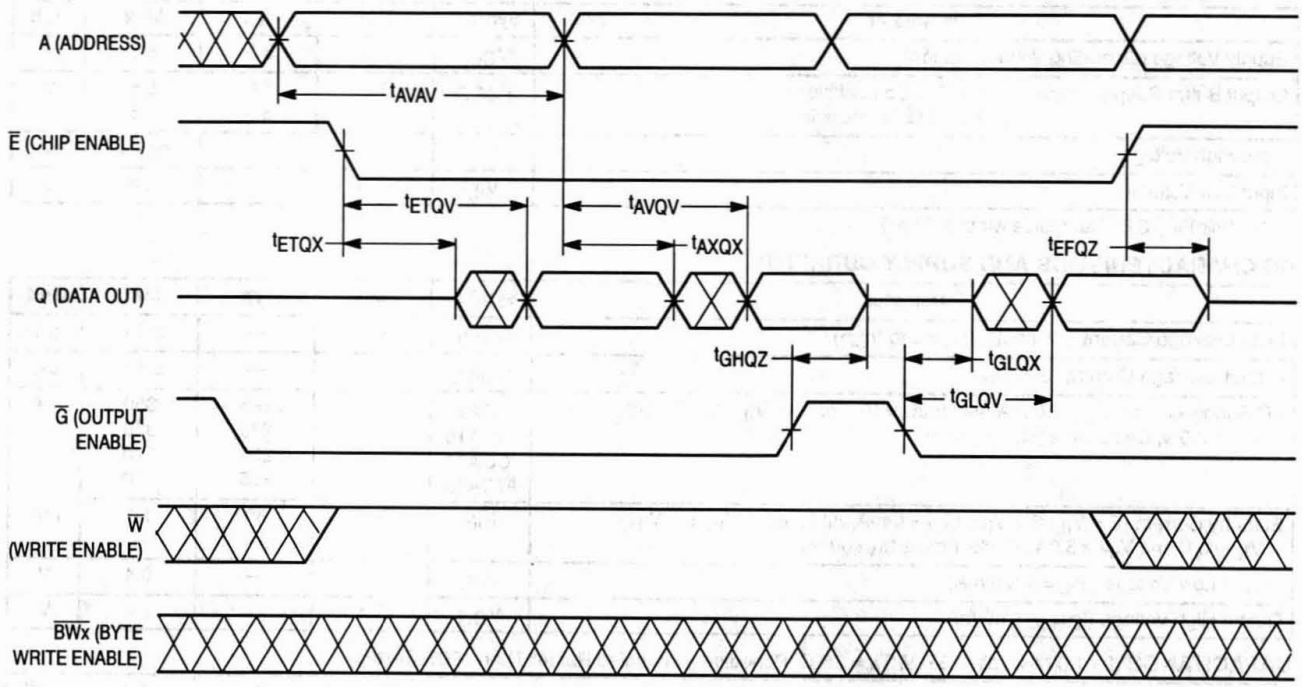
Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1a Unless Otherwise Noted

READ CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM62996–12		MCM62996–15		MCM62996–20		MCM62996–25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Times	t_{AVAV}	15	—	15	—	20	—	25	—	ns	4
Access Times:										ns	5
Address Valid to Output Valid	t_{AVQV}	—	12	—	15	—	20	—	25		
E, $\overline{E}$ "True" to Output Valid	t_{ETQV}	—	12	—	15	—	20	—	25		
Output Enable Low to Output Valid	t_{GLQV}	—	5	—	6	—	8	—	10		
Output Hold from Address Change	t_{AXQX}	4	—	4	—	4	—	4	—	ns	
Output Buffer Control:										ns	6
E, $\overline{E}$ "True" to Output Active	t_{ETQX}	2	—	2	—	2	—	2	—		
$\overline{G}$ Low to Output Active	t_{GLQX}	2	—	2	—	0	—	2	—		
E, $\overline{E}$ "False" to Output High–Z	t_{EFQZ}	2	9	2	9	0	9	2	10		
$\overline{G}$ High to Output High–Z	t_{GHQZ}	2	5	2	6	0	8	2	10		
Power Up Time	t_{ETICCH}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. Write Enable is equal to V_{IH} for all read cycles.
2. ET is defined by $\overline{E}$ going low coincident with or after E goes high, or E going high coincident with or after $\overline{E}$ goes low.
3. EF is defined by $\overline{E}$ going high or E going low.
4. All read cycle timing is referenced from the last valid address to the first transitioning address.
5. Addresses valid prior to or coincident with $\overline{E}$ going low or E going high.
6. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1b. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EFQZ} is less than t_{ETQX} and t_{GHQZ} is less than t_{GLQX} for a given device.

READ CYCLE



WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM62996–12		MCM62996–15		MCM62996–20		MCM62996–25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Times	t_{AVAV}	15	—	15	—	20	—	25	—	ns	5
Setup Times:										ns	
Address Valid to End of Write	t_{AVWH}	10		13		15		20			
Address Valid to End of Write	t_{AVEF}	10	—	13	—	15	—	20	—		
Address Valid to $\overline{W}$ Low	t_{AVWL}	0	—	0	—	0	—	0	—		
Address Valid to E, $\overline{E}$ "True"	t_{AVET}	0	—	0	—	0	—	0	—		
Data Valid to $\overline{W}$ High	t_{DVWH}	5	—	6	—	8	—	10	—		
Data Valid to E or $\overline{E}$ "False"	t_{DVEF}	6	—	6	—	8	—	10	—		
Byte Write Low to $\overline{W}$ High	t_{BWxLWH}	6	—	6	—	8	—	10	—		
Byte Write High to $\overline{W}$ Low (Abort)	t_{BWxHWL}	0	—	0	—	0	—	0	—		
Byte Write Low to E, $\overline{E}$ "False"	t_{BWxLEF}	6	—	6	—	8	—	10	—		
Hold Times:										ns	
$\overline{W}$ High to Address Invalid	t_{WHAX}	0	—	0	—	0	—	0	—		
E, $\overline{E}$ "False" to Address Invalid	t_{EFAX}	0	—	0	—	0	—	0	—		
$\overline{W}$ High to Data Invalid	t_{WHDX}	0	—	0	—	0	—	0	—		
E, $\overline{E}$ "False" to Data Invalid	t_{EFDX}	0	—	0	—	0	—	0	—		
$\overline{W}$ High to Byte Write Invalid	t_{WHBWxX}	2	—	2	—	2	—	2	—		
E, $\overline{E}$ "False" to Byte Write Invalid	t_{EFBWxX}	2	—	2	—	2	—	2	—		
Write Pulse Width:										ns	
Write Pulse Width	t_{WLWH}	12	—	13	—	15	—	20	—		
Write Pulse Width	t_{WLEF}	12	—	13	—	15	—	20	—		6
Enable to End of Write	t_{ETWH}	12	—	13	—	15	—	20	—		7
Enable to End of Write	t_{ETEF}	12	—	13	—	15	—	20	—		6, 7
Output Buffer Control:										ns	
$\overline{W}$ High to Output Valid	t_{WHQV}	12	—	18	—	20	—	25	—		
$\overline{W}$ High to Output Active	t_{WHQX}	5	—	5	—	5	—	5	—		8
$\overline{W}$ Low to Output High–Z	t_{WLQZ}	—	9	—	9	—	9	—	10		8, 9

NOTES:
1. A write occurs during the overlap of ET, $\overline{W}$ low and $\overline{BWx}$ low. An aborted write occurs when $\overline{BWx}$ remains at V_{IH} while $\overline{W}$ is low.
2. Write must be equal to V_{IH} for all address transitions.
3. ET is defined by $\overline{E}$ going low coincident with or after E goes high, or E going high coincident with or after $\overline{E}$ goes low.
4. EF is defined by $\overline{E}$ going high or E going low.
5. All write cycle timing is referenced from the last valid address to the first transitioning address.
6. If E or $\overline{E}$ goes false coincident with or before $\overline{W}$ goes high the output will remain in a high–impedance state.
7. If E and $\overline{E}$ go true coincident with or after $\overline{W}$ goes low the output will remain in a high–impedance state.
8. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1b. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{WLQZ} is less than t_{WHQX} for a given device.
9. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.

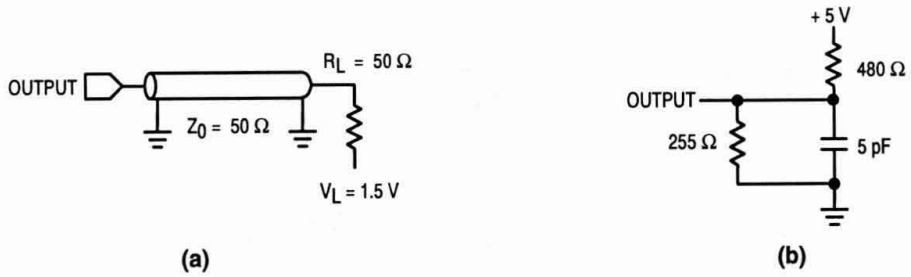
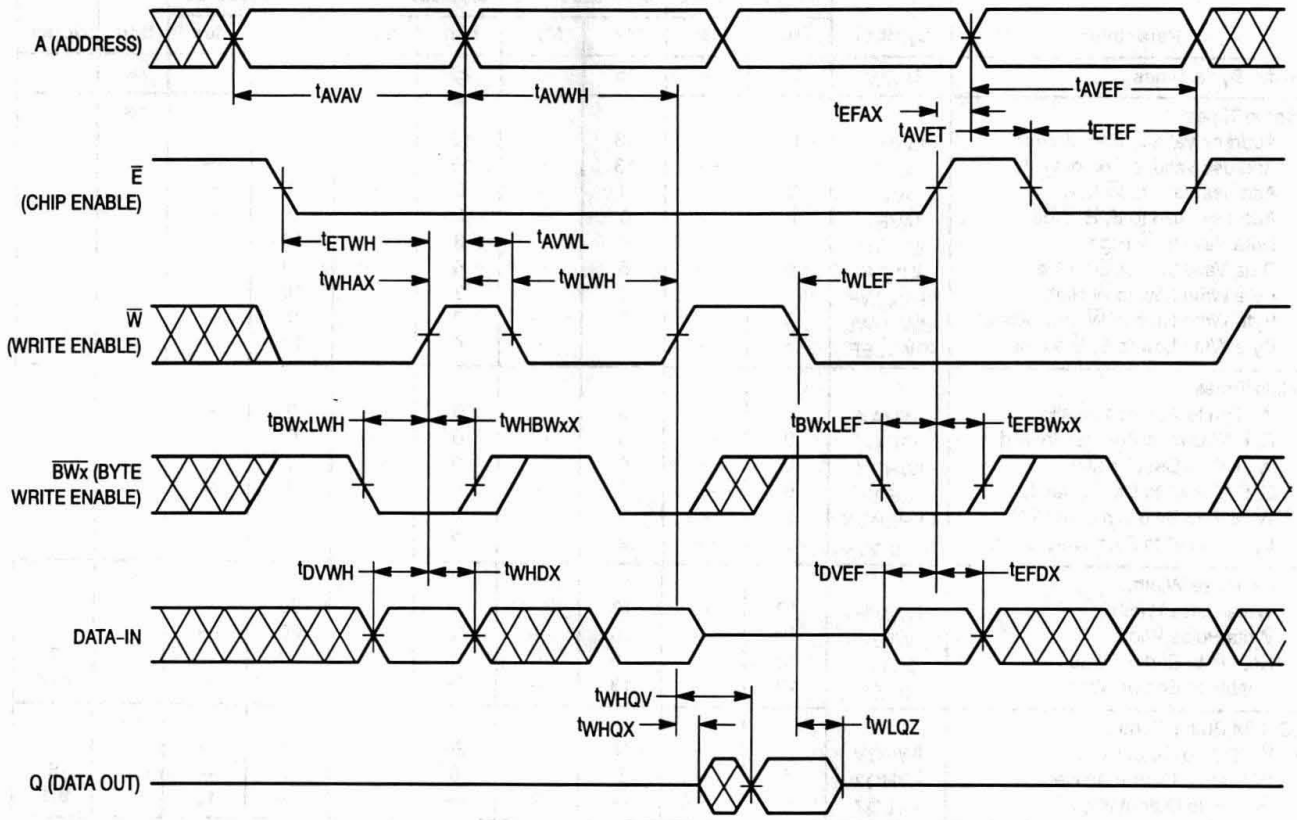


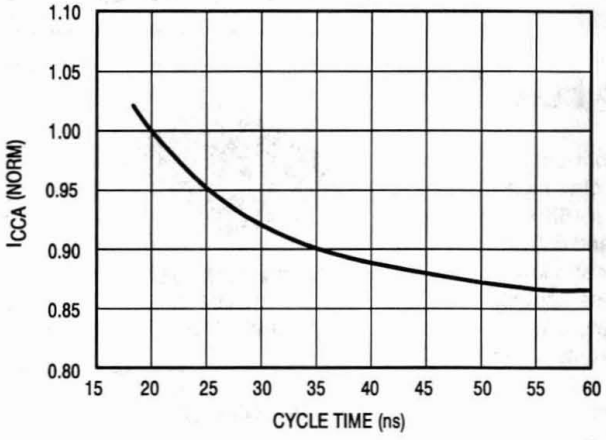
Figure 1. AC Test Loads

WRITE CYCLE

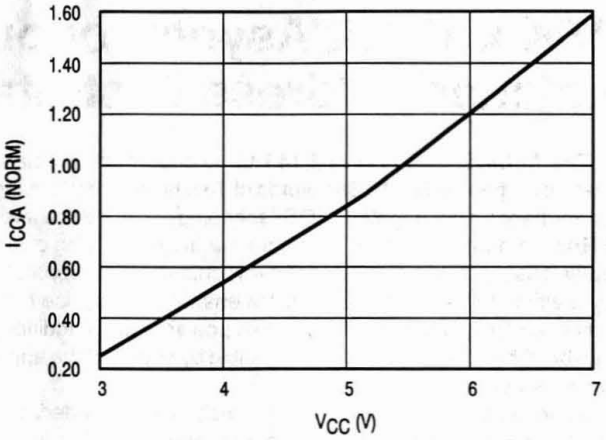

A (ADDRESS)
tAVAV
tAVWH
tAVEF
tEFAX
tAVET
tETEF
E
(CHIP ENABLE)
tETWH
tAVWL
tWHAX
tWLWH
tWLEF
W
(WRITE ENABLE)
tBWxLWH
tWHBWxX
tBWxLEF
tEFBWxX
BWx (BYTE
WRITE ENABLE)
tDVWH
tWHDX
tDVEF
tEFDX
DATA-IN
tWHQV
tWHQX
tWLQZ
Q (DATA OUT)

DERATING CURVES

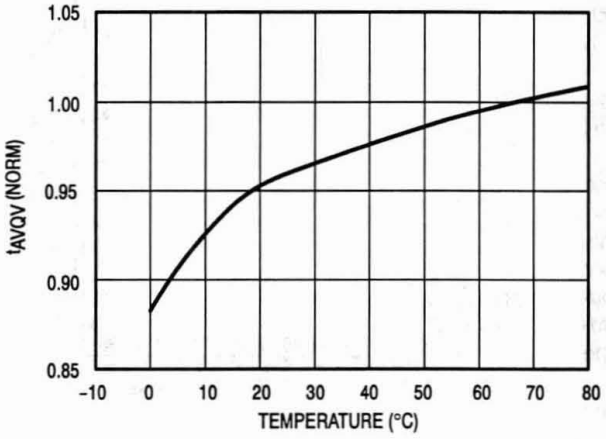
(Derating Curves Are Based On Component Typical Values)



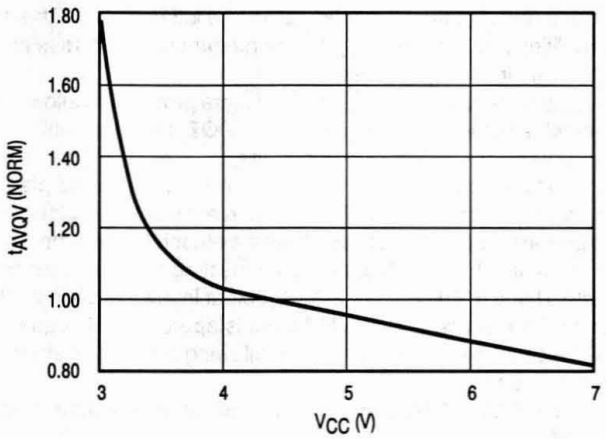
I_{CCA} vs Cycle Time



I_{CCA} vs V_{CC}



AVQV vs Temperature



AVQV vs V_{CC}

ORDERING INFORMATION

(Order by Full Part Number)

MCM	62996	FN	XX
Motorola Memory Prefix	Part Number	Package (FN = PLCC)	Speed (12 = 12 ns, 15 = 15 ns, 20 = 20 ns, 25 = 25 ns)

Full Part Numbers — MCM62996FN12 MCM62996FN15 MCM62996FN20 MCM62996FN25

MCM62995A

16K x 16 Bit Asynchronous/ Latched Address Fast Static RAM

2

The MCM62995A is a 262,144 bit latched address static random access memory organized as 16,384 words of 16 bits, fabricated using Motorola's high–performance silicon–gate CMOS technology. The device integrates a 16K x 16 SRAM core with advanced peripheral circuitry consisting of address and data input latches, active high and active low chip enables, separate upper and lower byte write strobes, and a fast output enable. This device has increased output drive capability supported by multiple power pins. In addition, the output levels can be either 3.3 V or 5 V TTL compatible by choice of the appropriate output bus power supply.

Address, data in, and chip enable latches are provided. When latch enable (LE for address and chip enables and DL for data in) is high, the address, data in, and chip enable latches are in the transparent state. If latch enable (LE, DL) is tied high, the device can be used as an asynchronous SRAM. When latch enable (LE, DL) is low, the address, data in and chip enable latches are in the latched state. This input latch simplifies read and write cycles by guaranteeing address and data–in hold time in a simple fashion.

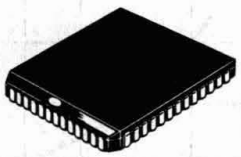
Dual write strobes ($\overline{BWL}$ and $\overline{BWH}$) are provided to allow individually writeable bytes. $\overline{BWL}$ controls DQ0 – DQ7 (the lower bits), while $\overline{BWH}$ controls DQ8 – DQ15 (the upper bits).

Additional power supply pins have been utilized and placed on the package for maximum performance. In addition, the output buffer power pins are electrically isolated from the other two and supply power only to the output buffers. This allows connecting the output buffers to 3.3 V instead of 5.0 V if desired. If 3.3 V output levels are chosen, the output buffer impedance in the "high" state is approximately equal to the impedance in the "low" state thereby allowing simplified transmission line terminations.

The MCM62995A is available in a 52 pin plastic leaded chip carrier (PLCC).

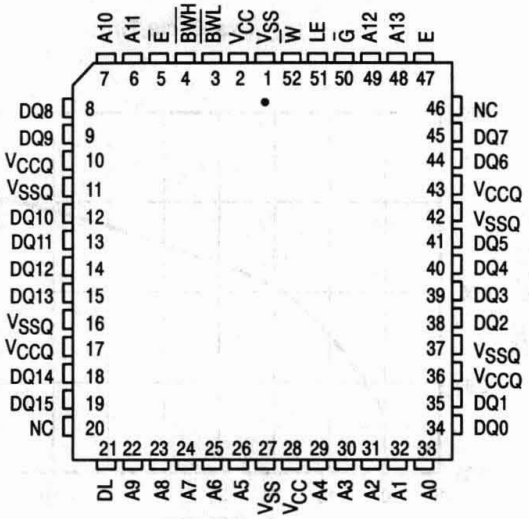
This device is ideally suited for systems which require wide data bus widths, cache memory and tag RAMs. See Figure 2 for applications information.

- Single 5 V ± 10% Power Supply
- Choice of 5 V or 3.3 V ± 10% Power Supplies for Output Buffers
- Fast Access Times: 12/15/20/25 ns Max
- Byte Writeable via Dual Write Strobes with Abort Write Capability
- Separate Data Input Latch for Simplified Write Cycles
- Address and Chip Enable Input Latches
- Common Data Inputs and Data Outputs
- Output Enable Controlled Three–State Outputs
- High Output Drive Capability: 85 pF/Output at Rated Access Time
- High Board Density 52 Lead PLCC Package



FN PACKAGE
PLASTIC
CASE 778–02

PIN ASSIGNMENT

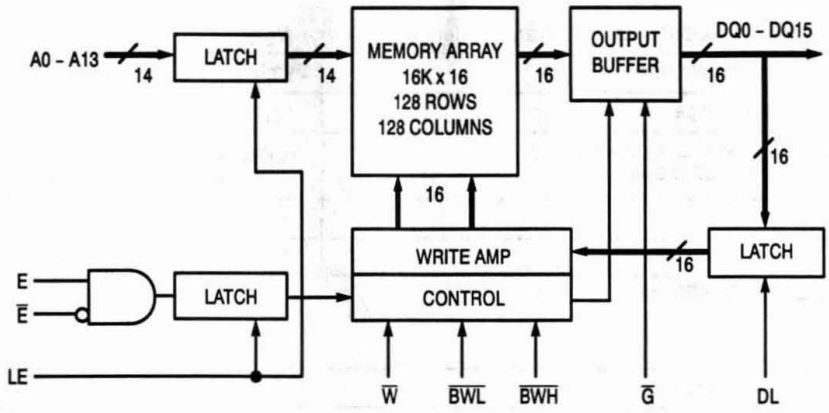


PIN NAMES	
A0 – A13	Address Inputs
LE	Latch Enable
DL	Data Latch Enable
$\overline{W}$	Write Enable
$\overline{BWL}$	Byte Write Strobe Low
$\overline{BWH}$	Byte Write Strobe High
E	Active High Chip Enable
$\overline{E}$	Active Low Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ15	Data Input/Output
V_{CC}	+5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SSQ}	Output Buffer Ground
V_{SS}	Ground
NC	No Connect

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

REV 2
5/95

BLOCK DIAGRAM



TRUTH TABLE

Es	$\overline{W}$	$\overline{BWL}$	$\overline{BWH}$	LE	DL	$\overline{G}$	Mode	Supply Current	I/O Status
F	X	X	X	X	X	X	Deselected Cycle	I_{SB}	High–Z
T	H	X	X	H	X	H	Read Cycle	I_{CC}	High–Z
T	H	X	X	H	X	L	Read Cycle	I_{CC}	Data Out
T	H	X	X	L	X	L	Latched Read Cycle	I_{CC}	Data Out
T	L	L	L	H	H	X	Write Cycle All Bits	I_{CC}	High–Z
T	L	H	H	X	X	X	Aborted Write Cycle	I_{CC}	High–Z
T	L	L	H	H	H	X	Write Cycle Lower 8 Bits	I_{CC}	High–Z
T	L	H	L	H	L	X	Write Cycle Upper 8 Bits Latched Data–In	I_{CC}	High–Z
T	L	L	L	L	L	X	Latched Write Cycle Latched Data–In	I_{CC}	High–Z

NOTE: True (T) is E = 1 and $\overline{E}$ = 0. E, $\overline{E}$, and Addresses satisfy the specified setup and hold times for the falling edge of LE. Data–in satisfies the specified setup and hold times for falling edge of DL.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = V_{SSQ} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC} and V_{CCQ}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = V_{CCQ} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = V_{SSQ} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible)	V_{CCQ}	4.5 3.0	5.0 3.3	5.5 3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	—	± 1.0	µA
AC Supply Current (I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{AVAV} min)	I_{CCA12} I_{CCA15} I_{CCA20} I_{CCA25}	— — — —	295 275 265 255	350 330 320 310	mA
Standby Current (E = V_{IL}, $\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{AVAV} min)	I_{SB}	—	40	50	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ15)	C_{in}	4	6	pF
Input/Output Capacitance (DQ0 – DQ15)	C_{out}	8	10	pF

AC TEST LOADS

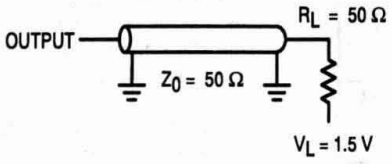


Figure 1A

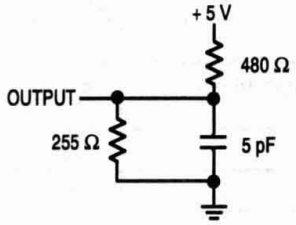


Figure 1B

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, V_{CCQ} = 3.3 V or 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

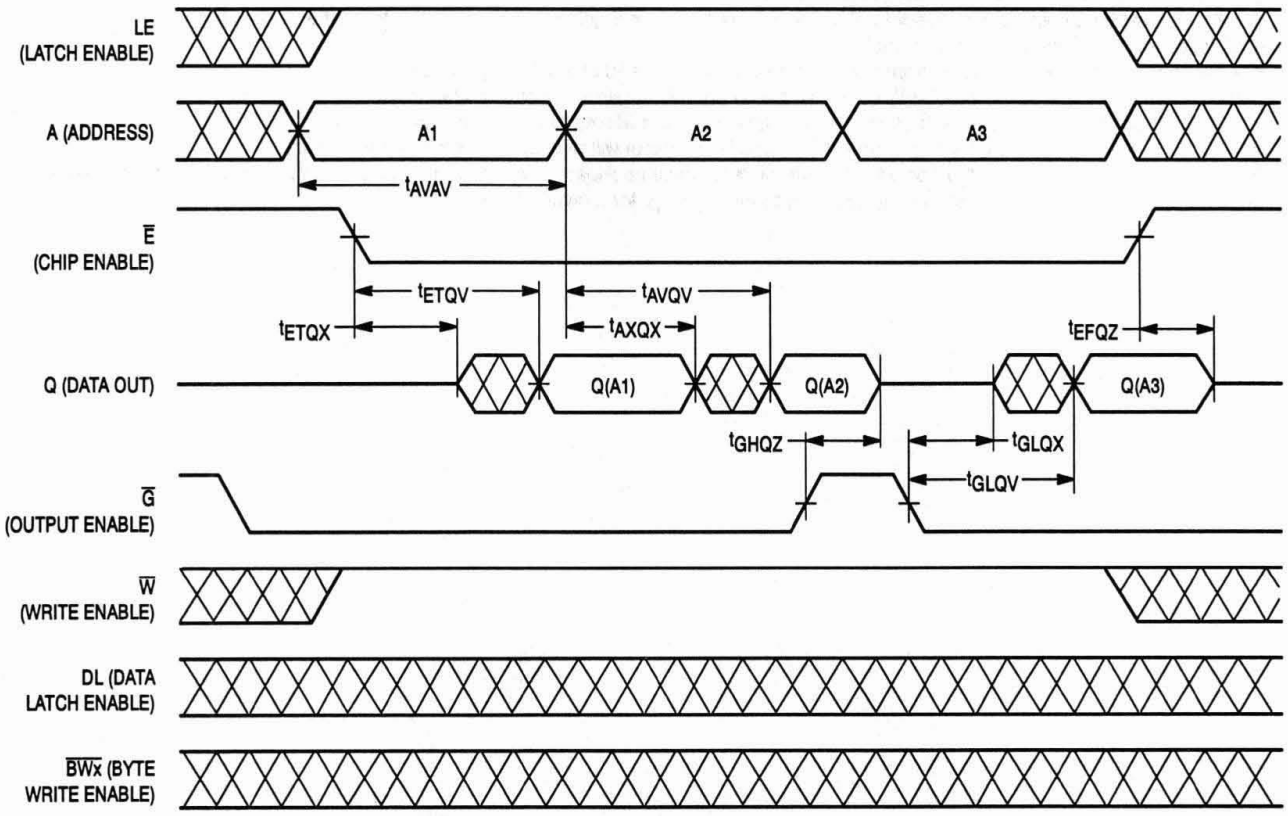
Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1 Unless Otherwise Noted

ASYNCHRONOUS READ CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	62995A–12		62995A–15		62995A–20		62995A–25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Times	t_{AVAV}	15	—	15	—	20	—	25	—	ns	5
Access Times:										ns	6
Address Valid to Output Valid	t_{AVQV}	—	12	—	15	—	20	—	25		
E, $\overline{E}$ "True" to Output Valid	t_{ETQV}	—	12	—	15	—	20	—	25		
Output Enable Low to Output Valid	t_{GLQV}	—	5	—	6	—	8	—	10		
Output Hold from Address Change	t_{AXQX}	4	—	4	—	4	—	4	—	ns	
Output Buffer Control:										ns	7
E, $\overline{E}$ "True" to Output Active	t_{ETQX}	2	—	2	—	2	—	2	—		
$\overline{G}$ Low to Output Active	t_{GLQX}	2	—	2	—	2	—	2	—		
E, $\overline{E}$ "False" to Output High–Z	t_{EFQZ}	2	9	2	9	2	9	2	10		
$\overline{G}$ High to Output High–Z	t_{GHQZ}	2	5	2	6	2	8	2	10		
Power Up Time	t_{ETICCA}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. LE and DL are equal to V_{IH} for all asynchronous cycles.
2. Write Enable is equal to V_{IH} for all read cycles.
3. ET is defined by $\overline{E}$ going low coincident with or after E goes high, or E going high coincident with or after $\overline{E}$ goes low.
4. EF is defined by $\overline{E}$ going high or E going low.
5. All read cycle timing is referenced from the last valid address to the first transitioning address.
6. Addresses valid prior to or coincident with $\overline{E}$ going low or E going high.
7. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EFQZ} is less than t_{ETQX} and t_{GHQZ} is less than t_{GLQX} for a given device.

ASYNCHRONOUS READ CYCLES



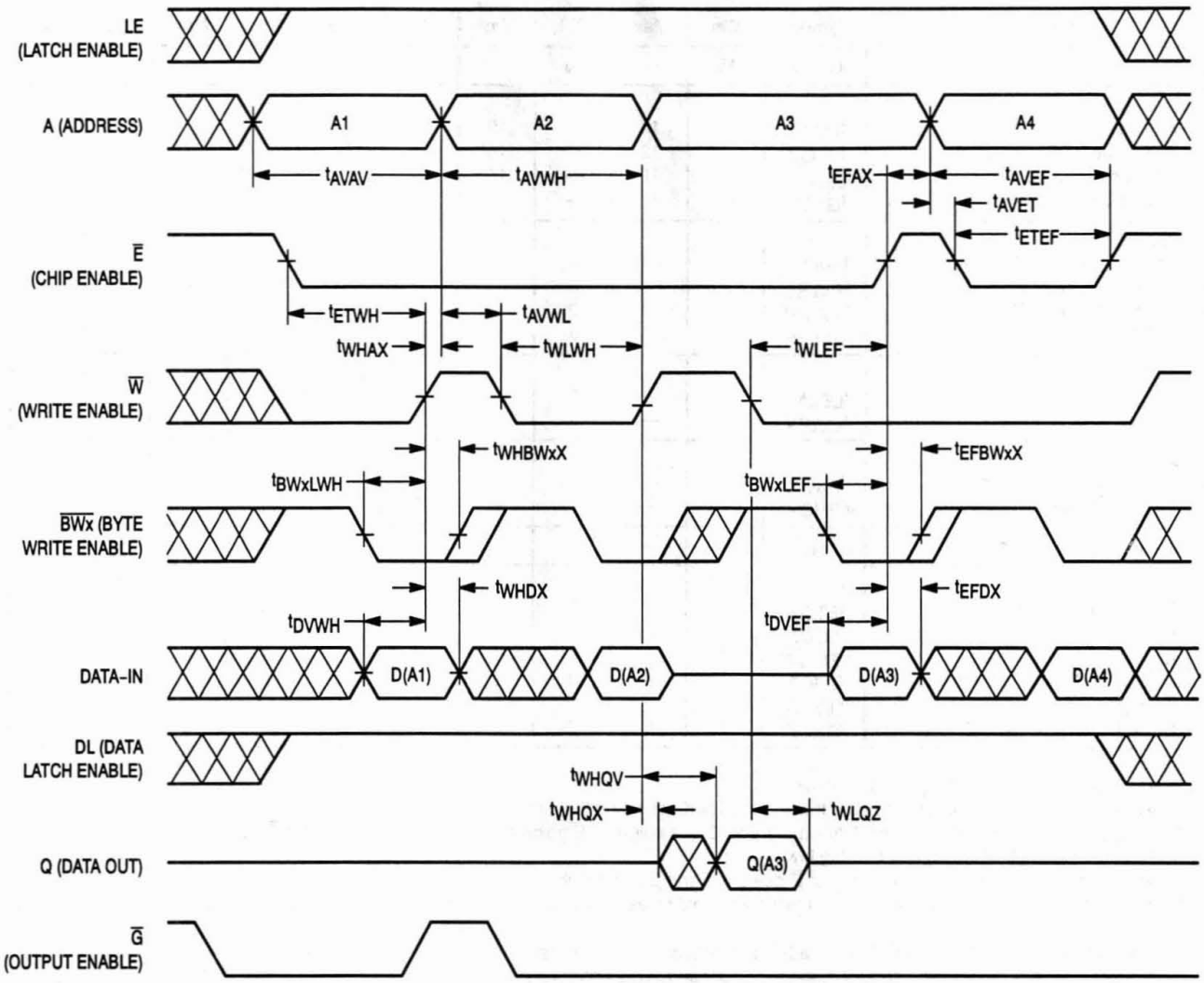
ASYNCHRONOUS WRITE CYCLE TIMING (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol	62995A–12		62995A–15		62995A–20		62995A–25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Times	t_{AVAV}	15	—	15	—	20	—	25	—	ns	6
Setup Times:										ns	
Address Valid to End of Write	t_{AVWH}	10	—	13	—	15	—	20	—		
Address Valid to E, $\overline{E}$ "False"	t_{AVEF}	10	—	13	—	15	—	20	—		
Address Valid to $\overline{W}$ Low	t_{AVWL}	0	—	0	—	0	—	0	—		
Address Valid to E, $\overline{E}$ "True"	t_{AVET}	0	—	0	—	0	—	0	—		
Data Valid to $\overline{W}$ High	t_{DVWH}	5	—	6	—	8	—	10	—		
Data Valid to E or $\overline{E}$ "False"	t_{DVEF}	5	—	6	—	8	—	10	—		
Byte Write Low to $\overline{W}$ High	t_{BWxLWH}	4	—	6	—	8	—	10	—		
Byte Write High to $\overline{W}$ Low (Abort)	t_{BWxHWL}	0	—	0	—	0	—	0	—		2
Byte Write Low to E, $\overline{E}$ "False"	t_{BWxLEF}	4	—	6	—	8	—	10	—		
Hold Times:										ns	
$\overline{W}$ High to Address Invalid	t_{WHAX}	0	—	0	—	0	—	0	—		
E, $\overline{E}$ "False" to Address Invalid	t_{EFAX}	0	—	0	—	0	—	0	—		
$\overline{W}$ High to Data Invalid	t_{WHDX}	0	—	0	—	0	—	0	—		
E, $\overline{E}$ "False" to Data Invalid	t_{EFDX}	0	—	0	—	0	—	0	—		
$\overline{W}$ High to Byte Write Invalid	t_{WHBWxX}	2	—	2	—	2	—	2	—		
E, $\overline{E}$ "False" to Byte Write Invalid	t_{EFBWxX}	2	—	2	—	2	—	2	—		
Write Pulse Width:										ns	
Write Pulse Width	t_{WLWH}	12	—	13	—	15	—	20	—		
Write Pulse Width	t_{WLEF}	12	—	13	—	15	—	20	—		9
Enable to End of Write	t_{ETWH}	12	—	13	—	15	—	20	—		8
Enable to End of Write	t_{ETEF}	12	—	13	—	15	—	20	—		8, 9
Output Buffer Control:										ns	
$\overline{W}$ High to Output Valid	t_{WHQV}	12	—	18	—	20	—	25	—		
$\overline{W}$ High to Output Active	t_{WHQX}	5	—	5	—	5	—	5	—		10
$\overline{W}$ High to Output High–Z	t_{WLQZ}	0	9	0	9	0	9	0	10		7, 10

NOTES:

1. LE and DL are equal to V_{IH} for all asynchronous cycles.
2. A write occurs during the overlap of ET, $\overline{W}$ low and $\overline{BWx}$ low. An aborted write occurs when $\overline{BWx}$ remains at V_{IH} while $\overline{W}$ is low.
3. Write must be equal to V_{IH} for all address transitions.
4. ET is defined by $\overline{E}$ going low coincident with or after E goes high, or E going high coincident with or after $\overline{E}$ goes low.
5. EF is defined by $\overline{E}$ going high or E going low.
6. All write cycle timing is referenced from the last valid address to the first transitioning address.
7. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
8. If E and $\overline{E}$ goes true coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.
9. If E or $\overline{E}$ goes false coincident with or before $\overline{W}$ goes high the output will remain in a high impedance state.
10. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{WLQZ} is less than t_{WHQX} for a given device.

ASYCHRONOUS WRITE CYCLE

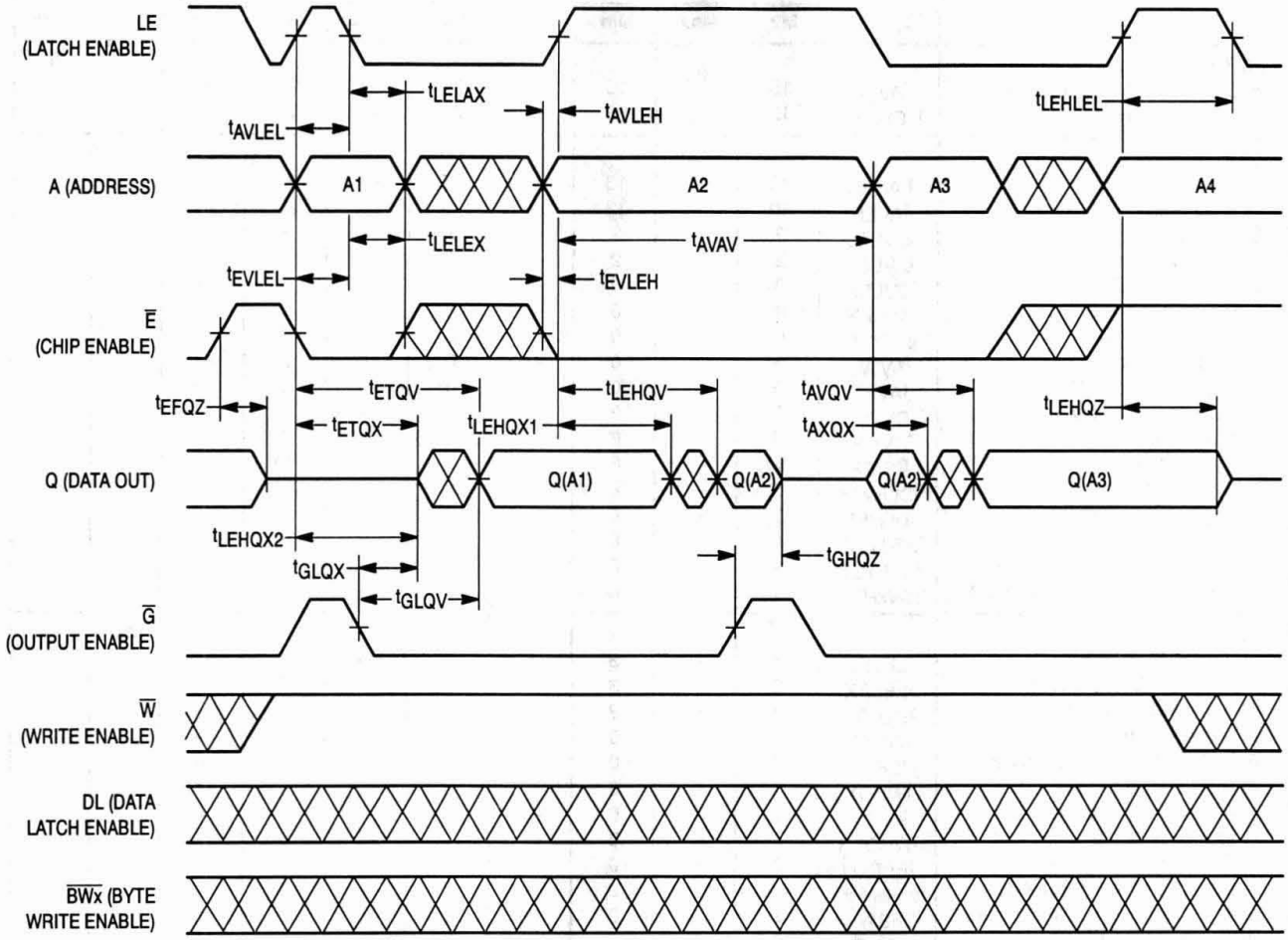


LATCHED READ CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	62995A–12		62995A–15		62995A–20		62995A–25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Times	t_{AVAV}	15	—	15	—	20	—	25	—	ns	5
Access Times:										ns	
Address Valid to Output Valid	t_{AVQV}	—	12	—	15	—	20	—	25		
E, $\overline{E}$ "True" to Output Valid	t_{ETQV}	—	12	—	15	—	20	—	25		5
LE High to Output Valid	t_{LEHQV}	—	12	—	15	—	20	—	25		6
Output Enable Low to Output Valid	t_{GLQV}	—	5	—	6	—	8	—	10		
Setup Times:										ns	
Address Valid to LE Low	t_{AVLEL}	2	—	2	—	2	—	2	—		6
E, $\overline{E}$ "Valid" to LE Low	t_{EVLEL}	2	—	2	—	2	—	2	—		6
Address Valid to LE High	t_{AVLEH}	0	—	0	—	0	—	0	—		
E, $\overline{E}$ "Valid" to LE High	t_{EVLEH}	0	—	0	—	0	—	0	—		
Hold Times:										ns	6
LE Low to Address Invalid	t_{LELAX}	3	—	3	—	3	—	3	—		
LE Low to E, $\overline{E}$ "Invalid"	t_{LELEX}	3	—	3	—	3	—	3	—		
Output Hold:										ns	
Address Invalid to Output Invalid	t_{AXQX}	4	—	4	—	4	—	4	—		
LE High to Output Invalid	t_{LEHQX1}	4	—	4	—	4	—	4	—		
Latch Enable High Pulse Width	t_{LEHLEL}	5	—	5	—	5	—	5	—	ns	
Output Buffer Control:										ns	7
E, $\overline{E}$ "True" to Output Active	t_{ETQX}	2	—	2	—	2	—	2	—		
$\overline{G}$ Low to Output Active	t_{GLQX}	2	—	2	—	2	—	2	—		
LE High to Output Active	t_{LEHQX2}	2	—	2	—	2	—	2	—		
E, $\overline{E}$ "False" to Output High–Z	t_{EFQZ}	2	9	2	9	2	10	2	10		
LE High to Output High–Z	t_{LEHQZ}	2	9	2	9	2	10	2	10		
$\overline{G}$ High to Output High–Z	t_{GHQZ}	2	5	2	6	2	8	2	10		

NOTES:
1. Write Enable is equal to V_{IH} for all read cycles.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. ET is defined by $\overline{E}$ going low coincident with or after E goes high, or E going high coincident with or after $\overline{E}$ goes low.
4. EF is defined by $\overline{E}$ going high or E going low.
5. Addresses valid prior to or coincident with $\overline{E}$ going low and E going high
6. All latched inputs must meet the specified setup and hold times with stable logic levels for ALL falling edges of latch enable (LE) and data latch enable (DL).
7. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EFQZ} is less than t_{ETQX} and t_{LEHQZ} is less than t_{LEHQX2} and t_{GHQZ} is less than t_{GLQX} for a given device.

LATCHED READ CYCLES



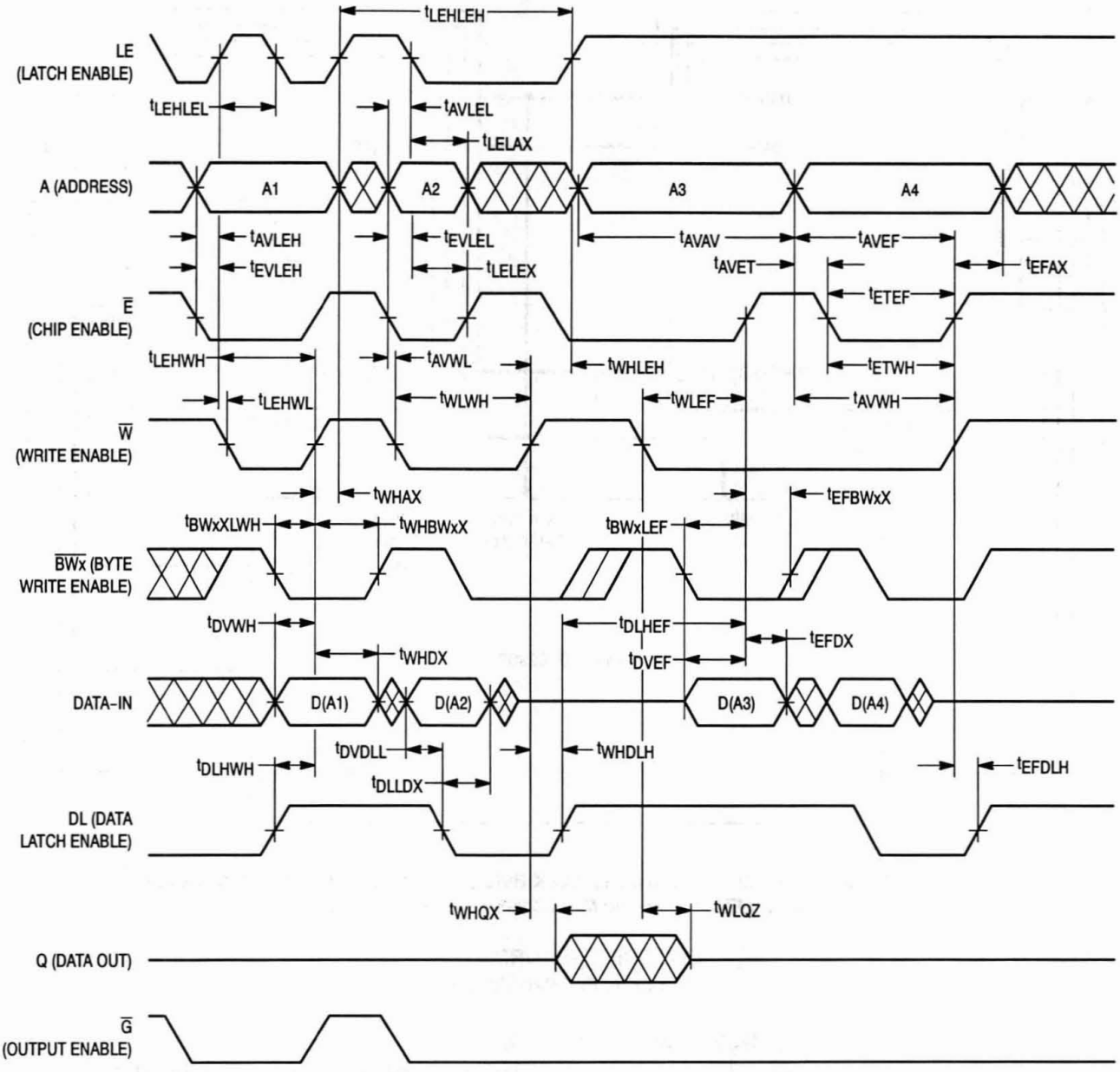
LATCHED WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	62995A–12		62995A–15		62995A–20		62995A–25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Times:										ns	5
Address Valid to Address Valid	t_{AVAV}	15	—	15	—	20	—	25	—		
LE High to LE High	t_{LEHLEH}	15	—	15	—	20	—	25	—		
Setup Times:										ns	
Address Valid to End of Write	t_{AVWH}	10	—	13	—	15	—	20	—		
Address Valid to End of Write	t_{AVEF}	10	—	13	—	15	—	20	—		
E, $\overline{E}$ "Valid" to LE Low	t_{EVLEL}	2	—	2	—	2	—	2	—		
Address Valid to LE Low	t_{AVLEL}	2	—	2	—	2	—	2	—		
E, $\overline{E}$ "Valid" to LE High	t_{EVLEH}	0	—	0	—	0	—	0	—		
Address Valid to LE High	t_{AVLEH}	0	—	0	—	0	—	0	—		
LE High to $\overline{W}$ Low	t_{LEHWL}	0	—	0	—	0	—	0	—		
Address Valid to $\overline{W}$ Low	t_{AVWL}	0	—	0	—	0	—	0	—		
Address Valid to E, $\overline{E}$ "True"	t_{AVET}	0	—	0	—	0	—	0	—		
Data Valid to DL Low	t_{DVDLL}	2	—	2	—	2	—	2	—		
Data Valid to $\overline{W}$ High	t_{DVWH}	5	—	6	—	8	—	10	—		
Data Valid to E or $\overline{E}$ "False"	t_{DVEF}	5	—	6	—	8	—	10	—		
DL High to $\overline{W}$ High	t_{DLHWH}	5	—	6	—	8	—	10	—		
DL High to E, $\overline{E}$ "False"	t_{DLHEF}	5	—	6	—	8	—	10	—		
Byte Write Low to $\overline{W}$ High	t_{BWxLWH}	4	—	6	—	8	—	10	—		
Byte Write Low to E, $\overline{E}$ "False"	t_{BWxLEF}	4	—	6	—	8	—	10	—		
Byte Write High to $\overline{W}$ Low (Abort)	t_{BWxHWL}	0	—	0	—	0	—	0	—		
Hold Times:										ns	
LE Low to E, $\overline{E}$ "Invalid"	t_{LELEX}	3	—	3	—	3	—	3	—		5
LE Low to Address Invalid	t_{LELAX}	3	—	3	—	3	—	3	—		5
DL Low to Data Invalid	t_{DLLDX}	2	—	2	—	2	—	2	—		
$\overline{W}$ High to Address Invalid	t_{WHAX}	0	—	0	—	0	—	0	—		
E, $\overline{E}$ "False" to Address Invalid	t_{EFAX}	0	—	0	—	0	—	0	—		
$\overline{W}$ High to Data Invalid	t_{WHDX}	0	—	0	—	0	—	0	—		
E, $\overline{E}$ "False" to Data Invalid	t_{EFDX}	0	—	0	—	0	—	0	—		
$\overline{W}$ High to DL High	t_{WHDLH}	0	—	0	—	0	—	0	—		
E, $\overline{E}$ "False" to DL High	t_{EFDLH}	0	—	0	—	0	—	0	—		
$\overline{W}$ High to Byte Write Invalid	t_{WHBWxX}	2	—	2	—	2	—	2	—		
E, $\overline{E}$ "False" to Byte Write Invalid	t_{EFBWxX}	2	—	2	—	2	—	2	—		
$\overline{W}$ High to LE High	t_{WHLEH}	0	—	0	—	0	—	0	—		
Write Pulse Width:										ns	
LE High to $\overline{W}$ High	t_{LEHWH}	12	—	13	—	15	—	20	—		6
Write Pulse Width	t_{WLWH}	12	—	13	—	15	—	20	—		
Write Pulse Width	t_{WLEF}	12	—	13	—	15	—	20	—		9
Enable to End of Write	t_{ETWH}	12	—	13	—	15	—	20	—		8
Enable to End of Write	t_{ETEF}	12	—	13	—	15	—	20	—		8, 9
Latch Enable High Pulse Width	t_{LEHLEL}	5	—	5	—	5	—	5	—	ns	
Output Buffer Control:										ns	
$\overline{W}$ High to Output Valid	t_{WHQV}	12	—	15	—	20	—	25	—		
$\overline{W}$ High to Output Active	t_{WHQX}	5	—	5	—	5	—	5	—		10
$\overline{W}$ Low to Output High–Z	t_{WLQZ}	0	9	0	9	0	9	0	10		7, 10

NOTES:

1. A write occurs during the overlap of ET, $\overline{W}$ low and $\overline{BWx}$ low. An aborted write occurs when $\overline{BWx}$ remians at V_{IH} while $\overline{W}$ is low.
2. Write must be equal to V_{IH} for all address transitions.
3. ET is defined by $\overline{E}$ going low coincident with or after E goes high, or E going high coincident with or after $\overline{E}$ goes low.
4. EF is defined by $\overline{E}$ going high or E going low.
5. All write cycle timing is referenced from the last valid address to the first transitioning address.
6. All latched inputs must meet the specified setup and hold times with stable logic levels for ALL falling edges of latch enable (LE) and data latch enable (DL).
7. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state
8. If E and $\overline{E}$ goes true coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.
9. If E or $\overline{E}$ goes false coincident with or before $\overline{W}$ goes high the output will remain in a high impedance state.
10. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{WLQZ} is less than t_{WHQX} for a given device.

LATCHED WRITE CYCLES



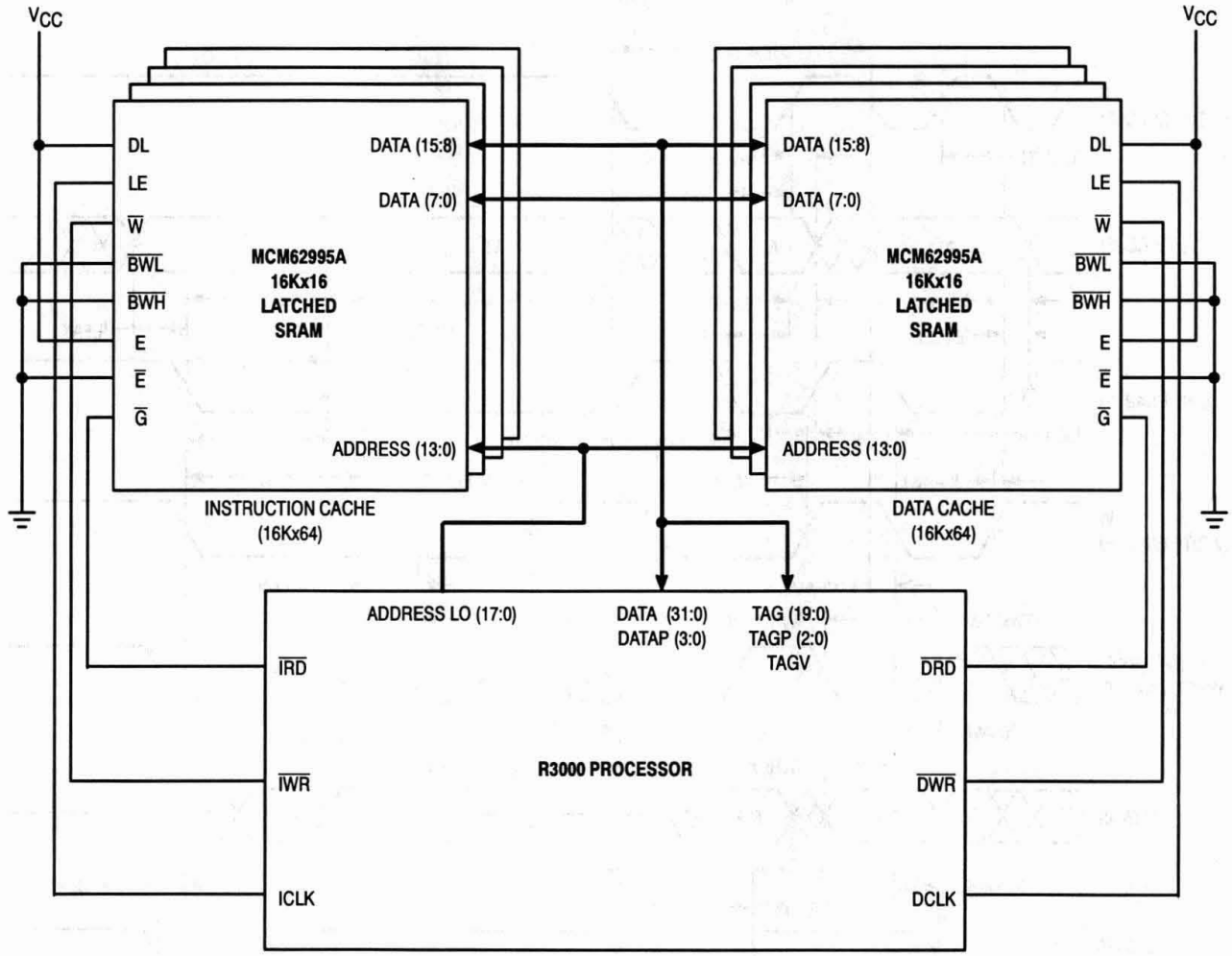


Figure 2. R3000 Application Example with 128K Byte Segregated Instruction/Data Cache Using Eight Motorola MCM62995A Latched SRAMs

ORDERING INFORMATION
(Order by Full Part Number)

MCM 62995A FN XX

- MCM — Motorola Memory Prefix
- 62995A — Part Number
- FN — Package (FN = PLCC)
- XX — Speed (12 = 12 ns, 15 = 15 ns, 20 = 20 ns 25 = 25 ns)

Full Part Numbers — MCM62995AFN12 MCM62995AFN15 MCM62995AFN20 MCM62995AFN25

MCM6206BA

32K x 8 Bit Fast Static RAM

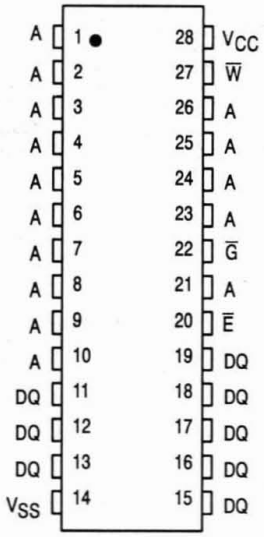
The MCM6206BA is a 262,144 bit static random access memory organized as 32,768 words of 8 bits. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

This device meets JEDEC standards for functionality and pinout, and is available in plastic small–outline J–leaded packages.

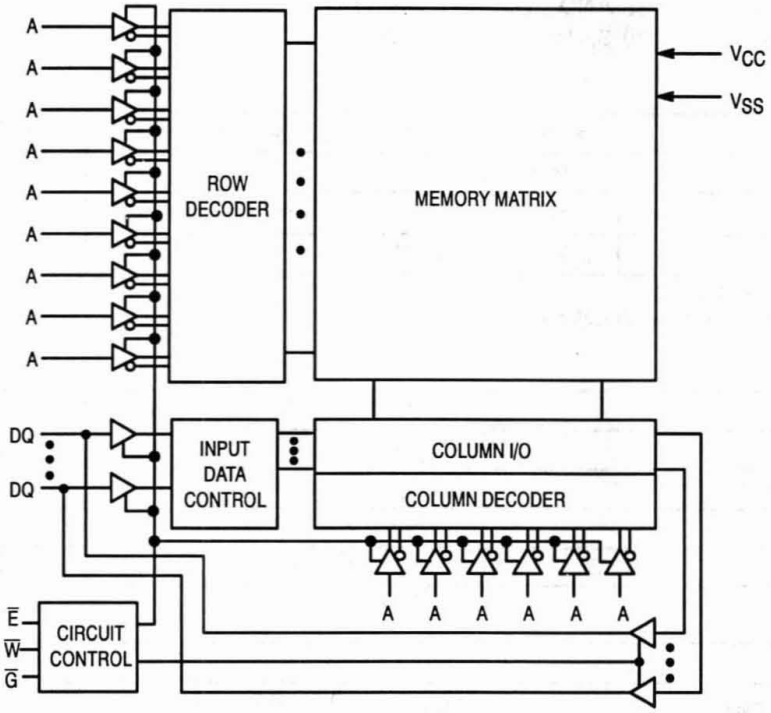
- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Times: 12/15/20/25 ns
- Equal Address and Chip Enable Access Times
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems
- Low Power Operation: 125 – 140 mA Maximum AC
- Fully TTL Compatible — Three State Output

J PACKAGE
300 MIL SOJ
CASE
810B–03

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A	Address Input
DQ	Data Input/Data Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground

REV 1
10/9/96

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	–
L	H	H	Output Disabled	I_{CCA}	High–Z	–
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High–Z	Write Cycle

2

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} For Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature—Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns)
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1	µA
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	– 12	– 15	– 20	– 25	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	140	135	130	125	mA
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = Max, f = f_{max})	I_{SB1}	40	35	35	30	mA
CMOS Standby Current (V_{CC} = Max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V)	I_{SB2}	10	10	10	10	mA

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, Periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Address Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{G}$, $\overline{W}$)	C_{in}	8	pF
I/O Capacitance	$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

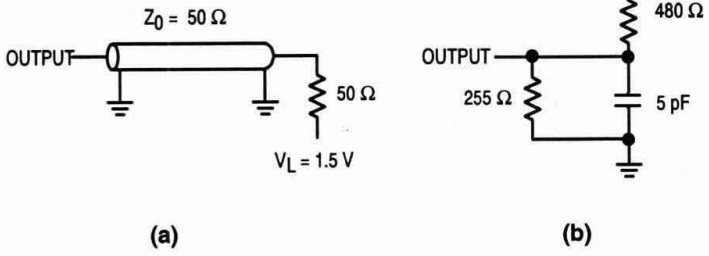
Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... Figure 1a Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter	Symbol	-12		-15		-20		-25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	12	—	15	—	20	—	25	—	ns	2
Address Access Time	t_{AVQV}	—	12	—	15	—	20	—	25	ns	
Enable Access Time	t_{ELQV}	—	12	—	15	—	20	—	25	ns	3
Output Enable Access Time	t_{GLQV}	—	6	—	8	—	10	—	12	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	3	—	ns	4,5,6
Enable Low to Output Active	t_{ELQX}	4	—	4	—	4	—	4	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	—	7	—	8	—	9	—	10	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	ns	4,5,6
Output Enable High to Output High–Z	t_{GHQZ}	—	6	—	7	—	8	—	10	ns	4,5,6
Power Up Time	t_{ELICCH}	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	—	12	—	15	—	20	—	25	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All timings are referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ} (max) is less than t_{ELQX} (min), and t_{GHQZ} (max) is less than t_{GLQX} (min), both for a given device and from device to device.
5. Transition is measured ±500 mV from steady–state voltage with load of Figure 1b.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).



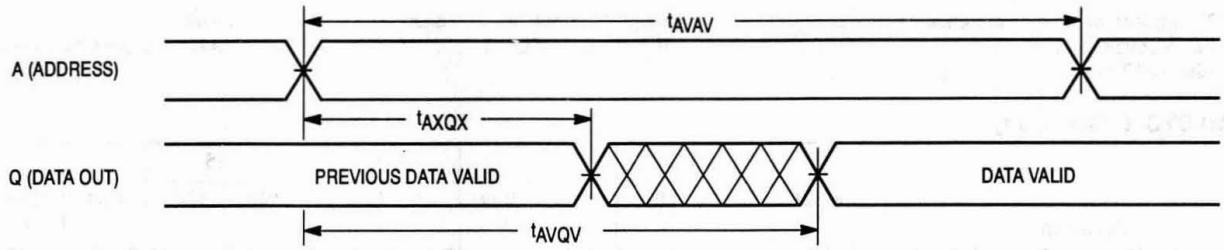
(a) (b)

TIMING LIMITS

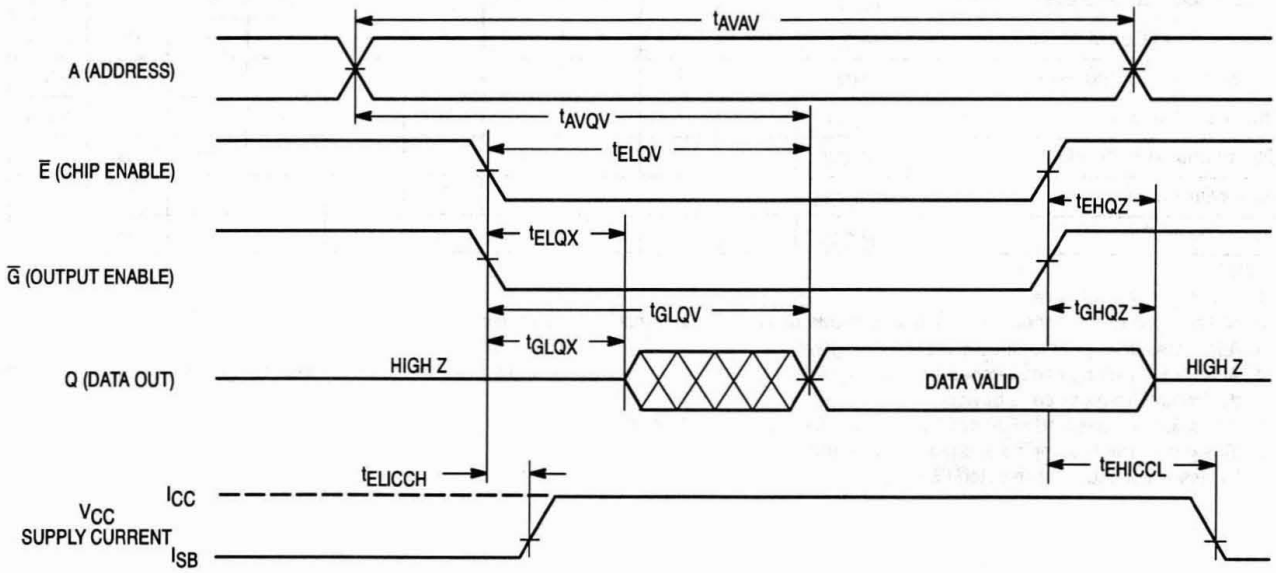
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Figure 1. AC Test Loads

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 3)

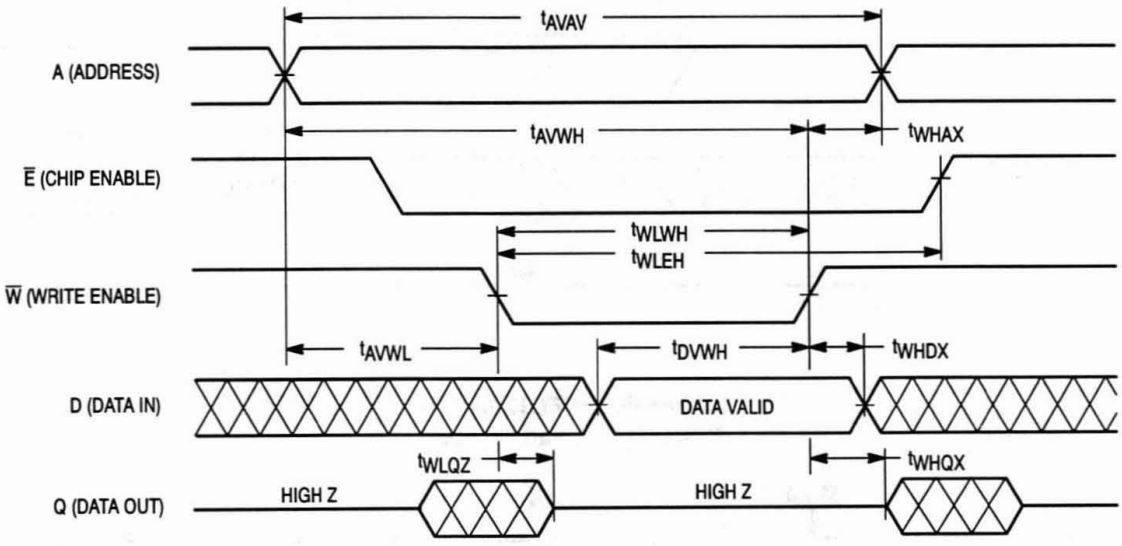


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	-12		-15		-20		-25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	12	—	15	—	20	—	25	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	10	—	12	—	15	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	10	—	12	—	15	—	20	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	10	—	10	—	12	—	15	—	ns	4
Data Valid to End of Write	t_{DVWH}	6	—	7	—	8	—	10	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	0	—	ns	
Write Low to Output High–Z	t_{WLQZ}	—	6	—	7	—	8	—	10	ns	5,6,7
Write High to Output Active	t_{WHQX}	2	—	2	—	2	—	2	—	ns	5,6,7
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
3. All timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{G} \geq V_{IH}$, the output will remain in a high impedance state.
5. At any given voltage and temperature, t_{WLQZ} (max) is less than t_{WHQX} (min), both for a given device and from device to device.
6. Transition is measured ±500 mV from steady–state voltage with load of Figure 1b.
7. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

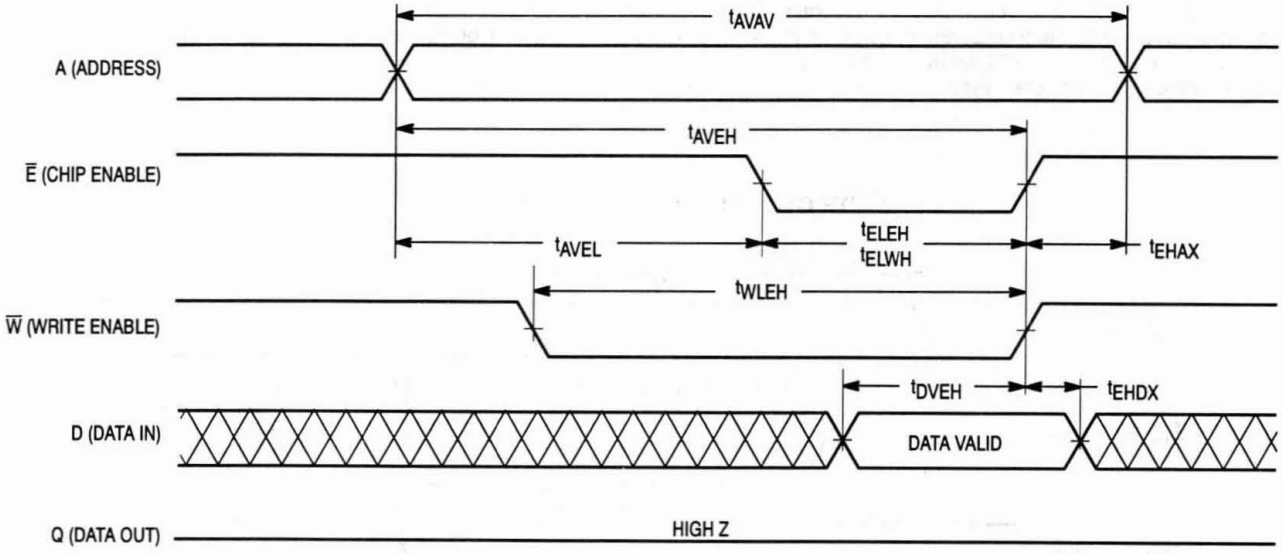


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)

Parameter	Symbol	–12		–15		–20		–25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	12	—	15	—	20	—	25	—	ns	
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	10	—	12	—	15	—	20	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	9	—	10	—	12	—	15	—	ns	3,4
Data Valid to End of Write	t_{DVEH}	6	—	7	—	8	—	10	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All timings are referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6206BA EJ XX X

Motorola Memory Prefix

Part Number

Shipping Method (R = Tape and Reel, Blank = Rails)

Speed (12 = 12 ns, 15 = 15 ns, 20 = 20 ns, 25 = 25 ns)

Package (J = 300 mil SOJ, E = Evolutionary Pinout)

Full Part Numbers — MCM6206BAEJ12 MCM6206BAEJ12R
MCM6206BAEJ15 MCM6206BAEJ15R
MCM6206BAEJ20 MCM6206BAEJ20R
MCM6206BAEJ25 MCM6206BAEJ25R

MCM6706B

Product Preview

32K x 8 Bit Static Random Access Memory

The MCM6706B is a 262,144 bit static random access memory organized as 32,768 words of 8 bits. Static design eliminates the need for external clocks or timing strobes.

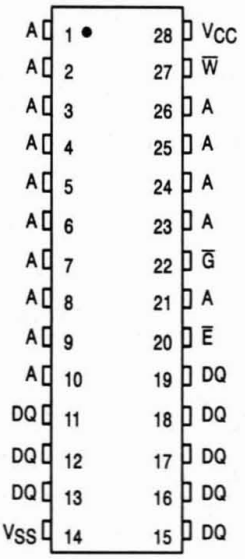
Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

The MCM6706B is available in a 300 mil, 28–lead surface–mount SOJ package.

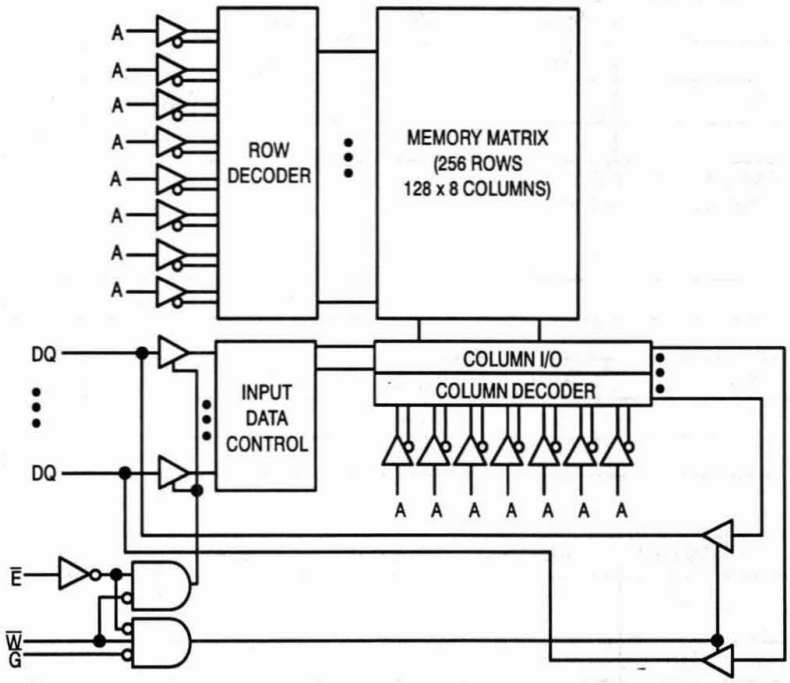
- Single 5.0 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: MCM6706B–8 = 8 ns
  MCM6706B–10 = 10 ns
  MCM6706B–12 = 12 ns

J PACKAGE
300 MIL SOJ
CASE 810B–03

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ	Data Input/Output
V_{CC}	+ 5.0 V Power Supply
V_{SS}	Ground

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

REV 1
10/9/96

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle
H	X	X	Not Selected	High–Z	—
L	H	H	Read	High–Z	—
L	L	H	Read	D_{out}	Read Cycle
L	X	L	Write	D_{in}	Write Cycle

2

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.
** V_{IL} (min) = – 0.5 V dc @ 30.0 mA; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	6706B–8	6706B–10	6706B–12	Unit	Notes
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max, f = f_{max})	I_{CCA}	195	185	175	mA	1, 2, 3
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	75	70	65	mA	1, 2, 3
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS}, or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	20	mA	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3 V, V_{IH} = 3 V).
2. All addresses transition simultaneously low (LSB) and then high (MSB).
3. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C_{in}	5	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{G}$, $\overline{W}$)	C_{in}	6	pF
I/O Capacitance	C_{out}	6	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

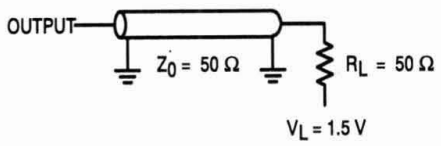
Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1a

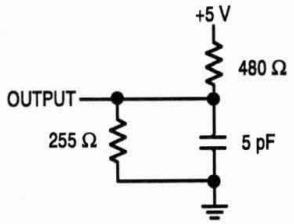
READ CYCLE (See Notes 1 and 2)

Parameter	Symbol	MCM6706B–8		MCM6706B–10		MCM6706B–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Access Time	t_{AVQV}	—	8	—	10	—	12	ns	
Chip Enable Access Time	t_{ELQV}	—	8	—	10	—	12	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	5	—	6	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	ns	
Chip Enable Low to Output Active	t_{ELQX}	1	—	1	—	1	—	ns	4 ,5, 6
Chip Enable High to Output High–Z	t_{EHQZ}	—	4.5	—	5	—	6	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4, 5, 6
Output Enable High to Output High–Z	t_{GHQZ}	—	4	—	5	—	6	ns	4, 5, 6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1b.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.



(a)



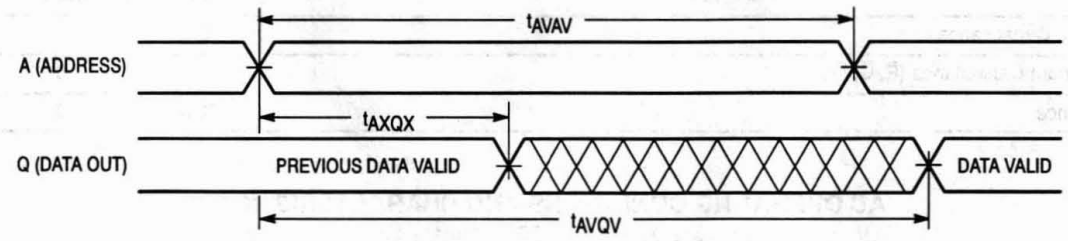
(b)

Figure 1. AC Test Loads

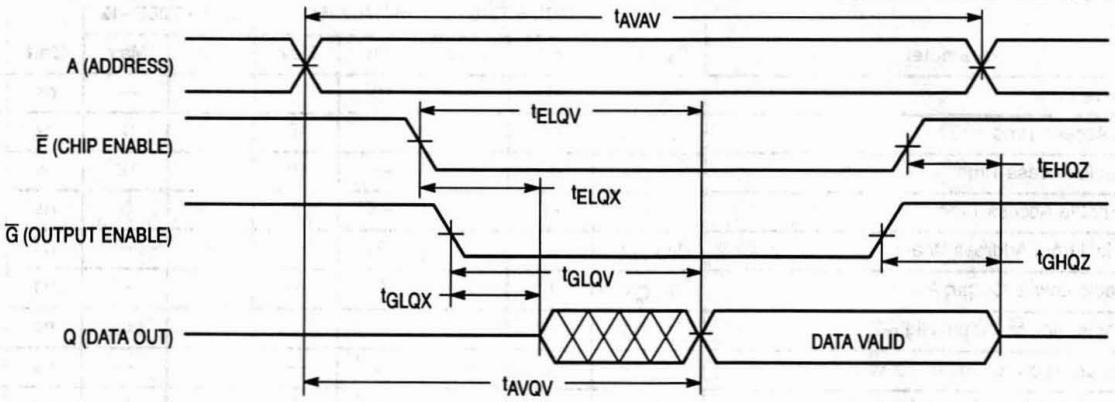
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

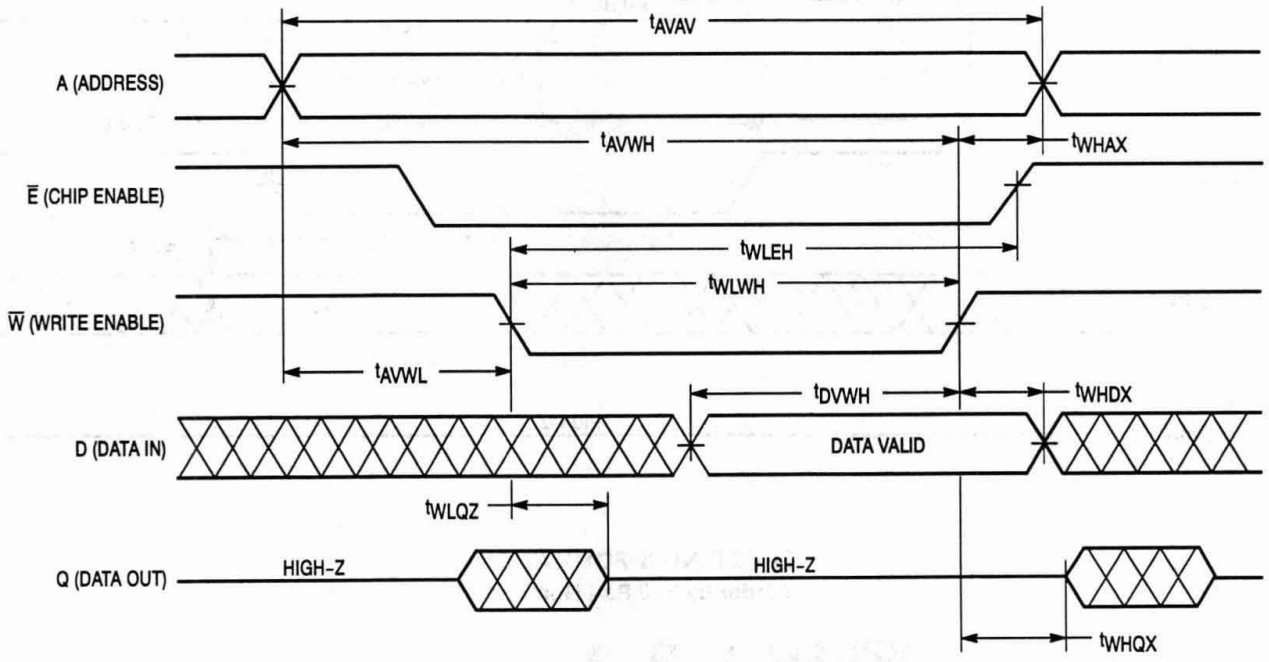


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6706B–8		MCM6706B–10		MCM6706B–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	—	4	—	5	—	6	ns	4, 5, 6
Wirte High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage with load of Figure 1b.
5. Parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

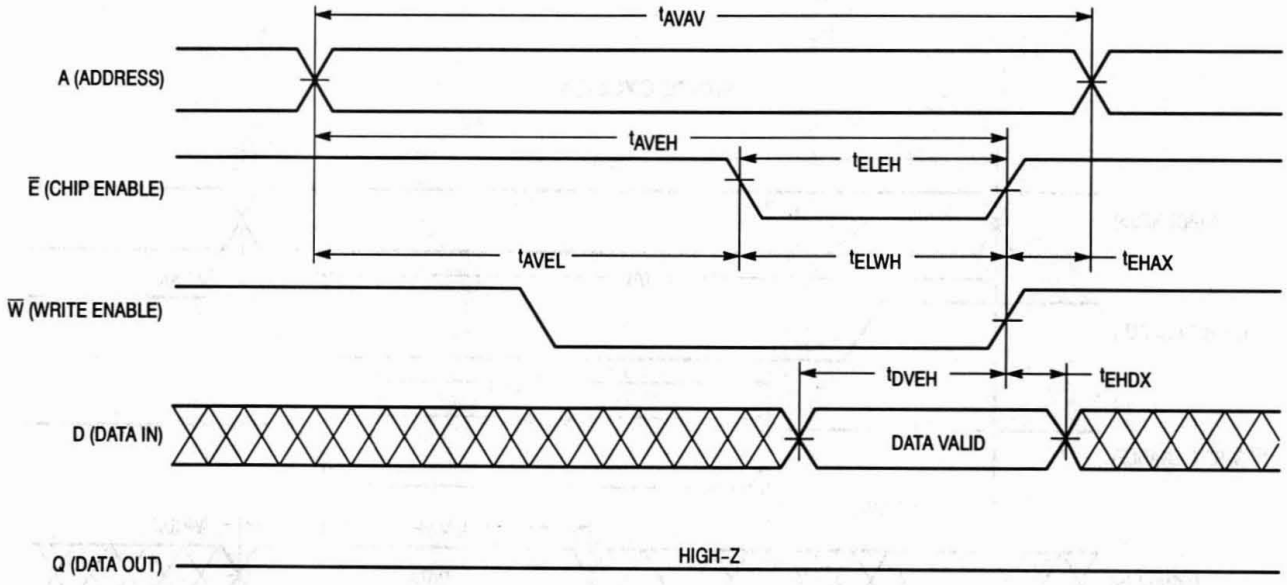


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6706B–8		MCM6706B–10		MCM6706B–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	8	—	9	—	10	—	ns	
Chip Enable to End of Write	t_{ELWH}, t_{ELEH}	7	—	8	—	9	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6706B X XX X

- MCM — Motorola Memory Prefix
- 6706B — Part Number
- X — Package (J = 300 mil SOJ)
- XX — Speed (8 = 8 ns, 10 = 10 ns, 12 = 12 ns)
- X — Shipping Method (R = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6706BJ8, MCM6706BJ8R, MCM6706BJ10, MCM6706BJ10R, MCM6706BJ12, MCM6706BJ12R

MCM6706BR

2

Product Preview

32K x 8 Bit Static Random Access Memory

J PACKAGE
300 MIL SOJ
CASE 857–02

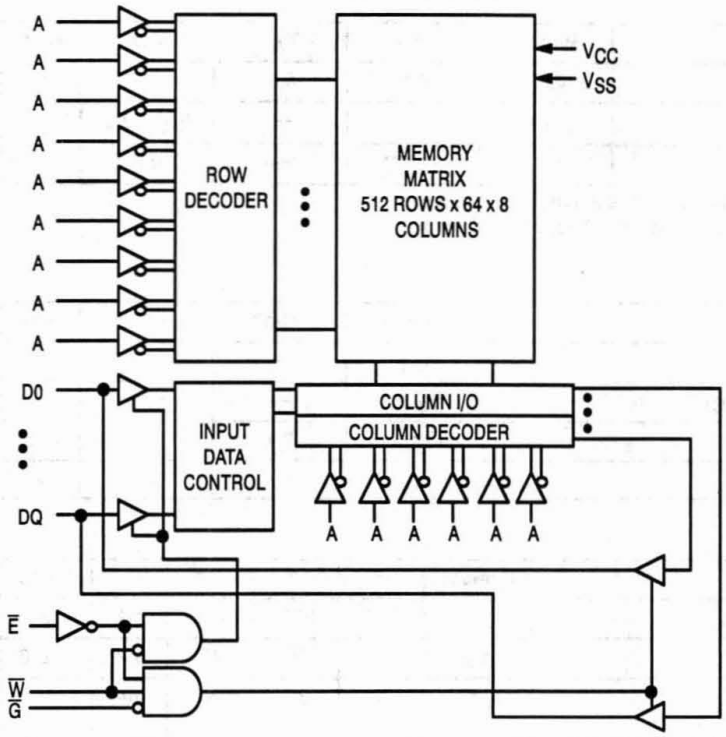
The MCM6706BR is a 262,144 bit static random access memory organized as 32,768 words of 8 bits. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

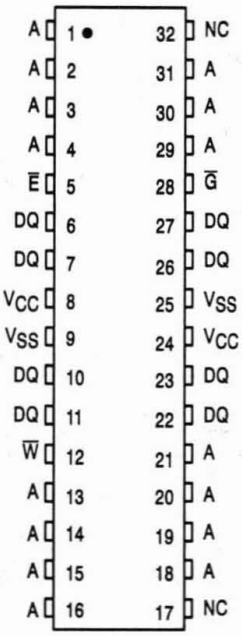
The MCM6706BR meets JEDEC standards and is available in a revolutionary pinout 300 mil, 32–lead surface–mount SOJ package.

- Single 5.0 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: MCM6706BR–6 = 6 ns
  MCM6706BR–7 = 7 ns
  MCM6706BR–8 = 8 ns
- Center Power and I/O Pins for Reduced Noise

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

A	Address
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

REV 1
10/9/96

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle
H	X	X	Not Selected	High–Z	—
L	H	H	Read	High–Z	—
L	L	H	Read	D_{out}	Read Cycle
L	X	L	Write	D_{in}	Write Cycle

2

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.
** V_{IL} (min) = – 0.5 V dc @ 30.0 mA; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	–6	–7	–8	Unit	Notes
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max, f = f_{max})	I_{CCA}	215	205	195	mA	1, 2, 3
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	95	85	75	mA	1, 2, 3
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS}, or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	20	mA	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
2. All addresses transition simultaneously low (LSB) and then high (MSB).
3. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C_{in}	5	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{G}$, $\overline{W}$)	C_{in}	6	pF
I/O Capacitance	C_{out}	6	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

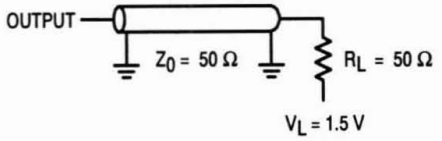
2

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1a

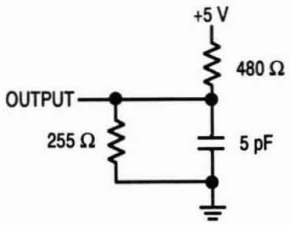
READ CYCLE (See Notes 1 and 2)

Parameter	Symbol	6706BR–6		6706BR–7		6706BR–8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	6	—	7	—	8	—	ns	3
Address Access Time	t_{AVQV}	—	6	—	7	—	8	ns	
Chip Enable Access Time	t_{ELQV}	—	6	—	7	—	8	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	4	—	4	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	ns	
Chip Enable Low to Output Active	t_{ELQX}	3	—	3	—	3	—	ns	4 ,5, 6
Chip Enable High to Output High–Z	t_{EHQZ}	—	3	—	3.5	—	3.5	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4, 5, 6
Output Enable High to Output High–Z	t_{GHQZ}	—	3	—	3.5	—	3.5	ns	4, 5, 6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1b.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.



(a)



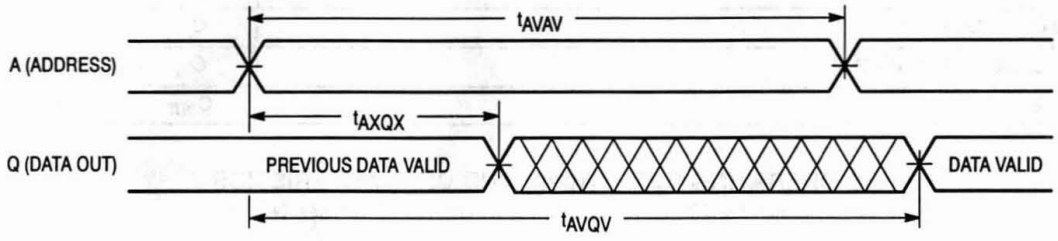
(b)

TIMING LIMITS

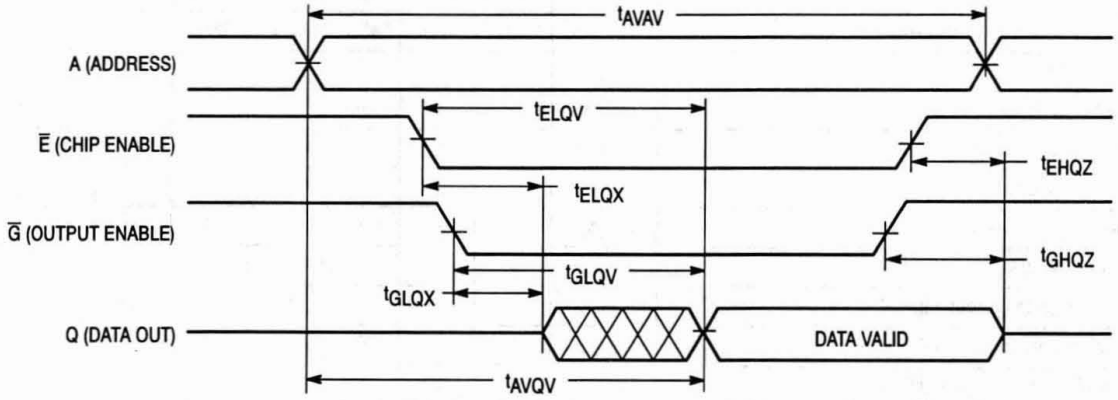
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Figure 1. AC Test Loads

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

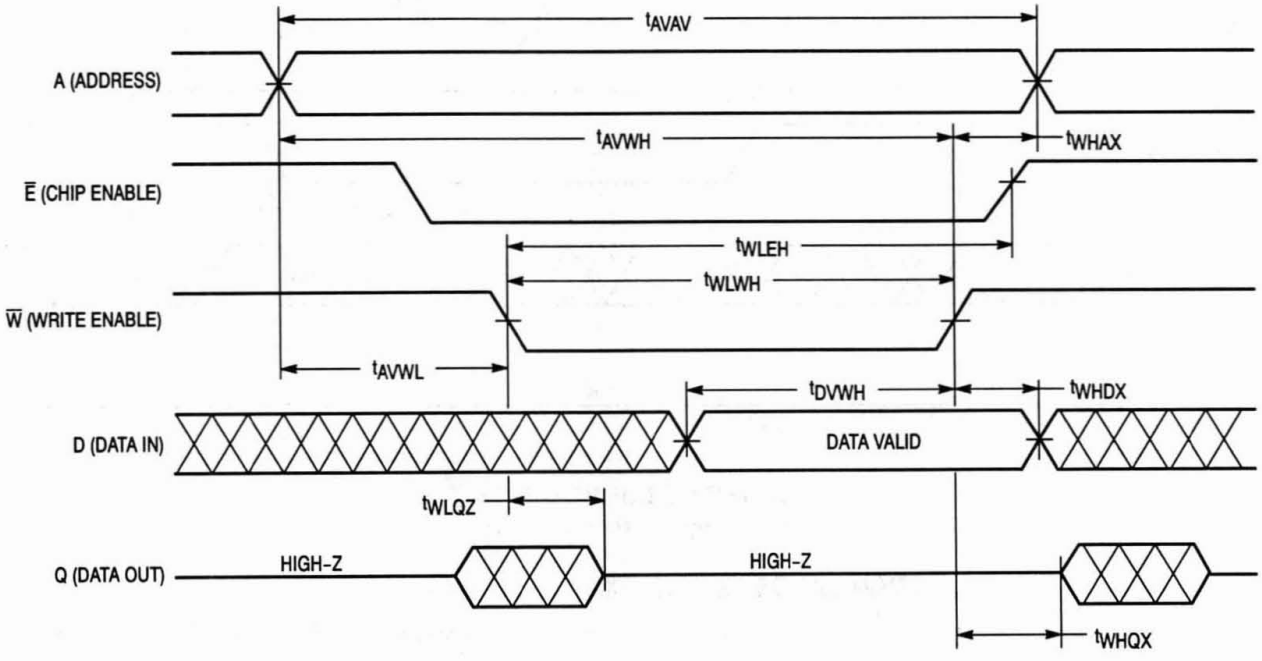


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6706BR–6		6706BR–7		6706BR–8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	6	—	7	—	8	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	6	—	7	—	8	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	6	—	7	—	8	—	ns	
Data Valid to End of Write	t_{DVWH}	3	—	3.5	—	3.5	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	—	3.5	—	3.5	—	3.5	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage with load of Figure 1b.
5. Parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

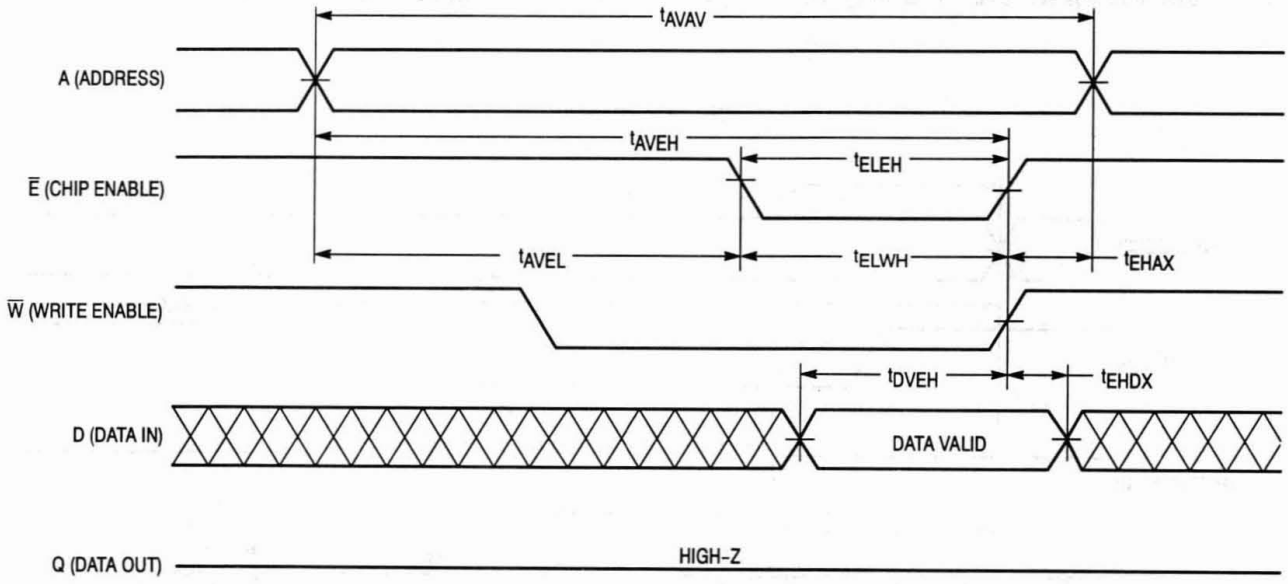


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6706BR–6		6706BR–7		6706BR–8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	6	—	7	—	8	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	6	—	7	—	8	—	ns	
Chip Enable to End of Write	t_{ELWH}, t_{ELEH}	5	—	6	—	6	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	3	—	3.5	—	3.5	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6706BR X X XX

- Motorola Memory Prefix
- Part Number
- Shipping Method (R = Tape and Reel, Blank = Rails)
- Speed (6 = 6 ns, 7 = 7 ns, 8 = 8 ns)
- Package (J = 300 mil SOJ)

Full Part Numbers — MCM6706BRJ6, MCM6706BRJ6R, MCM6706J7, MCM6706BRJ7R, MCM6706BRJ8, MCM6706BRJ8R

MCM6709B

2

Product Preview

64K x 4 Bit Static RAM

The MCM6709B is a 262,144 bit static random access memory organized as 65,536 words of 4 bit. Static design eliminates the need for external clocks or timing strobes.

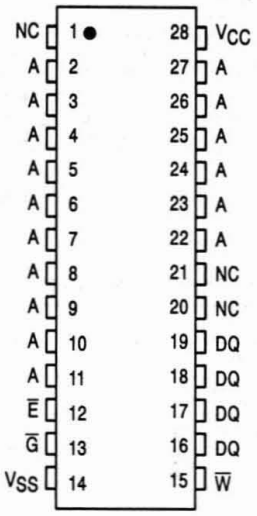
Output enable ($\overline{G}$), a special control feature of the MCM6709B, provides increased system flexibility and eliminates bus contention problems.

The MCM6709B is available in a 300 mil, 28 lead plastic surface–mount SOJ package.

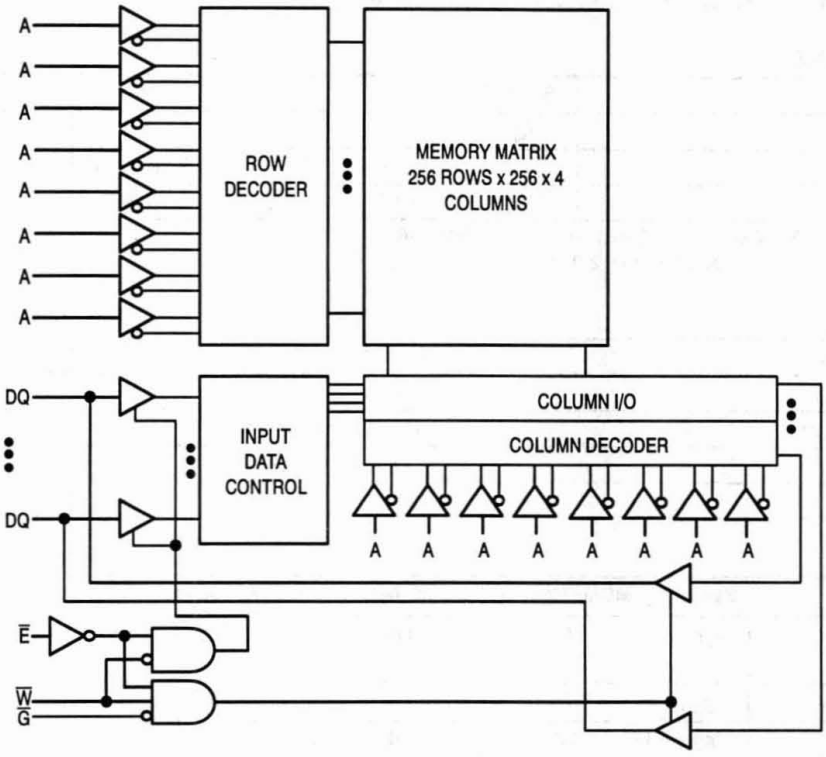
- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Fast Access Times: MCM6709B–8 = 8 ns
  MCM6709B–10 = 10 ns
  MCM6709B–12 = 12 ns

J PACKAGE
300 MIL SOJ
CASE 810B–03

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
DQ	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

This document contains informantion on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

REV 1
10/9/96

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	Output	Cycle
H	X	X	Not Selected	High–Z	—
L	H	H	Read	High–Z	—
L	L	H	Read	D_{out}	Read Cycle
L	X	L	Write	D_{in}	Write Cycle

2

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.
** V_{IL} (min) = – 0.5 V dc @ 30.0 mA; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	MCM6709B–8	MCM6709B–10	MCM6709B–12	Unit	Notes
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max, f = f_{max})	I_{CCA}	185	175	165	mA	1, 2, 3
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	120	110	105	mA	1, 2, 3
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS}, or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	20	mA	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
2. All addresses transition simultaneously low (LSB) and then high (MSB).
3. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C_{in}	5	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{G}$, $\overline{W}$)	C_{in}	5	pF
Input/Output Capacitance	$C_{I/O}$	6	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

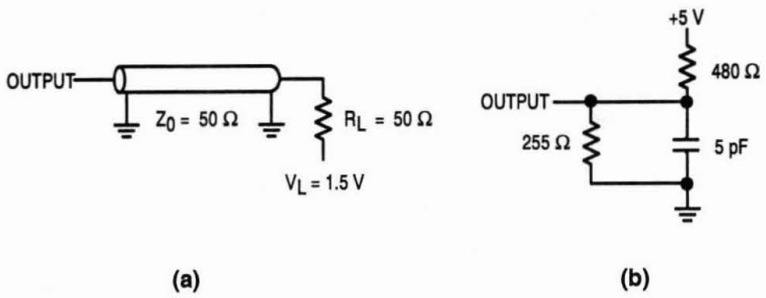
Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1a

READ CYCLES 1 AND 2 (See Notes 1 and 2)

Parameter	Symbol	MCM6709B–8		MCM6709B–10		MCM6709B–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Access Time	t_{AVQV}	—	8	—	10	—	12	ns	
Chip Enable Access Time	t_{ELQV}	—	8	—	10	—	12	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	5	—	6	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	ns	
Chip Enable Low to Output Active	t_{ELQX}	1	—	1	—	1	—	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4, 5, 6
Chip Enable High to Output High–Z	t_{EHQZ}	—	4.5	—	5	—	6	ns	4, 5, 6
Output Enable High to Output High–Z	t_{GHQZ}	—	4	—	5	—	6	ns	4, 5, 6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1b.
6. This parameter is sampled and not 100% tested.



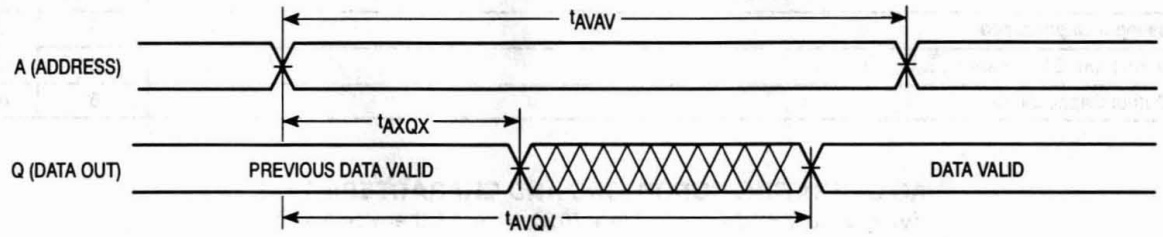
(a) (b)

Figure 1. AC Test Loads

TIMING LIMITS

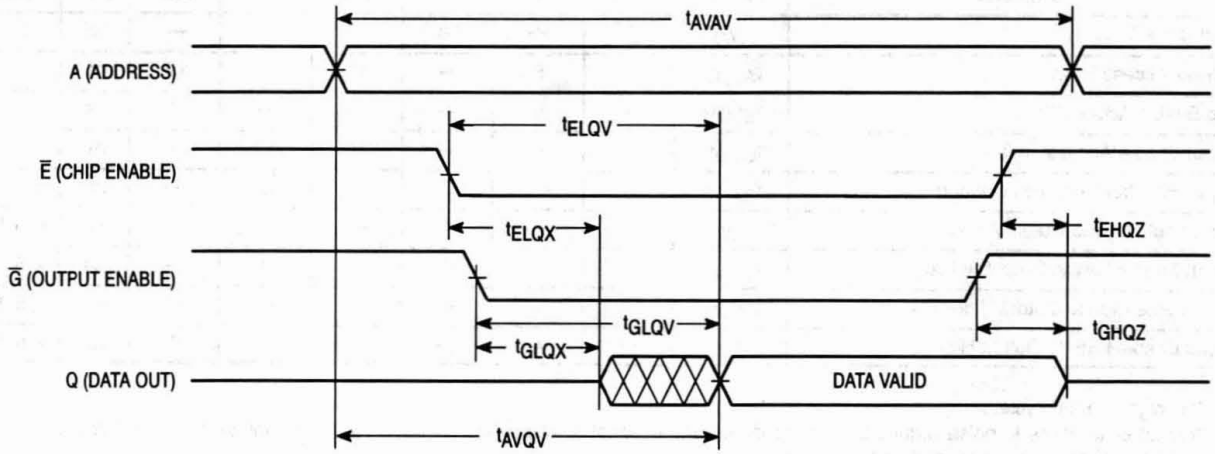
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note)



NOTE: Device is continuously selected ($\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$).

READ CYCLE 2 (See Note)



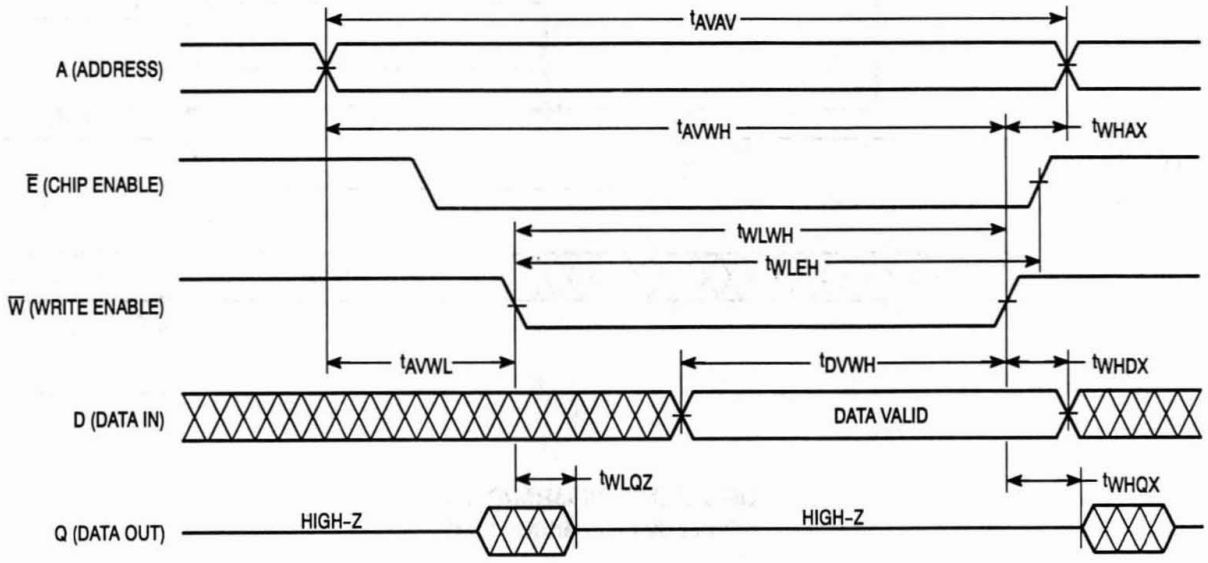
NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6709B–8		MCM6709B–10		MCM6709B–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	—	4	—	5	—	6	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady state voltage with load of Figure 1b.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

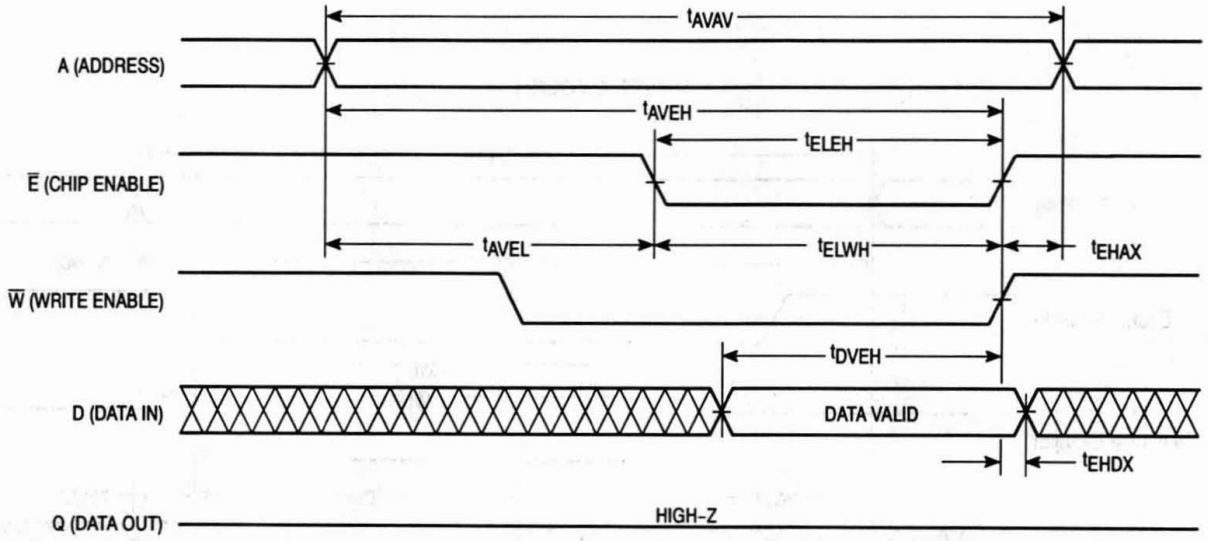


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6709B–8		MCM6709B–10		MCM6709B–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	8	—	9	—	10	—	ns	
Chip Enable to End of Write	t_{ELEH}, t_{ELWH}	7	—	8	—	9	—	ns	4, 5
Data Valid to End of Write	t_{DVEH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6709B X XX X

- MCM — Motorola Memory Prefix
- 6709B — Part Number
- X — Package (J = 300 mil SOJ)
- XX — Speed (8 = 8 ns, 10 = 10 ns, 12 = 12 ns)
- X — Shipping Method (R = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6709BJ8, MCM6709BJ10, MCM6709BJ12, MCM6709BJ8R, MCM6709BJ10R, MCM6709BJ12R

MCM6709BR

Product Preview

64K x 4 Bit Static RAM

The MCM6709BR is a 262,144 bit static random access memory organized as 65,536 words of 4 bits. Static design eliminates the need for external clocks or timing strobes.

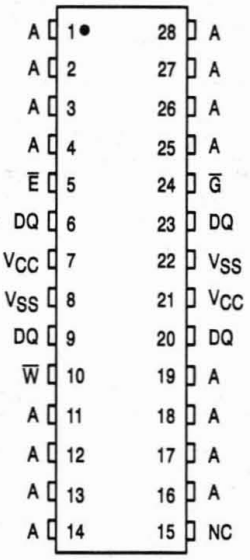
Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

The MCM6709BR meets JEDEC standards and is available in a revolutionary pinout 300 mil, 28 lead plastic surface–mount SOJ package.

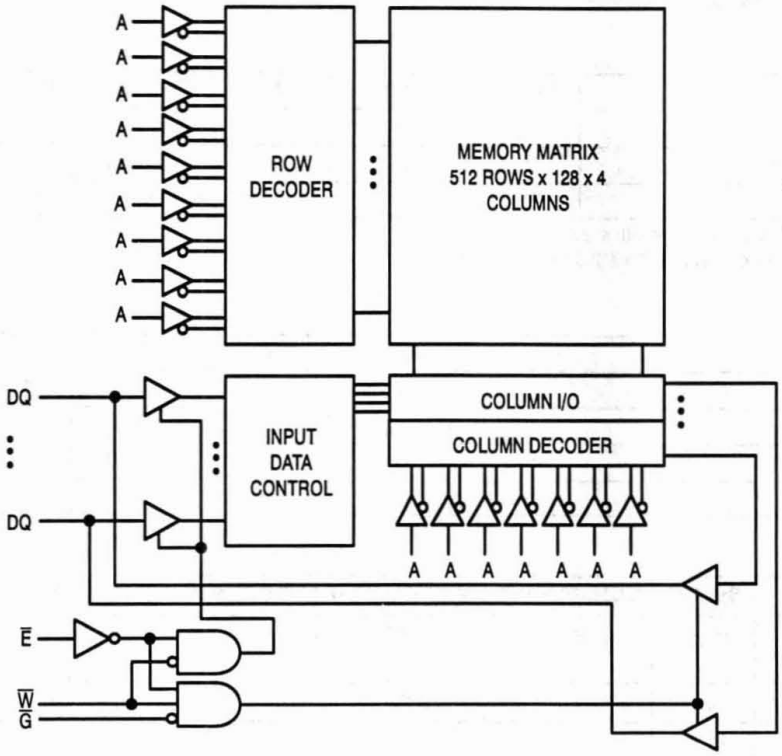
- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs are TTL Compatible
- Center Power and I/O Pins for Reduced Noise
- Three State Outputs
- Fast Access Times:
  MCM6709BR–6 = 6 ns
  MCM6709BR–7 = 7 ns
  MCM6709BR–8 = 8 ns

J PACKAGE
300 MIL SOJ
CASE 810B–03

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
DQ	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

REV 2
3/17/97

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	Output	Cycle
H	X	X	Not Selected	High–Z	—
L	H	H	Read	High–Z	—
L	L	H	Read	D_{out}	Read Cycle
L	X	L	Write	D_{in}	Write Cycle

2

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.
** V_{IL} (min) = – 0.5 V dc @ 30.0 mA; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	MCM6709BR–6	MCM6709BR–7	MCM6709BR–8	Unit	Notes
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max, f = f_{max})	I_{CCA}	215	205	195	mA	1, 2, 3
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	95	85	75	mA	1, 2, 3
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS}, or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	20	mA	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
2. All addresses transition simultaneously low (LSB) and then high (MSB).
3. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C_{in}	5	pF
Control Pin Input Capacitance($\overline{E}$, $\overline{G}$, $\overline{W}$)	C_{in}	6	pF
Input/Output Capacitance	$C_{I/O}$	6	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

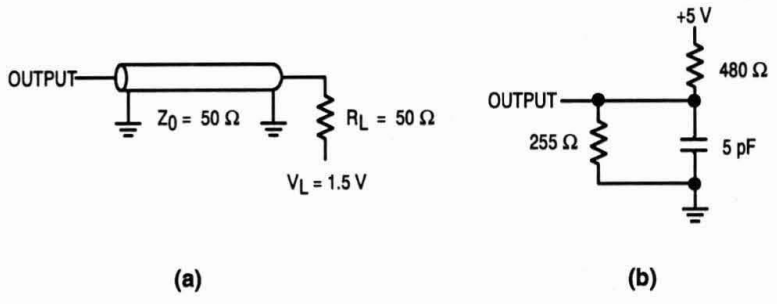
(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1a

READ CYCLES 1 AND 2 (See Notes 1 and 2)

Parameter	Symbol	MCM6709BR–6		MCM6709BR–7		MCM6709BR–8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	6	—	7	—	8	—	ns	3
Address Access Time	t_{AVQV}	—	6	—	7	—	8	ns	
Chip Enable Access Time	t_{ELQV}	—	6	—	7	—	8	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	4	—	4	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	ns	
Chip Enable Low to Output Active	t_{ELQX}	3	—	3	—	3	—	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4, 5, 6
Chip Enable High to Output High–Z	t_{EHQZ}	—	3	—	3.5	—	3.5	ns	4, 5, 6
Output Enable High to Output High–Z	t_{GHQZ}	—	3	—	3.5	—	3.5	ns	4, 5, 6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1b.
6. This parameter is sampled and not 100% tested.

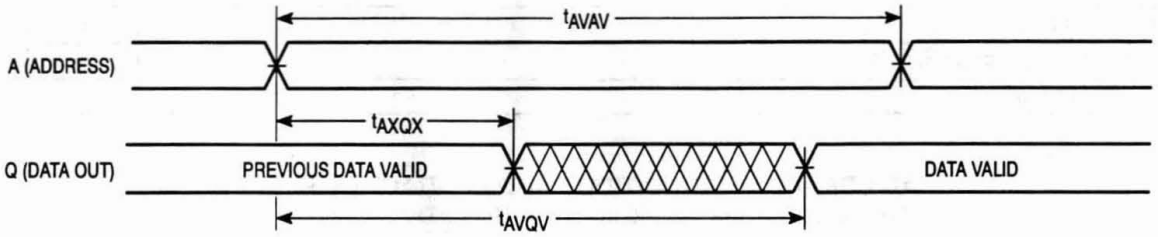


TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

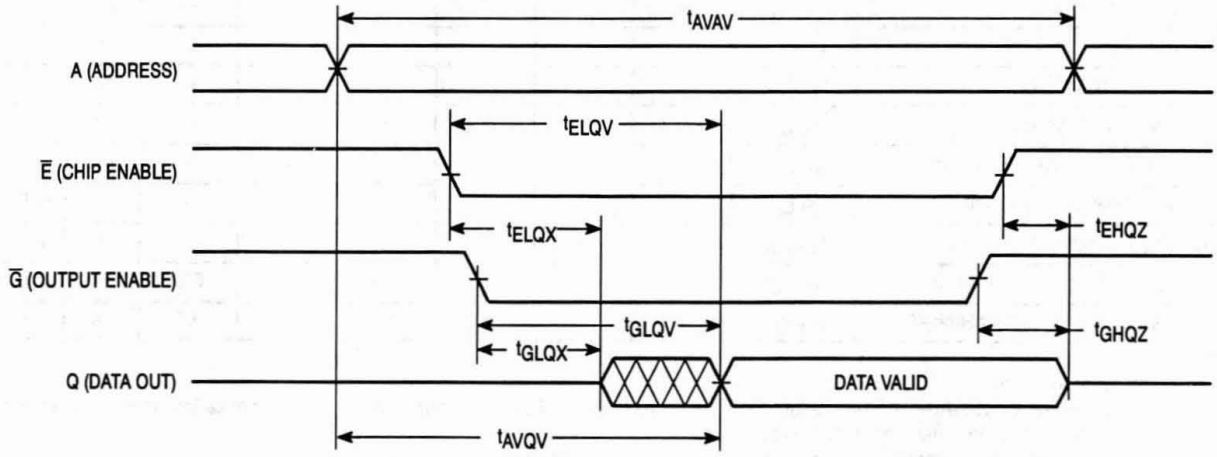
Figure 1. AC Test Loads

READ CYCLE 1 (See Note)



NOTE: Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).

READ CYCLE 2 (See Note)



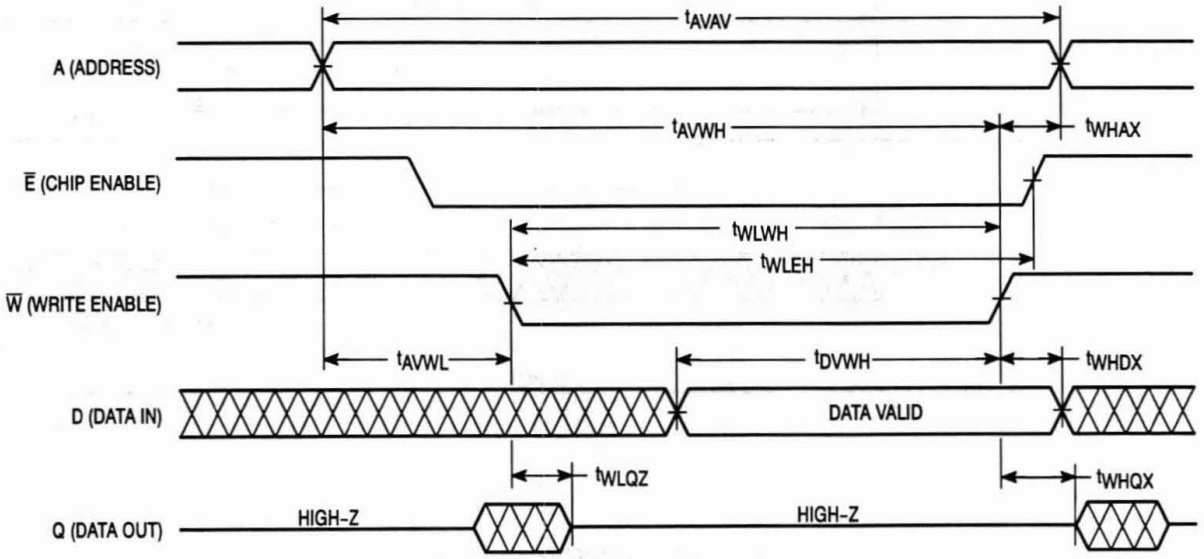
NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6709BR–6		MCM6709BR–7		MCM6709BR–8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	6	—	7	—	8	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	6	—	7	—	8	—	ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	6	—	7	—	8	—	ns	
Data Valid to End of Write	t_{DVWH}	3	—	3.5	—	3.5	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	—	3.5	—	3.5	—	3.5	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady state voltage with load of Figure 1b.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

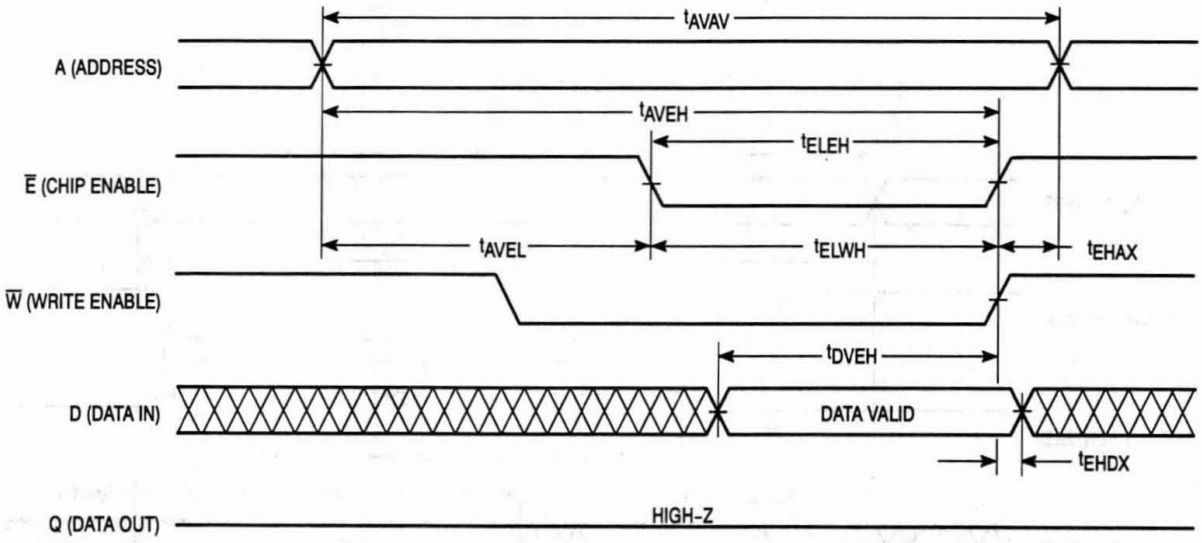


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6709BR–6		MCM6709BR–7		MCM6709BR–8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	6	—	7	—	8	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	6	—	7	—	8	—	ns	
Chip Enable to End of Write	t_{ELEH}, t_{ELWH}	5	—	6	—	7	—	ns	4, 5
Data Valid to End of Write	t_{DVEH}	3	—	3.5	—	3.5	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

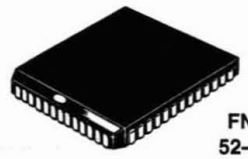
MCM 6709BR X X X

- MCM — Motorola Memory Prefix
- 6709BR — Part Number
- X — Package (J = 300 mil SOJ)
- X — Speed (6 = 6 ns, 7 = 7 ns, 8 = 8 ns)
- X — Shipping Method (R = Tape and Reel, Blank = Rails)

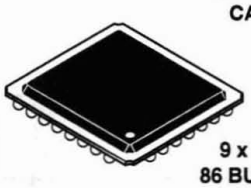
Full Part Numbers — MCM6709BRJ6, MCM6709BRJ7, MCM6709BRJ8, MCM6709BRJ6R, MCM6709BRJ7R, MCM6709BRJ8R

MCM56824A

DSPRAM™
8K x 24 Bit Fast Static RAM



FN PACKAGE
52–LEAD PLCC
CASE 778–02



9 x 10 GRID
86 BUMP PBGA
CASE 896A–01

The MCM56824A is a 196,608 bit static random access memory organized as 8,192 words of 24 bits. The device integrates an 8K x 24 SRAM core with multiple chip enable inputs, output enable, and an externally controlled single address pin multiplexer. These functions allow for direct connection to the Motorola DSP56001 Digital Signal Processor and provide a very efficient means for implementation of a reduced parts count system requiring no additional interface logic.

The availability of multiple chip enable ($\overline{E1}$ and E2) and output enable ($\overline{G}$) inputs provides for greater system flexibility when multiple devices are used. With either chip enable input unasserted, the device will enter standby mode, useful in low–power applications. A single on–chip multiplexer selects A12 or X/$\overline{Y}$ as the highest order address input depending upon the state of the V/$\overline{S}$ control input. This feature allows one physical static RAM component to efficiently store program and vector or scalar operands by dynamically re–partitioning the RAM array. Typical applications will logically map vector operands into upper memory with scalar operands being stored in lower memory. By connecting DSP56001 address A15 to the VECTOR/SCALAR (V/$\overline{S}$) MUX control pin, such partitioning can occur with no additional components. This allows efficient utilization of the RAM resource irrespective of operand type. See application diagrams at the end of this document for additional information.

Multiple power and ground pins have been utilized to minimize effects induced by output noise.

The MCM56824A is available in a 52 pin plastic leaded chip–carrier (PLCC) and a 9 x 10 grid, 86 bump surface mount PBGA.

- Single 5 V ± 10% Power Supply
- Fast Access and Cycle Times: 20/25/35 ns Max
- Fully Static Read and Write Operations
- Equal Address and Chip Enable Access Times
- Single Bit On–Chip Address Multiplexer
- Active High and Active Low Chip Enable Inputs
- Output Enable Controlled Three State Outputs
- High Board Density PLCC Package
- Low Power Standby Mode
- Fully TTL Compatible

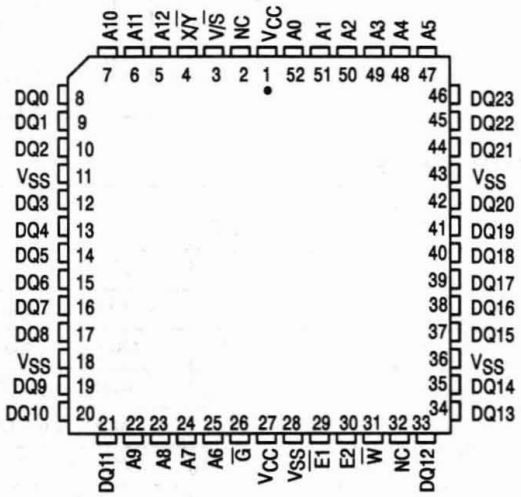
PIN NAMES	
A0 – A11	Address Inputs
A12, X/$\overline{Y}$	Multiplexed Address
V/$\overline{S}$	Address Multiplexer Control
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ23	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

For proper operation of the device, all V_{SS} pins must be connected to ground.

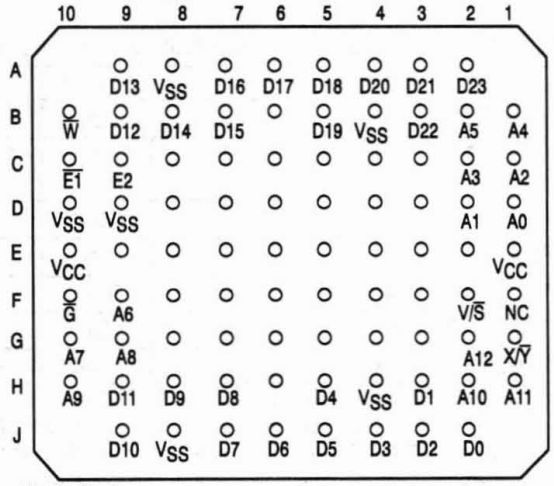
DSPRAM is a trademark of Motorola, Inc.

PIN ASSIGNMENTS

PLCC



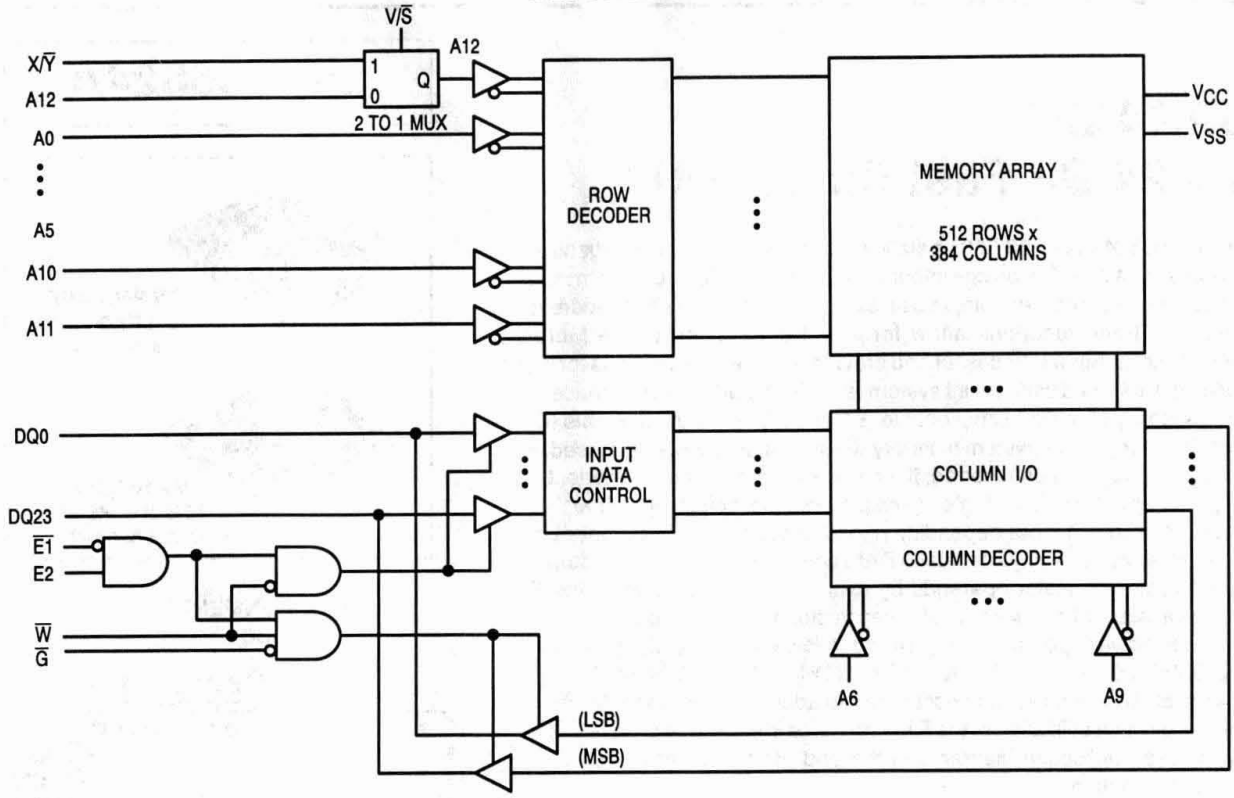
VIEW OF PBGA PACKAGE BOTTOM


10 9 8 7 6 5 4 3 2 1
A D13 VSS D16 D17 D18 D20 D21 D23
B W D12 D14 D15 D19 VSS D22 A5 A4
C E1 E2 A3 A2
D VSS VSS A1 A0
E VCC VCC
F G A6 V/S NC
G A7 A8 A12 X/Y
H A9 D11 D9 D8 D4 VSS D1 A10 A11
J D10 VSS D7 D6 D5 D3 D2 D0

Not to Scale

REV 2
4/95

BLOCK DIAGRAM



TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	V/$\overline{S}$	Mode	Supply Current	I/O Status
H	X	X	X	X	Not Selected	I_{SB}	High–Z
X	L	X	X	X	Not Selected	I_{SB}	High–Z
L	H	H	H	X	Output Disable	I_{CC}	High–Z
L	H	L	H	H	Read Using X/$\overline{Y}$	I_{CC}	Data Out
L	H	L	H	L	Read Using A12	I_{CC}	Data Out
L	H	X	L	H	Write Using X/$\overline{Y}$	I_{CC}	Data In
L	H	X	L	L	Write Using A12	I_{CC}	Data In

NOTE: X=don't care.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.75	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is assumed to be in a test socket or mounted on a printed circuit board with at least 300 LFPM of transverse air flow being maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

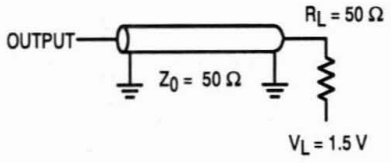
* V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

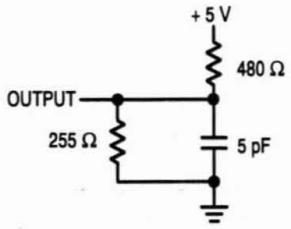
Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(i)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH}, $\overline{E1}$ = V_{IH}, E2 = V_{IL}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E1}$ = V_{IL}, E2 = V_{IH}, I_{out} = 0 mA, All Other Inputs ≥ V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V) MCM56824A–20 Cycle Time: ≥ 20 ns MCM56824A–25 Cycle Time: ≥ 25 ns MCM56824A–35 Cycle Time: ≥ 35 ns	I_{CCA}	 — — —	 260 220 180	mA
Standby Current ($\overline{E1}$ = V_{IH}, E2 = V_{IL}, All Inputs = V_{IL} or V_{IH})	I_{SB1}	—	15	mA
CMOS Standby Current ($\overline{E1}$ ≥ V_{CC} – 0.2 V, E2 ≤ 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V)	I_{SB2}	—	10	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	All Pins Except DQ0 – DQ23	C_{in}	4	6	pF
Input/Output Capacitance	DQ0 – DQ23	C_{out}	6	8	pF



(a)



(b)

Figure 1. AC Test Loads

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

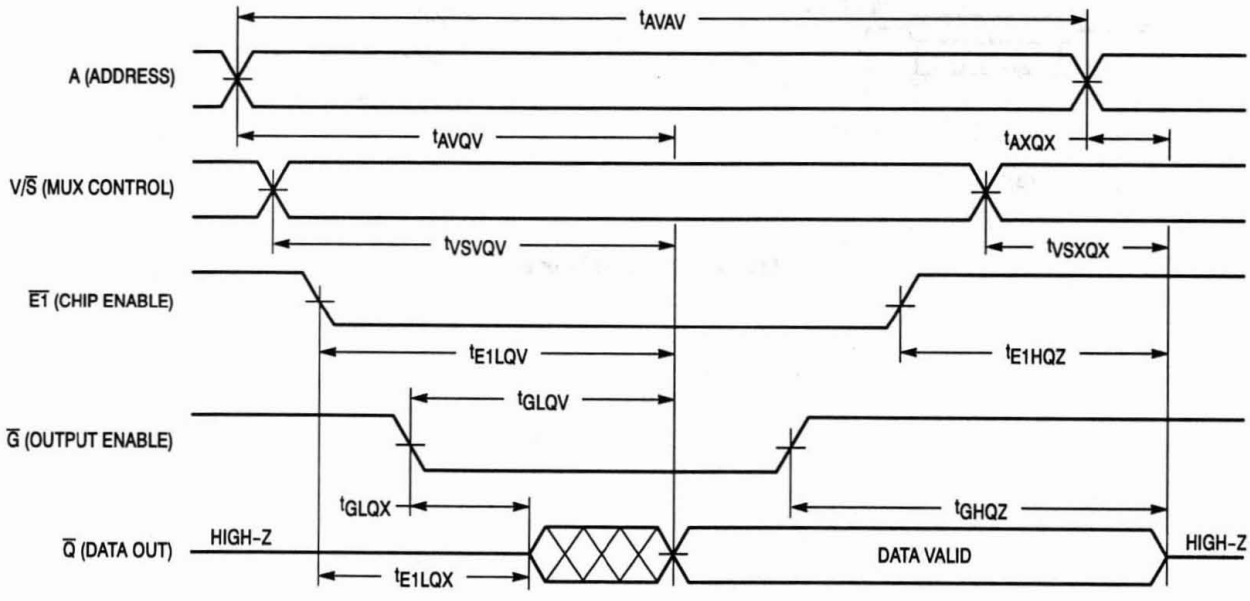
Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1a Unless Otherwise Noted

READ CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM56824A–20		MCM56824A–25		MCM56824A–35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	20	—	25	—	35	—	ns	
Address Access Time	t_{AVQV}	—	20	—	25	—	35	ns	
MUX Control Valid to Output Valid	t_{VSVQV}	—	20	—	25	—	35	ns	
Chip Enable to Output Valid	t_{E1LQV} t_{E2HQV}	—	20	—	25	—	35	ns	4
Output Enable to Output Valid	t_{GLQV}	—	8	—	10	—	15	ns	
Output Active from Chip Enable	t_{E1LQX} t_{E2HQX}	2	—	2	—	0	—	ns	4, 5
Output Active from Output Enable	t_{GLQX}	0	—	0	—	0	—	ns	5
Output Hold from Address Change	t_{AXQX}	4	—	5	—	5	—	ns	
Output Hold from MUX Control Change	t_{VSXQX}	4	—	5	—	5	—	ns	
Chip Enable to Output High–Z	t_{E1HQZ} t_{E2LQZ}	0	10	0	15	0	15	ns	4, 5
Output Enable High to Output High–Z	t_{GHQZ}	0	8	0	15	0	15	ns	5

NOTES:
1. A read cycle is defined by $\overline{W}$ high.
2. All read cycle timings are referenced from the last valid address or vector/scalar transition to the first address or vector/scalar transition.
3. Addresses valid prior to or coincident with $\overline{E1}$ going low or E2 going high.
4. $\overline{E1}$ in the timing diagrams represents both $\overline{E1}$ and E2 with $\overline{E1}$ asserted low and E2 asserted high.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1b. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{E1HQZ} max is less than t_{E1LQX} min, t_{E2LQZ} max is less than t_{E2HQX} min, and t_{GHQZ} max is less than t_{GLQX} min for a given device and from device to device.

READ CYCLE

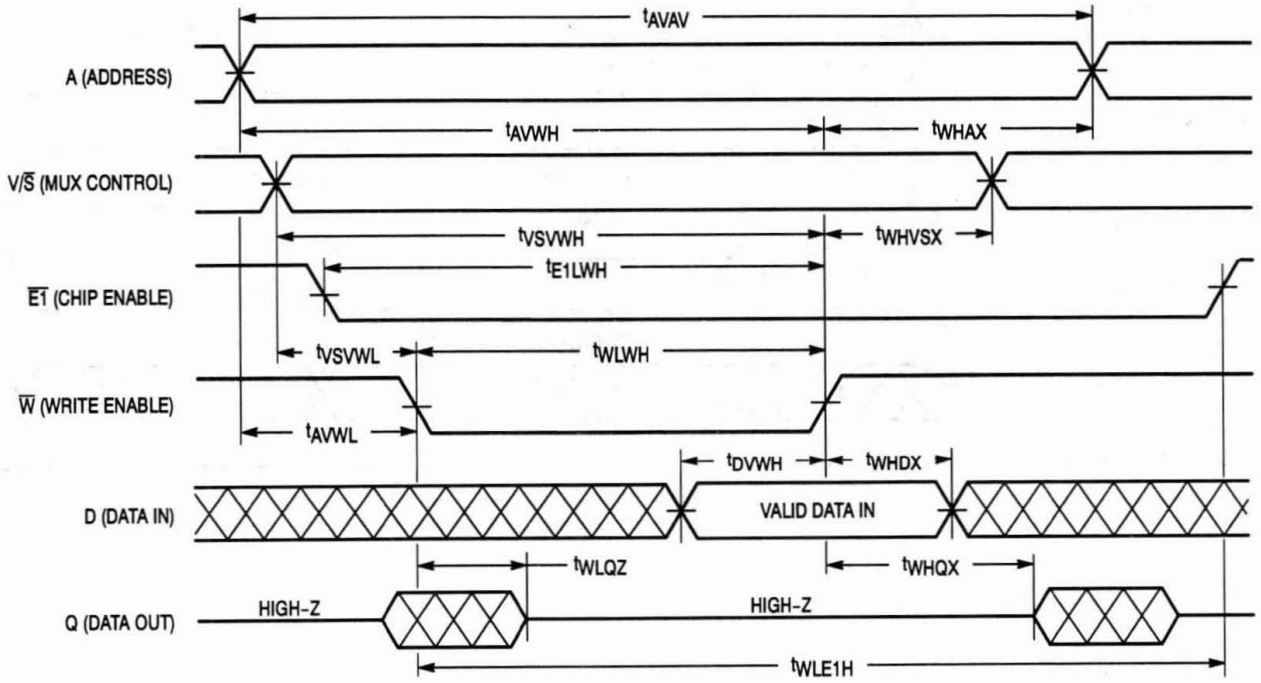


WRITE CYCLE TIMING (Write Enable Initiated, See Note 1)

Parameter	Symbol	MCM56824A–20		MCM56824A–25		MCM56824A–35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	35	—	ns	
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	2
MUX Control Setup Time	t_{VSVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	15	—	20	—	30	—	ns	
MUX Control Valid to End of Write	t_{VSVWH}	15	—	20	—	30	—	ns	
Write Pulse Width	t_{WLWH}	15	—	15	—	20	—	ns	3
Write Enable to Chip Enable Disable	t_{WLE1H} t_{WLE2L}	15	—	15	—	20	—	ns	3, 4
Chip Enable to End of Write	t_{E1LWH} t_{E2HWH}	15	—	15	—	20	—	ns	3, 4
Data Valid to End of Write	t_{DVWH}	8	—	10	—	15	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	5
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	2
MUX Control Recovery Time	t_{WHVSX}	0	—	0	—	0	—	ns	
Write High to Output Low–Z	t_{WHQX}	4	—	5	—	5	—	ns	6
Write Low to Output High–Z	t_{WLQZ}	0	15	0	15	0	15	ns	6

NOTES:
1. A write cycle starts at the latest transition of $\overline{E1}$ low, $\overline{W}$ low, or E2 high. A write cycle ends at the earliest transition of $\overline{E1}$ high, $\overline{W}$ high, or E2 low.
2. Write must be high for all address transitions.
3. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high the outputs will remain in a high–impedance state.
4. $\overline{E1}$ in the timing diagrams represents both $\overline{E1}$ and E2 with $\overline{E1}$ asserted low and E2 asserted high.
5. During this time the output pins may be in the output state. Signals of opposite phase must not be applied to the outputs at this time.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1b. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{E1HQZ} max is less than t_{E1LQX} min, t_{E2LQZ} max is less than t_{E2HQX} min, and t_{GHQZ} max is less than t_{GLQX} min for a given device and from device to device.

$\overline{WE}$ INITIATED WRITE CYCLE

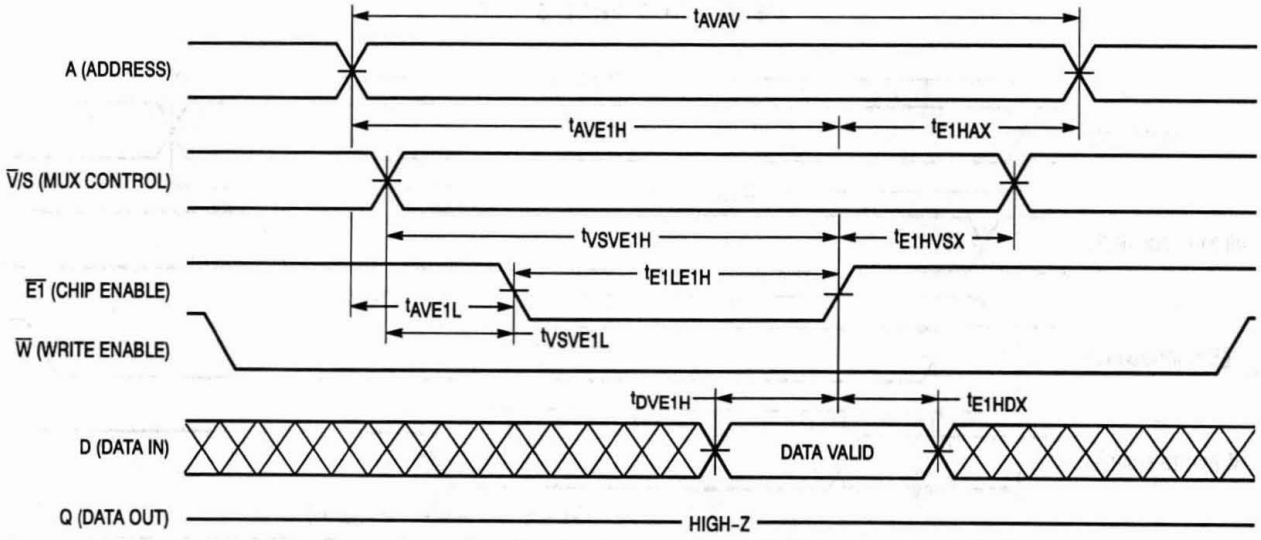


WRITE CYCLE TIMING (Chip Enable Initiated, See Note 1)

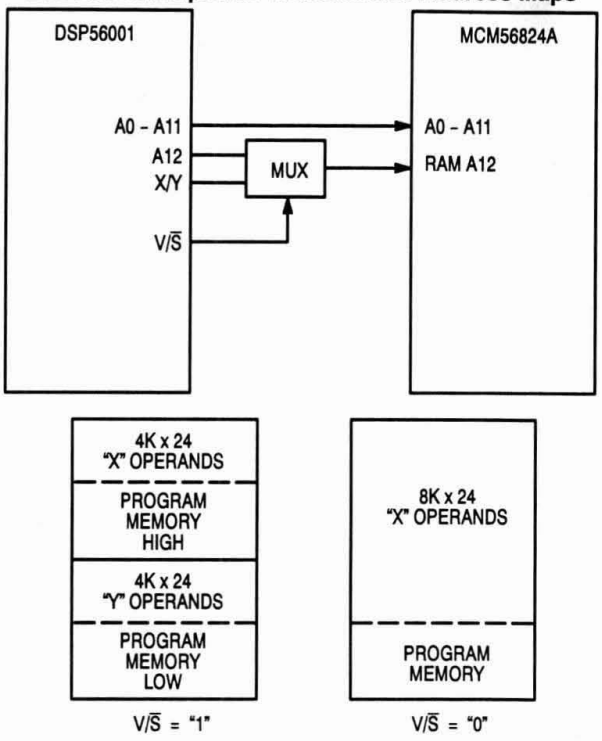
Parameter	Symbol	MCM56824A–20		MCM56824A–25		MCM56824A–35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	35	—	ns	
Address Setup Time	t_{AVE1L} t_{AVE2H}	0	—	0	—	0	—	ns	2
MUX Control Setup Time	t_{VSVE1L} t_{VSVE2H}	0	—	0	—	0	—	ns	2
Address Valid to End of Write	t_{AVE1H} t_{AVE2L}	15	—	20	—	30	—	ns	2
MUX Control Valid to End of Write	t_{VSVE1H} t_{VSVE2L}	15	—	20	—	30	—	ns	2
Chip Enable to End of Write	t_{E1LE1H} t_{E2HE2L}	12	—	15	—	20	—	ns	2, 3
Data Valid to End of Write	t_{DVE1H} t_{DVE2L}	8	—	10	—	15	—	ns	2
Data Hold Time	t_{E1HDX} t_{E2LDX}	0	—	0	—	0	—	ns	2, 4
Write Recovery Time	t_{E1HAX} t_{E2LAX}	0	—	0	—	0	—	ns	2
MUX Control Recovery Time	t_{E1HVSX} t_{E2LVSX}	0	—	0	—	0	—	ns	2

NOTES:
1. A write cycle starts at the latest transition of $\overline{E1}$ low, $\overline{W}$ low, or E2 high. A write cycle ends at the earliest transition of $\overline{E1}$ high, $\overline{W}$ high, or E2 low.
2. $\overline{E1}$ in the timing diagrams represents both $\overline{E1}$ and E2 with $\overline{E1}$ asserted low and E2 asserted high.
3. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high the outputs will remain in a high–impedance state.
4. During this time the output pins may be in the output state. Signals of opposite phase must not be applied to the outputs at this time.

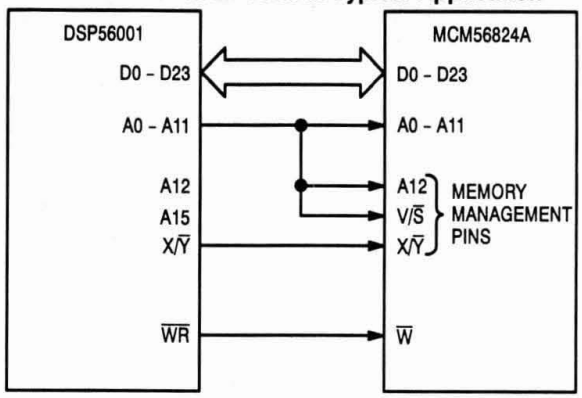
$\overline{E1}$ OR E2 INITIATED WRITE CYCLE



DSPRAM Multiplexed Vector/Scalar Address Maps



8K x 24 DSPRAM Used in Typical Application



2

ORDERING INFORMATION
(Order by Full Part Number)

MCM 56824A XX XX XX

Motorola Memory Prefix

Part Number

Shipping Method (R2 = Tape and Reel, Blank = rails)

Speed (20 = 20 ns, 25 = 25 ns, 35 = 35 ns)

Package (FN = PLCC, ZP = PBGA)

Full Part Numbers —	MCM56824AFN20	MCM56824AFN25	MCM56824AFN35
	MCM56824AZP20	MCM56824AZP25	MCM56824AZP35
	MCM56824AZP20R2	MCM56824AZP25R2	MCM56824AZP35R2

Late Write FSRAMs

3

256K x 18

3.3 V MCM69R818 3–3
3.3 V MCM69R818A 3–22
3.3 V MCM69R819 3–41
3.3 V MCM69R819A 3–59
3.3 V MCM69R820 3–77
3.3 V MCM69R820A 3–95
3.3 V MCM69R821A 3–113
3.3 V MCM69L818 3–135
3.3 V MCM69L818A 3–154
3.3 V MCM69L819 3–173
3.3 V MCM69L819A 3–191
3.3 V MCM69L820 3–209
3.3 V MCM69L820A 3–227

128K x 36

3.3 V MCM69R736 3–3
3.3 V MCM69R736A 3–22
3.3 V MCM69R737 3–41
3.3 V MCM69R737A 3–59
3.3 V MCM69R738 3–77
3.3 V MCM69R738A 3–95
3.3 V MCM69R739A 3–113
3.3 V MCM69L736 3–135
3.3 V MCM69L736A 3–154
3.3 V MCM69L737 3–173
3.3 V MCM69L737A 3–191
3.3 V MCM69L738 3–209
3.3 V MCM69L738A 3–227

64K x 18

3.3 V MCM69R618 3–245
3.3 V MCM69R619 3–264
3.3 V MCM69R620 3–283
3.3 V MCM69R621 3–302
3.3 V MCM69L618 3–324
3.3 V MCM69L619 3–343
3.3 V MCM69L620 3–362

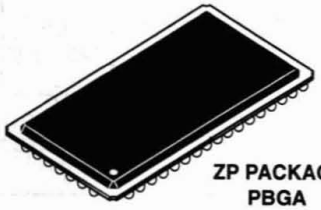
32K x 36

3.3 V MCM69R536 3–245
3.3 V MCM69R537 3–264
3.3 V MCM69R538 3–283
3.3 V MCM69R539 3–302
3.3 V MCM69L536 3–324
3.3 V MCM69L537 3–343
3.3 V MCM69L538 3–362

MCM69R736
MCM69R818

Advance Information

4M Late Write HSTL



ZP PACKAGE
PBGA
CASE 999–01

3

The MCM69R736/818 is a 4 megabit synchronous late write fast static RAM designed to provide high performance in secondary cache and ATM switch, Telecom, and other high speed memory applications. The MCM69R818 organized as 256K words by 18 bits, and the MCM69R736 organized as 128K words by 36 bits wide are fabricated in Motorola's high performance silicon gate BiCMOS technology.

The differential CK clock inputs control the timing of read/write operations of the RAM. At the rising edge of the CK clock all addresses, write enables, and synchronous selects are registered. An internal buffer and special logic enable the memory to accept write data on the rising edge of the CK clock a cycle after address and control signals. Read data is driven on the rising edge of the CK clock also.

The RAM uses HSTL inputs and outputs. The adjustable input trip – point (V_{ref}) and output voltage (V_{DDQ}) gives the system designer greater flexibility in optimizing system performance.

The synchronous write and byte enables allow writing to individual bytes or the entire word.

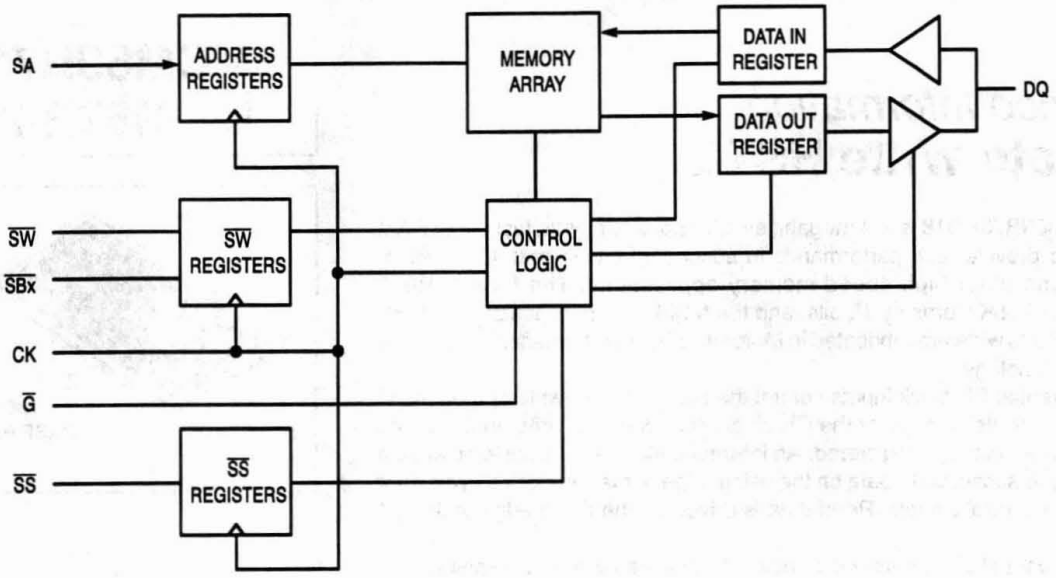
The impedance of the output buffers is programmable allowing the outputs to match the impedance of the circuit traces which reduces signal reflections.

- Byte Write Control
- Single 3.3 V + 10%, – 5% Operation
- HSTL – I/O (JEDEC Standard JESD8–6 Class I and Class II Compatible)
- HSTL – User Selectable Input Trip–Point
- HSTL – Compatible Programmable Impedance Output Drivers
- Register to Register Synchronous Operation
- Asynchronous Output Enable
- Boundary Scan (JTAG) IEEE 1149.1 Compatible
- Differential Clock Inputs
- Optional x 18 or x 36 organization
- MCM69R736/818–7 = 7 ns
  MCM69R736/818–8 = 8 ns
- 119 Bump, 50 mil (1.27 mm) Pitch, 14 mm x 22 mm Plastic Ball Grid Array (PBGA) Package

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 1
4/2/97

FUNCTIONAL BLOCK DIAGRAM



3

PIN ASSIGNMENTS

TOP VIEW

MCM69R736

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	SA	NC	SA	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQc	DQc	V_{SS}	ZQ	V_{SS}	DQb	DQb
E	DQc	DQc	V_{SS}	$\overline{SS}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{G}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{SBc}$	NC	$\overline{SBb}$	DQb	DQb
H	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	V_{ref}	V_{DD}	V_{ref}	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CK	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{SBd}$	$\overline{CK}$	$\overline{SBa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{SW}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
P	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
R	NC	SA	V_{SS}	V_{DD}	V_{DD}	SA	NC
T	NC	NC	SA	SA	SA	NC	NC
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69R818

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	SA	NC	SA	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQb	NC	V_{SS}	ZQ	V_{SS}	DQa	NC
E	NC	DQb	V_{SS}	$\overline{SS}$	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	$\overline{SBb}$	NC	V_{SS}	NC	DQa
H	DQb	NC	V_{SS}	NC	V_{SS}	DQa	NC
J	V_{DDQ}	V_{DD}	V_{ref}	V_{DD}	V_{ref}	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	CK	V_{SS}	NC	DQa
L	DQb	NC	V_{SS}	$\overline{CK}$	$\overline{SBa}$	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{SW}$	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	SA	V_{SS}	DQa	NC
P	NC	DQb	V_{SS}	SA	V_{SS}	NC	DQa
R	NC	SA	V_{SS}	V_{DD}	V_{DD}	SA	NC
T	NC	SA	SA	NC	SA	SA	NC
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69R736 PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6K, 7K, 6L, 7L, 6M, 6N, 7N, 6P, 7P (b) 6D, 7D, 6E, 7E, 6F, 6G, 7G, 6H, 7H (c) 1D, 2D, 1E, 2E, 2F, 1G, 2G, 1H, 2H (d) 1K, 2K, 1L, 2L, 2M, 1N, 2N, 1P, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 3T, 4T, 5T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 5G, 3G, 3L (a), (b), (c), (d)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
4D	ZQ	Input	Programmable Output Impedance: Programming pin.
3J, 5J	V_{ref}	Supply	Input Reference: provides reference voltage for input buffers.
4C, 2J, 4J, 6J, 4R, 5R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 3H, 5H, 3K, 5K, 3M, 5M, 3N, 5N, 3P, 5P, 3R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 4B, 6B, 7B, 1C, 7C, 4G, 4H, 1R, 7R, 1T, 2T, 6T, 7T, 6U	NC	—	No Connection: There is no connection to the chip.

MCM69R818 PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6D, 7E, 6F, 7G, 6H, 7K, 6L, 6N, 7P (b) 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 2T, 3T, 5T, 6T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 3G (a), (b)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
4D	ZQ	Input	Programmable Output Impedance: Programming pin.
4C, 2J, 4J, 6J, 4R, 5R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3J, 5J	V_{ref}	Supply	Input Reference: provides reference voltage for input buffers.
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P, 3R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 4B, 6B, 7B, 1C, 7C, 2D, 7D, 1E, 6E, 2F, 1G, 4G, 6G, 2H, 4H, 7H, 1K, 6K, 2L, 7L, 6M, 2N, 7N, 1P, 6P, 1R, 7R, 1T, 4T, 7T, 6U	NC	—	No Connection: There is no connection to the chip.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS}, See Note 1)

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Output Supply Voltage	V_{DDQ}	– 0.5 to V_{DD} + 0.5	V
Voltage On Any Pin	V_{in}	– 0.5 to V_{DD} + 0.5	V
Input Current (per I/O)	I_{in}	± 50	mA
Output Current (per I/O)	I_{out}	± 70	mA
Power Dissipation (See Note 2)	P_D	—	W
Operating Temperature	T_A	0 to + 70	°C
Temperature Under Bias	T_{bias}	–10 to + 85	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability will be dependent upon package characteristics and use environment. See enclosed thermal impedance data.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

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PBGA PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (Still Air)		$R_{\theta JA}$	53	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Single Layer Board	$R_{\theta JA}$	38	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Four Layer Board	$R_{\theta JA}$	22	°C/W	
Junction to Board (Bottom)		$R_{\theta JB}$	14	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	5	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(0 °C ≤ T_A ≤ 70 °C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (See Notes 1 through 4)

Parameter		Symbol	Min	Typ–7	Typ–8	Max	Unit	Notes
Core Power Supply Voltage		V_{DD}	3.15	—	—	3.6	V	
Output Driver Supply Voltage		V_{DDQ}	1.4	—	—	1.6	V	
Input Reference DC Voltage		V_{ref} (dc)	0.6	—	—	1.1	V	10
Active Power Supply Current	(x18) (x36)	I_{DD1}	— —	300 390	290 370	400 490	mA	5
Quiescent Active Power Supply Current		I_{DD2}	—	190	190	250	mA	6
Active Standby Power Supply Current		I_{SB1}	—	150	150	250	mA	7
Quiescent Standby Power Supply Current		I_{SB2}	—	140	140	230	mA	8

NOTES:
1. All data sheet parameters specified to full range of V_{DD} unless otherwise noted. All voltages are referenced to voltage applied to V_{SS} bumps.
2. Supply voltage applied to V_{DD} connections.
3. Supply voltage applied to V_{DDQ} connections when using the RAM in push–pull output configuration.
4. All power supply currents measured with outputs open or deselected.
5. V_{DD} = V_{DD} (max), t_{KHKH} = t_{KHKH} (min), $\overline{SS}$ registered active, 50% read cycles.
6. V_{DD} = V_{DD} (max), t_{KHKH} = dc, $\overline{SS}$ registered active.
7. V_{DD} = V_{DD} (max), t_{KHKH} = t_{KHKH} (min), $\overline{SS}$ registered inactive, ZZ low.
8. V_{DD} = V_{DD} (max), t_{KHKH} = dc, $\overline{SS}$ registered inactive, ZZ high.
9. 200 mV ≥ V_{in} ≥ V_{DDQ} – 200 mV.
10. Although considerable latitude in the selection of the nominal dc value (i.e., rms value) of V_{ref} is supported, the peak to peak ac component superimposed on V_{ref} may not exceed 5% of the dc component of V_{ref}.

DC INPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
DC Input Logic High	V_{IH} (dc)	V_{ref} + 0.1	V_{DD} + 0.3	V	
DC Input Logic Low	V_{IL} (dc)	– 0.3	V_{ref} – 0.1	V	1
Input Leakage Current	$I_{lkg(1)}$	—	± 5	µA	2
Clock Input Signal Voltage	V_{in}	– 0.3	V_{DD} + 0.3	V	
Clock Input Differential Voltage	V_{DIF} (dc)	0.2	V_{DD} + 0.6	V	3
Clock Input Common Mode Voltage Range (See Figure 2)	V_{CM} (dc)	0.68	1.1	V	4
Clock Input Crossing Point Voltage Range (See Figure 2)	V_X	0.68	1.1	V	

NOTES:
1. Inputs may undershoot to –0.5 V (peak) for up to 20% t_{KHKH} (e.g., 2 ns at a clock cycle time of 10 ns).
2. 0 V ≤ V_{in} ≤ V_{DDQ} for all pins.
3. Minimum instantaneous differential input voltage required for differential input clock operation.
4. Maximum rejectable common mode input voltage variation.

DC OUTPUT BUFFER CHARACTERISTICS – PROGRAMMABLE IMPEDANCE PUSH–PULL OUTPUT BUFFER MODE

(0 °C ≤ T_A ≤ 70 °C, ZQ = I_{ZQ} (out) (RQ)) (See Notes 5 and 6)

Parameter	Symbol	Min	Max	Unit	Notes
Output Logic Low	V_{OL}	V_{DDQ}/2 – 0.025	V_{DDQ}/2 +0.025	V	1
Output Logic High	V_{OH}	V_{DDQ}/2 – 0.025	V_{DDQ}/2 + 0.025	V	2
Light Load Output Logic Low	$V_{OL}1$	V_{SS}	0.2	V	3
Light Load Output Logic High	$V_{OH}1$	V_{DDQ} – 0.2	V_{DDQ}	V	4

NOTES:
1. I_{OL} = (V_{DDQ}/2)/(RQ/5) for values of RQ = 175 Ω ≤ RQ ≤ 350 Ω.
2. | I_{OH} | = (V_{DDQ}/2)/(RQ/5) for values of RQ = 175 Ω ≤ RQ ≤ 350 Ω.
3. I_{OL} ≤ 100 µA
4. | I_{OH} | ≤ 100 µA
5. The impedance controlled mode is expected to be used in point–to–point applications, driving high impedance inputs.
6. The ZQ pin is connected through RQ to V_{SS} for the controlled impedance mode.

PROGRAMMABLE IMPEDANCE OUTPUT BUFFER OPERATION

The output impedance is programmed by a resistor (RQ) attached between the ZQ pin and V_{SS}. RQ's value is five times the programmed impedance. For example, 250 Ω is required for an output impedance of 50 Ω.

Impedance updates occur early in cycles that do not activate the outputs, such as deselect cycles.

Impedance updates occur approximately every 32 clock cycles (CK clock). All clock cycles are counted. For example, after 32 + 1 contiguous read cycles have occurred, an impedance update will occur the next time $\overline{SS}$ is high or $\overline{SW}$ is low at the rising edge of CK clock.

DC OUTPUT BUFFER CHARACTERISTICS – MINIMUM IMPEDANCE PUSH–PULL OUTPUT BUFFER MODE

(0 °C ≤ T_A ≤ 70 °C, ZQ = V_{DD}) (See Notes 5 and 6)

Parameter	Symbol	Min	Max	Unit	Notes
Output Logic Low	$V_{OL}2$	V_{SS}	0.4	V	1
Output Logic High	$V_{OH}2$	V_{DDQ} – 0.4	V_{DDQ}	V	2
Light Load Output Logic Low	$V_{OL}3$	V_{SS}	0.2	V	3
Light Load Output Logic High	$V_{OH}3$	V_{DDQ} – 0.2	V_{DDQ}	V	4

NOTES:

1. I_{OL} ≤ 20 mA
2. $I\ I_{OH}\ I$ ≤ 20 mA
3. I_{OL} ≤ 100 µA
4. $I\ I_{OH}\ I$ ≤ 100 µA
5. The push–pull output mode is expected to be used in bussed applications and may be series or parallel terminated. Conforms to the JEDEC Standard JESD8–6 Class II.
6. The ZQ pin is connected to V_{DD} to enable the minimum impedance mode.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, 0 °C ≤ T_A ≤ 70 °C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	5	5	pF
Input/Output Capacitance	$C_{I/O}$	6	8	pF
CK, $\overline{CK}$ Capacitance	C_{CK}	6	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(0 °C ≤ T_A ≤ 70 °C, Unless Otherwise Noted)

Input Pulse Levels ..... 0.25 to 1.25 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 0.75 V
Output Timing Reference Level ..... 0.75 V
Clock Input Timing Reference Level ..... Differential Cross–Point
ZQ for 50 Ω Impedance ..... 250 Ω

READ/WRITE CYCLE TIMING (See Note 3)

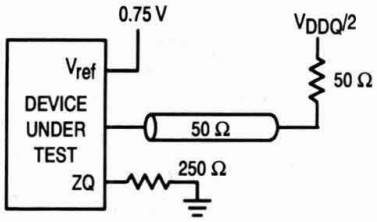
Parameter	Symbol	MCM69R736–7 MCM69R818–7		MCM69R736–8 MCM69R818–8		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{KHKH}	7	—	8	—	ns	
Clock High Pulse Width	t_{KHKL}	2.8	—	3.2	—	ns	
Clock Low Pulse Width	t_{KLKH}	2.8	—	3.2	—	ns	
Clock High to Output Low–Z	t_{KHQX1}	1	—	1	—	ns	2
Clock High to Output Valid	t_{KHQV}	—	3.5	—	4	ns	1
Clock High to Output Hold	t_{KHQX}	0.5	—	0.5	—	ns	1
Clock High to Output High–Z	t_{KHQZ}	0	3.5	0	4	ns	2
Output Enable Low to Output Low–Z	t_{GLQX}	0.5	—	0.5	—	ns	2
Output Enable Low to Output Valid	t_{GLQV}	—	3.5	—	4	ns	1
Output Enable to Output Hold	t_{GHQX}	0.5	—	0.5	—	ns	1
Output Enable High to Output High–Z	t_{GHQZ}	—	3.5	—	4	ns	2
Setup Times: Address, Data In, Chip Select, Write Enable	t_{AVKH}, t_{DVKH}, t_{SVKH}, t_{WVKH}	0.5	—	0.5	—	ns	
Hold Times: Address, Data In, Chip Select, Write Enable	t_{KHAX}, t_{KHDX}, t_{KHSX}, t_{KHWX}	1	—	1	—	ns	

NOTES:
1. Tested per AC Test Load diagram. See Figure 1.
2. Measured at ± 200 mV from steady state.
3. In no case may control input signals (e.g., $\overline{SS}$) be operated with pulse widths less than the minimum clock input pulse width specifications (e.g. t_{KHKL}) or at frequencies that exceed the applied K clock frequency.

AC INPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Note
AC Input Logic High (See Figure 4)	V_{IH} (ac)	V_{ref}+200 mV		
AC Input Logic Low (See Figures 2 and 4)	V_{IL} (ac)		V_{ref} – 200 mV	1
Input Reference Peak to Peak ac Voltage	V_{ref} (ac)		5% V_{ref} (dc)	2
Clock Input Differential Voltage	V_{dif} (ac)	400 mV	V_{DDQ} + 600 mV	3

NOTES:
1. Inputs may undershoot to – 0.5 V (peak) for up to 20% t_{KHKH} (e.g., 2 ns at a clock cycle time of 10 ns).
2. Although considerable latitude in the selection of the nominal dc value (i.e., rms value) of V_{ref} is supported, the peak to peak ac component superimposed on V_{ref} may not exceed 5% of the dc component of V_{ref}.
3. Minimum instantaneous differential input voltage required for differential input clock operation.



TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Figure 1. Test Load

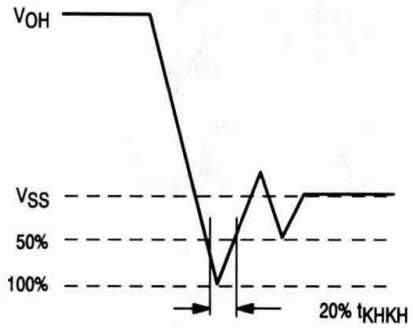
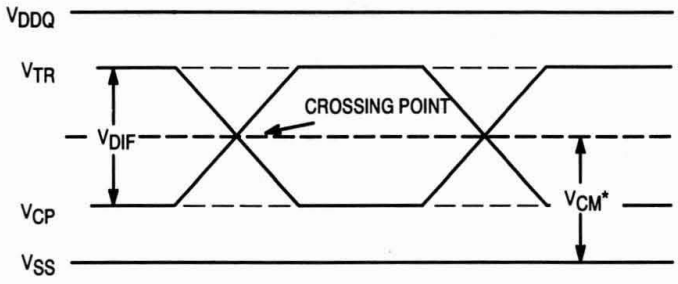


Figure 2. Undershoot Voltage



*V_{CM}, the Common Mode Input Voltage, equals $V_{TR} - ((V_{TR} - V_{CP})/2)$.

Figure 3. Differential Inputs/Common Mode Input Voltage

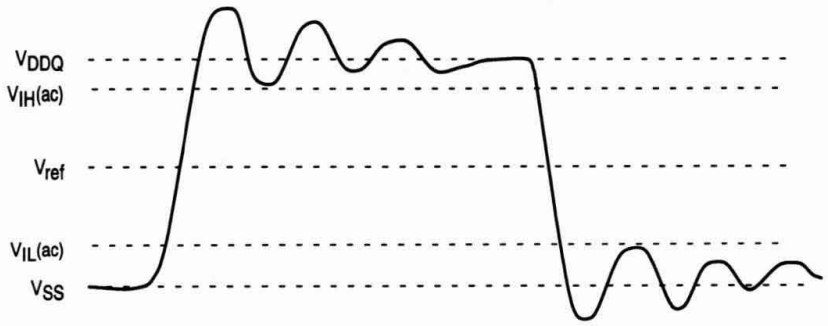
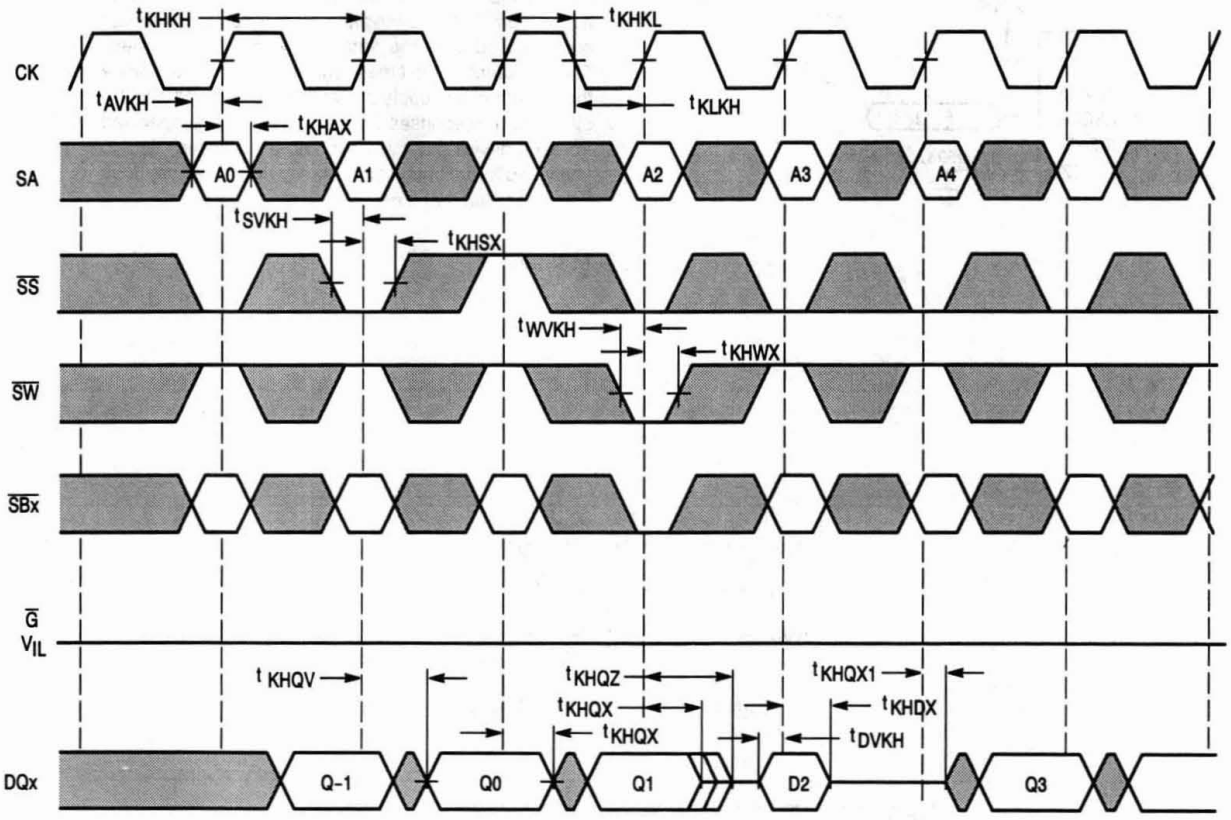
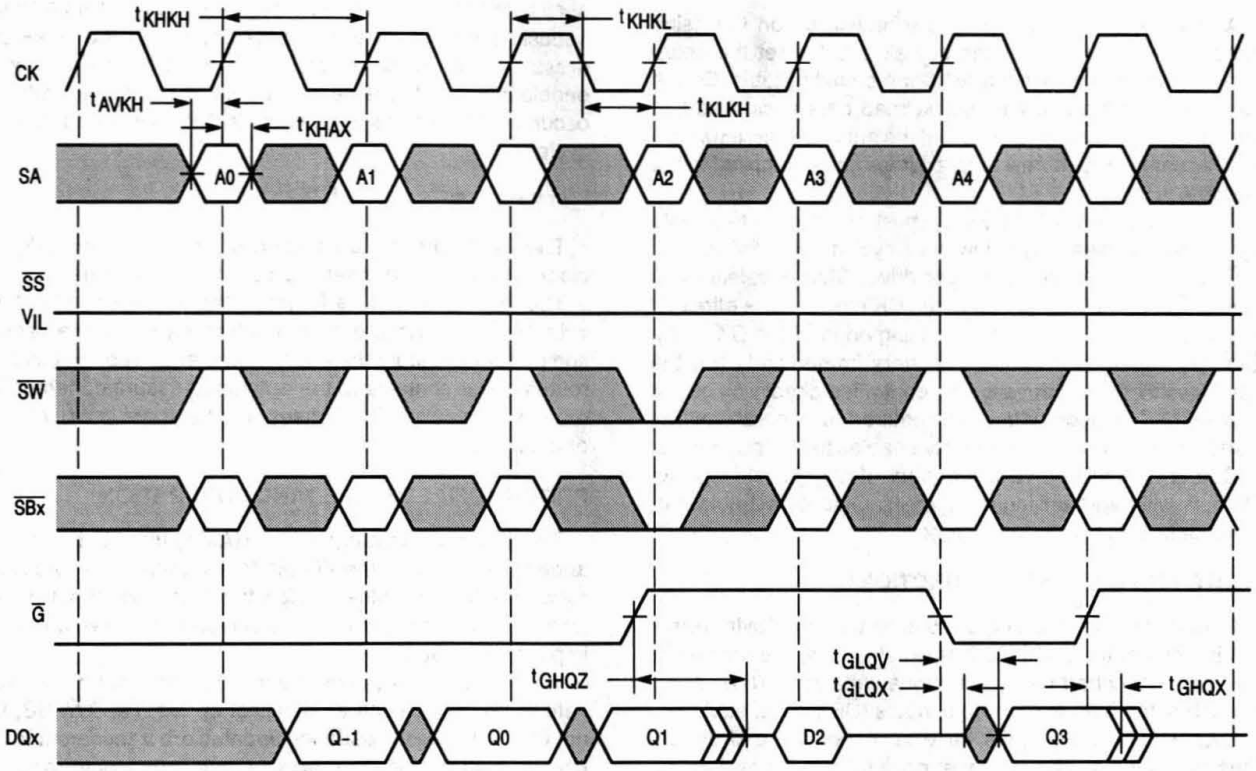


Figure 4. AC Input Conditions

REGISTER/REGISTER READ–WRITE–READ CYCLES



REGISTER/REGISTER READ–WRITE–READ
($\overline{G}$ Controlled)



3

FUNCTIONAL OPERATION

READ AND WRITE OPERATIONS

All control signals except $\overline{G}$ are registered on the rising edge of the CK clock. These signals must meet the setup and hold times shown in the AC Characteristics table. On the rising edge of the following clock, read data is clocked into the output register and available at the outputs at t_{KHQV}. During this same cycle a new read address can be applied to the address pins.

A deselect cycle (dead cycle) must occur prior to a write cycle. Read cycles may follow write cycles immediately.

$\overline{G}$, $\overline{SS}$, and $\overline{SW}$ control output drive. Chip deselect via a high on $\overline{SS}$ at the rising edge of the CK clock has its effect on the output drivers after the next rising edge of the CK clock. $\overline{SW}$ low deselects the output drivers immediately (on the same cycle). Output drive is also controlled directly by output enable, $\overline{G}$. No clock edges are required to generate output disable with $\overline{G}$. $\overline{G}$ asynchronously enables the output drivers.

Output data will be valid the latter of t_{GLQV} and t_{KHQV}. Outputs will begin driving at t_{KHQX1}. Outputs will hold previous data until t_{KHQX} or t_{GHQX}.

WRITE AND BYTE WRITE FUNCTIONS

Note that in the following discussion the term "byte" refers to nine bits of the RAM I/O bus. In all cases, the timing parameters described for synchronous write input ($\overline{SW}$) apply to each of the byte write enable inputs ($\overline{SBa}$, $\overline{SBb}$, etc.).

Byte write enable inputs have no effect on read cycles. This allows the system designer not interested in performing byte writes to connect the byte enable inputs to active low (V_{SS}). Reads of all bytes proceed normally and write cycles, activated via a low on $\overline{SW}$, and the rising edge of the CK clock, write the entire RAM I/O width. This way the designer is spared having to drive multiple write input buffer loads.

Byte writes are performed using the byte write enable inputs in conjunction with the synchronous write input ($\overline{SW}$). It is important to note that writing any one byte will inhibit a read of all bytes at the current address. The RAM cannot simultaneously read one byte and write another at the same address. A write cycle initiated with none of the byte write enable inputs active is neither a read or a write. No write will occur, but the outputs will be deselected as in a normal write cycle.

LATE WRITE

The write address is sampled on the first rising edge of clock and write data is sampled on the following rising edge.

The late write feature is implemented with single stage write buffering. Write buffering is transparent to the user. A comparator monitors the address bus and, when necessary, routes buffer contents to the outputs to assure coherent operation. This occurs in all cases whether there is a byte write or a full word is written.

PROGRAMMABLE IMPEDANCE OPERATION

The designer can program the RAMs output buffer impedance by terminating the ZQ pin to V_{SS} through a precision resistor (RQ). The value of RQ is five times the output impedance desired. For example, 250 Ω resistor will give an output impedance of 50 Ω.

Impedance updates occur early in cycles that do not activate the outputs, such as deselect cycles, i.e. $\overline{SW}$, $\overline{SS}$, but not $\overline{G}$. In all cases impedance updates are transparent to the user and do not produce access time "push–outs" or other anomalous behavior in the RAM.

The output buffers can also be programmed in a minimum impedance configuration. The output buffers have an output impedance similar to standard LVTTL outputs but maintain V_{DDQ} and V_{SS} as the maximum output voltages.

SERIAL BOUNDARY SCAN TEST ACCESS PORT OPERATION

OVERVIEW

The serial boundary scan test access port (TAP) on this RAM is designed to operate in a manner consistent with IEEE Standard 1149.1–1990 (commonly referred to as JTAG), but does not implement all of the functions required for 1149.1 compliance. Certain functions have been modified or eliminated because their implementation places extra delays in the RAMs critical speed path. Nevertheless, the RAM supports the standard TAP controller architecture. (The TAP controller is the state machine that controls the TAPs operation) and can be expected to function in a manner that does not conflict with the operation of devices with Standard 1149.1 compliant TAPs. The TAP operates using conventional JEDEC Standard 8–1B Low Voltage (3.3 V) TTL / CMOS logic level signaling.

DISABLING THE TEST ACCESS PORT

It is possible to use this device without utilizing the TAP. To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid level inputs. TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a 1 k resistor. TDO should be left unconnected.

3

TAP DC OPERATING CHARACTERISTICS

(0 °C ≤ T_A ≤ 70 °C, Unless Otherwise Noted)

Parameter	Symbol	Min	Max	Unit	Note
Logic Input Logic High	$V_{IH}1$	2.0	V_{DD} + 0.3	V	
Logic Input Logic Low	$V_{IL}1$	– 0.3	0.8	V	
Logic Input Leakage Current	I_{lkg}	—	± 5	µA	1
CMOS Output Logic Low	$V_{OL}1$	—	0.2	V	2
CMOS Output Logic High	$V_{OH}1$	V_{DD} – 0.2	—	V	3
TTL Output Logic Low	$V_{OL}2$	—	0.4	V	4
TTL Output Logic High	$V_{OH}2$	2.4	—	V	5

NOTES:
1. 0 V ≤ V_{in} ≤ V_{DDQ} for all logic input pins.
2. $I_{OL}1$ ≤ 100 µA @ V_{OL} = 0.2 V. Sampled, not 100% tested.
3. $|I_{OH}1|$ ≤ 100 µA @ V_{DDQ}–0.2 V. Sampled, not 100% tested.
4. $I_{OL}2$ ≤ 8 mA @ V_{OL} = 0.4 V
5. $|I_{OH}2|$ ≤ 8 mA @ V_{OH} = 2.4 V

TAP AC OPERATING CONDITIONS AND CHARACTERISTICS

(0 °C ≤ T_A ≤ 70 °C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V

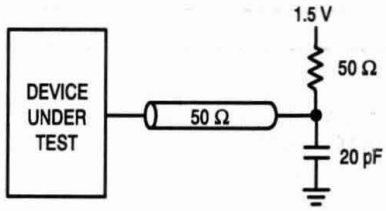
Output Test Load ..... 50 Ω Parallel Terminated T–line with 20 pF Receiver Input Capacitance
Test Load Termination Supply Voltage (V_T) ..... 1.5 V

TAP CONTROLLER TIMING

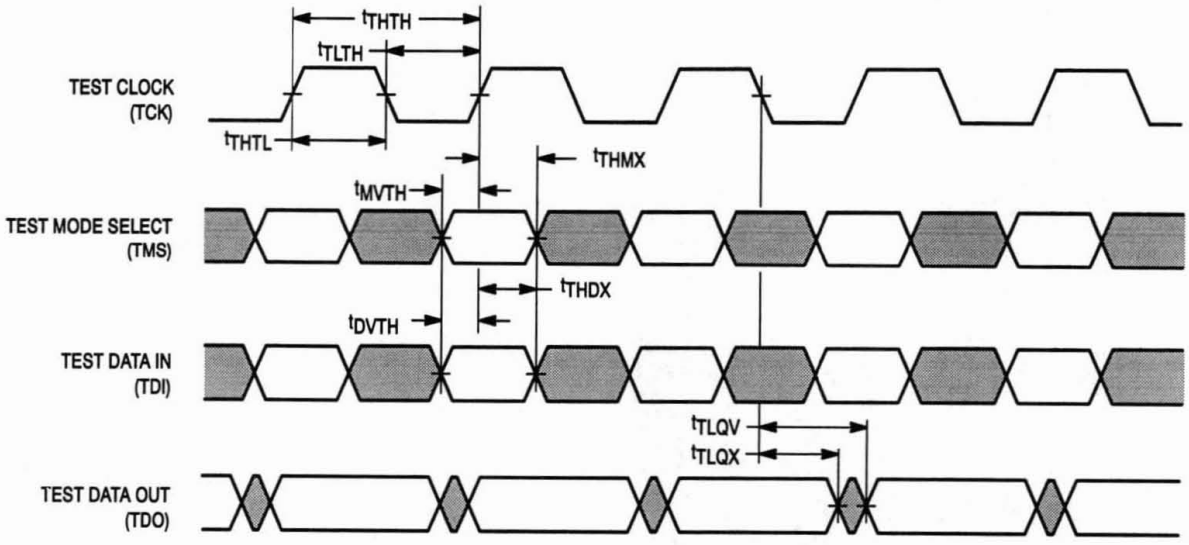
Parameter	Symbol	Min	Max	Unit	Notes
Cycle Time	t_{THTH}	100	—	ns	
Clock High Time	t_{THTL}	40	—	ns	
Clock Low Time	t_{TLTH}	40	—	ns	
TMS Setup	t_{MVTH}	10	—	ns	
TMS Hold	t_{THMX}	10	—	ns	
TDI Valid to TCK High	t_{DVTH}	10	—	ns	
TCK High to TDI Don't Care	t_{THDX}	10	—	ns	
Capture Setup	t_{CS}	10	—	ns	1
Capture Hold	t_{CH}	10	—	ns	1
TCK Low to TDO Unknown	t_{TLQX}	0	—	ns	
TCK Low to TDO Valid	t_{TLOV}	—	20	ns	

NOTES:
1. t_{CS} + t_{CH} defines the minimum pause in RAM I/O pad transitions to assure accurate pad data capture.

AC TEST LOAD



TAP CONTROLLER TIMING DIAGRAM



TEST ACCESS PORT PINS

TCK – TEST CLOCK (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

TMS – TEST MODE SELECT (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.

TDI – TEST DATA IN (INPUT)

The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (refer to Figure 6 TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.

TDO – TEST DATA OUT (OUTPUT)

Output that is active depending on the state of the TAP state machine (refer to Figure 6 TAP Controller State Diagram). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

TRST – TAP RESET

This device does not have a TRST pin. TRST is optional in **IEEE 1149.1.** The test–logic reset state is entered while TMS is held high for five rising edges of TCK. Power on reset circuitry is included internally. This type of reset does not affect the operation of the system logic. The reset affects test logic only.

TEST ACCESS PORT REGISTERS

OVERVIEW

The various TAP registers are selected (one at a time) via the sequences of ones and zeros input to the TMS pin as the TCK is strobed. Each of the TAPs registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on subsequent falling edge of TCK. When a register is selected it is "placed" between the TDI and TDO pins.

INSTRUCTION REGISTER

The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run test/idle or the various data register states. The instructions are three bits long. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power–up or whenever the controller is placed in test–logic–reset state.

BYPASS REGISTER

The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.

BOUNDARY SCAN REGISTER

The boundary scan register is identical in length to the number of active input and I/O connections on the RAM (not counting the TAP pins). This also includes a number of place holder locations (always set to a logic 1) reserved for density upgrade address pins. There are a total of 70 bits in the case of the x36 device and 51 bits in the case of the x18 device. The boundary scan register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture–DR state and then is placed between the TDI and TDO pins when the controller is moved to shift–DR state. Several TAP instructions can be used to activate the boundary scan register.

The Bump/Bit Scan Order tables describe which device bump connects to each boundary scan register location. The first column defines the bit's position in the boundary scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the input or I/O at the bump and the third column is the bump number.

IDENTIFICATION (ID) REGISTER

The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture–DR state with the IDCODE command loaded in the instruction register. The code is loaded from a 32 bit on–chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into shift–DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Presence Indicator

Bit #	0
Value	1

Motorola JEDEC ID Code (Compressed Format, per IEEE Standard 1149.1 – 1990

Bit #	11	10	9	8	7	6	5	4	3	2	1
Value	0	0	0	0	0	0	0	1	1	1	0

Reserved For Future Use

Bit #	17	16	15	14	13	12
Value	x	x	x	x	x	x

Device Width

Configuration	Bit #	22	21	20	19	18
128Kx36	Value	0	0	1	0	0
256Kx18	Value	0	0	0	1	1

Device Depth

Configuration	Bit #	27	26	25	24	23
128Kx36	Value	0	0	1	0	1
256Kx18	Value	0	0	1	1	0

Revision Number

Bit #	31	30	29	28
Value	x	x	x	x

Figure 5. ID Register Bit Meanings

MCM69R736 Bump/Bit Scan Order

BIT #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	SA	3B
2	SA	4P		37	NC	2B
3	SA	4T		38	SA	3A
4	SA	6R		39	SA	3C
5	SA	5T		40	SA	2C
6	NC	7T		41	SA	2A
7	DQa	6P		42	DQc	2D
8	DQa	7P		43	DQc	1D
9	DQa	6N		44	DQc	2E
10	DQa	7N		45	DQc	1E
11	DQa	6M		46	DQc	2F
12	DQa	6L		47	DQc	2G
13	DQa	7L		48	DQc	1G
14	DQa	6K		49	DQc	2H
15	DQa	7K		50	DQc	1H
16	$\overline{SBa}$	5L		51	$\overline{SBc}$	3G
17	$\overline{CK}$	4L		52	ZQ	4D
18	CK	4K		53	$\overline{SS}$	4E
19	$\overline{G}$	4F		54	NC	4G
20	$\overline{SBb}$	5G		55	NC	4H
21	DQb	7H		56	$\overline{SW}$	4M
22	DQb	6H		57	$\overline{SBd}$	3L
23	DQb	7G		58	DQd	1K
24	DQb	6G		59	DQd	2K
25	DQb	6F		60	DQd	1L
26	DQb	7E		61	DQd	2L
27	DQb	6E		62	DQd	2M
28	DQb	7D		63	DQd	1N
29	DQb	6D		64	DQd	2N
30	SA	6A		65	DQd	1P
31	SA	6C		66	DQd	2P
32	SA	5C		67	SA	3T
33	SA	5A		68	SA	2R
34	NC	6B		69	SA	4N
35	SA	5B		70	M1	3R

MCM69R818 Bump/Bit Scan Order

Bit #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	$\overline{SBb}$	3G
2	SA	6T		37	ZQ	4D
3	SA	4P		38	$\overline{SS}$	4E
4	SA	6R		39	NC	4G
5	SA	5T		40	NC	4H
6	NC	7T		41	$\overline{SW}$	4M
7	DQa	7P		42	DQb	2K
8	DQa	6N		43	DQb	1L
9	DQa	6L		44	DQb	2M
10	DQa	7K		45	DQb	1N
11	$\overline{SBa}$	5L		46	DQb	2P
12	$\overline{CK}$	4L		47	SA	3T
13	CK	4K		48	SA	2R
14	$\overline{G}$	4F		49	SA	4N
15	DQa	6H		50	SA	2T
16	DQa	7G		51	M1	3R
17	DQa	6F				
18	DQa	7E				
19	DQa	6D				
20	SA	6A				
21	SA	6C				
22	SA	5C				
23	SA	5A				
24	NC	6B				
25	SA	5B				
26	SA	3B				
27	NC	2B				
28	SA	3A				
29	SA	3C				
30	SA	2C				
31	SA	2A				
32	DQb	1D				
33	DQb	2E				
34	DQb	2G				
35	DQb	1H				

NOTES:

1. The NC pads listed in this table are indeed no connects, but are represented in the boundary scan register by a "place holder" bit that is forced to logic 1. These pads are reserved for use as address inputs on higher density RAMs that follow this pad out and scan order standard.
2. CK, $\overline{CK}$, are sampled individually. $\overline{CK}$ is not simply a forced complement of the CK input. In scan mode these differential inputs are referenced to V_{ref}, not each other.
3. ZQ, M1 and M2 are not ordinary inputs and may not respond to standard I/O logic levels. ZQ, M1 and M2 must be driven to within 100 mV of a V_{DD} or V_{SS} supply rail to ensure consistent results.

TAP Controller Instruction Set

OVERVIEW

There are two classes of instructions defined in the Standard 1149.1–1990; the standard (public) instructions, and device specific (private) instructions. Some public instructions, are mandatory for 1149.1 compliance. Optional public instructions must be implemented in prescribed ways.

Although the TAP controller in this device follows the 1149.1 conventions, it is not 1194.1 compliant because some of the mandatory instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads, but cannot be used to load address, data or control signals into the RAM or to preload the I/O buffers. In other words, the device will not perform Standard 1149.1 EXTEST, INTEST or the preload portion of the SAMPLE / PRELOAD command.

When the TAP controller is placed in capture–IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the shift–IR state the instruction register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to update–IR state. The TAP instruction sets for this device are listed in the following tables.

STANDARD (PUBLIC) INSTRUCTIONS

BYPASS

The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift–DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

Sample/preload is a Standard 1149.1 mandatory public instruction. When the sample / preload instruction is loaded in the Instruction register, moving the TAP controller into the capture–DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set–up plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register.

Moving the controller to shift–DR state then places the boundary scan register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the update–DR state with the SAMPLE / PRELOAD instruction loaded in the instruction register has the same effect as the pause–DR command. This functionality is not Standard 1149.1 compliant.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic 0s. EXTEST is not implemented in this device. Therefore this device is not 1149.1 compliant. Nevertheless, this RAMs TAP does respond to an all zeros instruction, as follows. With the EXTEST (000) instruction loaded in the instruction register the RAM responds just as it does in response to the SAMPLE / PRELOAD instruction described above, except the RAM outputs are forced to high–Z any time the instruction is loaded.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture–DR mode and places the ID register between the TDI and TDO pins in shift–DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test–logic–reset state.

THE DEVICE SPECIFIC (PUBLIC) INSTRUCTION

SAMPLE–Z

If the SAMPLE–Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high–Z) and the boundary scan register is connected between TDI and TDO when the TAP controller. is moved to the shift–DR state.

THE DEVICE SPECIFIC (PRIVATE) INSTRUCTION

NOOP

Do not use these instructions; they are reserved for future use.

STANDARD (PUBLIC) INSTRUCTION CODES

Instruction	Code*	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM outputs to High–Z state. *NOT 1149.1 COMPLIANT*
IDCODE	001**	Preloads ID register and places it between TDI and TDO. Does not affect RAM operation.
SAMPLE / PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect RAM operation. Does not implement 1149.1 Preload function. * NOT 1149.1 COMPLIANT *
BYPASS	111	Places bypass register between TDI and TDO. Does not affect RAM operation.
SAMPLE–Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM output drivers to High–Z.

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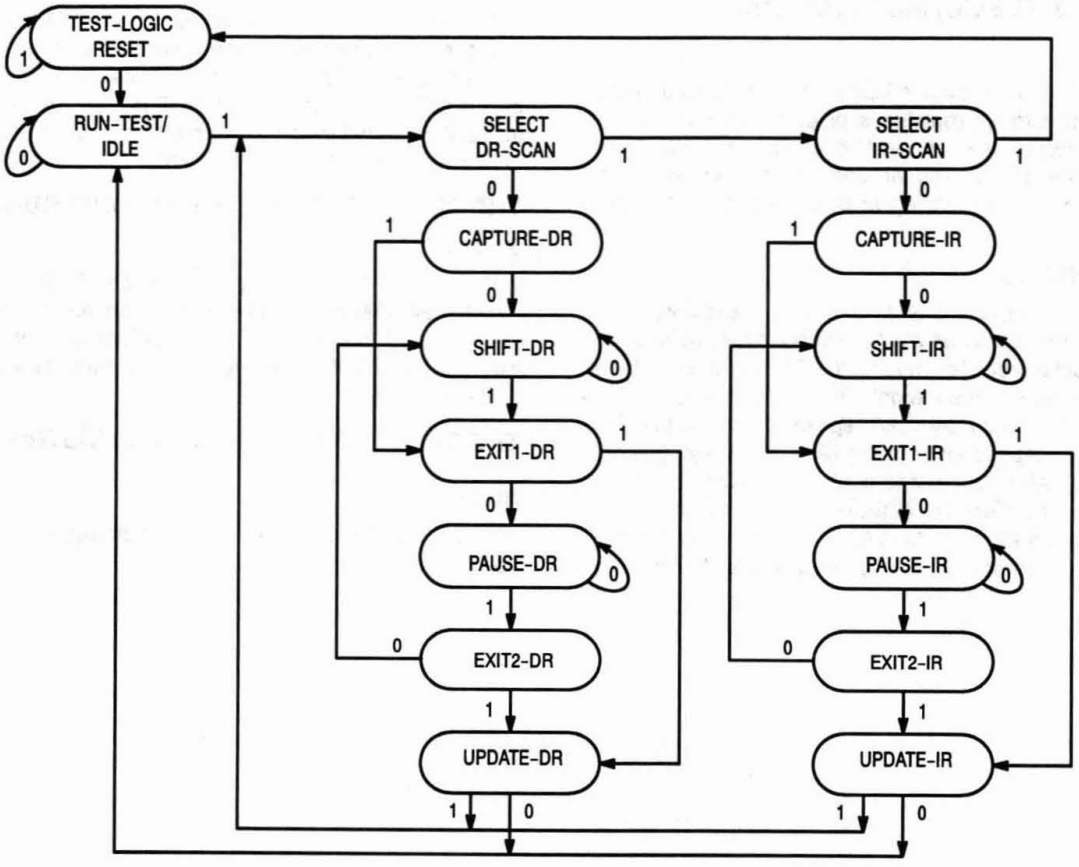
* Instruction codes expressed in binary, MSB on left, LSB on right.
** Default instruction automatically loaded at power–up and in test–logic–reset state.

STANDARD (PRIVATE) INSTRUCTION CODES

Instruction	Code*	Description
NO OP	011	Do not use these instructions; they are reserved for future use.
NO OP	101	Do not use these instructions; they are reserved for future use.
NO OP	110	Do not use these instructions; they are reserved for future use.

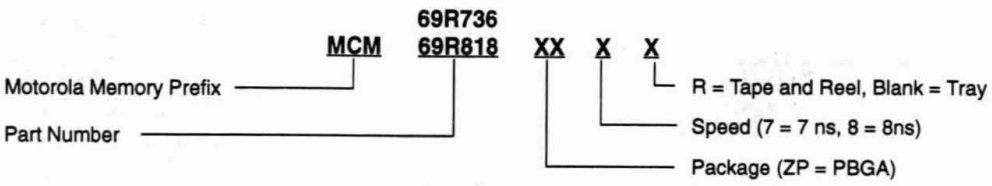
* Instruction codes expressed in binary, MSB on left, LSB on right.



NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 6. TAP Controller State Diagram

ORDERING INFORMATION
(Order by Full Part Number)



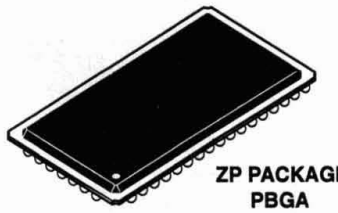
Full Part Numbers —	MCM69R736ZP7	MCM69R736ZP8
	MCM69R818ZP7	MCM69R818ZP8
	MCM69R736ZP7R	MCM69R736ZP8R
	MCM69R818ZP7R	MCM69R818ZP8R

3

MCM69R736A
MCM69R818A

Advance Information

4M Late Write HSTL



ZP PACKAGE
PBGA
CASE 999–01

3

The MCM69R736A/818A is a 4 megabit synchronous late write fast static RAM designed to provide high performance in secondary cache and ATM switch, Telecom, and other high speed memory applications. The MCM69R818A organized as 256K words by 18 bits, and the MCM69R736A organized as 128K words by 36 bits wide are fabricated in Motorola's high performance silicon gate BiCMOS technology.

The differential CK clock inputs control the timing of read/write operations of the RAM. At the rising edge of the CK clock all addresses, write enables, and synchronous selects are registered. An internal buffer and special logic enable the memory to accept write data on the rising edge of the CK clock a cycle after address and control signals. Read data is driven on the rising edge of the CK clock also.

The RAM uses HSTL inputs and outputs. The adjustable input trip – point (V_{ref}) and output voltage (V_{DDQ}) gives the system designer greater flexibility in optimizing system performance.

The synchronous write and byte enables allow writing to individual bytes or the entire word.

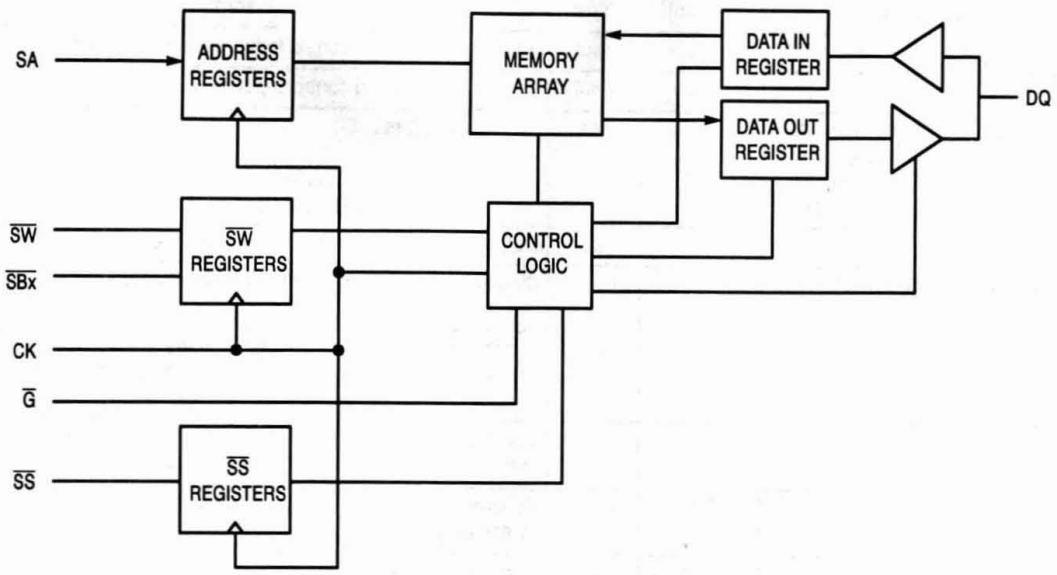
The impedance of the output buffers is programmable allowing the outputs to match the impedance of the circuit traces which reduces signal reflections.

- Byte Write Control
- Single 3.3 V +10%, – 5% Operation
- HSTL – I/O (JEDEC Standard JESD8–6 Class I and Class II Compatible)
- HSTL – User Selectable Input Trip–Point
- HSTL – Compatible Programmable Impedance Output Drivers
- Register to Register Synchronous Operation
- Asynchronous Output Enable
- Boundary Scan (JTAG) IEEE 1149.1 Compatible
- Differential Clock Inputs
- Optional x 18 or x 36 organization
- MCM69R736A/818A–5 = 5 ns
  MCM69R736A/818A–6 = 6 ns
  MCM69R736A/818A–7 = 7 ns
  MCM69R736A/818A–8 = 8 ns
- 119 Bump, 50 mil (1.27 mm) Pitch, 14 mm x 22 mm Plastic Ball Grid Array (PBGA) Package

This document contains information on a new product. Specifications and information herein are subject to change without notice.

4/2/97

FUNCTIONAL BLOCK DIAGRAM



3

PIN ASSIGNMENTS

TOP VIEW

MCM69R736A

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	SA	NC	SA	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQc	DQc	V_{SS}	ZQ	V_{SS}	DQb	DQb
E	DQc	DQc	V_{SS}	$\overline{SS}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{G}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{SBc}$	NC	$\overline{SBb}$	DQb	DQb
H	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	V_{ref}	V_{DD}	V_{ref}	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CK	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{SBd}$	$\overline{CK}$	$\overline{SBa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{SW}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
P	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
R	NC	SA	V_{SS}	V_{DD}	V_{DD}	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69R818A

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	SA	NC	SA	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQb	NC	V_{SS}	ZQ	V_{SS}	DQa	NC
E	NC	DQb	V_{SS}	$\overline{SS}$	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	$\overline{SBb}$	NC	V_{SS}	NC	DQa
H	DQb	NC	V_{SS}	NC	V_{SS}	DQa	NC
J	V_{DDQ}	V_{DD}	V_{ref}	V_{DD}	V_{ref}	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	CK	V_{SS}	NC	DQa
L	DQb	NC	V_{SS}	$\overline{CK}$	$\overline{SBa}$	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{SW}$	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	SA	V_{SS}	DQa	NC
P	NC	DQb	V_{SS}	SA	V_{SS}	NC	DQa
R	NC	SA	V_{SS}	V_{DD}	V_{DD}	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69R736A PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6K, 7K, 6L, 7L, 6M, 6N, 7N, 6P, 7P (b) 6D, 7D, 6E, 7E, 6F, 6G, 7G, 6H, 7H (c) 1D, 2D, 1E, 2E, 2F, 1G, 2G, 1H, 2H (d) 1K, 2K, 1L, 2L, 2M, 1N, 2N, 1P, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 3T, 4T, 5T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 5G, 3G, 3L (a), (b), (c), (d)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
4D	ZQ	Input	Programmable Output Impedance: Programming pin.
7T	ZZ	Input	Reserved for future use. Must be grounded.
4C, 2J, 4J, 6J, 4R, 5R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3J, 5J	V_{ref}	Supply	Input Reference: provides reference voltage for input buffers.
3D, 5D, 3E, 5E, 3F, 5F, 3H, 5H, 3K, 5K, 3M, 5M, 3N, 5N, 3P, 5P, 3R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 4B, 6B, 7B, 1C, 7C, 4G, 4H, 1R, 7R, 1T, 2T, 6T, 6U	NC	—	No Connection: There is no connection to the chip.

MCM69R818A PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6D, 7E, 6F, 7G, 6H, 7K, 6L, 6N, 7P (b) 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 2T, 3T, 5T, 6T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 3G (a), (b)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
4D	ZQ	Input	Programmable Output Impedance: Programming pin.
7T	ZZ	Input	Reserved for future use. Must be grounded.
4C, 2J, 4J, 6J, 4R, 5R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3J, 5J	V_{ref}	Supply	Input Reference: provides reference voltage for input buffers.
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P, 3R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 4B, 6B, 7B, 1C, 7C, 2D, 7D, 1E, 6E, 2F, 1G, 4G, 6G, 2H, 4H, 7H, 1K, 6K, 2L, 7L, 6M, 2N, 7N, 1P, 6P, 1R, 7R, 1T, 4T, 6U	NC	—	No Connection: There is no connection to the chip.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS}, See Note 1)

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Output Supply Voltage	V_{DDQ}	– 0.5 to V_{DD} + 0.5	V
Voltage On Any Pin	V_{in}	– 0.5 to V_{DD} + 0.5	V
Input Current (per I/O)	I_{in}	± 50	mA
Output Current (per I/O)	I_{out}	± 70	mA
Power Dissipation (See Note 2)	P_D	—	W
Operating Temperature	T_A	0 to + 70	°C
Temperature Under Bias	T_{bias}	–10 to + 85	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability will be dependent upon package characteristics and use environment. See enclosed thermal impedance data.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

PBGA PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (Still Air)		$R_{\theta JA}$	53	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Single Layer Board	$R_{\theta JA}$	38	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Four Layer Board	$R_{\theta JA}$	22	°C/W	
Junction to Board (Bottom)		$R_{\theta JB}$	14	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	5	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(0 °C ≤ T_A ≤ 70 °C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (See Notes 1 through 4)

Parameter		Symbol	Min	Typical –5	Typical –6	Typical –7	Typical –8	Max	Unit	Notes
Input Reference DC Voltage		V_{ref} (dc)	0.6	—	—	—	—	1.1	V	11
Core Power Supply Voltage		V_{DD}	3.15	—	—	—	—	3.6	V	
Output Driver Supply Voltage		V_{DDQ}	1.4	—	—	—	—	1.6	V	
Active Power Supply Current	(x18) (x36)	I_{DD1}	— —	350 460	330 430	300 390	290 370	450 560	mA	5
Quiescent Active Power Supply Current		I_{DD2}	—	190	190	190	190	250	mA	6, 10
Active Standby Power Supply Current		I_{SB1}	—	160	160	160	160	250	mA	7
Quiescent Standby Power Supply Current		I_{SB2}	—	140	140	140	140	230	mA	8, 10
Sleep Mode Power Supply Current		I_{SB3}	—	TBD	TBD	TBD	TBD	TBD	mA	9, 10

NOTES:

1. All data sheet parameters specified to full range of V_{DD} unless otherwise noted. All voltages are referenced to voltage applied to V_{SS} bumps.
2. Supply voltage applied to V_{DD} connections.
3. Supply voltage applied to V_{DDQ} connections.
4. All power supply currents measured with outputs open or deselected.
5. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered active, 50% read cycles.
6. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered active.
7. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered inactive.
8. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered inactive, ZZ low.
9. $V_{DD} = V_{DD}$ (Max), t_{KHKH} = dc, registered inactive, ZZ high.
10. 200 mV ≥ V_{in} ≥ V_{DDQ} – 200 mV.
11. Although considerable latitude in the selection of the nominal dc value (i.e., rms value) of V_{ref} is supported, the peak to peak ac component superimposed on V_{ref} may not exceed 5% of the dc component of V_{ref}.

DC INPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
DC Input Logic High	V_{IH} (dc)	V_{ref} + 0.1	V_{DD} + 0.3	V	
DC Input Logic Low	V_{IL} (dc)	– 0.3	V_{ref} – 0.1	V	1
Input Leakage Current	$I_{lkg(1)}$	—	± 5	µA	2
Clock Input Signal Voltage	V_{in}	– 0.3	V_{DD} + 0.3	V	
Clock Input Differential Voltage	V_{DIF} (dc)	0.2	V_{DD} + 0.6	V	3
Clock Input Common Mode Voltage Range (See Figure 2)	V_{CM} (dc)	0.68	1.1	V	4
Clock Input Crossing Point Voltage Range (See Figure 2)	V_X	0.68	1.1	V	

NOTES:

1. Inputs may undershoot to –0.5 V (peak) for up to 20% t_{KHKH} (e.g., 2 ns at a clock cycle time of 10 ns).
2. 0 V ≤ V_{in} ≤ V_{DDQ} for all pins.
3. Minimum instantaneous differential input voltage required for differential input clock operation.
4. Maximum rejectable common mode input voltage variation.

DC OUTPUT BUFFER CHARACTERISTICS – PROGRAMMABLE IMPEDANCE PUSH–PULL OUTPUT BUFFER MODE

(0 °C ≤ T_A ≤ 70 °C, ZQ = I_{ZQ} (out) (RQ)) (See Notes 5 and 6)

Parameter	Symbol	Min	Max	Unit	Notes
Output Logic Low	V_{OL}	V_{DDQ}/2 – 0.025	V_{DDQ}/2 + 0.025	V	1
Output Logic High	V_{OH}	V_{DDQ}/2 – 0.025	V_{DDQ}/2 + 0.025	V	2
Light Load Output Logic Low	V_{OL}1	V_{SS}	0.2	V	3
Light Load Output Logic High	V_{OH}1	V_{DDQ} – 0.2	V_{DDQ}	V	4

NOTES:

1. I_{OL} = (V_{DDQ}/2)/(RQ/5) for values of RQ = 175 Ω ≤ RQ ≤ 350 Ω.
2. $|I_{OH}|$ = (V_{DDQ}/2)/(RQ/5) for values of RQ = 175 Ω ≤ RQ ≤ 350 Ω.
3. I_{OL} ≤ 100 µA
4. $|I_{OH}|$ ≤ 100 µA
5. The impedance controlled mode is expected to be used in point–to–point applications, driving high impedance inputs.
6. The ZQ pin is connected through RQ to V_{SS} for the controlled impedance mode.

PROGRAMMABLE IMPEDANCE OUTPUT BUFFER OPERATION

The output impedance is programmed by a resistor (RQ) attached between the ZQ pin and V_{SS}. RQ's value is five times the programmed impedance. For example, 250 Ω is required for an output impedance of 50 Ω.

DC OUTPUT BUFFER CHARACTERISTICS – MINIMUM IMPEDANCE PUSH–PULL OUTPUT BUFFER MODE

(0 °C ≤ T_A ≤ 70 °C, ZQ = V_{DD}) (See Notes 5 and 6)

Parameter	Symbol	Min	Max	Unit	Notes
Output Logic Low	$V_{OL}2$	V_{SS}	0.4	V	1
Output Logic High	$V_{OH}2$	V_{DDQ} – 0.4	V_{DDQ}	V	2
Light Load Output Logic Low	$V_{OL}3$	V_{SS}	0.2	V	3
Light Load Output Logic High	$V_{OH}3$	V_{DDQ} – 0.2	V_{DDQ}	V	4

NOTES:

1. I_{OL} ≤ 16 mA
2. $I\ I_{OH}\ I$≤ 16 mA
3. I_{OL} ≤ 100 µA
4. $I\ I_{OH}\ I$≤ 100 µA
5. The push–pull output mode is expected to be used in bussed applications and may be series or parallel terminated. Conforms to the JEDEC Standard JESD8–6 Class II.
6. The ZQ pin is connected to V_{DD} to enable the minimum impedance mode.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, 0 °C ≤ T_A ≤ 70 °C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	5	pF
Input/Output Capacitance	$C_{I/O}$	7	8	pF
CK, $\overline{CK}$ Capacitance	C_{CK}	4	5	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(0 °C ≤ T_A ≤ 70 °C, Unless Otherwise Noted)

Input Pulse Levels ..... 0.25 to 1.25 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 0.75 V
Output Timing Reference Level ..... 0.75 V
Clock Input Timing Reference Level ..... Differential Cross–Point
ZQ for 50 Ω Impedance ..... 250 Ω

READ/WRITE CYCLE TIMING (See Note 3)

Parameter	Symbol	MCM69R736A–5 MCM69R818A–5		MCM69R736A–6 MCM69R818A–6		MCM69R736A–7 MCM69R818A–7		MCM69R736A–8 MCM69R818A–8		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	5	—	6	—	7	—	8	—	ns	
Clock High Pulse Width	t_{KHKL}	2.4	—	2.4	—	2.8	—	3.2	—	ns	
Clock Low Pulse Width	t_{KLKH}	2.4	—	2.4	—	2.8	—	3.2	—	ns	
Clock High to Output Low–Z	t_{KHQX1}	1	—	1	—	1	—	1	—	ns	2
Clock High to Output Valid	t_{KHQV}	—	2.5	—	3	—	3.5	—	4	ns	1
Clock High to Output Hold	t_{KHQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	2
Clock High to Output High–Z	t_{KHQZ}	—	2.5	—	3	—	3.5	—	4	ns	2
Output Enable Low to Output Low–Z	t_{GLQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	2
Output Enable Low to Output Valid	t_{GLQV}	—	2.5	—	3	—	3.5	—	4	ns	2
Output Enable to Output Hold	t_{GHQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	2
Output Enable High to Output High–Z	t_{GHQZ}	—	2.5	—	3	—	3.5	—	4	ns	2
Setup Times: Address Data In Chip Select Write Enable	t_{AVKH} t_{DVKH} t_{SVKH} t_{WVKH}	0.5	—	0.5	—	0.5	—	0.5	—	ns	
Hold Times: Address Data In Chip Select Write Enable	t_{KHAX} t_{KHDX} t_{KHSX} t_{KHWX}	1	—	1	—	1	—	1	—	ns	

NOTES:
1. Tested per AC Test Load diagram. See Figure 1.
2. Measured at ± 200 mV from steady state.
3. In no case may control input signals (e.g., $\overline{SS}$) be operated with pulse widths less than the minimum clock input pulse width specifications (e.g., t_{KHKL}) or at frequencies that exceed the applied K clock frequency.

AC INPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Note
AC Input Logic High (See Figure 4)	V_{IH} (ac)	V_{ref} + 200 mV		
AC Input Logic Low (See Figures 2 and 4)	V_{IL} (ac)		V_{ref} – 200 mV	1
Input Reference Peak to Peak ac Voltage	V_{ref} (ac)		5% V_{ref} (dc)	2
Clock Input Differential Voltage	V_{dif} (ac)	400 mV	V_{DDQ} + 600 mV	3

NOTES:
1. Inputs may undershoot to –0.5 V (peak) for up to 20% t_{KHKH} (e.g., 2 ns at a clock cycle time of 10 ns).
2. Although considerable latitude in the selection of the nominal dc value (i.e., rms value) of V_{ref} is supported, the peak to peak ac component superimposed on V_{ref} may not exceed 5% of the dc component of V_{ref}.
3. Minimum instantaneous differential input voltage required for differential input clock operation.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

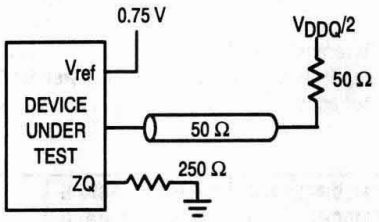


Figure 1. Test Load

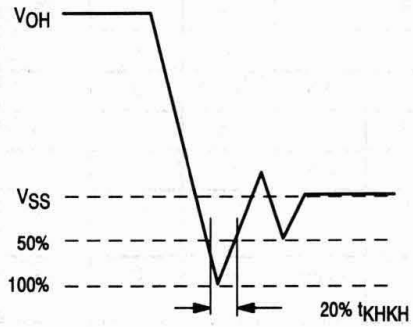
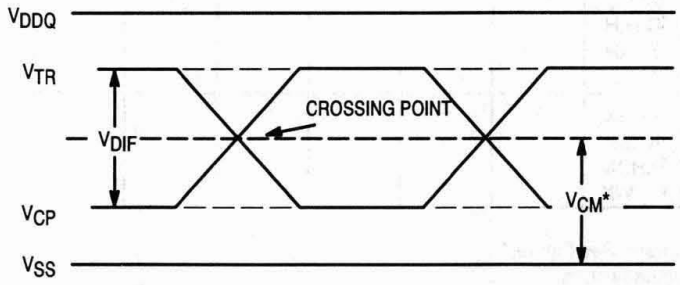


Figure 2. Undershoot Voltage



*V_{CM}, the Common Mode Input Voltage, equals $V_{TR} - ((V_{TR} - V_{CP})/2)$.

Figure 3. Differential Inputs/Common Mode Input Voltage

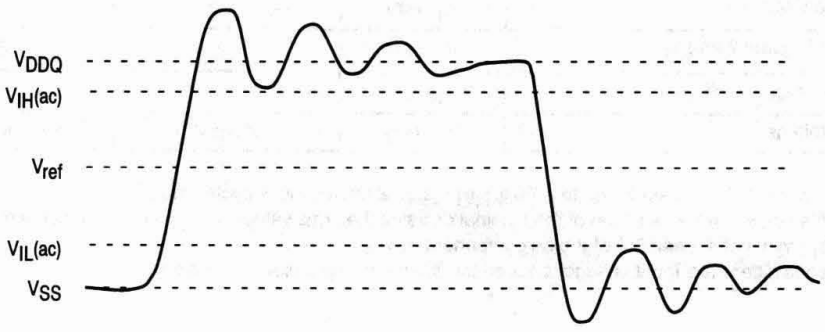
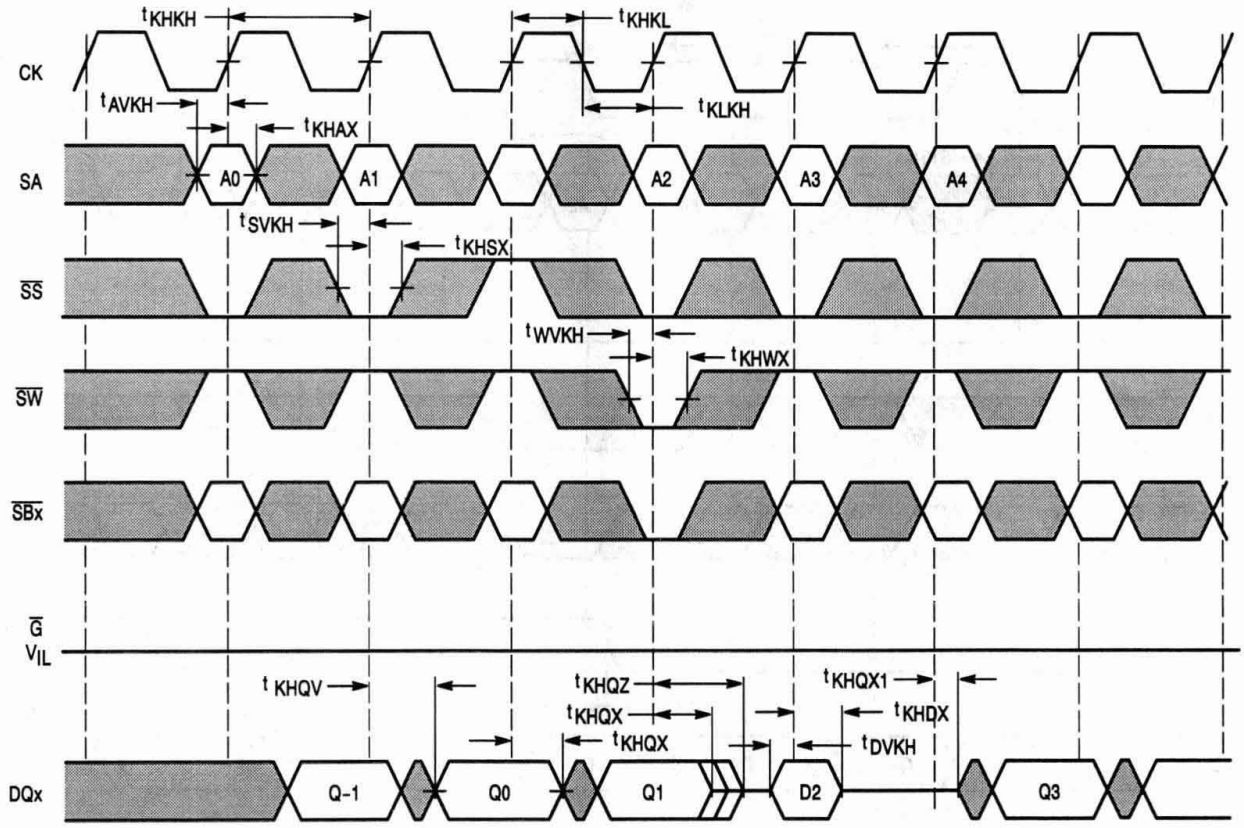


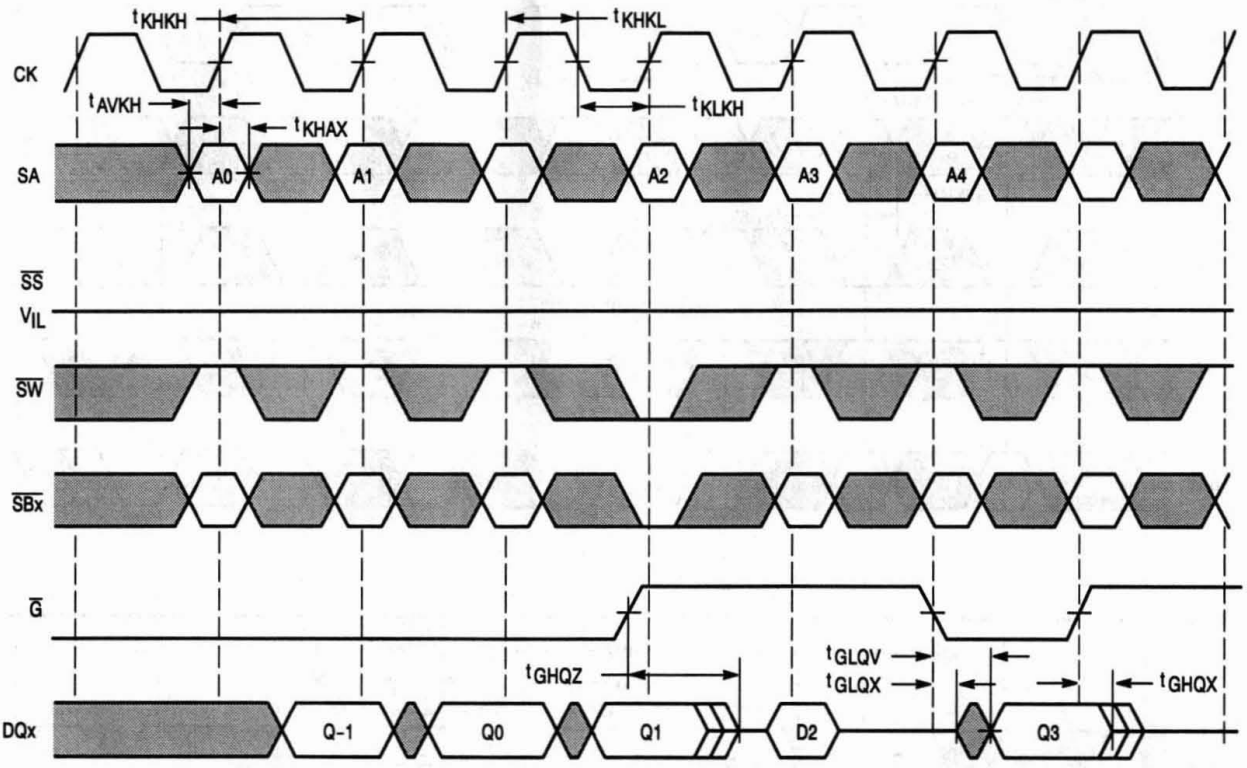
Figure 4. AC Input Conditions

REGISTER/REGISTER READ–WRITE–READ CYCLES



3

REGISTER/REGISTER READ–WRITE–READ
($\overline{G}$ Controlled)



FUNCTIONAL OPERATION

READ AND WRITE OPERATIONS

All control signals except $\overline{G}$ are registered on the rising edge of the CK clock. These signals must meet the setup and hold times shown in the AC Characteristics table. On the rising edge of the following clock, read data is clocked into the output register and available at the outputs at t_{KHQV}. During this same cycle a new read address can be applied to the address pins.

A deselect cycle (dead cycle) must occur prior to a write cycle. Read cycles may follow write cycles immediately.

$\overline{G}$, $\overline{SS}$, and $\overline{SW}$ control output drive. Chip deselect via a high on $\overline{SS}$ at the rising edge of the CK clock has its effect on the output drivers after the next rising edge of the CK clock. $\overline{SW}$ low deselects the output drivers immediately (on the same cycle). Output drive is also controlled directly by output enable, $\overline{G}$. No clock edges are required to generate output disable with $\overline{G}$. $\overline{G}$ asynchronously enables the output drivers.

Output data will be valid the latter of t_{GLQV} and t_{KHQV}. Outputs will begin driving at t_{KHQX1}. Outputs will hold previous data until t_{KHQX} or t_{GHQX}.

WRITE AND BYTE WRITE FUNCTIONS

Note that in the following discussion the term "byte" refers to nine bits of the RAM I/O bus. In all cases, the timing parameters described for synchronous write input ($\overline{SW}$) apply to each of the byte write enable inputs ($\overline{SBa}$, $\overline{SBb}$, etc.).

Byte write enable inputs have no effect on read cycles. This allows the system designer not interested in performing byte writes to connect the byte enable inputs to active low (V_{SS}). Reads of all bytes proceed normally and write cycles, activated via a low on $\overline{SW}$, and the rising edge of the CK clock, write the entire RAM I/O width. This way the designer is spared having to drive multiple write input buffer loads.

Byte writes are performed using the byte write enable inputs in conjunction with the synchronous write input ($\overline{SW}$). It is important to note that writing any one byte will inhibit a read of all bytes at the current address. The RAM cannot simultaneously read one byte and write another at the same address. A write cycle initiated with none of the byte write enable inputs active is neither a read or a write. No write will occur, but the outputs will be deselected as in a normal write cycle.

LATE WRITE

The write address is sampled on the first rising edge of clock and write data is sampled on the following rising edge.

The late write feature is implemented with single stage write buffering. Write buffering is transparent to the user. A comparator monitors the address bus and, when necessary, routes buffer contents to the outputs to assure coherent operation. This occurs in all cases whether there is a byte write or a full word is written.

PROGRAMMABLE IMPEDANCE OPERATION

The designer can program the RAMs output buffer impedance by terminating the $\overline{ZQ}$ pin to V_{SS} through a precision resistor (RQ). The value of RQ is five times the output impedance desired. For example, 250 Ω resistor will give an output impedance of 50 Ω.

Impedance updates occur continuously and the frequency of the update is based on the subdivided K clock. Note that if the K clock stops so does the impedance update.

The actual change in the impedance occurs in small increments and is monotonic. There are no significant disturbances that occur on the output because of this smooth update method.

The impedance update is not related to any particular type of cycle because the impedance is updated continuously and is based on the K clock. Updates occur regardless of whether the the device is performing a read, write or a deselect cycle and does not depend on the state of $\overline{G}$.

At power up, the output impedance defaults to approximately 50 ohms. It will take 4,000 to 16,000 cycles for the impedance to be completely updated if the programmed impedance is much higher or lower than 50 Ω.

The output buffers can also be programmed in a minimum impedance configuration by connecting ZQ to V_{DD}.

SERIAL BOUNDARY SCAN TEST ACCESS PORT OPERATION

OVERVIEW

The serial boundary scan test access port (TAP) on this RAM is designed to operate in a manner consistent with IEEE Standard 1149.1–1990 (commonly referred to as JTAG), but does not implement all of the functions required for 1149.1 compliance. Certain functions have been modified or eliminated because their implementation places extra delays in the RAMs critical speed path. Nevertheless, the RAM supports the standard TAP controller architecture. (The TAP controller is the state machine that controls the TAPs operation) and can be expected to function in a manner that does not conflict with the operation of devices with Standard 1149.1 compliant TAPs. The TAP operates using conventional JEDEC Standard 8–1B Low Voltage (3.3 V) TTL / CMOS logic level signaling.

DISABLING THE TEST ACCESS PORT

It is possible to use this device without utilizing the TAP. To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid level inputs. TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a 1 k resistor. TDO should be left unconnected.

3

TAP DC OPERATING CHARACTERISTICS

(0 °C ≤ T_A ≤ 70 °C, Unless Otherwise Noted)

Parameter	Symbol	Min	Max	Unit	Note
Logic Input Logic High	$V_{IH}1$	2.0	V_{DD} + 0.3	V	
Logic Input Logic Low	$V_{IL}1$	– 0.3	0.8	V	
Logic Input Leakage Current	I_{lkg}	—	± 5	µA	1
CMOS Output Logic Low	$V_{OL}1$	—	0.2	V	2
CMOS Output Logic High	$V_{OH}1$	V_{DD} – 0.2	—	V	3
TTL Output Logic Low	$V_{OL}2$	—	0.4	V	4
TTL Output Logic High	$V_{OH}2$	2.4	—	V	5

NOTES:
1. 0 V ≤ V_{in} ≤ V_{DDQ} for all logic input pins.
2. $I_{OL}1$ ≤ 100 µA @ V_{OL} = 0.2 V. Sampled, not 100% tested.
3. $|I_{OH}1|$ ≤ 100 µA @ V_{DDQ} – 0.2 V. Sampled, not 100% tested.
4. $I_{OL}2$ ≤ 8 mA @ V_{OL} = 0.4 V
5. $|I_{OH}2|$ ≤ 8 mA @ V_{OH} = 2.4 V

TAP AC OPERATING CONDITIONS AND CHARACTERISTICS

(0 °C ≤ T_A ≤ 70 °C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V

Output Test Load ..... 50 Ω Parallel Terminated T–line with 20 pF Receiver Input Capacitance
Test Load Termination Supply Voltage (V_T) ..... 1.5 V

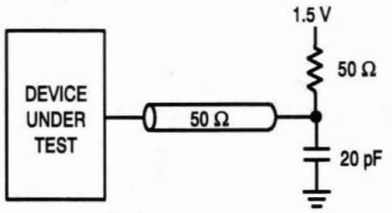
TAP CONTROLLER TIMING

Parameter	Symbol	Min	Max	Unit	Notes
Cycle Time	t_{THTH}	100	—	ns	
Clock High Time	t_{THTL}	40	—	ns	
Clock Low Time	t_{TLTH}	40	—	ns	
TMS Setup	t_{MVTH}	10	—	ns	
TMS Hold	t_{THMX}	10	—	ns	
TDI Valid to TCK High	t_{DVTH}	10	—	ns	
TCK High to TDI Don't Care	t_{THDX}	10	—	ns	
Capture Setup	t_{CS}	10	—	ns	1
Capture Hold	t_{CH}	10	—	ns	1
TCK Low to TDO Unknown	t_{TLQX}	0	—	ns	
TCK Low to TDO Valid	t_{TLOV}	—	20	ns	

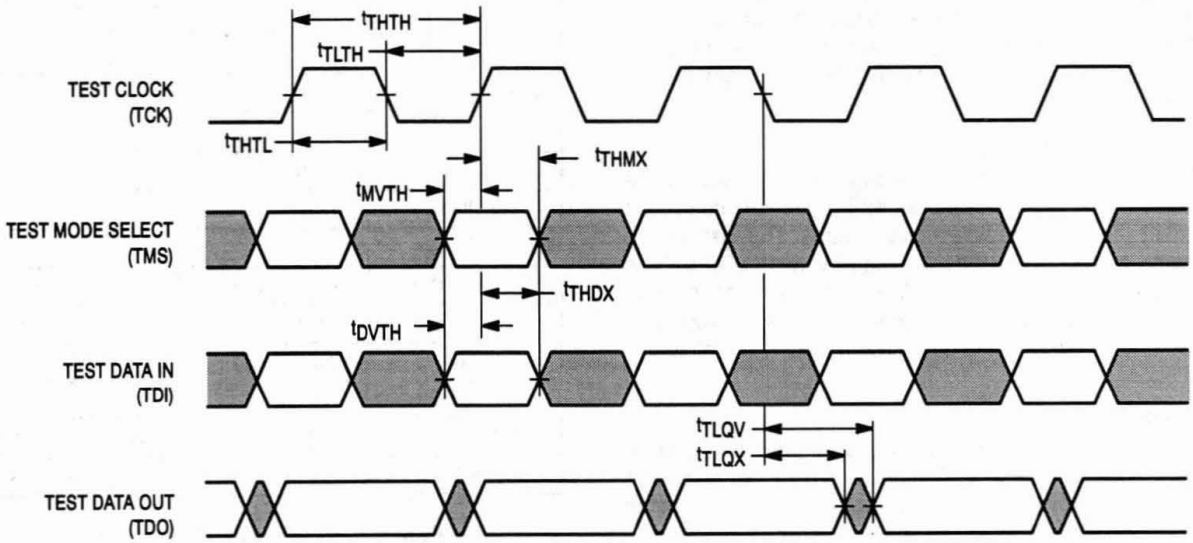
NOTES:
1. t_{CS} + t_{CH} defines the minimum pause in RAM I/O pad transitions to assure accurate pad data capture.

3

AC TEST LOAD



TAP CONTROLLER TIMING DIAGRAM



TEST ACCESS PORT PINS

TCK – TEST CLOCK (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

TMS – TEST MODE SELECT (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.

TDI – TEST DATA IN (INPUT)

The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (refer to Figure 6 TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.

TDO – TEST DATA OUT (OUTPUT)

Output that is active depending on the state of the TAP state machine (refer to Figure 6 TAP Controller State Diagram). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

TRST – TAP RESET

This device does not have a TRST pin. TRST is optional in **IEEE 1149.1.** The test–logic reset state is entered while TMS is held high for five rising edges of TCK. Power on reset circuitry is included internally. This type of reset does not affect the operation of the system logic. The reset affects test logic only.

TEST ACCESS PORT REGISTERS

OVERVIEW

The various TAP registers are selected (one at a time) via the sequences of ones and zeros input to the TMS pin as the TCK is strobed. Each of the TAPs registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on subsequent falling edge of TCK. When a register is selected it is "placed" between the TDI and TDO pins.

INSTRUCTION REGISTER

The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run test/idle or the various data register states. The instructions are three bits long. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power–up or whenever the controller is placed in test–logic–reset state.

BYPASS REGISTER

The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.

BOUNDARY SCAN REGISTER

The boundary scan register is identical in length to the number of active input and I/O connections on the RAM (not counting the TAP pins). This also includes a number of place holder locations (always set to a logic 1) reserved for density upgrade address pins. There are a total of 70 bits in the case of the x36 device and 51 bits in the case of the x18 device. The boundary scan register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture–DR state and then is placed between the TDI and TDO pins when the controller is moved to shift–DR state. Several TAP instructions can be used to activate the boundary scan register.

The Bump/Bit Scan Order tables describe which device bump connects to each boundary scan register location. The first column defines the bit's position in the boundary scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the input or I/O at the bump and the third column is the bump number.

IDENTIFICATION (ID) REGISTER

The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture–DR state with the IDCODE command loaded in the instruction register. The code is loaded from a 32 bit on–chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into shift–DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Presence Indicator

Bit #	0
Value	1

Motorola JEDEC ID Code (Compressed Format, per IEEE Standard 1149.1 – 1990

Bit #	11	10	9	8	7	6	5	4	3	2	1
Value	0	0	0	0	0	0	0	1	1	1	0

Reserved For Future Use

Bit #	17	16	15	14	13	12
Value	x	x	x	x	x	x

Device Width

Configuration	Bit #	22	21	20	19	18
128Kx36	Value	0	0	1	0	0
256Kx18	Value	0	0	0	1	1

Device Depth

Configuration	Bit #	27	26	25	24	23
128Kx36	Value	0	0	1	0	1
256Kx18	Value	0	0	1	1	0

Revision Number

Bit #	31	30	29	28
Value	x	x	x	x

Figure 5. ID Register Bit Meanings

MCM69R736A Bump/Bit Scan Order

BIT #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	SA	3B
2	SA	4P		37	NC	2B
3	SA	4T		38	SA	3A
4	SA	6R		39	SA	3C
5	SA	5T		40	SA	2C
6	ZZ	7T		41	SA	2A
7	DQa	6P		42	DQc	2D
8	DQa	7P		43	DQc	1D
9	DQa	6N		44	DQc	2E
10	DQa	7N		45	DQc	1E
11	DQa	6M		46	DQc	2F
12	DQa	6L		47	DQc	2G
13	DQa	7L		48	DQc	1G
14	DQa	6K		49	DQc	2H
15	DQa	7K		50	DQc	1H
16	$\overline{SBa}$	5L		51	$\overline{SBc}$	3G
17	$\overline{CK}$	4L		52	ZQ	4D
18	CK	4K		53	$\overline{SS}$	4E
19	$\overline{G}$	4F		54	NC	4G
20	$\overline{SBb}$	5G		55	NC	4H
21	DQb	7H		56	$\overline{SW}$	4M
22	DQb	6H		57	$\overline{SBd}$	3L
23	DQb	7G		58	DQd	1K
24	DQb	6G		59	DQd	2K
25	DQb	6F		60	DQd	1L
26	DQb	7E		61	DQd	2L
27	DQb	6E		62	DQd	2M
28	DQb	7D		63	DQd	1N
29	DQb	6D		64	DQd	2N
30	SA	6A		65	DQd	1P
31	SA	6C		66	DQd	2P
32	SA	5C		67	SA	3T
33	SA	5A		68	SA	2R
34	NC	6B		69	SA	4N
35	SA	5B		70	M1	3R

MCM69R818A Bump/Bit Scan Order

Bit #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	$\overline{SBb}$	3G
2	SA	6T		37	ZQ	4D
3	SA	4P		38	$\overline{SS}$	4E
4	SA	6R		39	NC	4G
5	SA	5T		40	NC	4H
6	ZZ	7T		41	$\overline{SW}$	4M
7	DQa	7P		42	DQb	2K
8	DQa	6N		43	DQb	1L
9	DQa	6L		44	DQb	2M
10	DQa	7K		45	DQb	1N
11	$\overline{SBa}$	5L		46	DQb	2P
12	$\overline{CK}$	4L		47	SA	3T
13	CK	4K		48	SA	2R
14	$\overline{G}$	4F		49	SA	4N
15	DQa	6H		50	SA	2T
16	DQa	7G		51	M1	3R
17	DQa	6F				
18	DQa	7E				
19	DQa	6D				
20	SA	6A				
21	SA	6C				
22	SA	5C				
23	SA	5A				
24	NC	6B				
25	SA	5B				
26	SA	3B				
27	NC	2B				
28	SA	3A				
29	SA	3C				
30	SA	2C				
31	SA	2A				
32	DQb	1D				
33	DQb	2E				
34	DQb	2G				
35	DQb	1H				

NOTES:

1. The NC pads listed in this table are indeed no connects, but are represented in the boundary scan register by a "place holder" bit that is forced to logic 1. These pads are reserved for use as address inputs on higher density RAMs that follow this pad out and scan order standard.
2. CK, $\overline{CK}$, are sampled individually. $\overline{CK}$ is not simply a forced complement of the CK input. In scan mode these differential inputs are referenced to V_{ref}, not each other.
3. ZQ, M1 and M2 are not ordinary inputs and may not respond to standard I/O logic levels. ZQ, M1 and M2 must be driven to within 100 mV of a V_{DD} or V_{SS} supply rail to ensure consistent results.
4. ZZ must remain at V_{IL} during boundary scan to ensure consistent results.

TAP Controller Instruction Set

OVERVIEW

There are two classes of instructions defined in the Standard 1149.1–1990; the standard (public) instructions, and device specific (private) instructions. Some public instructions, are mandatory for 1149.1 compliance. Optional public instructions must be implemented in prescribed ways.

Although the TAP controller in this device follows the 1149.1 conventions, it is not 1194.1 compliant because some of the mandatory instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads, but cannot be used to load address, data or control signals into the RAM or to preload the I/O buffers. In other words, the device will not perform Standard 1149.1 EXTEST, INTEST or the preload portion of the SAMPLE / PRELOAD command.

When the TAP controller is placed in capture–IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the shift–IR state the instruction register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to update–IR state. The TAP instruction sets for this device are listed in the following tables.

STANDARD (PUBLIC) INSTRUCTIONS

BYPASS

The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift–DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

Sample/preload is a Standard 1149.1 mandatory public instruction. When the sample / preload instruction is loaded in the Instruction register, moving the TAP controller into the capture–DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set–up plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register.

Moving the controller to shift–DR state then places the boundary scan register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the update–DR state with the SAMPLE / PRELOAD instruction loaded in the instruction register has the same effect as the pause–DR command. This functionality is not Standard 1149.1 compliant.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic 0s. EXTEST is not implemented in this device. Therefore this device is not 1149.1 compliant. Nevertheless, this RAMs TAP does respond to an all zeros instruction, as follows. With the EXTEST (000) instruction loaded in the instruction register the RAM responds just as it does in response to the SAMPLE / PRELOAD instruction described above, except the RAM outputs are forced to high–Z any time the instruction is loaded.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture–DR mode and places the ID register between the TDI and TDO pins in shift–DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test–logic–reset state.

THE DEVICE SPECIFIC (PUBLIC) INSTRUCTION

SAMPLE–Z

If the SAMPLE–Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high–Z) and the boundary scan register is connected between TDI and TDO when the TAP controller. is moved to the shift–DR state.

THE DEVICE SPECIFIC (PRIVATE) INSTRUCTION

NOOP

Do not use these instructions; they are reserved for future use.

STANDARD (PUBLIC) INSTRUCTION CODES

Instruction	Code*	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM outputs to High–Z state. *NOT 1149.1 COMPLIANT*
IDCODE	001**	Preloads ID register and places it between TDI and TDO. Does not affect RAM operation.
SAMPLE / PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect RAM operation. Does not implement 1149.1 Preload function. * NOT 1149.1 COMPLIANT *
BYPASS	111	Places bypass register between TDI and TDO. Does not affect RAM operation.
SAMPLE–Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM output drivers to High–Z.

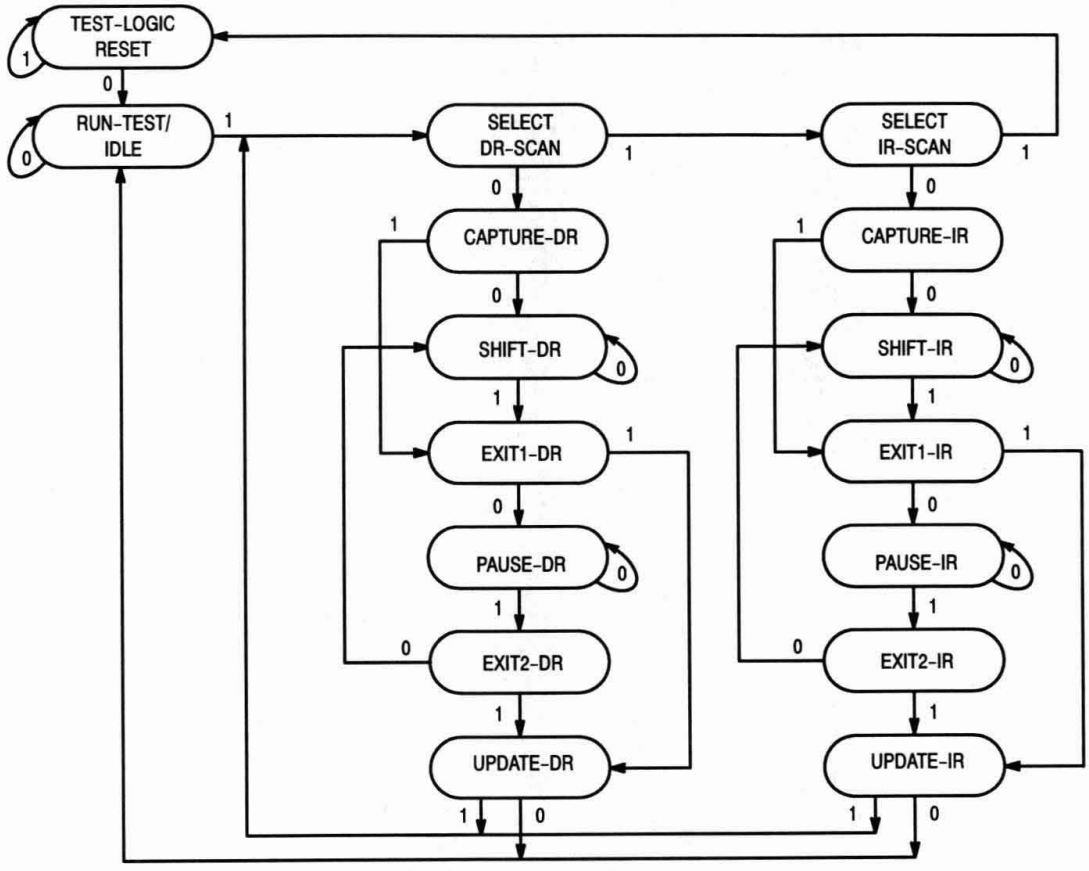
* Instruction codes expressed in binary, MSB on left, LSB on right.
** Default instruction automatically loaded at power–up and in test–logic–reset state.

3

STANDARD (PRIVATE) INSTRUCTION CODES

Instruction	Code*	Description
NO OP	011	Do not use these instructions; they are reserved for future use.
NO OP	101	Do not use these instructions; they are reserved for future use.
NO OP	110	Do not use these instructions; they are reserved for future use.

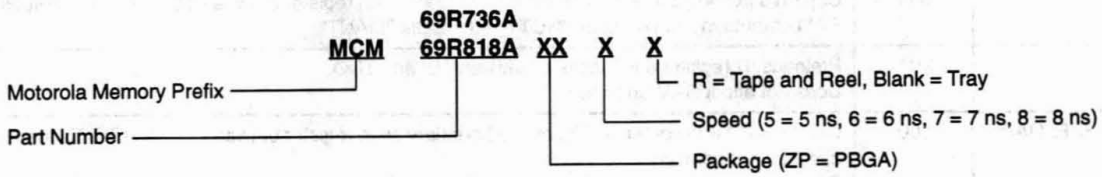
* Instruction codes expressed in binary, MSB on left, LSB on right.



NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 6. TAP Controller State Diagram

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers —	MCM69R736AZP5	MCM69R736AZP6	MCM69R736AZP7	MCM69R736AZP8
	MCM69R818AZP5	MCM69R818AZP6	MCM69R818AZP7	MCM69R818AZP8
	MCM69R736AZP5R	MCM69R736AZP6R	MCM69R736AZP7R	MCM69R736AZP8R
	MCM69R818AZP5R	MCM69R818AZP6R	MCM69R818AZP7R	MCM69R818AZP8R

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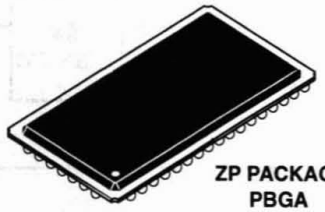
MCM69R737
MCM69R819

Advance Information

4M Late Write LVTTL



ZP PACKAGE
PBGA
CASE 999–01

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The MCM69R737/819 is a 4 megabit synchronous late write fast static RAM designed to provide high performance in secondary cache and ATM switch, Telecom, and other high speed memory applications. The MCM69R819 organized as 256K words by 18 bits, and the MCM69R737 organized as 128K words by 36 bits wide are fabricated in Motorola's high performance silicon gate BiCMOS technology.

The differential CK clock inputs control the timing of read/write operations of the RAM. At the rising edge of the CK clock all addresses, write enables, and synchronous selects are registered. An internal buffer and special logic enable the memory to accept write data on the rising edge of the CK clock a cycle after address and control signals. Read data is driven on the rising edge of the CK clock also.

The RAM uses LVTTL 3.3 V inputs and outputs.

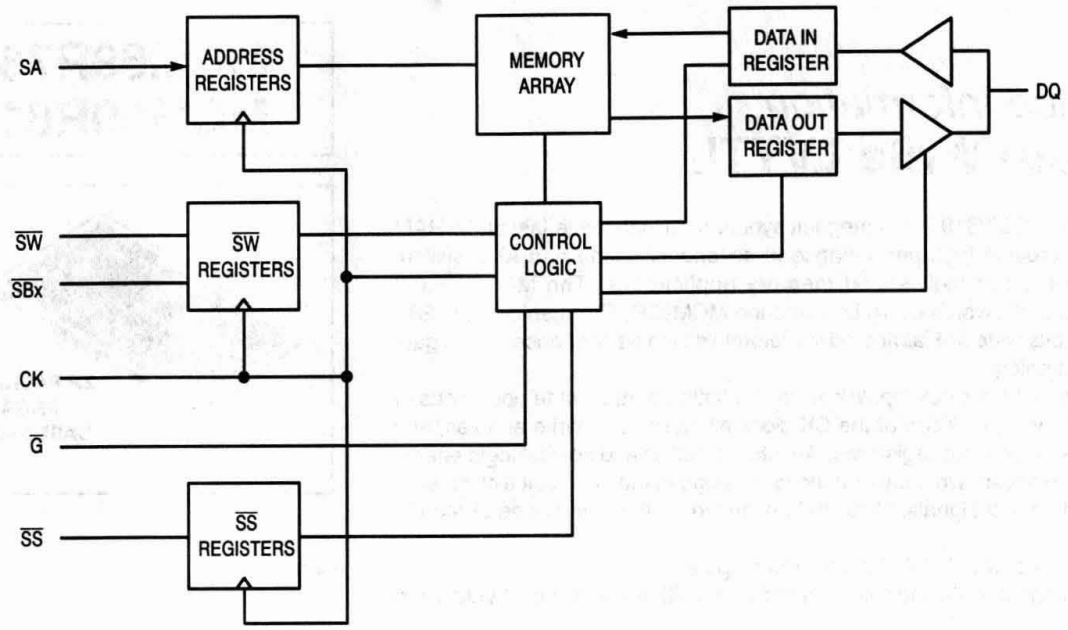
The synchronous write and byte enables allow writing to individual bytes or the entire word.

- Byte Write Control
- Single 3.3 V + 10%, – 5% Operation
- LVTTL 3.3 V I/O
- Register to Register Synchronous Operation
- Asynchronous Output Enable
- Boundary Scan (JTAG) IEEE 1149.1 Compatible
- Differential Clock Inputs
- Optional x 18 or x 36 organization
- MCM69R737/819–7 = 7 ns
  MCM69R737/819–8 = 8 ns
- 119 Bump, 50 mil (1.27 mm) Pitch, 14 mm x 22 mm Plastic Ball Grid Array (PBGA) Package

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 3
4/3/97

FUNCTIONAL BLOCK DIAGRAM



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PIN ASSIGNMENTS

TOP VIEW

MCM69R737

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	SA	NC	SA	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
E	DQc	DQc	V_{SS}	$\overline{SS}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{G}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{SBc}$	NC	$\overline{SBb}$	DQb	DQb
H	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CK	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{SBd}$	$\overline{CK}$	$\overline{SBa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{SW}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
P	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
R	NC	SA	V_{SS}	V_{DD}	V_{DD}	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69R819

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	SA	NC	SA	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQb	NC	V_{SS}	NC	V_{SS}	DQa	NC
E	NC	DQb	V_{SS}	$\overline{SS}$	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	$\overline{SBb}$	NC	V_{SS}	NC	DQa
H	DQb	NC	V_{SS}	NC	V_{SS}	DQa	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	CK	V_{SS}	NC	DQa
L	DQb	NC	V_{SS}	$\overline{CK}$	$\overline{SBa}$	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{SW}$	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	SA	V_{SS}	DQa	NC
P	NC	DQb	V_{SS}	SA	V_{SS}	NC	DQa
R	NC	SA	V_{SS}	V_{DD}	V_{DD}	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69R737 PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6K, 7K, 6L, 7L, 6M, 6N, 7N, 6P, 7P (b) 6D, 7D, 6E, 7E, 6F, 6G, 7G, 6H, 7H (c) 1D, 2D, 1E, 2E, 2F, 1G, 2G, 1H, 2H (d) 1K, 2K, 1L, 2L, 2M, 1N, 2N, 1P, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 3T, 4T, 5T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 5G, 3G, 3L (a), (b), (c), (d)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
7T	ZZ	Input	Enables sleep mode.
4C, 2J, 4J, 6J, 4R, 5R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 3H, 5H, 3K, 5K, 3M, 5M, 3N, 5N, 3P, 5P, 3R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 4B, 6B, 7B, 1C, 7C, 4D, 4G, 4H, 3J, 5J, 1R, 7R, 1T, 2T, 6T, 6U	NC	—	No Connection: There is no connection to the chip. Note: 3J and 5J are tied common.

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MCM69R819 PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6D, 7E, 6F, 7G, 6H, 7K, 6L, 6N, 7P (b) 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 2T, 3T, 5T, 6T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 3G (a), (b)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
7T	ZZ	Input	Enables sleep mode.
4C, 2J, 4J, 6J, 4R, 5R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P, 3R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 4B, 6B, 7B, 1C, 7C, 2D, 4D, 7D, 1E, 6E, 2F, 1G, 4G, 6G, 2H, 4H, 7H, 3J, 5J, 1K, 6K, 2L, 7L, 6M, 2N, 7N, 1P, 6P, 1R, 7R, 1T, 4T, 6U	NC	—	No Connection: There is no connection to the chip. Note: 3J and 5J are tied common.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS}, See Note 1)

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Output Supply Voltage	V_{DDQ}	– 0.5 to V_{DD} + 0.5	V
Voltage On Any Pin	V_{in}	– 0.5 to V_{DD} + 0.5	V
Input Current (per I/O)	I_{in}	± 50	mA
Output Current (per I/O)	I_{out}	± 70	mA
Power Dissipation (See Note 2)	P_D	—	W
Operating Temperature	T_A	0 to + 70	°C
Temperature Under Bias	T_{bias}	–10 to + 85	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability will be dependent upon package characteristics and use environment. See enclosed thermal impedance data.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

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PBGA PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (Still Air)		$R_{\theta JA}$	53	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Single Layer Board	$R_{\theta JA}$	38	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Four Layer Board	$R_{\theta JA}$	22	°C/W	
Junction to Board (Bottom)		$R_{\theta JB}$	14	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	5	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

($0°C \le T_A \le 70$ °C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (See Notes 1 through 4)

Parameter		Symbol	Min	Typical –7	Typical –8	Max	Unit	Notes
Core Power Supply Voltage		V_{DD}	3.15	—	—	3.6	V	
Output Driver Supply Voltage		V_{DDQ}	3.15	—	—	3.6	V	
Active Power Supply Current	(x18) (x36)	I_{DD1}	— —	330 390	320 370	430 490	mA	5
Quiescent Active Power Supply Current		I_{DD2}	—	180	180	250	mA	6, 10
Active Standby Power Supply Current		I_{SB1}	—	160	160	250	mA	7
Quiescent Standby Power Supply Current		I_{SB2}	—	140	140	230	mA	8, 10
Sleep Mode Power Supply Current		I_{SB3}	—	30	30	50	mA	9, 10

NOTES:
1. All data sheet parameters specified to full range of V_{DD} unless otherwise noted. All voltages are referenced to voltage applied to V_{SS} bumps.
2. Supply voltage applied to V_{DD} connections.
3. Supply voltage applied to V_{DDQ} connections.
4. All power supply currents measured with outputs open or deselected.
5. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered active, 50% read cycles.
6. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered active.
7. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered inactive.
8. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered inactive. ZZ low.
9. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered inactive, ZZ high.
10. 200 mV $\ge V_{in} \ge V_{DDQ} - 200$ mV.

DC INPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
DC Input Logic High	V_{IH} (dc)	2.0	$V_{DD} + 0.3$	V	
DC Input Logic Low	V_{IL} (dc)	– 0.3	0.8	V	1
Input Leakage Current	$I_{lkg(1)}$	—	± 5	µA	2
Clock Input Leakage Current	$I_{clkg(1)}$	—	± 8	µA	2
Clock Input Signal Voltage	V_{in}	– 0.3	$V_{DD} + 0.3$	V	
Clock Input Differential Voltage	V_{DIF} (dc)	0.2	$V_{DD} + 0.6$	V	3
Clock Input Common Mode Voltage Range	V_{CM} (dc)	1.2	2.1	V	4, Fig. 3

NOTES:
1. Inputs may undershoot to –0.5 V (peak) for up to 20% t_{KHKH} (e.g., 2 ns at a clock cycle time of 10 ns).
2. $0 V \pm V_{in} \pm V_{DDQ}$ for all pins.
3. Minimum instantaneous differential input voltage required for differential input clock operation.
4. Maximum rejectable common mode input voltage variation.

DC OUTPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
Output Leakage Current	$I_{lkg(0)}$	–1.0	1.0	µA	
Output Low Voltage	V_{OL}	—	0.4	V	1
Output High Voltage	V_{OH}	2.4	—	V	2

NOTES:
1. $I_{OL} = 8.0$ mA
2. $I_{OH} = -8.0$ mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, $0°C \le T_A \le 70$ °C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	5	5	pF
Input/Output Capacitance	$C_{I/O}$	6	8	pF
CK, $\overline{CK}$ Capacitance	C_{CK}	6	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T_A ≤ 70 °C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V
Clock Input Timing Reference Level ..... Differential Cross–Point
Clock Input Pulse Level ..... 1.8 V to 2.1 V

READ/WRITE CYCLE TIMING (See Note 3)

Parameter	Symbol	MCM69R737–7 MCM69R819–7		MCM69R737–8 MCM69R819–8		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{KHKH}	7	—	8	—	ns	
Clock High Pulse Width	t_{KHKL}	2.8	—	3.2	—	ns	
Clock Low Pulse Width	t_{KLKH}	2.8	—	3.2	—	ns	
Clock High to Output Low–Z	t_{KHQX1}	1	—	1	—	ns	2
Clock High to Output Valid	t_{KHQV}	—	3.5	—	4	ns	1
Clock High to Output Hold	t_{KHQX}	0.5	—	0.5	—	ns	1
Clock High to Output High–Z	t_{KHQZ}	0	3.5	0	4	ns	2
Output Enable Low to Output Low–Z	t_{GLQX}	1.0	—	1.0	—	ns	2
Output Enable Low to Output Valid	t_{GLQV}	—	3.5	—	4	ns	1
Output Enable to Output Hold	t_{GHQX}	1	—	1	—	ns	1
Output Enable High to Output High–Z	t_{GHQZ}	—	3.5	—	4	ns	2
Setup Times: Address / Data In / Chip Select / Write Enable	t_{AVKH} / t_{DVKH} / t_{SVKH} / t_{WVKH}	0.5	—	0.5	—	ns	
Hold Times: Address / Data In / Chip Select / Write Enable	t_{KHAX} / t_{KHDX} / t_{KHSX} / t_{KHWX}	1	—	1	—	ns	

NOTES:
1. Tested per AC Test Load diagram. See Figure 1.
2. Measured at ± 200 mV from steady state.
3. In no case may control input signals (e.g., $\overline{SS}$) be operated with pulse widths less than the minimum clock input pulse width specifications (e.g., t_{KHKL}) or at frequencies that exceed the applied K clock frequency.

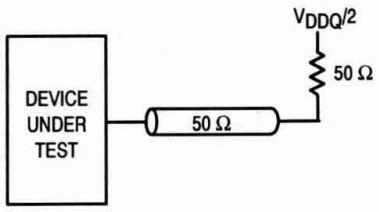

Figure 1. AC Test Load

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

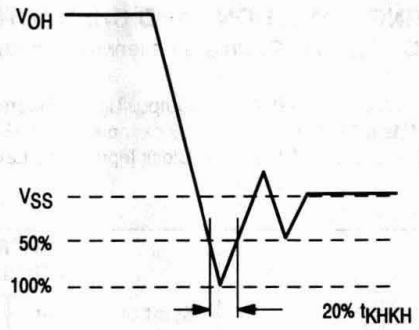

Figure 2. Undershoot Voltage

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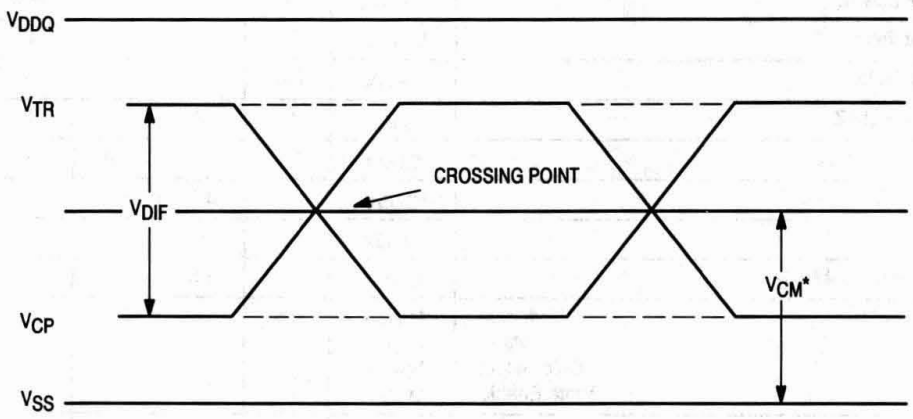
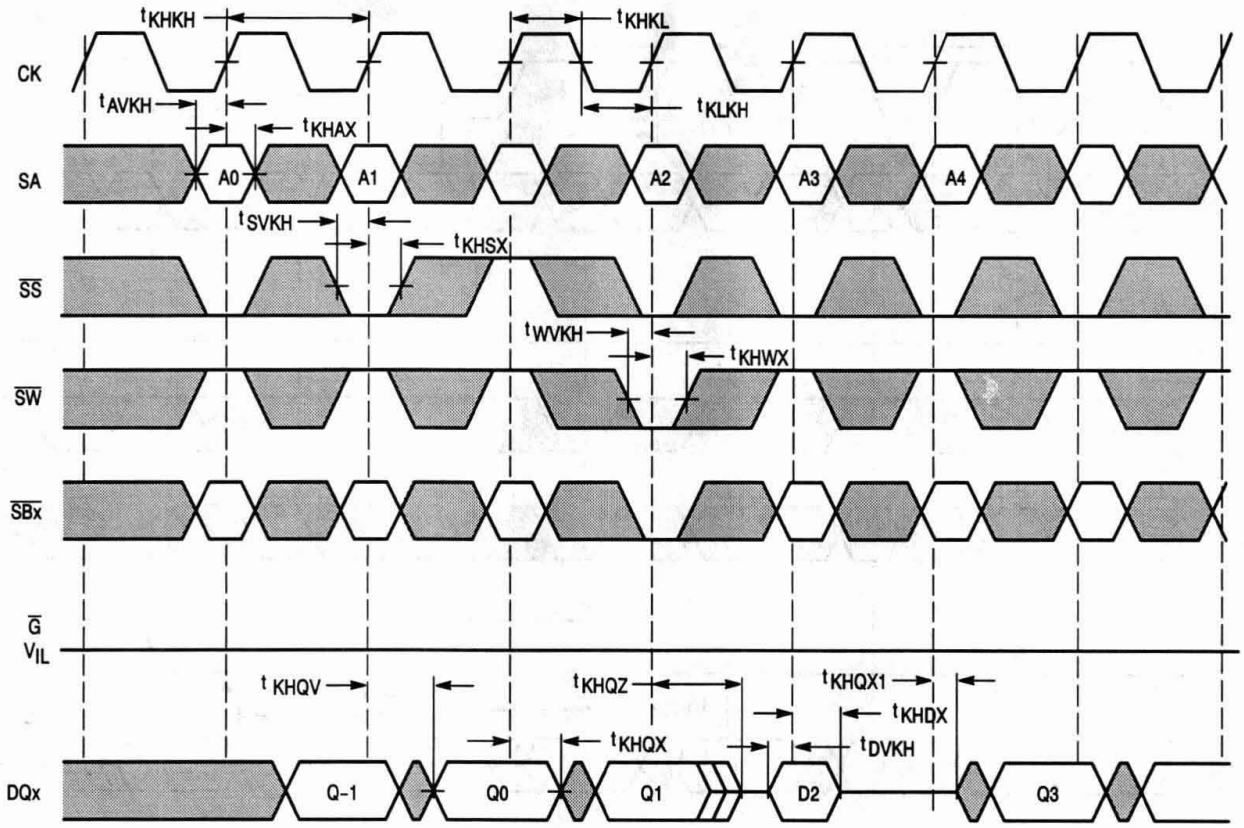


* V_{CM}, the Common Mode Input Voltage, equals $V_{TR} - ((V_{TR} - V_{CP})/2)$.

Figure 3. Differential Inputs/ Common Mode Input Voltage

REGISTER/REGISTER READ–WRITE–READ CYCLES



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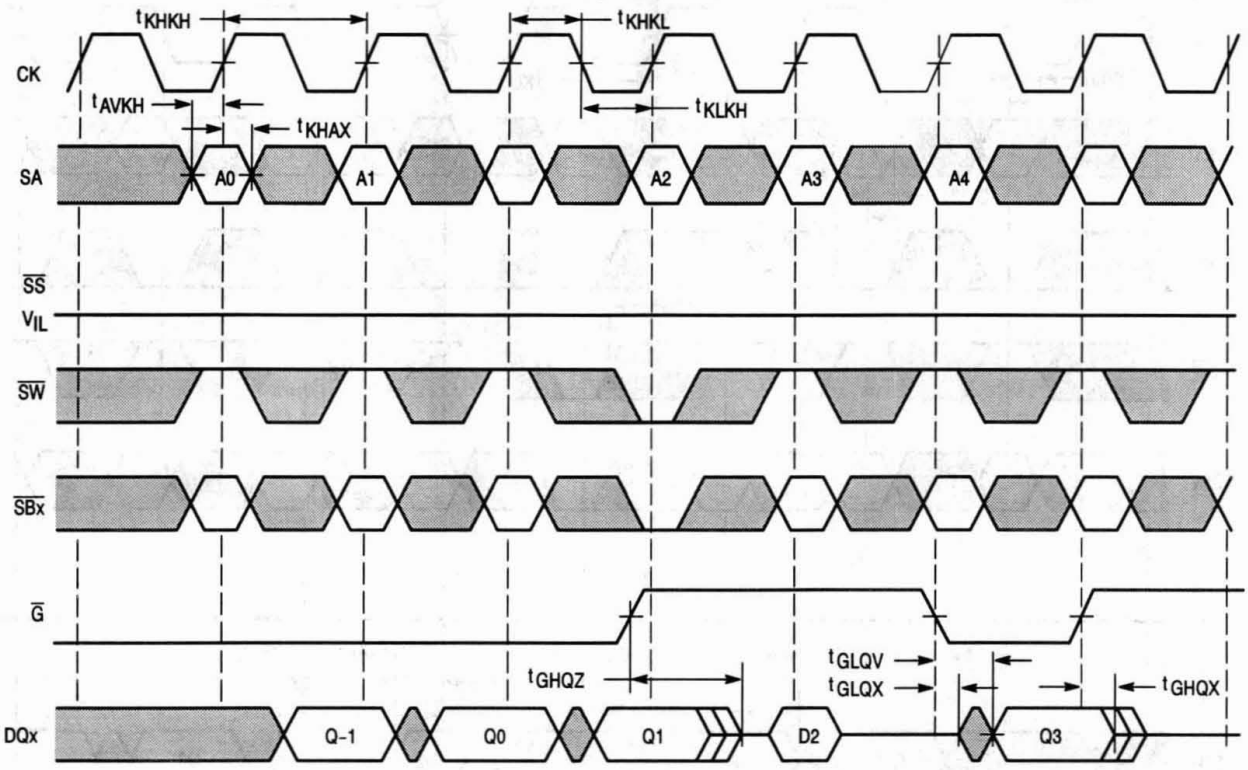
REGISTER/REGISTER READ–WRITE–READ
($\overline{G}$ Controlled)



FUNCTIONAL OPERATION

READ AND WRITE OPERATIONS

All control signals except $\overline{G}$ are registered on the rising edge of the CK clock. These signals must meet the setup and hold times shown in the AC Characteristics table. On the rising edge of the following clock, read data is clocked into the output register and available at the outputs at t_{KHQV}. During this same cycle a new read address can be applied to the address pins.

A deselect cycle (dead cycle) must occur prior to a write cycle. Read cycles may follow write cycles immediately.

$\overline{G}$, $\overline{SS}$, and $\overline{SW}$ control output drive. Chip deselect via a high on $\overline{SS}$ at the rising edge of the CK clock has its effect on the output drivers after the next rising edge of the CK clock. $\overline{SW}$ low deselects the output drivers immediately (on the same cycle). Output selecting via a low on $\overline{SS}$ and high on $\overline{SW}$ at a rising CK clock has its effect on the output drivers after the next rising edge of the CK clock. Output drive is also controlled directly by output enable, $\overline{G}$. $\overline{G}$ is an asynchronous input. No clock edges are required to enable/disable the output using $\overline{G}$.

Output data will be valid the latter of t_{GLQV} and t_{KHQV}. Outputs will begin driving at t_{KHQX1}. Outputs will hold previous data until t_{KHQX} or t_{GHQX}.

WRITE AND BYTE WRITE FUNCTIONS

Note that in the following discussion the term "byte" refers to nine bits of the RAM I/O bus. In all cases, the timing parameters described for synchronous write input ($\overline{SW}$) apply to each of the byte write enable inputs ($\overline{SBa}$, $\overline{SBb}$, etc.).

Byte write enable inputs have no effect on read cycles. This allows the system designer not interested in performing byte writes to connect the byte enable inputs to active low (V_{SS}). Reads of all bytes proceed normally and write cycles, activated via a low on $\overline{SW}$, and the rising edge of the CK clock, write the entire RAM I/O width. This way the designer is spared having to drive multiple write input buffer loads.

Byte writes are performed using the byte write enable inputs in conjunction with the synchronous write input ($\overline{SW}$). It is important to note that writing any one byte will inhibit a read of all bytes at the current address. The RAM cannot simultaneously read one byte and write another at the same address. A write cycle initiated with none of the byte write enable inputs active is neither a read or a write. No write will occur, but the outputs will be deselected as in a normal write cycle.

LATE WRITE

The write address is sampled on the first rising edge of clock and write data is sampled on the following rising edge.

The late write feature is implemented with single stage write buffering. Write buffering is transparent to the user. A comparator monitors the address bus and, when necessary, routes buffer contents to the outputs to assure coherent operation. This occurs in all cases whether there is a byte write or a full word is written.

POWER UP AND INITIALIZATION

Once supplies have reached specification levels, a minimum dwell of 1.0 µs with CK clock inputs cycling is required before beginning normal operations.

SERIAL BOUNDARY SCAN TEST ACCESS PORT OPERATION

OVERVIEW

The serial boundary scan test access port (TAP) on this RAM is designed to operate in a manner consistent with IEEE Standard 1149.1–1990 (commonly referred to as JTAG), but does not implement all of the functions required for 1149.1 compliance. Certain functions have been modified or eliminated because their implementation places extra delays in the RAMs critical speed path. Nevertheless, the RAM supports the standard TAP controller architecture. (The TAP controller is the state machine that controls the TAPs operation) and can be expected to function in a manner that does not conflict with the operation of devices with Standard 1149.1 compliant TAPs. The TAP operates using conventional JEDEC Standard 8–1B Low Voltage (3.3 V) TTL / CMOS logic level signaling.

DISABLING THE TEST ACCESS PORT

It is possible to use this device without utilizing the TAP. To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid level inputs. TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a 1 k resistor. TDO should be left unconnected.

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TAP DC OPERATING CHARACTERISTICS

($0°C \le T_A \le 70$ °C, Unless Otherwise Noted)

Parameter	Symbol	Min	Max	Unit	Note
Logic Input Logic High	$V_{IH}1$	2.0	V_{DD} + 0.3	V	
Logic Input Logic Low	$V_{IL}1$	– 0.3	0.8	V	
Logic Input Leakage Current	I_{lkg}	—	± 5	µA	1
CMOS Output Logic Low	$V_{OL}1$	—	0.2	V	2
CMOS Output Logic High	$V_{OH}1$	V_{DD} – 0.2	—	V	3
TTL Output Logic Low	$V_{OL}2$	—	0.4	V	4
TTL Output Logic High	$V_{OH}2$	2.4	—	V	5

NOTES:
1. $0 V \le V_{in} \le V_{DDQ}$ for all logic input pins.
2. $I_{OL}1 \le 100$ µA @ $V_{OL} = 0.2$ V. Sampled, not 100% tested.
3. $|I_{OH}1| \le 100$ µA @ $V_{DDQ} - 0.2$ V. Sampled, not 100% tested.
4. $I_{OL}2 \le 8$ mA @ $V_{OL} = 0.4$ V
5. $|I_{OH}2| \le 8$ mA @ $V_{OH} = 2.4$ V

TAP AC OPERATING CONDITIONS AND CHARACTERISTICS

($0°C \le T_A \le 70°C$, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V

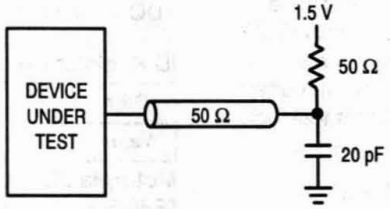
Output Test Load ..... 50 Ω Parallel Terminated T–line with 20 pF
Receiver Input Capacitance
Test Load Termination Supply Voltage (V_T) ..... 1.5 V

TAP CONTROLLER TIMING

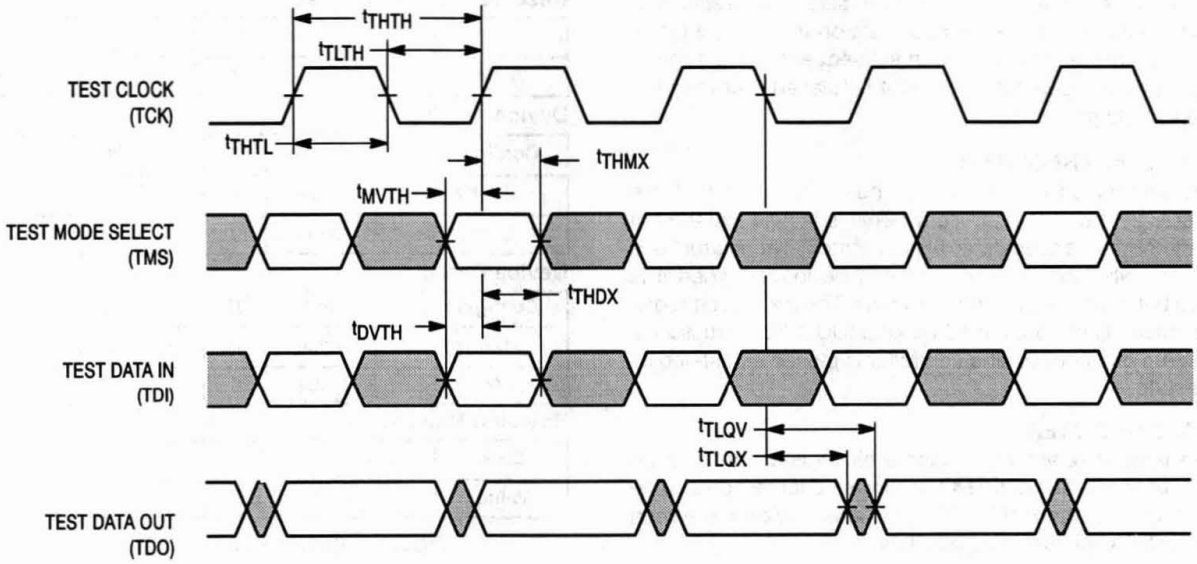
Parameter	Symbol	Min	Max	Unit	Notes
Cycle Time	t_{THTH}	100	—	ns	
Clock High Time	t_{THTL}	40	—	ns	
Clock Low Time	t_{TLTH}	40	—	ns	
TMS Setup	t_{MVTH}	10	—	ns	
TMS Hold	t_{THMX}	10	—	ns	
TDI Valid to TCK High	t_{DVTH}	10	—	ns	
TCK High to TDI Don't Care	t_{THDX}	10	—	ns	
Capture Setup	t_{CS}	10	—	ns	1
Capture Hold	t_{CH}	10	—	ns	1
TCK Low to TDO Unknown	t_{TLQX}	0	—	ns	
TCK Low to TDO Valid	t_{TLOV}	—	20	ns	

NOTES:
1. $t_{CS} + t_{CH}$ defines the minimum pause in RAM I/O pad transitions to assure accurate pad data capture.

AC TEST LOAD



TAP CONTROLLER TIMING DIAGRAM



TEST ACCESS PORT PINS

TCK – TEST CLOCK (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

TMS – TEST MODE SELECT (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.

TDI – TEST DATA IN (INPUT)

The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (refer to Figure 5 TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.

TDO – TEST DATA OUT (OUTPUT)

Output that is active depending on the state of the TAP state machine (refer to Figure 5 TAP Controller State Diagram). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

TRST – TAP RESET

This device does not have a TRST pin. TRST is optional in **IEEE 1149.1.** The test–logic reset state is entered while TMS is held high for five rising edges of TCK. Power on reset circuitry is included internally. This type of reset does not affect the operation of the system logic. The reset affects test logic only.

TEST ACCESS PORT REGISTERS

OVERVIEW

The various TAP registers are selected (one at a time) via the sequences of ones and zeros input to the TMS pin as the TCK is strobed. Each of the TAPs registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on subsequent falling edge of TCK. When a register is selected it is "placed" between the TDI and TDO pins.

INSTRUCTION REGISTER

The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run test/idle or the various data register states. The instructions are three bits long. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power–up or whenever the controller is placed in test–logic–reset state.

BYPASS REGISTER

The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.

BOUNDARY SCAN REGISTER

The boundary scan register is identical in length to the number of active input and I/O connections on the RAM (not counting the TAP pins). This also includes a number of place holder locations (always set to a logic 1) reserved for density upgrade address pins. There are a total of 70 bits in the case of the x36 device and 51 bits in the case of the x18 device. The boundary scan register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture–DR state and then is placed between the TDI and TDO pins when the controller is moved to shift–DR state. Several TAP instructions can be used to activate the boundary scan register.

The Bump/Bit Scan Order tables describe which device bump connects to each boundary scan register location. The first column defines the bit's position in the boundary scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the input or I/O at the bump and the third column is the bump number.

IDENTIFICATION (ID) REGISTER

The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture–DR state with the IDCODE command loaded in the instruction register. The code is loaded from a 32 bit on–chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into shift–DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Presence Indicator

Bit #	0
Value	1

Motorola JEDEC ID Code (Compressed Format, per IEEE Standard 1149.1 – 1990

Bit #	11	10	9	8	7	6	5	4	3	2	1
Value	0	0	0	0	0	0	0	1	1	1	0

Reserved For Future Use

Bit #	17	16	15	14	13	12
Value	x	x	x	x	x	x

Device Width

Configuration	Bit #	22	21	20	19	18
128Kx36	Value	0	0	1	0	0
256Kx18	Value	0	0	0	1	1

Device Depth

Configuration	Bit #	27	26	25	24	23
128Kx36	Value	0	0	1	0	1
256Kx18	Value	0	0	1	1	0

Revision Number

Bit #	31	30	29	28
Value	x	x	x	x

Figure 4. ID Register Bit Meanings

MCM69R737 Bump/Bit Scan Order

BIT #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	SA	3B
2	SA	4P		37	NC	2B
3	SA	4T		38	SA	3A
4	SA	6R		39	SA	3C
5	SA	5T		40	SA	2C
6	ZZ	7T		41	SA	2A
7	DQa	6P		42	DQc	2D
8	DQa	7P		43	DQc	1D
9	DQa	6N		44	DQc	2E
10	DQa	7N		45	DQc	1E
11	DQa	6M		46	DQc	2F
12	DQa	6L		47	DQc	2G
13	DQa	7L		48	DQc	1G
14	DQa	6K		49	DQc	2H
15	DQa	7K		50	DQc	1H
16	$\overline{SBa}$	5L		51	$\overline{SBc}$	3G
17	$\overline{CK}$	4L		52	NC	4D
18	CK	4K		53	$\overline{SS}$	4E
19	$\overline{G}$	4F		54	NC	4G
20	$\overline{SBb}$	5G		55	NC	4H
21	DQb	7H		56	$\overline{SW}$	4M
22	DQb	6H		57	$\overline{SBd}$	3L
23	DQb	7G		58	DQd	1K
24	DQb	6G		59	DQd	2K
25	DQb	6F		60	DQd	1L
26	DQb	7E		61	DQd	2L
27	DQb	6E		62	DQd	2M
28	DQb	7D		63	DQd	1N
29	DQb	6D		64	DQd	2N
30	SA	6A		65	DQd	1P
31	SA	6C		66	DQd	2P
32	SA	5C		67	SA	3T
33	SA	5A		68	SA	2R
34	NC	6B		69	SA	4N
35	SA	5B		70	M1	3R

MCM69R819 Bump/Bit Scan Order

Bit #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	$\overline{SBb}$	3G
2	SA	6T		37	NC	4D
3	SA	4P		38	$\overline{SS}$	4E
4	SA	6R		39	NC	4G
5	SA	5T		40	NC	4H
6	ZZ	7T		41	$\overline{SW}$	4M
7	DQa	7P		42	DQb	2K
8	DQa	6N		43	DQb	1L
9	DQa	6L		44	DQb	2M
10	DQa	7K		45	DQb	1N
11	$\overline{SBa}$	5L		46	DQb	2P
12	$\overline{CK}$	4L		47	SA	3T
13	CK	4K		48	SA	2R
14	$\overline{G}$	4F		49	SA	4N
15	DQa	6H		50	SA	2T
16	DQa	7G		51	M1	3R
17	DQa	6F				
18	DQa	7E				
19	DQa	6D				
20	SA	6A				
21	SA	6C				
22	SA	5C				
23	SA	5A				
24	NC	6B				
25	SA	5B				
26	SA	3B				
27	NC	2B				
28	SA	3A				
29	SA	3C				
30	SA	2C				
31	SA	2A				
32	DQb	1D				
33	DQb	2E				
34	DQb	2G				
35	DQb	1H				

NOTES:

1. The NC pads listed in this table are indeed no connects, but are represented in the boundary scan register by a "place holder" bit that is forced to logic 1. These pads are reserved for use as address inputs on higher density RAMs that follow this pad out and scan order standard.
2. CK, $\overline{CK}$, are sampled individually. $\overline{CK}$ is not simply a forced complement of the CK input. In scan mode these differential inputs are referenced to each other.
3. M1 and M2 are not ordinary inputs and may not respond to standard I/O logic levels. M1 and M2 must be driven to within 100 mV of a V_{DD} or V_{SS} supply rail to ensure consistent results.
4. ZZ must remain at V_{IL} during boundary scan to ensure consistent results.

3

TAP Controller Instruction Set

OVERVIEW

There are two classes of instructions defined in the Standard 1149.1–1990; the standard (public) instructions, and device specific (private) instructions. Some public instructions, are mandatory for 1149.1 compliance. Optional public instructions must be implemented in prescribed ways.

Although the TAP controller in this device follows the 1149.1 conventions, it is not 1194.1 compliant because some of the mandatory instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads, but cannot be used to load address, data or control signals into the RAM or to preload the I/O buffers. In other words, the device will not perform Standard 1149.1 EXTEST, INTEST or the preload portion of the SAMPLE / PRELOAD command.

3

When the TAP controller is placed in capture–IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the shift–IR state the instruction register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to update–IR state. The TAP instruction sets for this device are listed in the following tables.

STANDARD (PUBLIC) INSTRUCTIONS

BYPASS

The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift–DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

Sample/preload is a Standard 1149.1 mandatory public instruction. When the sample / preload instruction is loaded in the Instruction register, moving the TAP controller into the capture–DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set–up plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register.

Moving the controller to shift–DR state then places the boundary scan register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the update–DR state with the SAMPLE / PRELOAD instruction loaded in the instruction register has the same effect as the pause–DR command. This functionality is not Standard 1149.1 compliant.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic 0s. EXTEST is not implemented in this device. Therefore this device is not 1149.1 compliant. Nevertheless, this RAMs TAP does respond to an all zeros instruction, as follows. With the EXTEST (000) instruction loaded in the instruction register the RAM responds just as it does in response to the SAMPLE / PRELOAD instruction described above, except the RAM outputs are forced to high–Z any time the instruction is loaded.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture–DR mode and places the ID register between the TDI and TDO pins in shift–DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test–logic–reset state.

THE DEVICE SPECIFIC (PUBLIC) INSTRUCTION

SAMPLE–Z

If the SAMPLE–Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high–Z) and the boundary scan register is connected between TDI and TDO when the TAP controller. is moved to the shift–DR state.

THE DEVICE SPECIFIC (PRIVATE) INSTRUCTION

NOOP

Do not use these instructions; they are reserved for future use.

STANDARD (PUBLIC) INSTRUCTION CODES

Instruction	Code*	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM outputs to High–Z state. *NOT 1149.1 COMPLIANT*
IDCODE	001**	Preloads ID register and places it between TDI and TDO. Does not affect RAM operation.
SAMPLE / PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect RAM operation. Does not implement 1149.1 Preload function. * NOT 1149.1 COMPLIANT *
BYPASS	111	Places bypass register between TDI and TDO. Does not affect RAM operation.
SAMPLE–Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM output drivers to High–Z.

* Instruction codes expressed in binary, MSB on left, LSB on right.
** Default instruction automatically loaded at power–up and in test–logic–reset state.

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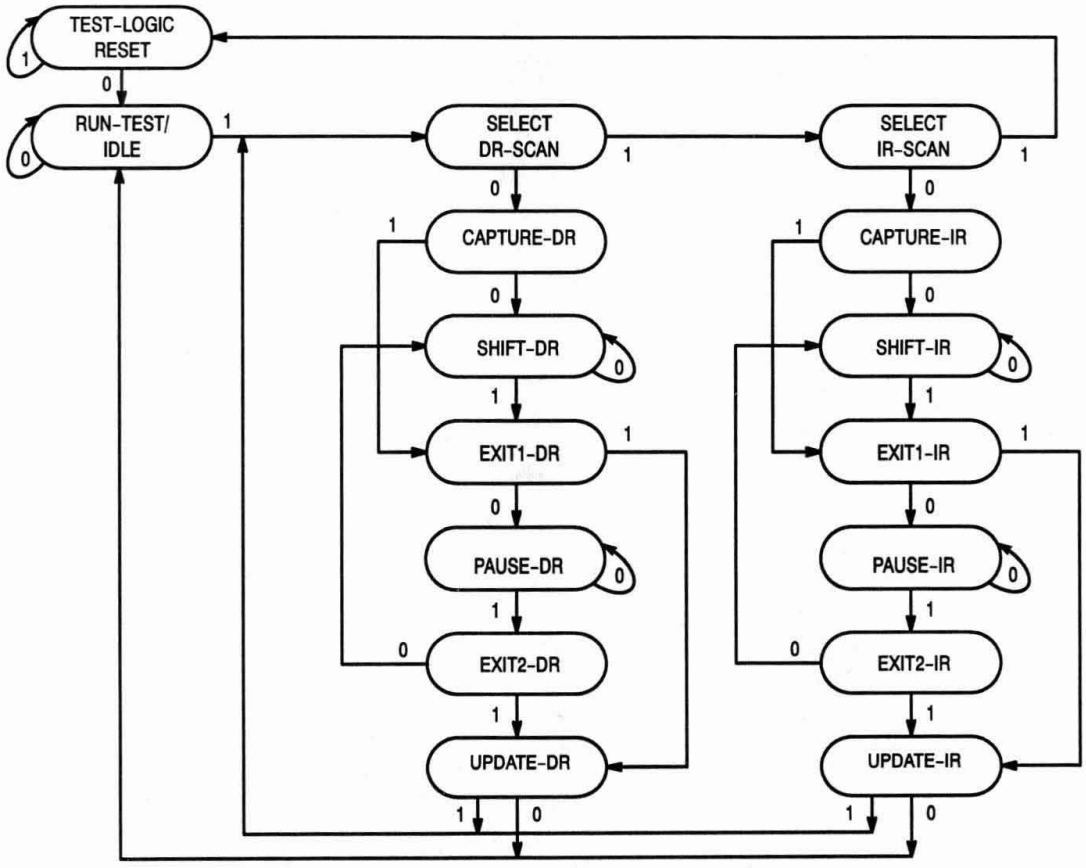
STANDARD (PRIVATE) INSTRUCTION CODES

Instruction	Code*	Description
NO OP	011	Do not use these instructions; they are reserved for future use.
NO OP	101	Do not use these instructions; they are reserved for future use.
NO OP	110	Do not use these instructions; they are reserved for future use.

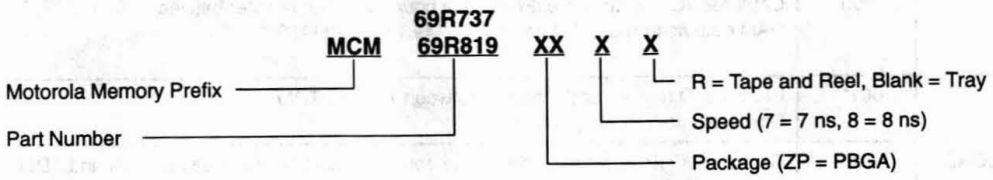
* Instruction codes expressed in binary, MSB on left, LSB on right.



NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 5. TAP Controller State Diagram

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM69R737ZP7 MCM69R737ZP8
MCM69R819ZP7 MCM69R819ZP8
MCM69R737ZP7R MCM69R737ZP8R
MCM69R819ZP7R MCM69R819ZP8R

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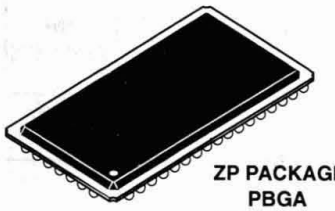
MCM69R737A
MCM69R819A

Advance Information

4M Late Write LVTTL



ZP PACKAGE
PBGA
CASE 999–01

3

The MCM69R737A/819A is a 4 megabit synchronous late write fast static RAM designed to provide high performance in secondary cache and ATM switch, Telecom, and other high speed memory applications. The MCM69R819A organized as 256K words by 18 bits, and the MCM69R737A organized as 128K words by 36 bits wide are fabricated in Motorola's high performance silicon gate BiCMOS technology.

The differential CK clock inputs control the timing of read/write operations of the RAM. At the rising edge of the CK clock all addresses, write enables, and synchronous selects are registered. An internal buffer and special logic enable the memory to accept write data on the rising edge of the CK clock a cycle after address and control signals. Read data is driven on the rising edge of the CK clock also.

The RAM uses LVTTL 3.3 V inputs and outputs.

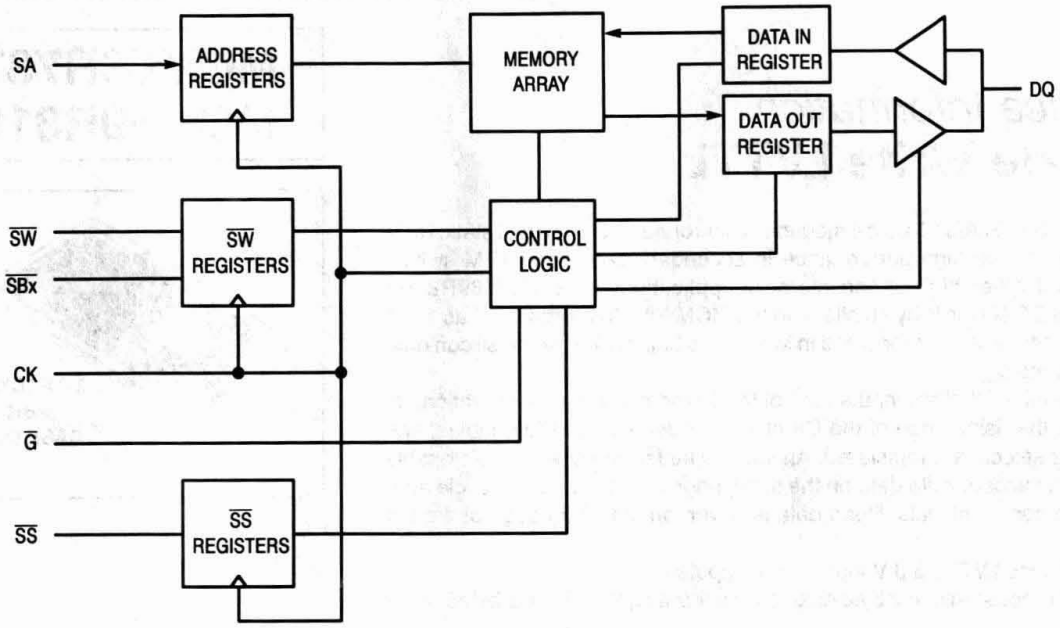
The synchronous write and byte enables allow writing to individual bytes or the entire word.

- Byte Write Control
- Single 3.3 V + 10%, – 5% Operation
- LVTTL 3.3 V I/O
- Register to Register Synchronous Operation
- Asynchronous Output Enable
- Boundary Scan (JTAG) IEEE 1149.1 Compatible
- Differential Clock Inputs
- Optional x 18 or x 36 organization
- MCM69R737A/819A–5 = 5 ns
  MCM69R737A/819A–6 = 6 ns
  MCM69R737A/819A–7 = 7 ns
  MCM69R737A/819A–8 = 8 ns
- 119 Bump, 50 mil (1.27 mm) Pitch, 14 mm x 22 mm Plastic Ball Grid Array (PBGA) Package

This document contains information on a new product. Specifications and information herein are subject to change without notice.

4/3/97

FUNCTIONAL BLOCK DIAGRAM



3

PIN ASSIGNMENTS

TOP VIEW

MCM69R737A

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	SA	NC	SA	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
E	DQc	DQc	V_{SS}	$\overline{SS}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{G}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{SBc}$	NC	$\overline{SBb}$	DQb	DQb
H	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CK	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{SBd}$	$\overline{CK}$	$\overline{SBa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{SW}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
P	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
R	NC	SA	V_{SS}	V_{DD}	V_{DD}	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69R819A

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	SA	NC	SA	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQb	NC	V_{SS}	NC	V_{SS}	DQa	NC
E	NC	DQb	V_{SS}	$\overline{SS}$	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	$\overline{SBb}$	NC	V_{SS}	NC	DQa
H	DQb	NC	V_{SS}	NC	V_{SS}	DQa	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	CK	V_{SS}	NC	DQa
L	DQb	NC	V_{SS}	$\overline{CK}$	$\overline{SBa}$	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{SW}$	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	SA	V_{SS}	DQa	NC
P	NC	DQb	V_{SS}	SA	V_{SS}	NC	DQa
R	NC	SA	V_{SS}	V_{DD}	V_{DD}	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69R737A PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6K, 7K, 6L, 7L, 6M, 6N, 7N, 6P, 7P (b) 6D, 7D, 6E, 7E, 6F, 6G, 7G, 6H, 7H (c) 1D, 2D, 1E, 2E, 2F, 1G, 2G, 1H, 2H (d) 1K, 2K, 1L, 2L, 2M, 1N, 2N, 1P, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 3T, 4T, 5T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 5G, 3G, 3L (a), (b), (c), (d)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
7T	ZZ	Input	Enables sleep mode.
4C, 2J, 4J, 6J, 4R, 5R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 3H, 5H, 3K, 5K, 3M, 5M, 3N, 5N, 3P, 5P, 3R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 4B, 6B, 7B, 1C, 7C, 4D, 4G, 4H, 3J, 5J, 1R, 7R, 1T, 2T, 6T, 6U	NC	—	No Connection: There is no connection to the chip. Note: 3J and 5J are tied common.

3

MCM69R819A PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6D, 7E, 6F, 7G, 6H, 7K, 6L, 6N, 7P (b) 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 2T, 3T, 5T, 6T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 3G (a), (b)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
7T	ZZ	Input	Enables sleep mode.
4C, 2J, 4J, 6J, 4R, 5R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P, 3R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 4B, 6B, 7B, 1C, 7C, 2D, 4D, 7D, 1E, 6E, 2F, 1G, 4G, 6G, 2H, 4H, 7H, 3J, 5J, 1K, 6K, 2L, 7L, 6M, 2N, 7N, 1P, 6P, 1R, 7R, 1T, 4T, 6U	NC	—	No Connection: There is no connection to the chip. Note: 3J and 5J are tied common.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS}, See Note 1)

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Output Supply Voltage	V_{DDQ}	– 0.5 to V_{DD} + 0.5	V
Voltage On Any Pin	V_{in}	– 0.5 to V_{DD} + 0.5	V
Input Current (per I/O)	I_{in}	± 50	mA
Output Current (per I/O)	I_{out}	± 70	mA
Power Dissipation (See Note 2)	P_D	—	W
Operating Temperature	T_A	0 to + 70	°C
Temperature Under Bias	T_{bias}	–10 to + 85	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability will be dependent upon package characteristics and use environment. See enclosed thermal impedance data.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

3

PBGA PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (Still Air)		$R_{\theta JA}$	53	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Single Layer Board	$R_{\theta JA}$	38	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Four Layer Board	$R_{\theta JA}$	22	°C/W	
Junction to Board (Bottom)		$R_{\theta JB}$	14	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	5	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

($0°C \le T_A \le 70°C$, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (See Notes 1 through 4)

Parameter	Symbol	Min	Typical –5	Typical –6	Typical –7	Typical –8	Max	Unit	Notes
Core Power Supply Voltage	V_{DD}	3.15	—	—	—	—	3.6	V	
Output Driver Supply Voltage	V_{DDQ}	3.15	—	—	—	—	3.6	V	
Active Power Supply Current (x18) (x36)	I_{DD1}	— —	380 450	360 420	330 390	320 370	480 550	mA	5
Quiescent Active Power Supply Current	I_{DD2}	— —	180	180	180	180	250	mA	6, 10
Active Standby Power Supply Current)	I_{SB1}	— —	170	170	170	170	250	mA	7
Quiescent Standby Power Supply Current	I_{SB2}	— —	150	150	150	150	230	mA	8, 10
Sleep Mode Power Supply Current	I_{SB3}	—	30	30	30	30	50	mA	9, 10

NOTES:
1. All data sheet parameters specified to full range of V_{DD} unless otherwise noted. All voltages are referenced to voltage applied to V_{SS} bumps.
2. Supply voltage applied to V_{DD} connections.
3. Supply voltage applied to V_{DDQ} connections.
4. All power supply currents measured with outputs open or deselected.
5. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered active, 50% read cycles.
6. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered active.
7. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered inactive.
8. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered inactive. ZZ low.
9. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered inactive, ZZ high.
10. $200 \text{ mV} \ge V_{in} \ge V_{DDQ} - 200 \text{ mV}$.

DC INPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
DC Input Logic High	V_{IH} (dc)	2.0	$V_{DD} + 0.3$	V	
DC Input Logic Low	V_{IL} (dc)	– 0.3	0.8	V	1
Input Leakage Current	$I_{lkg(1)}$	—	± 5	µA	2
Clock Input Leakage Current	$I_{clkg(1)}$	—	± 8	µA	2
Clock Input Signal Voltage	V_{in}	– 0.3	$V_{DD} + 0.3$	V	
Clock Input Differential Voltage	V_{DIF} (dc)	0.2	$V_{DD} + 0.6$	V	3
Clock Input Common Mode Voltage Range	V_{CM} (dc)	1.2	2.1	V	4, Fig. 3

NOTES:
1. Inputs may undershoot to – 0.5 V (peak) for up to 20% t_{KHKH} (e.g., 2 ns at a clock cycle time of 10 ns).
2. $0 \text{ V} \le V_{in} \le V_{DDQ}$ for all pins.
3. Minimum instantaneous differential input voltage required for differential input clock operation.
4. Maximum rejectable common mode input voltage variation.

DC OUTPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
Output Leakage Current	$I_{lkg(0)}$	–1.0	1.0	µA	
Output Low Voltage	V_{OL}	—	0.4	V	1
Output High Voltage	V_{OH}	2.4	—	V	2

NOTES:
1. $I_{OL} = 8.0$ mA
2. $I_{OH} = – 8.0$ mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, 0°C ≤ T_A ≤ 70 °C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	5	pF
Input/Output Capacitance	$C_{I/O}$	7	8	pF
CK, $\overline{CK}$ Capacitance	C_{CK}	4	5	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T_A ≤ 70 °C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V
Clock Input Timing Reference Level ..... Differential Cross–Point
Clock Input Pulse Level ..... 1.8 V to 2.1 V

READ/WRITE CYCLE TIMING (See Note 3)

Parameter	Symbol	MCM69R737A–5 MCM69R819A–5		MCM69R737A–6 MCM69R819A–6		MCM69R737A–7 MCM69R819A–7		MCM69R737A–8 MCM69R819A–8		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	5	—	6	—	7	—	8	—	ns	
Clock High Pulse Width	t_{KHKL}	2.4	—	2.4	—	2.8	—	3.2	—	ns	
Clock Low Pulse Width	t_{KLKH}	2.4	—	2.4	—	2.8	—	3.2	—	ns	
Clock High to Output Low–Z	t_{KHQX1}	1	—	1	—	1	—	1	—	ns	2
Clock High to Output Valid	t_{KHQV}	—	2.5	—	3	—	3.5	—	4	ns	1
Clock High to Output Hold	t_{KHQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	1
Clock High to Output High–Z	t_{KHQZ}	—	2.5	—	3	—	3.5	—	4	ns	2
Output Enable Low to Output Low–Z	t_{GLQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	2
Output Enable Low to Output Valid	t_{GLQV}	—	2.5	—	3	—	3.5	—	4	ns	1
Output Enable to Output Hold	t_{GHQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	1
Output Enable High to Output High–Z	t_{GHQZ}	—	2.5	—		—	3.5	—	4	ns	2
Setup Times: Address Data In Chip Select Write Enable	t_{AVKH} t_{DVKH} t_{SVKH} t_{WVKH}	0.5	—	0.5	—	0.5	—	0.5	—	ns	
Hold Times: Address Data In Chip Select Write Enable	t_{KHAX} t_{KHDX} t_{KHSX} t_{KHWX}	1	—	1	—	1	—	1	—	ns	

NOTES:
1. Tested per AC Test Load diagram. See Figure 1.
2. Measured at ± 200 mV from steady state.
3. In no case may control input signals (e.g., $\overline{SS}$) be operated with pulse widths less than the minimum clock input pulse width specifications (e.g., t_{KHKL}) or at frequencies that exceed the applied K clock frequency.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

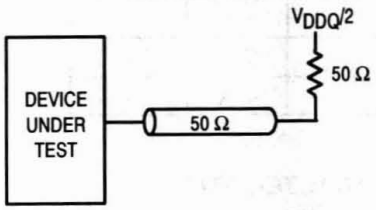


Figure 1. AC Test Load

3

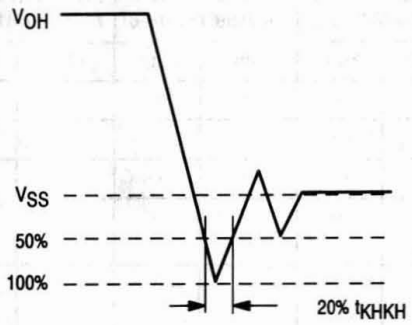
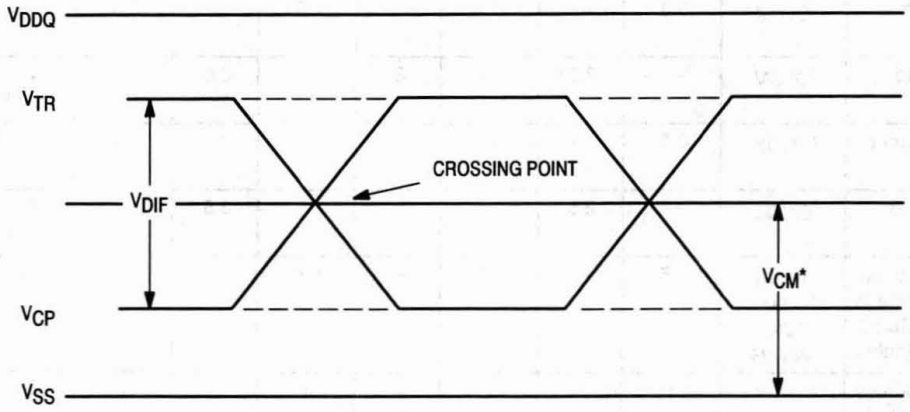


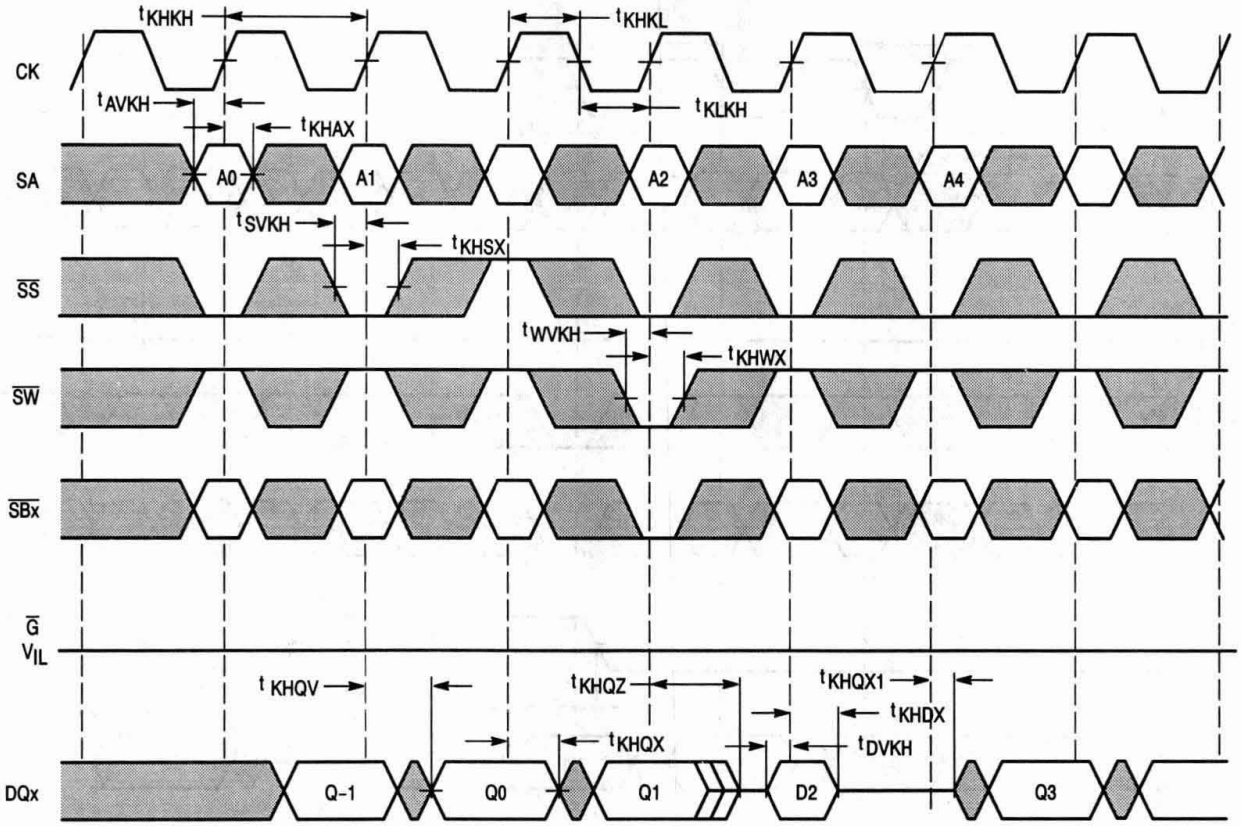
Figure 2. Undershoot Voltage



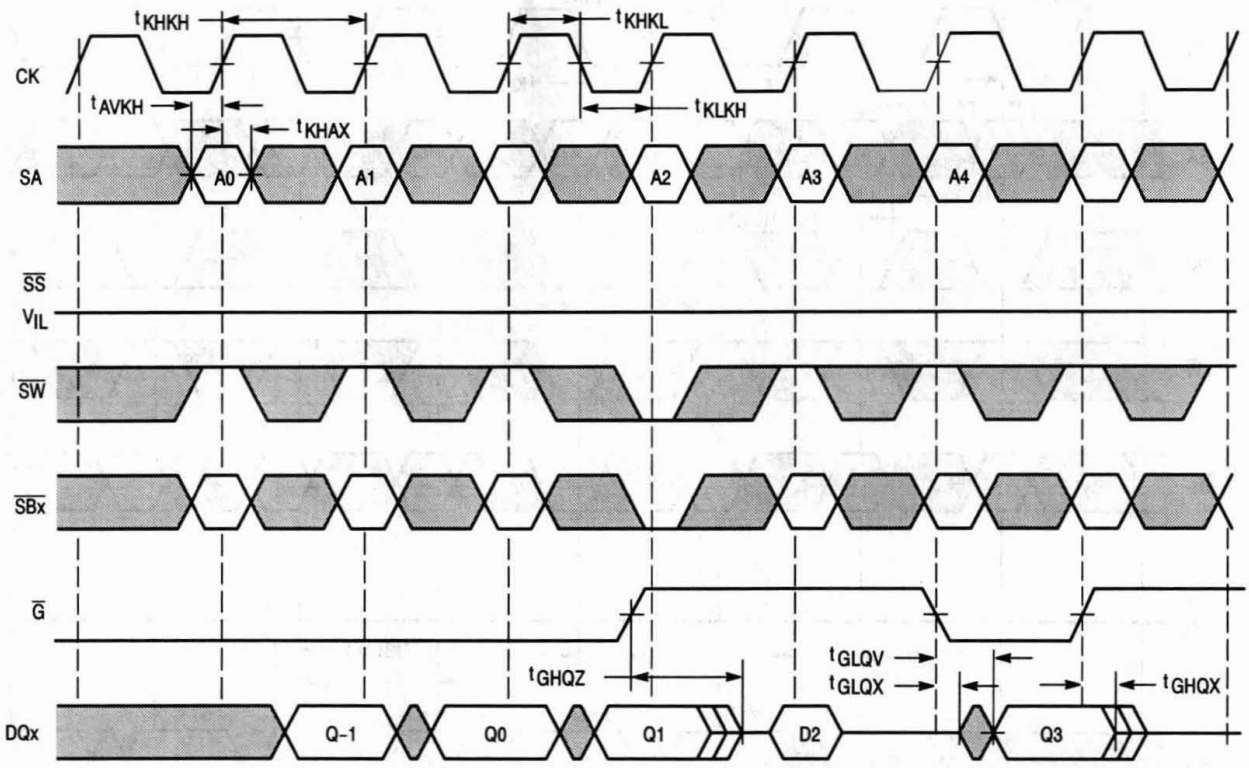
* V_{CM}, the Common Mode Input Voltage, equals $V_{TR} - ((V_{TR} - V_{CP})/2)$.

Figure 3. Differential Inputs/Common Mode Input Voltage

REGISTER/REGISTER READ–WRITE–READ CYCLES



REGISTER/REGISTER READ–WRITE–READ
($\overline{G}$ Controlled)



3

FUNCTIONAL OPERATION

READ AND WRITE OPERATIONS

All control signals except $\overline{G}$ are registered on the rising edge of the CK clock. These signals must meet the setup and hold times shown in the AC Characteristics table. On the rising edge of the following clock, read data is clocked into the output register and available at the outputs at t_{KHQV}. During this same cycle a new read address can be applied to the address pins.

A deselect cycle (dead cycle) must occur prior to a write cycle. Read cycles may follow write cycles immediately.

$\overline{G}$, $\overline{SS}$, and $\overline{SW}$ control output drive. Chip deselect via a high on $\overline{SS}$ at the rising edge of the CK clock has its effect on the output drivers after the next rising edge of the CK clock. $\overline{SW}$ low deselects the output drivers immediately (on the same cycle). Output selecting via a low on $\overline{SS}$ and high on $\overline{SW}$ at a rising CK clock has its effect on the output drivers after the next rising edge of the CK clock. Output drive is also controlled directly by output enable, $\overline{G}$. $\overline{G}$ is an asynchronous input. No clock edges are required to enable/disable the output using $\overline{G}$.

Output data will be valid the latter of t_{GLQV} and t_{KHQV}. Outputs will begin driving at t_{KHQX1}. Outputs will hold previous data until t_{KHQX} or t_{GHQX}.

WRITE AND BYTE WRITE FUNCTIONS

Note that in the following discussion the term "byte" refers to nine bits of the RAM I/O bus. In all cases, the timing parameters described for synchronous write input ($\overline{SW}$) apply to each of the byte write enable inputs ($\overline{SBa}$, $\overline{SBb}$, etc.).

Byte write enable inputs have no effect on read cycles. This allows the system designer not interested in performing byte writes to connect the byte enable inputs to active low (V_{SS}). Reads of all bytes proceed normally and write cycles, activated via a low on $\overline{SW}$, and the rising edge of the CK clock, write the entire RAM I/O width. This way the designer is spared having to drive multiple write input buffer loads.

Byte writes are performed using the byte write enable inputs in conjunction with the synchronous write input ($\overline{SW}$). It is important to note that writing any one byte will inhibit a read of all bytes at the current address. The RAM cannot simultaneously read one byte and write another at the same address. A write cycle initiated with none of the byte write enable inputs active is neither a read or a write. No write will occur, but the outputs will be deselected as in a normal write cycle.

LATE WRITE

The write address is sampled on the first rising edge of clock and write data is sampled on the following rising edge.

The late write feature is implemented with single stage write buffering. Write buffering is transparent to the user. A comparator monitors the address bus and, when necessary, routes buffer contents to the outputs to assure coherent operation. This occurs in all cases whether there is a byte write or a full word is written.

POWER UP AND INITIALIZATION

Once supplies have reached specification levels, a minimum dwell of 1.0 µs with CK clock inputs cycling is required before beginning normal operations.

SERIAL BOUNDARY SCAN TEST ACCESS PORT OPERATION

OVERVIEW

The serial boundary scan test access port (TAP) on this RAM is designed to operate in a manner consistent with IEEE Standard 1149.1–1990 (commonly referred to as JTAG), but does not implement all of the functions required for 1149.1 compliance. Certain functions have been modified or eliminated because their implementation places extra delays in the RAMs critical speed path. Nevertheless, the RAM supports the standard TAP controller architecture. (The TAP controller is the state machine that controls the TAPs operation) and can be expected to function in a manner that does not conflict with the operation of devices with Standard 1149.1 compliant TAPs. The TAP operates using conventional JEDEC Standard 8–1B Low Voltage (3.3 V) TTL / CMOS logic level signaling.

DISABLING THE TEST ACCESS PORT

It is possible to use this device without utilizing the TAP. To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid level inputs. TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a 1 k resistor. TDO should be left unconnected.

3

TAP DC OPERATING CHARACTERISTICS

(0°C ≤ T_A ≤ 70 °C, Unless Otherwise Noted)

Parameter	Symbol	Min	Max	Unit	Note
Logic Input Logic High	$V_{IH}1$	2.0	V_{DD} + 0.3	V	
Logic Input Logic Low	$V_{IL}1$	– 0.3	0.8	V	
Logic Input Leakage Current	I_{lkg}	—	± 5	µA	1
CMOS Output Logic Low	$V_{OL}1$	—	0.2	V	2
CMOS Output Logic High	$V_{OH}1$	V_{DD} – 0.2	—	V	3
TTL Output Logic Low	$V_{OL}2$	—	0.4	V	4
TTL Output Logic High	$V_{OH}2$	2.4	—	V	5

NOTES:
1. 0 V ≤ V_{in} ≤ V_{DDQ} for all logic input pins.
2. $I_{OL}1$ ≤ 100 µA @ V_{OL} = 0.2 V. Sampled, not 100% tested.
3. $|I_{OH}1|$ ≤ 100 µA @ V_{DDQ} – 0.2 V. Sampled, not 100% tested.
4. $I_{OL}2$ ≤ 8 mA @ V_{OL} = 0.4 V
5. $|I_{OH}2|$ ≤ 8 mA @ V_{OH} = 2.4 V

TAP AC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T_A ≤ 70 °C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V

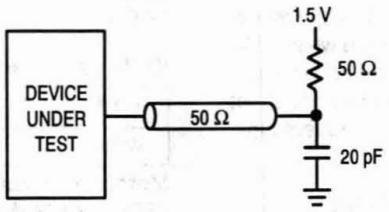
Output Test Load ..... 50 Ω Parallel Terminated T–line with 20 pF Receiver Input Capacitance
Test Load Termination Supply Voltage (V_T) ..... 1.5 V

TAP CONTROLLER TIMING

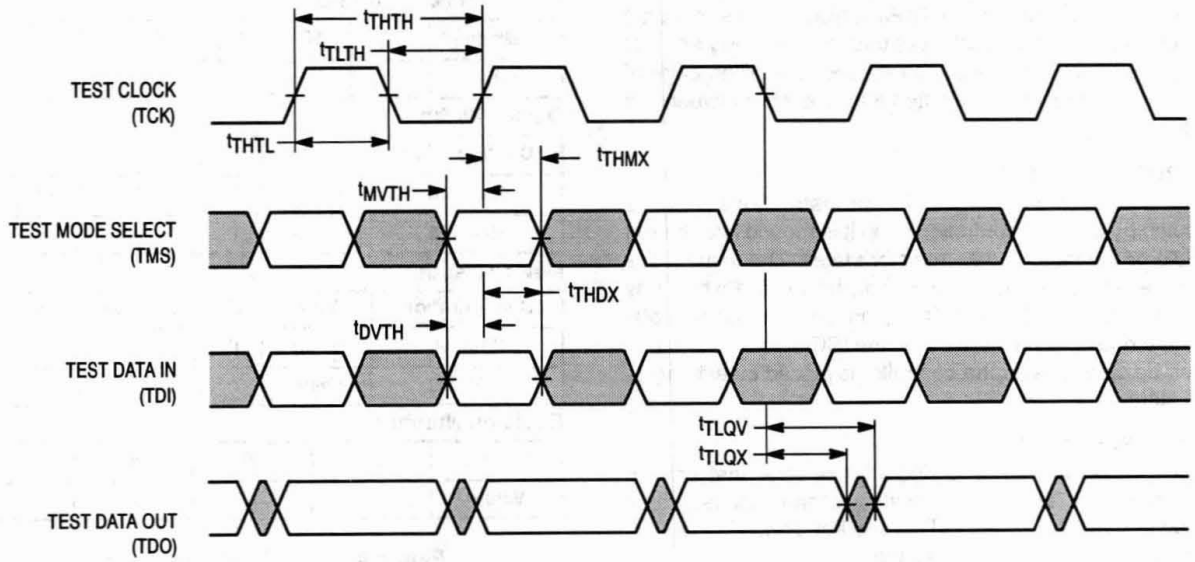
Parameter	Symbol	Min	Max	Unit	Notes
Cycle Time	t_{THTH}	100	—	ns	
Clock High Time	t_{THTL}	40	—	ns	
Clock Low Time	t_{TLTH}	40	—	ns	
TMS Setup	t_{MVTH}	10	—	ns	
TMS Hold	t_{THMX}	10	—	ns	
TDI Valid to TCK High	t_{DVTH}	10	—	ns	
TCK High to TDI Don't Care	t_{THDX}	10	—	ns	
Capture Setup	t_{CS}	10	—	ns	1
Capture Hold	t_{CH}	10	—	ns	1
TCK Low to TDO Unknown	t_{TLQX}	0	—	ns	
TCK Low to TDO Valid	t_{TLOV}	—	20	ns	

NOTES:
1. t_{CS} + t_{CH} defines the minimum pause in RAM I/O pad transitions to assure accurate pad data capture.

AC TEST LOAD



TAP CONTROLLER TIMING DIAGRAM



TEST ACCESS PORT PINS

TCK – TEST CLOCK (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

TMS – TEST MODE SELECT (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.

TDI – TEST DATA IN (INPUT)

The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (refer to Figure 5 TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.

TDO – TEST DATA OUT (OUTPUT)

Output that is active depending on the state of the TAP state machine (refer to Figure 5 TAP Controller State Diagram). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

TRST – TAP RESET

This device does not have a TRST pin. TRST is optional in **IEEE 1149.1.** The test–logic reset state is entered while TMS is held high for five rising edges of TCK. Power on reset circuitry is included internally. This type of reset does not affect the operation of the system logic. The reset affects test logic only.

TEST ACCESS PORT REGISTERS

OVERVIEW

The various TAP registers are selected (one at a time) via the sequences of ones and zeros input to the TMS pin as the TCK is strobed. Each of the TAPs registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on subsequent falling edge of TCK. When a register is selected it is "placed" between the TDI and TDO pins.

INSTRUCTION REGISTER

The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run test/idle or the various data register states. The instructions are three bits long. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power–up or whenever the controller is placed in test–logic–reset state.

BYPASS REGISTER

The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.

BOUNDARY SCAN REGISTER

The boundary scan register is identical in length to the number of active input and I/O connections on the RAM (not counting the TAP pins). This also includes a number of place holder locations (always set to a logic 1) reserved for density upgrade address pins. There are a total of 70 bits in the case of the x36 device and 51 bits in the case of the x18 device. The boundary scan register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture–DR state and then is placed between the TDI and TDO pins when the controller is moved to shift–DR state. Several TAP instructions can be used to activate the boundary scan register.

The Bump/Bit Scan Order tables describe which device bump connects to each boundary scan register location. The first column defines the bit's position in the boundary scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the input or I/O at the bump and the third column is the bump number.

IDENTIFICATION (ID) REGISTER

The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture–DR state with the IDCODE command loaded in the instruction register. The code is loaded from a 32 bit on–chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into shift–DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Presence Indicator

Bit #	0
Value	1

Motorola JEDEC ID Code (Compressed Format, per IEEE Standard 1149.1 – 1990

Bit #	11	10	9	8	7	6	5	4	3	2	1
Value	0	0	0	0	0	0	0	1	1	1	0

Reserved For Future Use

Bit #	17	16	15	14	13	12
Value	x	x	x	x	x	x

Device Width

Configuration	Bit #	22	21	20	19	18
128Kx36	Value	0	0	1	0	0
256Kx18	Value	0	0	0	1	1

Device Depth

Configuration	Bit #	27	26	25	24	23
128Kx36	Value	0	0	1	0	1
256Kx18	Value	0	0	1	1	0

Revision Number

Bit #	31	30	29	28
Value	x	x	x	x

Figure 4. ID Register Bit Meanings

MCM69R737A Bump/Bit Scan Order

BIT #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	SA	3B
2	SA	4P		37	NC	2B
3	SA	4T		38	SA	3A
4	SA	6R		39	SA	3C
5	SA	5T		40	SA	2C
6	ZZ	7T		41	SA	2A
7	DQa	6P		42	DQc	2D
8	DQa	7P		43	DQc	1D
9	DQa	6N		44	DQc	2E
10	DQa	7N		45	DQc	1E
11	DQa	6M		46	DQc	2F
12	DQa	6L		47	DQc	2G
13	DQa	7L		48	DQc	1G
14	DQa	6K		49	DQc	2H
15	DQa	7K		50	DQc	1H
16	$\overline{SBa}$	5L		51	$\overline{SBc}$	3G
17	$\overline{CK}$	4L		52	NC	4D
18	CK	4K		53	$\overline{SS}$	4E
19	$\overline{G}$	4F		54	NC	4G
20	$\overline{SBb}$	5G		55	NC	4H
21	DQb	7H		56	$\overline{SW}$	4M
22	DQb	6H		57	$\overline{SBd}$	3L
23	DQb	7G		58	DQd	1K
24	DQb	6G		59	DQd	2K
25	DQb	6F		60	DQd	1L
26	DQb	7E		61	DQd	2L
27	DQb	6E		62	DQd	2M
28	DQb	7D		63	DQd	1N
29	DQb	6D		64	DQd	2N
30	SA	6A		65	DQd	1P
31	SA	6C		66	DQd	2P
32	SA	5C		67	SA	3T
33	SA	5A		68	SA	2R
34	NC	6B		69	SA	4N
35	SA	5B		70	M1	3R

MCM69R819A Bump/Bit Scan Order

Bit #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	$\overline{SBb}$	3G
2	SA	6T		37	NC	4D
3	SA	4P		38	$\overline{SS}$	4E
4	SA	6R		39	NC	4G
5	SA	5T		40	NC	4H
6	ZZ	7T		41	$\overline{SW}$	4M
7	DQa	7P		42	DQb	2K
8	DQa	6N		43	DQb	1L
9	DQa	6L		44	DQb	2M
10	DQa	7K		45	DQb	1N
11	$\overline{SBa}$	5L		46	DQb	2P
12	$\overline{CK}$	4L		47	SA	3T
13	CK	4K		48	SA	2R
14	$\overline{G}$	4F		49	SA	4N
15	DQa	6H		50	SA	2T
16	DQa	7G		51	M1	3R
17	DQa	6F				
18	DQa	7E				
19	DQa	6D				
20	SA	6A				
21	SA	6C				
22	SA	5C				
23	SA	5A				
24	NC	6B				
25	SA	5B				
26	SA	3B				
27	NC	2B				
28	SA	3A				
29	SA	3C				
30	SA	2C				
31	SA	2A				
32	DQb	1D				
33	DQb	2E				
34	DQb	2G				
35	DQb	1H				

NOTES:

1. The NC pads listed in this table are indeed no connects, but are represented in the boundary scan register by a "place holder" bit that is forced to logic 1. These pads are reserved for use as address inputs on higher density RAMs that follow this pad out and scan order standard.
2. CK, $\overline{CK}$, are sampled individually. $\overline{CK}$ is not simply a forced complement of the CK input. In scan mode these differential inputs are referenced to each other.
3. M1 and M2 are not ordinary inputs and may not respond to standard I/O logic levels. M1 and M2 must be driven to within 100 mV of a V_{DD} or V_{SS} supply rail to ensure consistent results.
4. ZZ must remain at V_{IL} during boundary scan to ensure consistent results.

TAP Controller Instruction Set

OVERVIEW

There are two classes of instructions defined in the Standard 1149.1–1990; the standard (public) instructions, and device specific (private) instructions. Some public instructions, are mandatory for 1149.1 compliance. Optional public instructions must be implemented in prescribed ways.

Although the TAP controller in this device follows the 1149.1 conventions, it is not 1194.1 compliant because some of the mandatory instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads, but cannot be used to load address, data or control signals into the RAM or to preload the I/O buffers. In other words, the device will not perform Standard 1149.1 EXTEST, INTEST or the preload portion of the SAMPLE / PRELOAD command.

When the TAP controller is placed in capture–IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the shift–IR state the instruction register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to update–IR state. The TAP instruction sets for this device are listed in the following tables.

STANDARD (PUBLIC) INSTRUCTIONS

BYPASS

The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift–DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

Sample/preload is a Standard 1149.1 mandatory public instruction. When the sample / preload instruction is loaded in the Instruction register, moving the TAP controller into the capture–DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set–up plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register.

Moving the controller to shift–DR state then places the boundary scan register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the update–DR state with the SAMPLE / PRELOAD instruction loaded in the instruction register has the same effect as the pause–DR command. This functionality is not Standard 1149.1 compliant.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic 0s. EXTEST is not implemented in this device. Therefore this device is not 1149.1 compliant. Nevertheless, this RAMs TAP does respond to an all zeros instruction, as follows. With the EXTEST (000) instruction loaded in the instruction register the RAM responds just as it does in response to the SAMPLE / PRELOAD instruction described above, except the RAM outputs are forced to high–Z any time the instruction is loaded.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture–DR mode and places the ID register between the TDI and TDO pins in shift–DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test–logic–reset state.

THE DEVICE SPECIFIC (PUBLIC) INSTRUCTION

SAMPLE–Z

If the SAMPLE–Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high–Z) and the boundary scan register is connected between TDI and TDO when the TAP controller. is moved to the shift–DR state.

THE DEVICE SPECIFIC (PRIVATE) INSTRUCTION

NOOP

Do not use these instructions; they are reserved for future use.

STANDARD (PUBLIC) INSTRUCTION CODES

Instruction	Code*	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM outputs to High–Z state. *NOT 1149.1 COMPLIANT*
IDCODE	001**	Preloads ID register and places it between TDI and TDO. Does not affect RAM operation.
SAMPLE / PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect RAM operation. Does not implement 1149.1 Preload function. * NOT 1149.1 COMPLIANT *
BYPASS	111	Places bypass register between TDI and TDO. Does not affect RAM operation.
SAMPLE–Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM output drivers to High–Z.

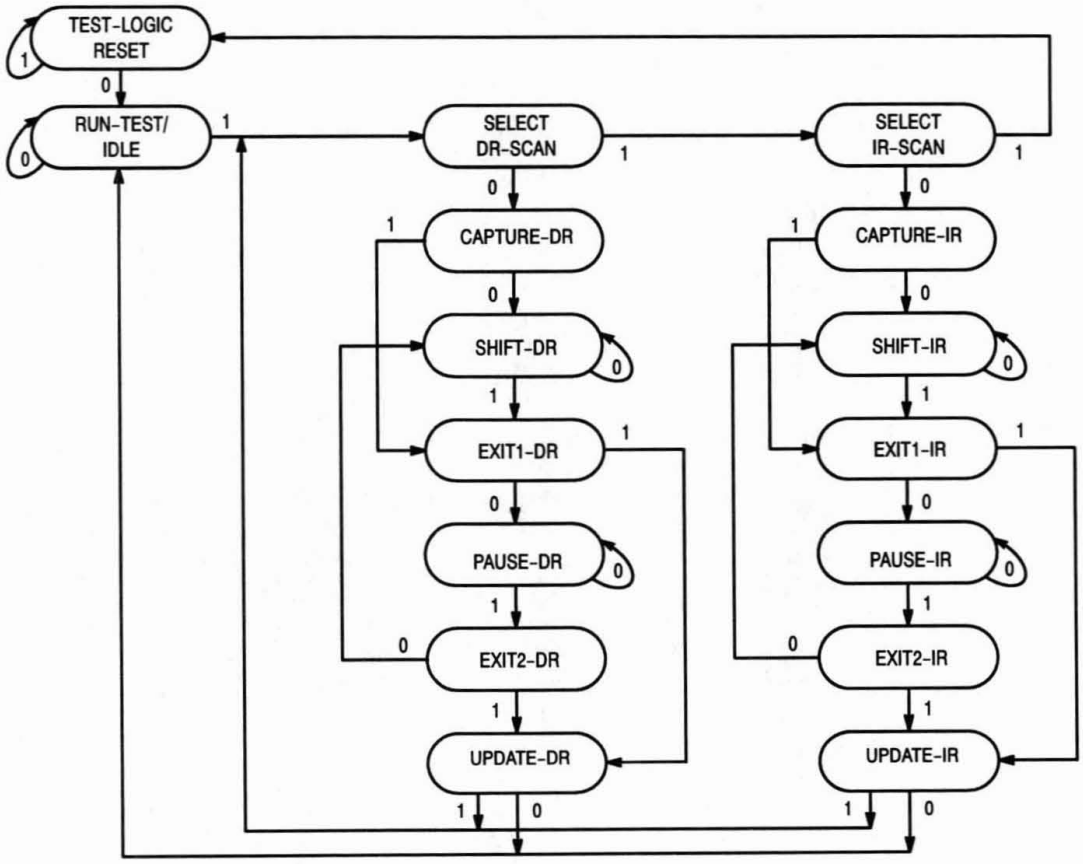
* Instruction codes expressed in binary, MSB on left, LSB on right.
** Default instruction automatically loaded at power–up and in test–logic–reset state.

3

STANDARD (PRIVATE) INSTRUCTION CODES

Instruction	Code*	Description
NO OP	011	Do not use these instructions; they are reserved for future use.
NO OP	101	Do not use these instructions; they are reserved for future use.
NO OP	110	Do not use these instructions; they are reserved for future use.

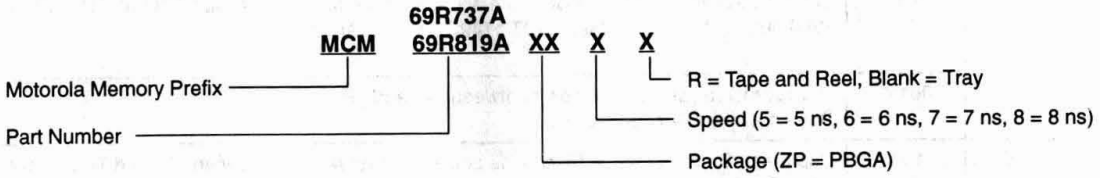
* Instruction codes expressed in binary, MSB on left, LSB on right.



NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 5. TAP Controller State Diagram

ORDERING INFORMATION
(Order by Full Part Number)


69R737A
MCM 69R819A XX X X
Motorola Memory Prefix
Part Number
R = Tape and Reel, Blank = Tray
Speed (5 = 5 ns, 6 = 6 ns, 7 = 7 ns, 8 = 8 ns)
Package (ZP = PBGA)

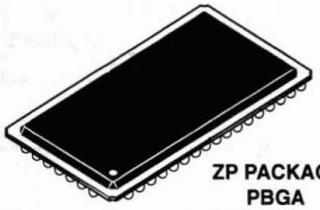
Full Part Numbers — MCM69R737AZP5 MCM69R737AZP6 MCM69R737AZP7 MCM69R737AZP8
MCM69R819AZP5 MCM69R819AZP6 MCM69R819AZP7 MCM69R819AZP8
MCM69R737AZP5R MCM69R737AZP6R MCM69R737AZP7R MCM69R737AZP8R
MCM69R819AZP5R MCM69R819AZP6R MCM69R819AZP7R MCM69R819AZP8R

3

MCM69R738
MCM69R820

Advance Information

4M Late Write 2.5 V I/O



ZP PACKAGE
PBGA
CASE 999–01

3

The MCM69R738/820 is a 4 megabit synchronous late write fast static RAM designed to provide high performance in secondary cache and ATM switch, Telecom, and other high speed memory applications. The MCM69R820 organized as 256K words by 18 bits, and the MCM69R738 organized as 128K words by 36 bits wide are fabricated in Motorola's high performance silicon gate BiCMOS technology.

The differential CK clock inputs control the timing of read/write operations of the RAM. At the rising edge of the CK clock all addresses, write enables, and synchronous selects are registered. An internal buffer and special logic enable the memory to accept write data on the rising edge of the CK clock a cycle after address and control signals. Read data is driven on the rising edge of the CK clock also.

The RAM uses 2.5 V inputs and outputs.

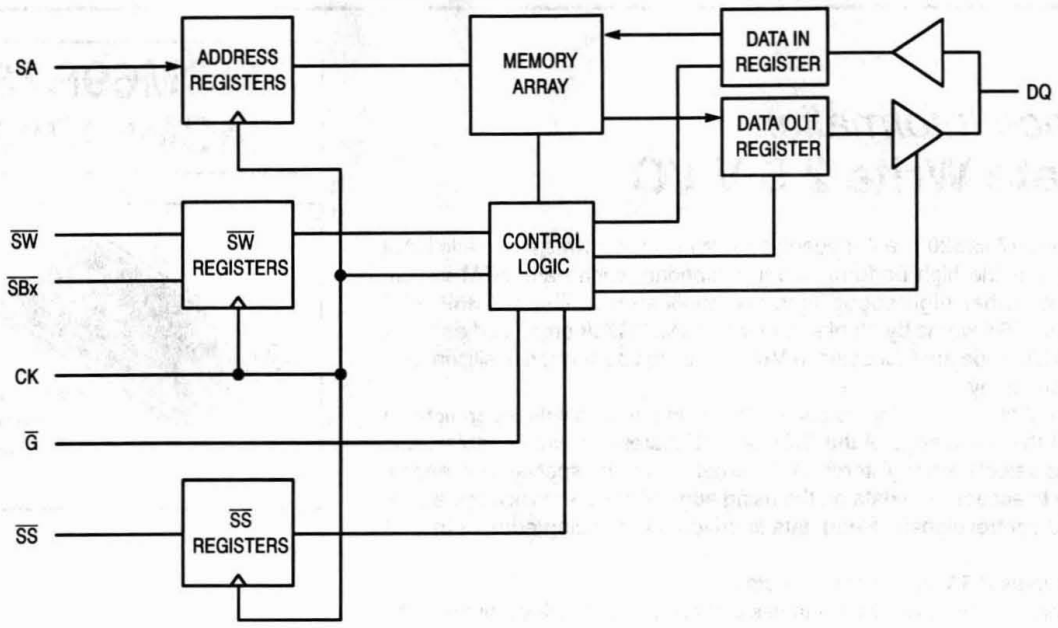
The synchronous write and byte enables allow writing to individual bytes or the entire word.

- Byte Write Control
- Single 3.3 V +10%, – 5% Operation
- 2.5 V I/O
- Register to Register Synchronous Operation
- Asynchronous Output Enable
- Boundary Scan (JTAG) IEEE 1149.1 Compatible
- Differential Clock Inputs
- Optional x 18 or x 36 organization
- MCM69R738/820–7 = 7 ns
  MCM69R738/820–8 = 8 ns
- 119 Bump, 50 mil (1.27 mm) Pitch, 14 mm x 22 mm Plastic Ball Grid Array (PBGA) Package

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 3
4/3/97

FUNCTIONAL BLOCK DIAGRAM



3

PIN ASSIGNMENTS

TOP VIEW

MCM69R738

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	SA	NC	SA	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
E	DQc	DQc	V_{SS}	$\overline{SS}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{G}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{SBc}$	NC	$\overline{SBb}$	DQb	DQb
H	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CK	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{SBd}$	$\overline{CK}$	$\overline{SBa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{SW}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
P	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
R	NC	SA	V_{SS}	V_{DD}	V_{DD}	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69R820

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	SA	NC	SA	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQb	NC	V_{SS}	NC	V_{SS}	DQa	NC
E	NC	DQb	V_{SS}	$\overline{SS}$	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	$\overline{SBb}$	NC	V_{SS}	NC	DQa
H	DQb	NC	V_{SS}	NC	V_{SS}	DQa	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	CK	V_{SS}	NC	DQa
L	DQb	NC	V_{SS}	$\overline{CK}$	$\overline{SBa}$	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{SW}$	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	SA	V_{SS}	DQa	NC
P	NC	DQb	V_{SS}	SA	V_{SS}	NC	DQa
R	NC	SA	V_{SS}	V_{DD}	V_{DD}	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69R738 PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6K, 7K, 6L, 7L, 6M, 6N, 7N, 6P, 7P (b) 6D, 7D, 6E, 7E, 6F, 6G, 7G, 6H, 7H (c) 1D, 2D, 1E, 2E, 2F, 1G, 2G, 1H, 2H (d) 1K, 2K, 1L, 2L, 2M, 1N, 2N, 1P, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 3T, 4T, 5T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 5G, 3G, 3L (a), (b), (c), (d)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
7T	ZZ	Input	Enables sleep mode.
4C, 2J, 4J, 6J, 4R, 5R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 3H, 5H, 3K, 5K, 3M, 5M, 3N, 5N, 3P, 5P, 3R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 4B, 6B, 7B, 1C, 7C, 4D, 4G, 4H, 3J, 5J, 1R, 7R, 1T, 2T, 6T, 6U	NC	—	No Connection: There is no connection to the chip. Note: 3J and 5J are tied common.

3

MCM69R820 PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6D, 7E, 6F, 7G, 6H, 7K, 6L, 6N, 7P (b) 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 2T, 3T, 5T, 6T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 3G (a), (b)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
7T	ZZ	Input	Enables sleep mode.
4C, 2J, 4J, 6J, 4R, 5R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P, 3R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 4B, 6B, 7B, 1C, 7C, 2D, 4D, 7D, 1E, 6E, 2F, 1G, 4G, 6G, 2H, 4H, 7H, 3J, 5J, 1K, 6K, 2L, 7L, 6M, 2N, 7N, 1P, 6P, 1R, 7R, 1T, 4T, 6U	NC	—	No Connection: There is no connection to the chip. Note: 3J and 5J are tied common.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS}, See Note 1)

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Output Supply Voltage	V_{DDQ}	– 0.5 to V_{DD} + 0.5	V
Voltage On Any Pin	V_{in}	– 0.5 to V_{DD} + 0.5	V
Input Current (per I/O)	I_{in}	± 50	mA
Output Current (per I/O)	I_{out}	± 70	mA
Power Dissipation (See Note 2)	P_D	—	W
Operating Temperature	T_A	0 to + 70	°C
Temperature Under Bias	T_{bias}	–10 to + 85	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability will be dependent upon package characteristics and use environment. See enclosed thermal impedance data.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

3

PBGA PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (Still Air)		$R_{\theta JA}$	53	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Single Layer Board	$R_{\theta JA}$	38	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Four Layer Board	$R_{\theta JA}$	22	°C/W	
Junction to Board (Bottom)		$R_{\theta JB}$	14	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	5	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

($0°C \le T_A \le 70°C$, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (See Notes 1 through 4)

Parameter	Symbol	Min	Typical –7	Typical –8	Max	Unit	Notes
Core Power Supply Voltage	V_{DD}	3.15	—	—	3.6	V	
Output Driver Supply Voltage	V_{DDQ}	2.3	—	—	2.7	V	
Active Power Supply Current (x18) (x36)	I_{DD1}	—	330 390	320 370	430 490	mA	5
Quiescent Active Power Supply Current	I_{DD2}	—	180	180	250	mA	6, 10
Active Standby Power Supply Current	I_{SB1}	—	160	160	250	mA	7
Quiescent Standby Power Supply Current	I_{SB2}	—	140	140	230	mA	8, 10
Sleep Mode Power Supply Current	I_{SB3}	—	30	30	50	mA	9, 10

NOTES:
1. All data sheet parameters specified to full range of V_{DD} unless otherwise noted. All voltages are referenced to voltage applied to V_{SS} bumps.
2. Supply voltage applied to V_{DD} connections.
3. Supply voltage applied to V_{DDQ} connections.
4. All power supply currents measured with outputs open or deselected.
5. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered active, 50% read cycles.
6. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered active.
7. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered inactive.
8. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered inactive. ZZ low.
9. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered inactive, ZZ high.
10. $200 \text{ mV} \ge V_{in} \ge V_{DDQ} - 200 \text{ mV}$.

DC INPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
DC Input Logic High	V_{IH} (dc)	1.7	$V_{DD} + 0.3$	V	
DC Input Logic Low	V_{IL} (dc)	– 0.3	0.7	V	1
Input Leakage Current	$I_{lkg(1)}$	—	± 5	µA	2
Clock Input Leakage Current	$I_{clkg(1)}$	—	± 8	µA	2
Clock Input Signal Voltage	V_{in}	– 0.3	$V_{DDQ} + 0.3$	V	
Clock Input Differential Voltage	V_{DIF} (dc)	0.2	$V_{DDQ} + 0.6$	V	3
Clock Input Common Mode Voltage Range (See Figure 3)	V_{CM} (dc)	1.1	2.1	V	4

NOTES:
1. Inputs may undershoot to – 0.5 V (peak) for up to 20% t_{KHKH} (e.g., 2 ns at a clock cycle time of 10 ns).
2. $0 \text{ V} \le V_{in} \le V_{DDQ}$ for all pins.
3. Minimum instantaneous differential input voltage required for differential input clock operation.
4. Maximum rejectable common mode input voltage variation.

DC OUTPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
Output Leakage Current	$I_{lkg(0)}$	–1.0	1.0	µA	
Output Low Voltage	V_{OL}	—	0.7	V	1
Output High Voltage	V_{OH}	1.7	—	V	2

NOTES:
1. $I_{OL} = 8.0$ mA
2. $I_{OH} = -8.0$ mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, $0 °C \le T_A \le 70°C$, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	5	5	pF
Input/Output Capacitance	$C_{I/O}$	6	8	pF
CK, $\overline{CK}$ Capacitance	C_{CK}	6	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

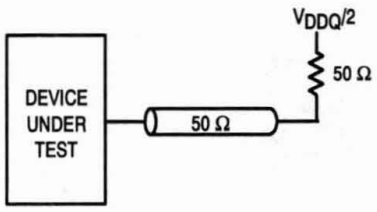
(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 2.5 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.25 V
Output Timing Reference Level ..... 1.25 V
Clock Input Timing Reference Level ..... Differential Cross–Point
Clock Input Pulse Level ..... 1.8 V to 2.1 V

READ/WRITE CYCLE TIMING (See Note 3)

Parameter	Symbol	MCM69R738–7 MCM69R820–7		MCM69R738–8 MCM69R820–8		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{KHKH}	7	—	8	—	ns	
Clock High Pulse Width	t_{KHKL}	2.8	—	3.2	—	ns	
Clock Low Pulse Width	t_{KLKH}	2.8	—	3.2	—	ns	
Clock High to Output Low–Z	t_{KHQX1}	1	—	1	—	ns	2
Clock High to Output Valid	t_{KHQV}	—	3.5	—	4	ns	1
Clock High to Output Hold	t_{KHQX}	0.5	—	0.5	—	ns	1
Clock High to Output High–Z	t_{KHQZ}	0	3.5	0	4	ns	2
Output Enable Low to Output Low–Z	t_{GLQX}	0.5	—	0.5	—	ns	2
Output Enable Low to Output Valid	t_{GLQV}	—	3.5	—	4	ns	1
Output Enable to Output Hold	t_{GHQX}	0.5	—	0.5	—	ns	1
Output Enable High to Output High–Z	t_{GHQZ}	—	3.5	—	4	ns	2
Setup Times: Address Data In Chip Select Write Enable	t_{AVKH} t_{DVKH} t_{SVKH} t_{WVKH}	0.5	—	0.5	—	ns	
Hold Times: Address Data In Chip Select Write Enable	t_{KHAX} t_{KHDX} t_{KHSX} t_{KHWX}	1	—	1	—	ns	

NOTES:
1. Tested per AC Test Load diagram. See Figure 1.
2. Measured at ± 200 mV from steady state.
3. In no case may control input signals (e.g., $\overline{SS}$) be operated with pulse widths less than the minimum clock input pulse width specifications (e.g., t_{KHKL}) or at frequencies that exceed the applied K clock frequency.



TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Figure 1. AC Test Load

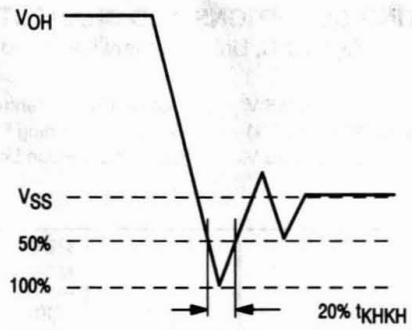
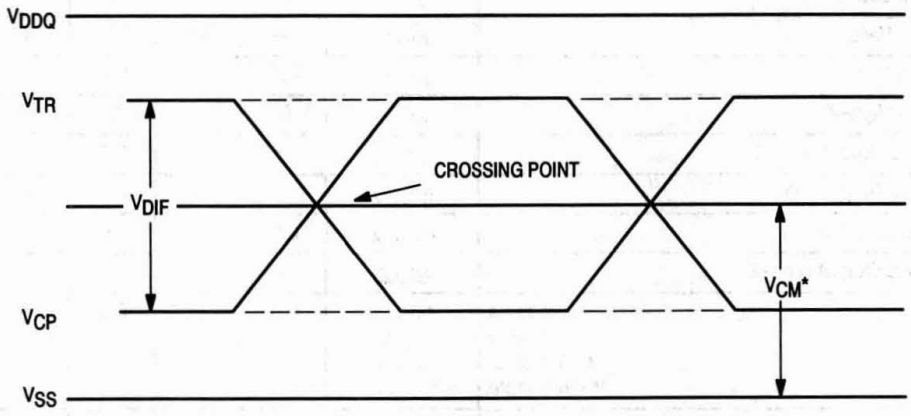


Figure 2. Undershoot Voltage

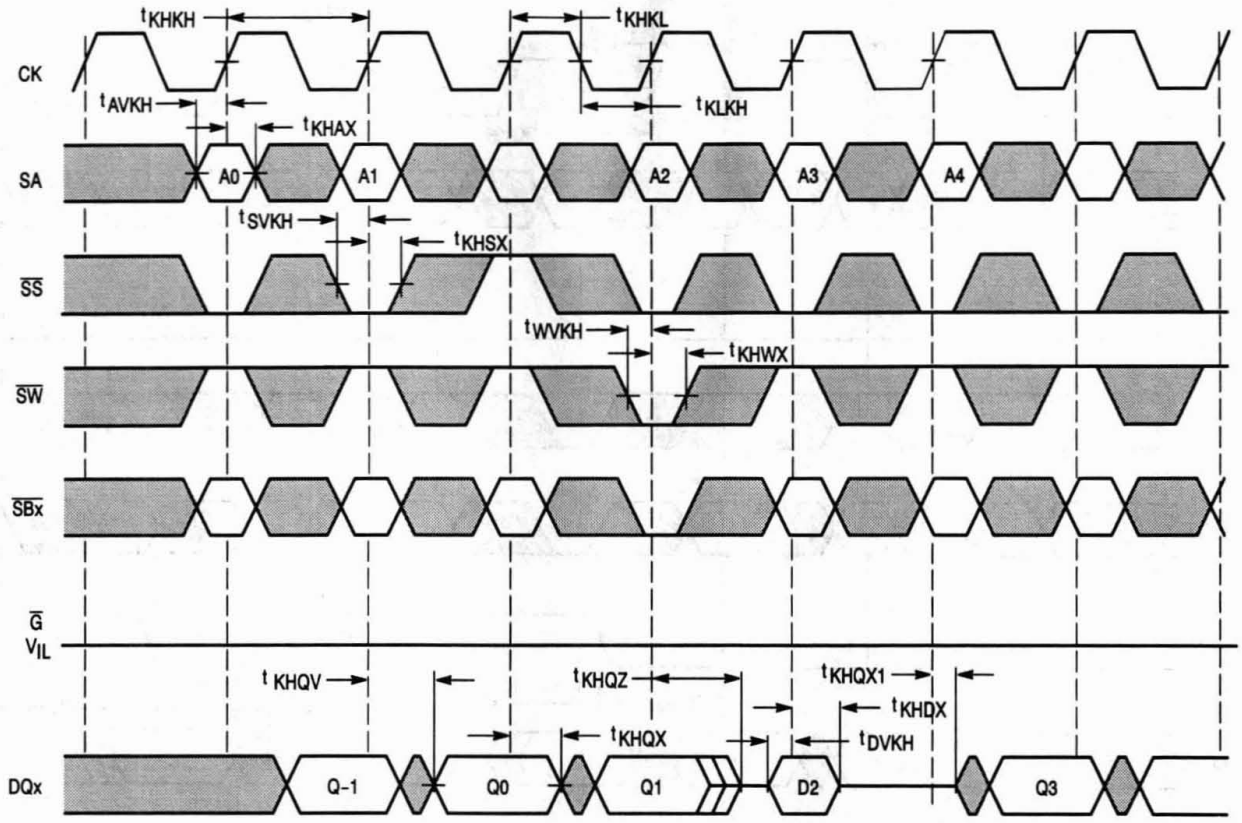
3



* V_{CM}, the Common Mode Input Voltage, equals $V_{TR} - ((V_{TR} - V_{CP})/2)$.

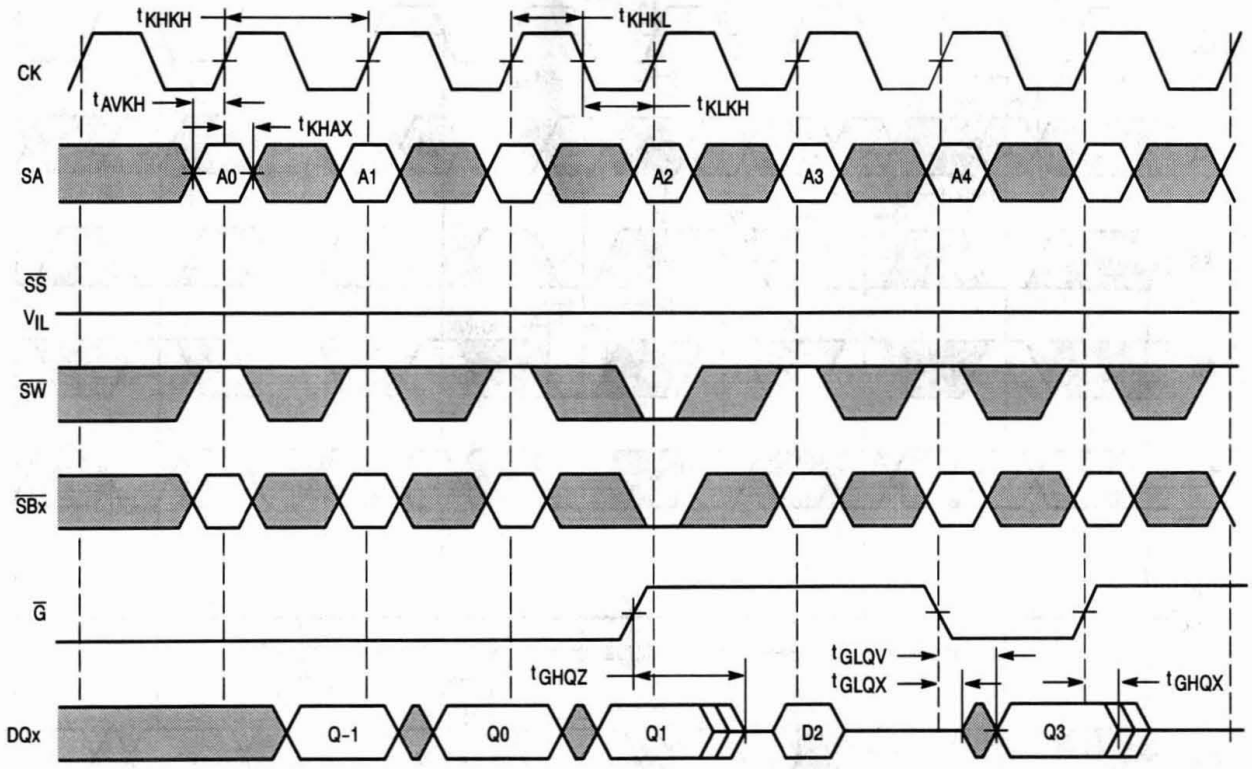
Figure 3. Differential Inputs/ Common Mode Input Voltage

REGISTER/REGISTER READ–WRITE–READ CYCLES



3

REGISTER/REGISTER READ–WRITE–READ
($\overline{G}$ Controlled)



FUNCTIONAL OPERATION

READ AND WRITE OPERATIONS

All control signals except $\overline{G}$ are registered on the rising edge of the CK clock. These signals must meet the setup and hold times shown in the AC Characteristics table. On the rising edge of the following clock, read data is clocked into the output register and available at the outputs at t_{KHQV}. During this same cycle a new read address can be applied to the address pins.

A deselect cycle (dead cycle) must occur prior to a write cycle. Read cycles may follow write cycles immediately.

$\overline{G}$, $\overline{SS}$, and $\overline{SW}$ control output drive. Chip deselect via a high on $\overline{SS}$ at the rising edge of the CK clock has its effect on the output drivers after the next rising edge of the CK clock. $\overline{SW}$ low deselects the output drivers immediately (on the same cycle). Output selecting via a low on $\overline{SS}$ and high on $\overline{SW}$ at a rising CK clock has its effect on the output drivers after the next rising edge of the CK clock. Output drive is also controlled directly by output enable, $\overline{G}$. $\overline{G}$ is an asynchronous input. No clock edges are required to enable/disable the output using $\overline{G}$.

Output data will be valid the latter of t_{GLQV} and t_{KHQV}. Outputs will begin driving at t_{KHQX1}. Outputs will hold previous data until t_{KHQX} or t_{GHQX}.

WRITE AND BYTE WRITE FUNCTIONS

Note that in the following discussion the term "byte" refers to nine bits of the RAM I/O bus. In all cases, the timing parameters described for synchronous write input ($\overline{SW}$) apply to each of the byte write enable inputs ($\overline{SBa}$, $\overline{SBb}$, etc.).

Byte write enable inputs have no effect on read cycles. This allows the system designer not interested in performing byte writes to connect the byte enable inputs to active low (V_{SS}). Reads of all bytes proceed normally and write cycles, activated via a low on $\overline{SW}$, and the rising edge of the CK clock, write the entire RAM I/O width. This way the designer is spared having to drive multiple write input buffer loads.

Byte writes are performed using the byte write enable inputs in conjunction with the synchronous write input ($\overline{SW}$). It is important to note that writing any one byte will inhibit a read of all bytes at the current address. The RAM cannot simultaneously read one byte and write another at the same address. A write cycle initiated with none of the byte write enable inputs active is neither a read or a write. No write will occur, but the outputs will be deselected as in a normal write cycle.

LATE WRITE

The write address is sampled on the first rising edge of clock and write data is sampled on the following rising edge.

The late write feature is implemented with single stage write buffering. Write buffering is transparent to the user. A comparator monitors the address bus and, when necessary, routes buffer contents to the outputs to assure coherent operation. This occurs in all cases whether there is a byte write or a full word is written.

POWER UP AND INITIALIZATION

Once supplies have reached specification levels, a minimum dwell of 1.0 µs with CK clock inputs cycling is required before beginning normal operations.

SERIAL BOUNDARY SCAN TEST ACCESS PORT OPERATION

OVERVIEW

The serial boundary scan test access port (TAP) on this RAM is designed to operate in a manner consistent with IEEE Standard 1149.1–1990 (commonly referred to as JTAG), but does not implement all of the functions required for 1149.1 compliance. Certain functions have been modified or eliminated because their implementation places extra delays in the RAMs critical speed path. Nevertheless, the RAM supports the standard TAP controller architecture. (The TAP controller is the state machine that controls the TAPs operation) and can be expected to function in a manner that does not conflict with the operation of devices with Standard 1149.1 compliant TAPs. The TAP operates using conventional JEDEC Standard 8–1B Low Voltage (3.3 V) TTL / CMOS logic level signaling.

DISABLING THE TEST ACCESS PORT

It is possible to use this device without utilizing the TAP. To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid level inputs. TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a 1 k resistor. TDO should be left unconnected.

3

TAP DC OPERATING CHARACTERISTICS

($0°C \le T_A \le 70°C$, Unless Otherwise Noted)

Parameter	Symbol	Min	Max	Unit	Note
Logic Input Logic High	$V_{IH}1$	2.0	V_{DD} + 0.3	V	
Logic Input Logic Low	$V_{IL}1$	– 0.3	0.8	V	
Logic Input Leakage Current	I_{lkg}	—	± 5	µA	1
CMOS Output Logic Low	$V_{OL}1$	—	0.2	V	2
CMOS Output Logic High	$V_{OH}1$	V_{DD} – 0.2	—	V	3
TTL Output Logic Low	$V_{OL}2$	—	0.4	V	4
TTL Output Logic High	$V_{OH}2$	2.4	—	V	5

NOTES:
1. $0 V \pm V_{in} \pm V_{DDQ}$ for all logic input pins.
2. $I_{OL}1 \le 100$ µA @ $V_{OL} = 0.2$ V. Sampled, not 100% tested.
3. $|I_{OH}1| \le 100$ µA @ $V_{DDQ} - 0.2$ V. Sampled, not 100% tested.
4. $I_{OL}2 \le 8$ mA @ $V_{OL} = 0.4$ V
5. $|I_{OH}2| \le 8$ mA @ $V_{OH} = 2.4$ V

TAP AC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V

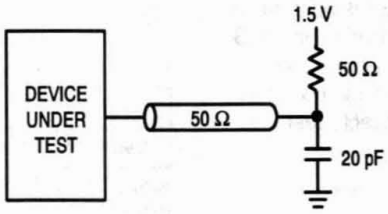
Output Test Load ..... 50 Ω Parallel Terminated T–line with 20 pF Receiver Input Capacitance
Test Load Termination Supply Voltage (V_T) ..... 1.5 V

TAP CONTROLLER TIMING

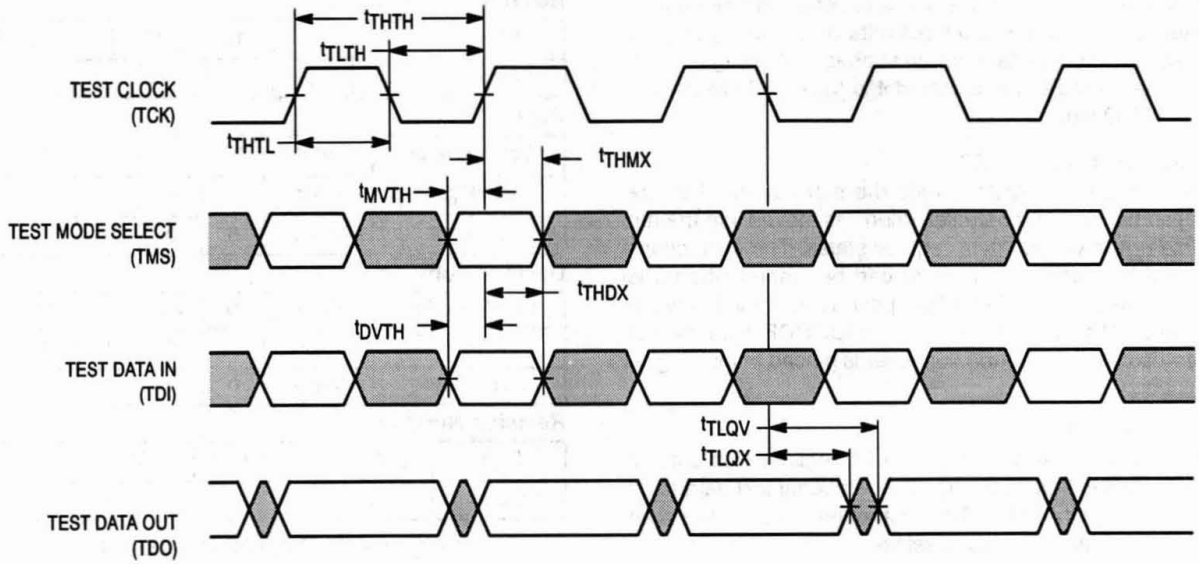
Parameter	Symbol	Min	Max	Unit	Notes
Cycle Time	t_{THTH}	100	—	ns	
Clock High Time	t_{THTL}	40	—	ns	
Clock Low Time	t_{TLTH}	40	—	ns	
TMS Setup	t_{MVTH}	10	—	ns	
TMS Hold	t_{THMX}	10	—	ns	
TDI Valid to TCK High	t_{DVTH}	10	—	ns	
TCK High to TDI Don't Care	t_{THDX}	10	—	ns	
Capture Setup	t_{CS}	10	—	ns	1
Capture Hold	t_{CH}	10	—	ns	1
TCK Low to TDO Unknown	t_{TLQX}	0	—	ns	
TCK Low to TDO Valid	t_{TLOV}	—	20	ns	

NOTES:
1. t_{CS} + t_{CH} defines the minimum pause in RAM I/O pad transitions to assure accurate pad data capture.

AC TEST LOAD



TAP CONTROLLER TIMING DIAGRAM



TEST ACCESS PORT PINS

TCK – TEST CLOCK (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

TMS – TEST MODE SELECT (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.

TDI – TEST DATA IN (INPUT)

The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (refer to Figure 5 TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.

TDO – TEST DATA OUT (OUTPUT)

Output that is active depending on the state of the TAP state machine (refer to Figure 5 TAP Controller State Diagram). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

TRST – TAP RESET

This device does not have a TRST pin. TRST is optional in **IEEE 1149.1.** The test–logic reset state is entered while TMS is held high for five rising edges of TCK. Power on reset circuitry is included internally. This type of reset does not affect the operation of the system logic. The reset affects test logic only.

TEST ACCESS PORT REGISTERS

OVERVIEW

The various TAP registers are selected (one at a time) via the sequences of ones and zeros input to the TMS pin as the TCK is strobed. Each of the TAPs registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on subsequent falling edge of TCK. When a register is selected it is "placed" between the TDI and TDO pins.

INSTRUCTION REGISTER

The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run test/idle or the various data register states. The instructions are three bits long. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power–up or whenever the controller is placed in test–logic–reset state.

BYPASS REGISTER

The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.

BOUNDARY SCAN REGISTER

The boundary scan register is identical in length to the number of active input and I/O connections on the RAM (not counting the TAP pins). This also includes a number of place holder locations (always set to a logic 1) reserved for density upgrade address pins. There are a total of 70 bits in the case of the x36 device and 51 bits in the case of the x18 device. The boundary scan register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture–DR state and then is placed between the TDI and TDO pins when the controller is moved to shift–DR state. Several TAP instructions can be used to activate the boundary scan register.

The Bump/Bit Scan Order tables describe which device bump connects to each boundary scan register location. The first column defines the bit's position in the boundary scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the input or I/O at the bump and the third column is the bump number.

IDENTIFICATION (ID) REGISTER

The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture–DR state with the IDCODE command loaded in the instruction register. The code is loaded from a 32 bit on–chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into shift–DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Presence Indicator

Bit #	0
Value	1

Motorola JEDEC ID Code (Compressed Format, per IEEE Standard 1149.1 – 1990

Bit #	11	10	9	8	7	6	5	4	3	2	1
Value	0	0	0	0	0	0	0	1	1	1	0

Reserved For Future Use

Bit #	17	16	15	14	13	12
Value	x	x	x	x	x	x

Device Width

Configuration	Bit #	22	21	20	19	18
128Kx36	Value	0	0	1	0	0
256Kx18	Value	0	0	0	1	1

Device Depth

Configuration	Bit #	27	26	25	24	23
128Kx36	Value	0	0	1	0	1
256Kx18	Value	0	0	1	1	0

Revision Number

Bit #	31	30	29	28
Value	x	x	x	x

Figure 4. ID Register Bit Meanings

MCM69R738 Bump/Bit Scan Order

BIT #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	SA	3B
2	SA	4P		37	NC	2B
3	SA	4T		38	SA	3A
4	SA	6R		39	SA	3C
5	SA	5T		40	SA	2C
6	ZZ	7T		41	SA	2A
7	DQa	6P		42	DQc	2D
8	DQa	7P		43	DQc	1D
9	DQa	6N		44	DQc	2E
10	DQa	7N		45	DQc	1E
11	DQa	6M		46	DQc	2F
12	DQa	6L		47	DQc	2G
13	DQa	7L		48	DQc	1G
14	DQa	6K		49	DQc	2H
15	DQa	7K		50	DQc	1H
16	$\overline{SBa}$	5L		51	$\overline{SBc}$	3G
17	$\overline{CK}$	4L		52	NC	4D
18	CK	4K		53	$\overline{SS}$	4E
19	$\overline{G}$	4F		54	NC	4G
20	$\overline{SBb}$	5G		55	NC	4H
21	DQb	7H		56	$\overline{SW}$	4M
22	DQb	6H		57	$\overline{SBd}$	3L
23	DQb	7G		58	DQd	1K
24	DQb	6G		59	DQd	2K
25	DQb	6F		60	DQd	1L
26	DQb	7E		61	DQd	2L
27	DQb	6E		62	DQd	2M
28	DQb	7D		63	DQd	1N
29	DQb	6D		64	DQd	2N
30	SA	6A		65	DQd	1P
31	SA	6C		66	DQd	2P
32	SA	5C		67	SA	3T
33	SA	5A		68	SA	2R
34	NC	6B		69	SA	4N
35	SA	5B		70	M1	3R

MCM69R820 Bump/Bit Scan Order

Bit #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	$\overline{SBb}$	3G
2	SA	6T		37	NC	4D
3	SA	4P		38	$\overline{SS}$	4E
4	SA	6R		39	NC	4G
5	SA	5T		40	NC	4H
6	ZZ	7T		41	$\overline{SW}$	4M
7	DQa	7P		42	DQb	2K
8	DQa	6N		43	DQb	1L
9	DQa	6L		44	DQb	2M
10	DQa	7K		45	DQb	1N
11	$\overline{SBa}$	5L		46	DQb	2P
12	$\overline{CK}$	4L		47	SA	3T
13	CK	4K		48	SA	2R
14	$\overline{G}$	4F		49	SA	4N
15	DQa	6H		50	SA	2T
16	DQa	7G		51	M1	3R
17	DQa	6F				
18	DQa	7E				
19	DQa	6D				
20	SA	6A				
21	SA	6C				
22	SA	5C				
23	SA	5A				
24	NC	6B				
25	SA	5B				
26	SA	3B				
27	NC	2B				
28	SA	3A				
29	SA	3C				
30	SA	2C				
31	SA	2A				
32	DQb	1D				
33	DQb	2E				
34	DQb	2G				
35	DQb	1H				

NOTES:

1. The NC pads listed in this table are indeed no connects, but are represented in the boundary scan register by a "place holder" bit that is forced to logic 1. These pads are reserved for use as address inputs on higher density RAMs that follow this pad out and scan order standard.
2. CK, $\overline{CK}$, are sampled individually. $\overline{CK}$ is not simply a forced complement of the CK input. In scan mode these differential inputs are referenced to each other.
3. M1 and M2 are not ordinary inputs and may not respond to standard I/O logic levels. M1 and M2 must be driven to within 100 mV of a V_{DD} or V_{SS} supply rail to ensure consistent results.
4. ZZ must remain at V_{IL} during boundary scan to ensure consistent results.

TAP Controller Instruction Set

OVERVIEW

There are two classes of instructions defined in the Standard 1149.1–1990; the standard (public) instructions, and device specific (private) instructions. Some public instructions, are mandatory for 1149.1 compliance. Optional public instructions must be implemented in prescribed ways.

Although the TAP controller in this device follows the 1149.1 conventions, it is not 1194.1 compliant because some of the mandatory instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads, but cannot be used to load address, data or control signals into the RAM or to preload the I/O buffers. In other words, the device will not perform Standard 1149.1 EXTEST, INTEST or the preload portion of the SAMPLE / PRELOAD command.

When the TAP controller is placed in capture–IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the shift–IR state the instruction register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to update–IR state. The TAP instruction sets for this device are listed in the following tables.

STANDARD (PUBLIC) INSTRUCTIONS

BYPASS

The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift–DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

Sample/preload is a Standard 1149.1 mandatory public instruction. When the sample / preload instruction is loaded in the Instruction register, moving the TAP controller into the capture–DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set–up plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register.

Moving the controller to shift–DR state then places the boundary scan register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the update–DR state with the SAMPLE / PRELOAD instruction loaded in the instruction register has the same effect as the pause–DR command. This functionality is not Standard 1149.1 compliant.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic 0s. EXTEST is not implemented in this device. Therefore this device is not 1149.1 compliant. Nevertheless, this RAMs TAP does respond to an all zeros instruction, as follows. With the EXTEST (000) instruction loaded in the instruction register the RAM responds just as it does in response to the SAMPLE / PRELOAD instruction described above, except the RAM outputs are forced to high–Z any time the instruction is loaded.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture–DR mode and places the ID register between the TDI and TDO pins in shift–DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test–logic–reset state.

THE DEVICE SPECIFIC (PUBLIC) INSTRUCTION

SAMPLE–Z

If the SAMPLE–Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high–Z) and the boundary scan register is connected between TDI and TDO when the TAP controller. is moved to the shift–DR state.

THE DEVICE SPECIFIC (PRIVATE) INSTRUCTION

NOOP

Do not use these instructions; they are reserved for future use.

STANDARD (PUBLIC) INSTRUCTION CODES

Instruction	Code*	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM outputs to High–Z state. *NOT 1149.1 COMPLIANT*
IDCODE	001**	Preloads ID register and places it between TDI and TDO. Does not affect RAM operation.
SAMPLE / PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect RAM operation. Does not implement 1149.1 Preload function. * NOT 1149.1 COMPLIANT *
BYPASS	111	Places bypass register between TDI and TDO. Does not affect RAM operation.
SAMPLE–Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM output drivers to High–Z.

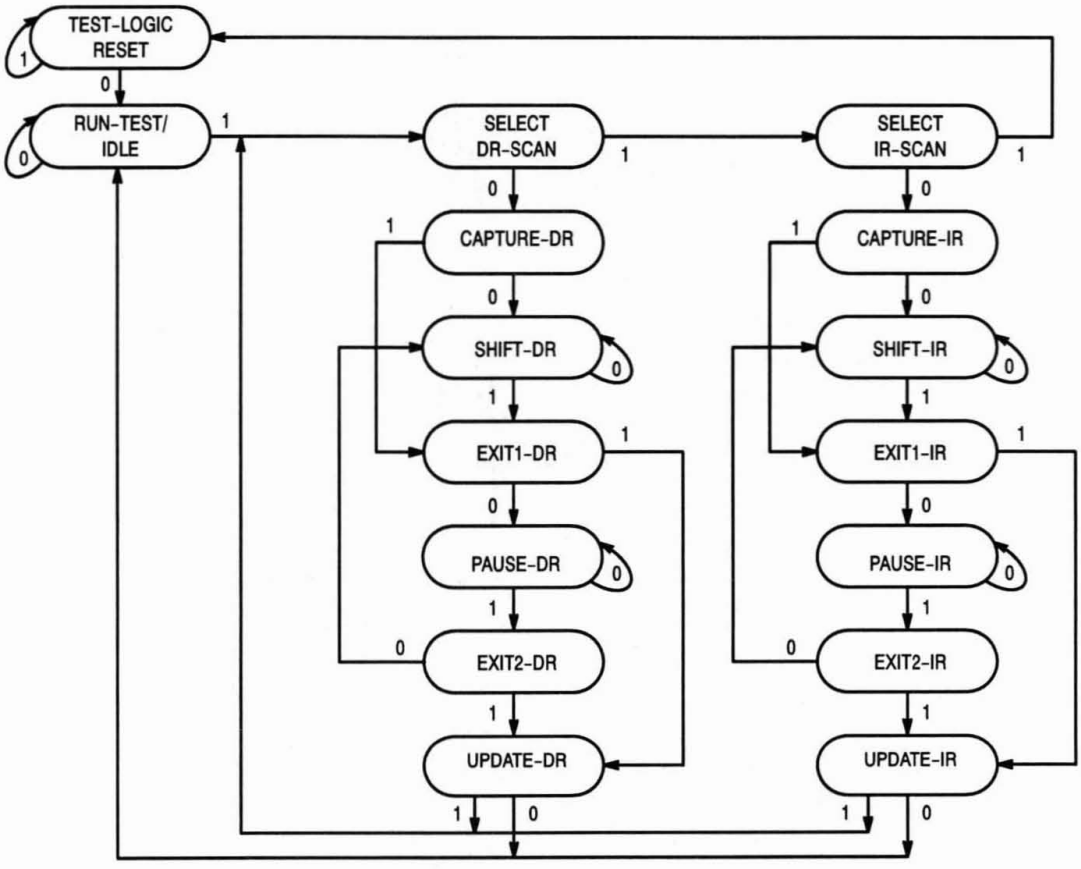
* Instruction codes expressed in binary, MSB on left, LSB on right.
** Default instruction automatically loaded at power–up and in test–logic–reset state.

3

STANDARD (PRIVATE) INSTRUCTION CODES

Instruction	Code*	Description
NO OP	011	Do not use these instructions; they are reserved for future use.
NO OP	101	Do not use these instructions; they are reserved for future use.
NO OP	110	Do not use these instructions; they are reserved for future use.

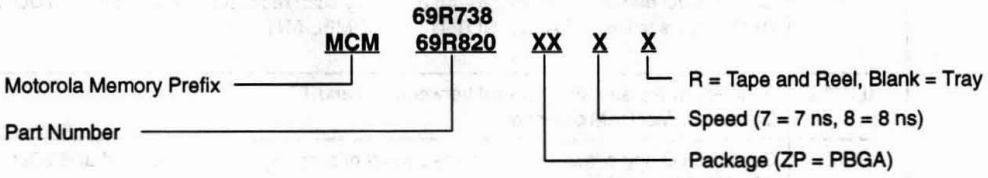
* Instruction codes expressed in binary, MSB on left, LSB on right.



NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 5. TAP Controller State Diagram

ORDERING INFORMATION
(Order by Full Part Number)



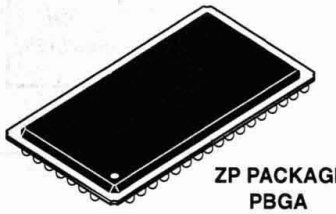
Full Part Numbers —	MCM69R738ZP7	MCM69R738ZP8
	MCM69R820ZP7	MCM69R820ZP8
	MCM69R738ZP7R	MCM69R738ZP8R
	MCM69R820ZP7R	MCM69R820ZP8R

3

MCM69R738A
MCM69R820A

Advance Information

4M Late Write 2.5 V I/O



ZP PACKAGE
PBGA
CASE 999–01

The MCM69R738A/820A is a 4 megabit synchronous late write fast static RAM designed to provide high performance in secondary cache and ATM switch, Telecom, and other high speed memory applications. The MCM69R820A organized as 256K words by 18 bits, and the MCM69R738A organized as 128K words by 36 bits wide are fabricated in Motorola's high performance silicon gate BiCMOS technology.

The differential CK clock inputs control the timing of read/write operations of the RAM. At the rising edge of the CK clock all addresses, write enables, and synchronous selects are registered. An internal buffer and special logic enable the memory to accept write data on the rising edge of the CK clock a cycle after address and control signals. Read data is driven on the rising edge of the CK clock also.

The RAM uses 2.5 V inputs and outputs.

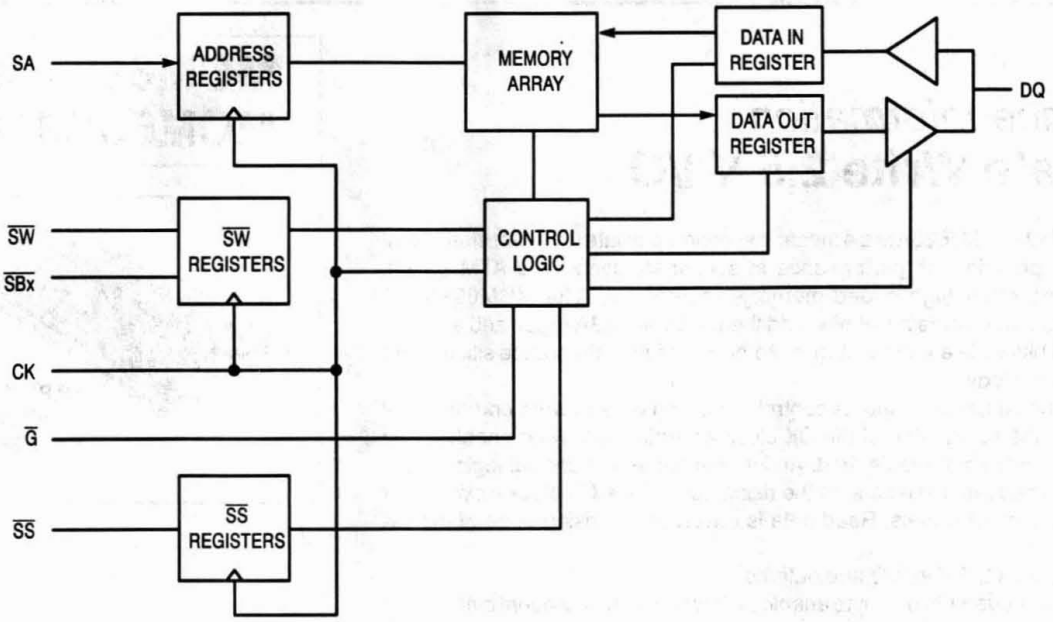
The synchronous write and byte enables allow writing to individual bytes or the entire word.

- Byte Write Control
- Single 3.3 V +10%, – 5% Operation
- 2.5 V I/O
- Register to Register Synchronous Operation
- Asynchronous Output Enable
- Boundary Scan (JTAG) IEEE 1149.1 Compatible
- Differential Clock Inputs
- Optional x 18 or x 36 organization
- MCM69R738A/820A–5 = 5 ns
  MCM69R738A/820A–6 = 6 ns
  MCM69R738A/820A–7 = 7 ns
  MCM69R738A/820A–8 = 8 ns
- 119 Bump, 50 mil (1.27 mm) Pitch, 14 mm x 22 mm Plastic Ball Grid Array (PBGA) Package

This document contains information on a new product. Specifications and information herein are subject to change without notice.

4/3/97

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENTS

TOP VIEW

MCM69R738A

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	SA	NC	SA	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
E	DQc	DQc	V_{SS}	$\overline{SS}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{G}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{SBc}$	NC	$\overline{SBb}$	DQb	DQb
H	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CK	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{SBd}$	$\overline{CK}$	$\overline{SBa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{SW}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
P	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
R	NC	SA	V_{SS}	V_{DD}	V_{DD}	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69R820A

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	SA	NC	SA	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQb	NC	V_{SS}	NC	V_{SS}	DQa	NC
E	NC	DQb	V_{SS}	$\overline{SS}$	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	$\overline{SBb}$	NC	V_{SS}	NC	DQa
H	DQb	NC	V_{SS}	NC	V_{SS}	DQa	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	CK	V_{SS}	NC	DQa
L	DQb	NC	V_{SS}	$\overline{CK}$	$\overline{SBa}$	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{SW}$	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	SA	V_{SS}	DQa	NC
P	NC	DQb	V_{SS}	SA	V_{SS}	NC	DQa
R	NC	SA	V_{SS}	V_{DD}	V_{DD}	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69R738A PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6K, 7K, 6L, 7L, 6M, 6N, 7N, 6P, 7P (b) 6D, 7D, 6E, 7E, 6F, 6G, 7G, 6H, 7H (c) 1D, 2D, 1E, 2E, 2F, 1G, 2G, 1H, 2H (d) 1K, 2K, 1L, 2L, 2M, 1N, 2N, 1P, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 3T, 4T, 5T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 5G, 3G, 3L (a), (b), (c), (d)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
7T	ZZ	Input	Enables sleep mode.
4C, 2J, 4J, 6J, 4R, 5R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 3H, 5H, 3K, 5K, 3M, 5M, 3N, 5N, 3P, 5P, 3R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 4B, 6B, 7B, 1C, 7C, 4D, 4G, 4H, 3J, 5J, 1R, 7R, 1T, 2T, 6T, 6U	NC	—	No Connection: There is no connection to the chip. Note: 3J and 5J are tied common.

MCM69R820A PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6D, 7E, 6F, 7G, 6H, 7K, 6L, 6N, 7P (b) 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 2T, 3T, 5T, 6T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 3G (a), (b)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
7T	ZZ	Input	Enables sleep mode.
4C, 2J, 4J, 6J, 4R, 5R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P, 3R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 4B, 6B, 7B, 1C, 7C, 2D, 4D, 7D, 1E, 6E, 2F, 1G, 4G, 6G, 2H, 4H, 7H, 3J, 5J, 1K, 6K, 2L, 7L, 6M, 2N, 7N, 1P, 6P, 1R, 7R, 1T, 4T, 6U	NC	—	No Connection: There is no connection to the chip. Note: 3J and 5J are tied common.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS}, See Note 1)

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Output Supply Voltage	V_{DDQ}	– 0.5 to V_{DD} + 0.5	V
Voltage On Any Pin	V_{in}	– 0.5 to V_{DD} + 0.5	V
Input Current (per I/O)	I_{in}	± 50	mA
Output Current (per I/O)	I_{out}	± 70	mA
Power Dissipation (See Note 2)	P_D	—	W
Operating Temperature	T_A	0 to + 70	°C
Temperature Under Bias	T_{bias}	–10 to + 85	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability will be dependent upon package characteristics and use environment. See enclosed thermal impedance data.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

3

PBGA PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (Still Air)		$R_{\theta JA}$	53	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Single Layer Board	$R_{\theta JA}$	38	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Four Layer Board	$R_{\theta JA}$	22	°C/W	
Junction to Board (Bottom)		$R_{\theta JB}$	14	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	5	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

($0°C \le T_A \le 70°C$, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (See Notes 1 through 4)

Parameter	Symbol	Min	Typical –5	Typical –6	Typical –7	Typical –8	Max	Unit	Notes
Core Power Supply Voltage	V_{DD}	3.15	—	—	—	—	3.6	V	
Output Driver Supply Voltage	V_{DDQ}	2.3	—	—	—	—	2.7	V	
Active Power Supply Current (x18) (x36)	I_{DD1}	— —	390 450	360 420	330 390	320 370	490 550	mA	5
Quiescent Active Power Supply Current)	I_{DD2}	—	180	180	180	180	250	mA	6, 10
Active Standby Power Supply Current)	I_{SB1}	—	170	170	170	170	250	mA	7
Quiescent Standby Power Supply Current	I_{SB2}	—	150	150	150	150	230	mA	8, 10
Sleep Mode Power Supply Current	I_{SB3}	—	30	30	30	30	50	mA	9, 10

NOTES:
1. All data sheet parameters specified to full range of V_{DD} unless otherwise noted. All voltages are referenced to voltage applied to V_{SS} bumps.
2. Supply voltage applied to V_{DD} connections.
3. Supply voltage applied to V_{DDQ} connections.
4. All power supply currents measured with outputs open or deselected.
5. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered active, 50% read cycles.
6. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered active.
7. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered inactive.
8. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered inactive. ZZ low.
9. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered inactive, ZZ high.
10. $200 \text{ mV} \ge V_{in} \ge V_{DDQ} - 200 \text{ mV}$.

DC INPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
DC Input Logic High	V_{IH} (dc)	1.7	$V_{DD} + 0.3$	V	
DC Input Logic Low	V_{IL} (dc)	– 0.3	0.7	V	1
Input Leakage Current	$I_{lkg(1)}$	—	± 5	µA	2
Clock Input Leakage Current	$I_{clkg(1)}$	—	± 8	µA	2
Clock Input Signal Voltage	V_{in}	– 0.3	$V_{DDQ} + 0.3$	V	
Clock Input Differential Voltage	V_{DIF} (dc)	0.2	$V_{DDQ} + 0.6$	V	3
Clock Input Common Mode Voltage Range	V_{CM} (dc)	1.1	2.1	V	4, Fig. 3

NOTES:
1. Inputs may undershoot to – 0.5 V (peak) for up to 20% t_{KHKH} (e.g., 2 ns at a clock cycle time of 10 ns).
2. $0 \text{ V} \le V_{in} \le V_{DDQ}$ for all pins.
3. Minimum instantaneous differential input voltage required for differential input clock operation.
4. Maximum rejectable common mode input voltage variation.

DC OUTPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
Output Leakage Current	$I_{lkg(0)}$	–1.0	1.0	µA	
Output Low Voltage	V_{OL}	—	0.7	V	1
Output High Voltage	V_{OH}	1.7	—	V	2

NOTES:
1. $I_{OL} = 8.0$ mA.
2. $I_{OH} = – 8.0$ mA.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, $0°C \le T_A \le 70$ °C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	5	pF
Input/Output Capacitance	$C_{I/O}$	7	8	pF
CK, $\overline{CK}$ Capacitance	C_{CK}	4	5	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

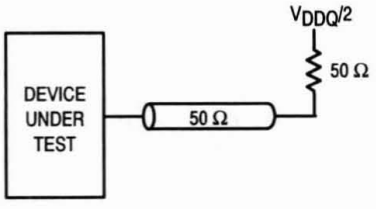
(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 2.5 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.25 V
Output Timing Reference Level ..... 1.25 V
Clock Input Timing Reference Level ..... Differential Cross–Point
Clock Input Pulse Level ..... 1.8 V to 2.1 V

READ/WRITE CYCLE TIMING (See Note 3)

Parameter	Symbol	MCM69R738A–5 MCM69R820A–5		MCM69R738A–6 MCM69R820A–6		MCM69R738A–7 MCM69R820A–7		MCM69R738A–8 MCM69R820A–8		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	5	—	6	—	7	—	8	—	ns	
Clock High Pulse Width	t_{KHKL}	2.4	—	2.4	—	2.8	—	3.2	—	ns	
Clock Low Pulse Width	t_{KLKH}	2.4	—	2.4	—	2.8	—	3.2	—	ns	
Clock High to Output Low–Z	t_{KHQX1}	1	—	1	—	1	—	1	—	ns	2
Clock High to Output Valid	t_{KHQV}	—	2.5	—	3	—	3.5	—	4	ns	1
Clock High to Output Hold	t_{KHQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	1
Clock High to Output High–Z	t_{KHQZ}	—	2.5	—	3	0	3.5	0	4	ns	2
Output Enable Low to Output Low–Z	t_{GLQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	2
Output Enable Low to Output Valid	t_{GLQV}	—	2.5	—	3	—	3.5	—	4	ns	1
Output Enable to Output Hold	t_{GHQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	1
Output Enable High to Output High–Z	t_{GHQZ}	—	2.5	—	3	—	3.5	—	4	ns	2
Setup Times: Address Data In Chip Select Write Enable	t_{AVKH} t_{DVKH} t_{SVKH} t_{WVKH}	0.5	—	0.5	—	0.5	—	0.5	—	ns	
Hold Times: Address Data In Chip Select Write Enable	t_{KHAX} t_{KHDX} t_{KHSX} t_{KHWX}	1	—	1	—	1	—	1	—	ns	

NOTES:
1. Tested per AC Test Load diagram. See Figure 1.
2. Measured at ± 200 mV from steady state.
3. In no case may control input signals (e.g., $\overline{SS}$) be operated with pulse widths less than the minimum clock input pulse width specifications (e.g., t_{KHKL}) or at frequencies that exceed the applied K clock frequency.



TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Figure 1. AC Test Load

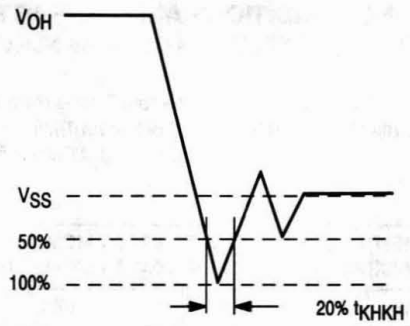
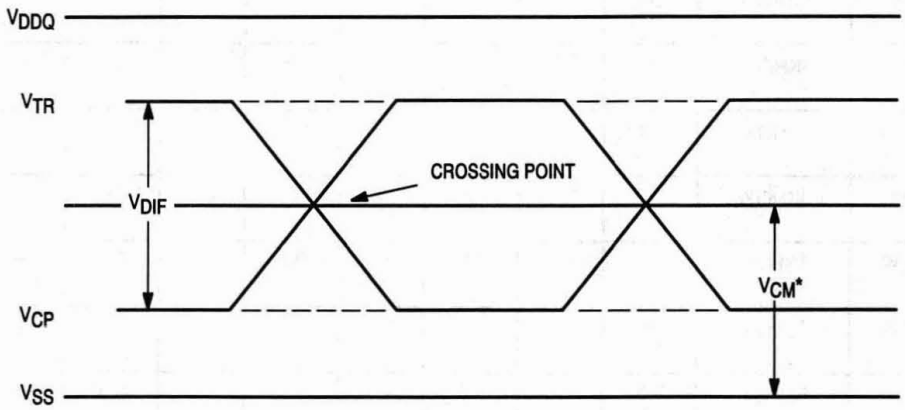


Figure 2. Undershoot Voltage

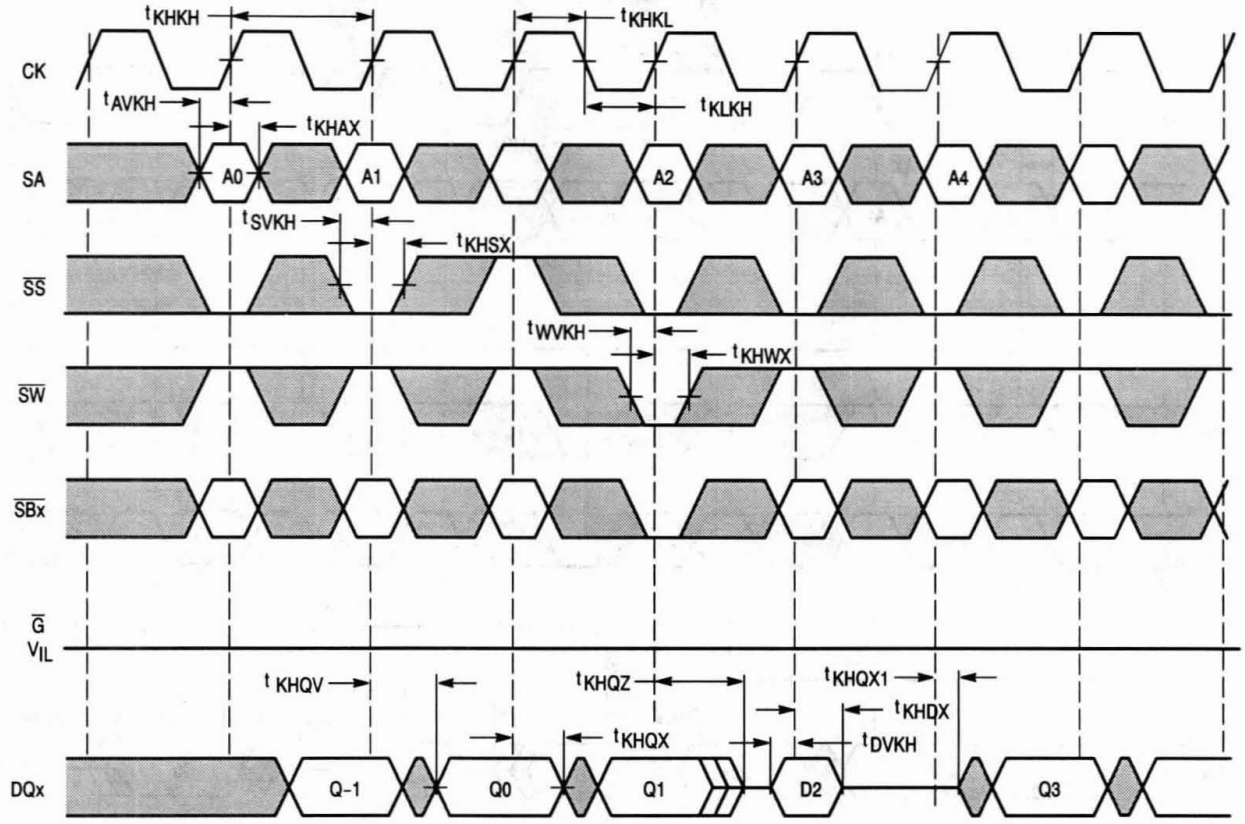
3



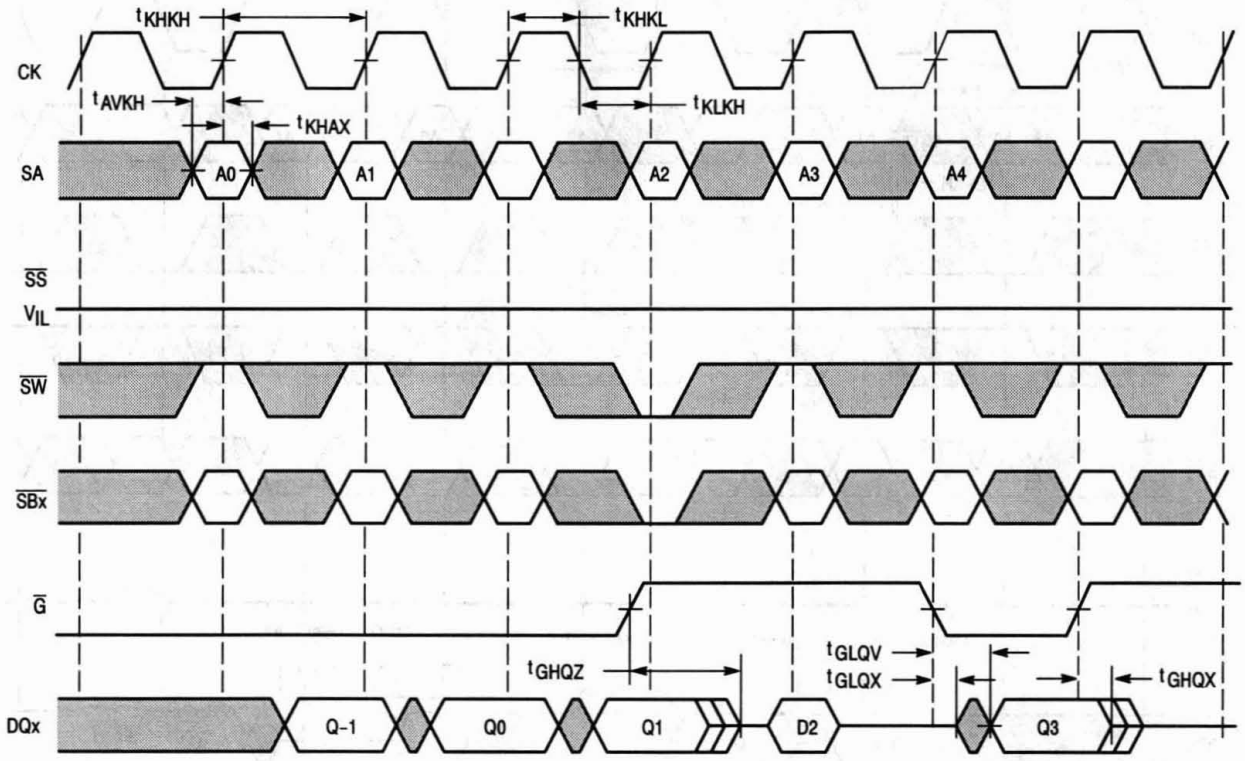
* V_{CM}, the Common Mode Input Voltage, equals $V_{TR} - ((V_{TR} - V_{CP})/2)$.

Figure 3. Differential Inputs/ Common Mode Input Voltage

REGISTER/REGISTER READ–WRITE–READ CYCLES



REGISTER/REGISTER READ–WRITE–READ
($\overline{G}$ Controlled)



FUNCTIONAL OPERATION

READ AND WRITE OPERATIONS

All control signals except $\overline{G}$ are registered on the rising edge of the CK clock. These signals must meet the setup and hold times shown in the AC Characteristics table. On the rising edge of the following clock, read data is clocked into the output register and available at the outputs at t_{KHQV}. During this same cycle a new read address can be applied to the address pins.

A deselect cycle (dead cycle) must occur prior to a write cycle. Read cycles may follow write cycles immediately.

$\overline{G}$, $\overline{SS}$, and $\overline{SW}$ control output drive. Chip deselect via a high on $\overline{SS}$ at the rising edge of the CK clock has its effect on the output drivers after the next rising edge of the CK clock. $\overline{SW}$ low deselects the output drivers immediately (on the same cycle). Output selecting via a low on $\overline{SS}$ and high on $\overline{SW}$ at a rising CK clock has its effect on the output drivers after the next rising edge of the CK clock. Output drive is also controlled directly by output enable, $\overline{G}$. $\overline{G}$ is an asynchronous input. No clock edges are required to enable/disable the output using $\overline{G}$.

Output data will be valid the latter of t_{GLQV} and t_{KHQV}. Outputs will begin driving at t_{KHQX1}. Outputs will hold previous data until t_{KHQX} or t_{GHQX}.

WRITE AND BYTE WRITE FUNCTIONS

Note that in the following discussion the term "byte" refers to nine bits of the RAM I/O bus. In all cases, the timing parameters described for synchronous write input ($\overline{SW}$) apply to each of the byte write enable inputs ($\overline{SBa}$, $\overline{SBb}$, etc.).

Byte write enable inputs have no effect on read cycles. This allows the system designer not interested in performing byte writes to connect the byte enable inputs to active low (V_{SS}). Reads of all bytes proceed normally and write cycles, activated via a low on $\overline{SW}$, and the rising edge of the CK clock, write the entire RAM I/O width. This way the designer is spared having to drive multiple write input buffer loads.

Byte writes are performed using the byte write enable inputs in conjunction with the synchronous write input ($\overline{SW}$). It is important to note that writing any one byte will inhibit a read of all bytes at the current address. The RAM cannot simultaneously read one byte and write another at the same address. A write cycle initiated with none of the byte write enable inputs active is neither a read or a write. No write will occur, but the outputs will be deselected as in a normal write cycle.

LATE WRITE

The write address is sampled on the first rising edge of clock and write data is sampled on the following rising edge.

The late write feature is implemented with single stage write buffering. Write buffering is transparent to the user. A comparator monitors the address bus and, when necessary, routes buffer contents to the outputs to assure coherent operation. This occurs in all cases whether there is a byte write or a full word is written.

POWER UP AND INITIALIZATION

Once supplies have reached specification levels, a minimum dwell of 1.0 µs with CK clock inputs cycling is required before beginning normal operations.

SERIAL BOUNDARY SCAN TEST ACCESS PORT OPERATION

OVERVIEW

The serial boundary scan test access port (TAP) on this RAM is designed to operate in a manner consistent with IEEE Standard 1149.1–1990 (commonly referred to as JTAG), but does not implement all of the functions required for 1149.1 compliance. Certain functions have been modified or eliminated because their implementation places extra delays in the RAMs critical speed path. Nevertheless, the RAM supports the standard TAP controller architecture. (The TAP controller is the state machine that controls the TAPs operation) and can be expected to function in a manner that does not conflict with the operation of devices with Standard 1149.1 compliant TAPs. The TAP operates using conventional JEDEC Standard 8–1B Low Voltage (3.3 V) TTL / CMOS logic level signaling.

DISABLING THE TEST ACCESS PORT

It is possible to use this device without utilizing the TAP. To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid level inputs. TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a 1 k resistor. TDO should be left unconnected.

TAP DC OPERATING CHARACTERISTICS

($0°C \le T_A \le 70°C$, Unless Otherwise Noted)

Parameter	Symbol	Min	Max	Unit	Note
Logic Input Logic High	$V_{IH}1$	2.0	V_{DD} + 0.3	V	
Logic Input Logic Low	$V_{IL}1$	– 0.3	0.8	V	
Logic Input Leakage Current	I_{lkg}	—	± 5	µA	1
CMOS Output Logic Low	$V_{OL}1$	—	0.2	V	2
CMOS Output Logic High	$V_{OH}1$	V_{DD} – 0.2	—	V	3
TTL Output Logic Low	$V_{OL}2$	—	0.4	V	4
TTL Output Logic High	$V_{OH}2$	2.4	—	V	5

NOTES:
1. $0 V \pm V_{in} \pm V_{DDQ}$ for all logic input pins.
2. $I_{OL}1 \le 100$ µA @ $V_{OL} = 0.2$ V. Sampled, not 100% tested.
3. $|I_{OH}1| \le 100$ µA @ $V_{DDQ} - 0.2$ V. Sampled, not 100% tested.
4. $I_{OL}2 \le 8$ mA @ $V_{OL} = 0.4$ V
5. $|I_{OH}2| \le 8$ mA @ $V_{OH} = 2.4$ V

TAP AC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V

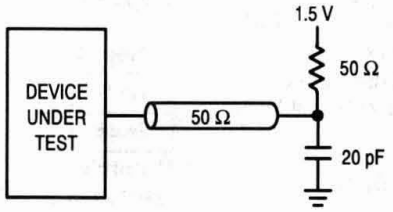
Output Test Load ..... 50 Ω Parallel Terminated T–line with 20 pF Receiver Input Capacitance
Test Load Termination Supply Voltage (V_T) ..... 1.5 V

TAP CONTROLLER TIMING

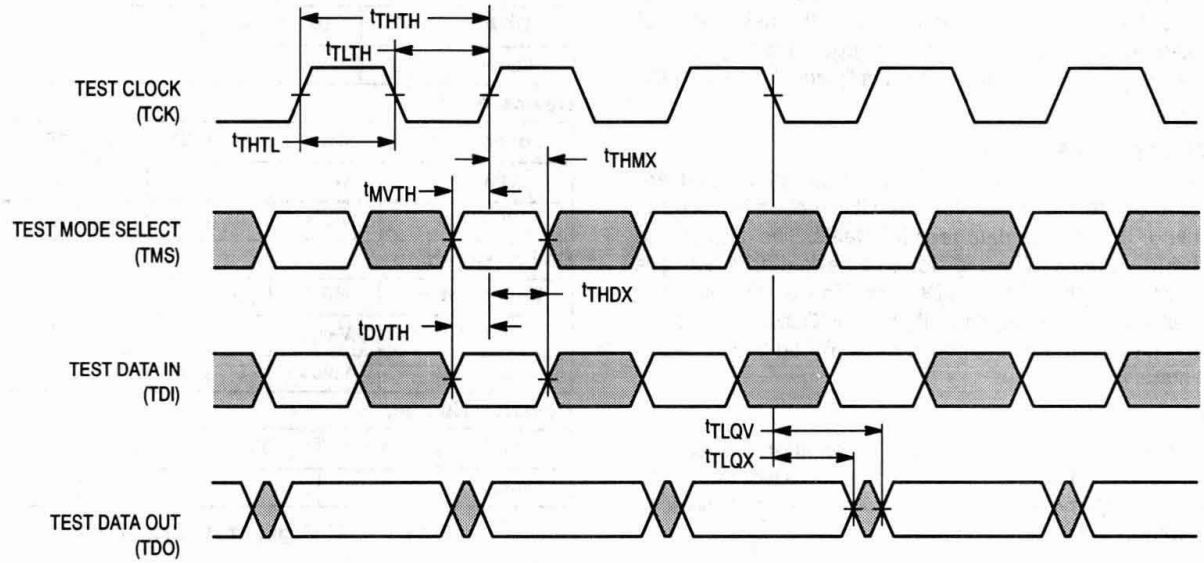
Parameter	Symbol	Min	Max	Unit	Notes
Cycle Time	t_{THTH}	100	—	ns	
Clock High Time	t_{THTL}	40	—	ns	
Clock Low Time	t_{TLTH}	40	—	ns	
TMS Setup	t_{MVTH}	10	—	ns	
TMS Hold	t_{THMX}	10	—	ns	
TDI Valid to TCK High	t_{DVTH}	10	—	ns	
TCK High to TDI Don't Care	t_{THDX}	10	—	ns	
Capture Setup	t_{CS}	10	—	ns	1
Capture Hold	t_{CH}	10	—	ns	1
TCK Low to TDO Unknown	t_{TLQX}	0	—	ns	
TCK Low to TDO Valid	t_{TLOV}	—	20	ns	

NOTES:
1. t_{CS} + t_{CH} defines the minimum pause in RAM I/O pad transitions to assure accurate pad data capture.

AC TEST LOAD



TAP CONTROLLER TIMING DIAGRAM



TEST ACCESS PORT PINS

TCK – TEST CLOCK (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

TMS – TEST MODE SELECT (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.

TDI – TEST DATA IN (INPUT)

The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (refer to Figure 5 TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.

TDO – TEST DATA OUT (OUTPUT)

Output that is active depending on the state of the TAP state machine (refer to Figure 5 TAP Controller State Diagram). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

TRST – TAP RESET

This device does not have a TRST pin. TRST is optional in **IEEE 1149.1.** The test–logic reset state is entered while TMS is held high for five rising edges of TCK. Power on reset circuitry is included internally. This type of reset does not affect the operation of the system logic. The reset affects test logic only.

TEST ACCESS PORT REGISTERS

OVERVIEW

The various TAP registers are selected (one at a time) via the sequences of ones and zeros input to the TMS pin as the TCK is strobed. Each of the TAPs registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on subsequent falling edge of TCK. When a register is selected it is "placed" between the TDI and TDO pins.

INSTRUCTION REGISTER

The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run test/idle or the various data register states. The instructions are three bits long. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power–up or whenever the controller is placed in test–logic–reset state.

BYPASS REGISTER

The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.

BOUNDARY SCAN REGISTER

The boundary scan register is identical in length to the number of active input and I/O connections on the RAM (not counting the TAP pins). This also includes a number of place holder locations (always set to a logic 1) reserved for density upgrade address pins. There are a total of 70 bits in the case of the x36 device and 51 bits in the case of the x18 device. The boundary scan register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture–DR state and then is placed between the TDI and TDO pins when the controller is moved to shift–DR state. Several TAP instructions can be used to activate the boundary scan register.

The Bump/Bit Scan Order tables describe which device bump connects to each boundary scan register location. The first column defines the bit's position in the boundary scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the input or I/O at the bump and the third column is the bump number.

IDENTIFICATION (ID) REGISTER

The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture–DR state with the IDCODE command loaded in the instruction register. The code is loaded from a 32 bit on–chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into shift–DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Presence Indicator

Bit #	0
Value	1

Motorola JEDEC ID Code (Compressed Format, per IEEE Standard 1149.1 – 1990

Bit #	11	10	9	8	7	6	5	4	3	2	1
Value	0	0	0	0	0	0	0	1	1	1	0

Reserved For Future Use

Bit #	17	16	15	14	13	12
Value	x	x	x	x	x	x

Device Width

Configuration	Bit #	22	21	20	19	18
128Kx36	Value	0	0	1	0	0
256Kx18	Value	0	0	0	1	1

Device Depth

Configuration	Bit #	27	26	25	24	23
128Kx36	Value	0	0	1	0	1
256Kx18	Value	0	0	1	1	0

Revision Number

Bit #	31	30	29	28
Value	x	x	x	x

Figure 4. ID Register Bit Meanings

MCM69R738A Bump/Bit Scan Order

BIT #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	SA	3B
2	SA	4P		37	NC	2B
3	SA	4T		38	SA	3A
4	SA	6R		39	SA	3C
5	SA	5T		40	SA	2C
6	ZZ	7T		41	SA	2A
7	DQa	6P		42	DQc	2D
8	DQa	7P		43	DQc	1D
9	DQa	6N		44	DQc	2E
10	DQa	7N		45	DQc	1E
11	DQa	6M		46	DQc	2F
12	DQa	6L		47	DQc	2G
13	DQa	7L		48	DQc	1G
14	DQa	6K		49	DQc	2H
15	DQa	7K		50	DQc	1H
16	$\overline{SBa}$	5L		51	$\overline{SBc}$	3G
17	$\overline{CK}$	4L		52	NC	4D
18	CK	4K		53	$\overline{SS}$	4E
19	$\overline{G}$	4F		54	NC	4G
20	$\overline{SBb}$	5G		55	NC	4H
21	DQb	7H		56	$\overline{SW}$	4M
22	DQb	6H		57	$\overline{SBd}$	3L
23	DQb	7G		58	DQd	1K
24	DQb	6G		59	DQd	2K
25	DQb	6F		60	DQd	1L
26	DQb	7E		61	DQd	2L
27	DQb	6E		62	DQd	2M
28	DQb	7D		63	DQd	1N
29	DQb	6D		64	DQd	2N
30	SA	6A		65	DQd	1P
31	SA	6C		66	DQd	2P
32	SA	5C		67	SA	3T
33	SA	5A		68	SA	2R
34	NC	6B		69	SA	4N
35	SA	5B		70	M1	3R

MCM69R820A Bump/Bit Scan Order

Bit #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	$\overline{SBb}$	3G
2	SA	6T		37	NC	4D
3	SA	4P		38	$\overline{SS}$	4E
4	SA	6R		39	NC	4G
5	SA	5T		40	NC	4H
6	ZZ	7T		41	$\overline{SW}$	4M
7	DQa	7P		42	DQb	2K
8	DQa	6N		43	DQb	1L
9	DQa	6L		44	DQb	2M
10	DQa	7K		45	DQb	1N
11	$\overline{SBa}$	5L		46	DQb	2P
12	$\overline{CK}$	4L		47	SA	3T
13	CK	4K		48	SA	2R
14	$\overline{G}$	4F		49	SA	4N
15	DQa	6H		50	SA	2T
16	DQa	7G		51	M1	3R
17	DQa	6F				
18	DQa	7E				
19	DQa	6D				
20	SA	6A				
21	SA	6C				
22	SA	5C				
23	SA	5A				
24	NC	6B				
25	SA	5B				
26	SA	3B				
27	NC	2B				
28	SA	3A				
29	SA	3C				
30	SA	2C				
31	SA	2A				
32	DQb	1D				
33	DQb	2E				
34	DQb	2G				
35	DQb	1H				

NOTES:

1. The NC pads listed in this table are indeed no connects, but are represented in the boundary scan register by a "place holder" bit that is forced to logic 1. These pads are reserved for use as address inputs on higher density RAMs that follow this pad out and scan order standard.
2. CK, $\overline{CK}$, are sampled individually. $\overline{CK}$ is not simply a forced complement of the CK input. In scan mode these differential inputs are referenced to each other.
3. M1 and M2 are not ordinary inputs and may not respond to standard I/O logic levels. M1 and M2 must be driven to within 100 mV of a V_{DD} or V_{SS} supply rail to ensure consistent results.
4. ZZ must remain at V_{IL} during boundary scan to ensure consistent results.

TAP Controller Instruction Set

OVERVIEW

There are two classes of instructions defined in the Standard 1149.1–1990; the standard (public) instructions, and device specific (private) instructions. Some public instructions, are mandatory for 1149.1 compliance. Optional public instructions must be implemented in prescribed ways.

Although the TAP controller in this device follows the 1149.1 conventions, it is not 1194.1 compliant because some of the mandatory instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads, but cannot be used to load address, data or control signals into the RAM or to preload the I/O buffers. In other words, the device will not perform Standard 1149.1 EXTEST, INTEST or the preload portion of the SAMPLE / PRELOAD command.

When the TAP controller is placed in capture–IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the shift–IR state the instruction register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to update–IR state. The TAP instruction sets for this device are listed in the following tables.

STANDARD (PUBLIC) INSTRUCTIONS

BYPASS

The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift–DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

Sample/preload is a Standard 1149.1 mandatory public instruction. When the sample / preload instruction is loaded in the Instruction register, moving the TAP controller into the capture–DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set–up plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register.

Moving the controller to shift–DR state then places the boundary scan register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the update–DR state with the SAMPLE / PRELOAD instruction loaded in the instruction register has the same effect as the pause–DR command. This functionality is not Standard 1149.1 compliant.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic 0s. EXTEST is not implemented in this device. Therefore this device is not 1149.1 compliant. Nevertheless, this RAMs TAP does respond to an all zeros instruction, as follows. With the EXTEST (000) instruction loaded in the instruction register the RAM responds just as it does in response to the SAMPLE / PRELOAD instruction described above, except the RAM outputs are forced to high–Z any time the instruction is loaded.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture–DR mode and places the ID register between the TDI and TDO pins in shift–DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test–logic–reset state.

THE DEVICE SPECIFIC (PUBLIC) INSTRUCTION

SAMPLE–Z

If the SAMPLE–Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high–Z) and the boundary scan register is connected between TDI and TDO when the TAP controller. is moved to the shift–DR state.

THE DEVICE SPECIFIC (PRIVATE) INSTRUCTION

NOOP

Do not use these instructions; they are reserved for future use.

STANDARD (PUBLIC) INSTRUCTION CODES

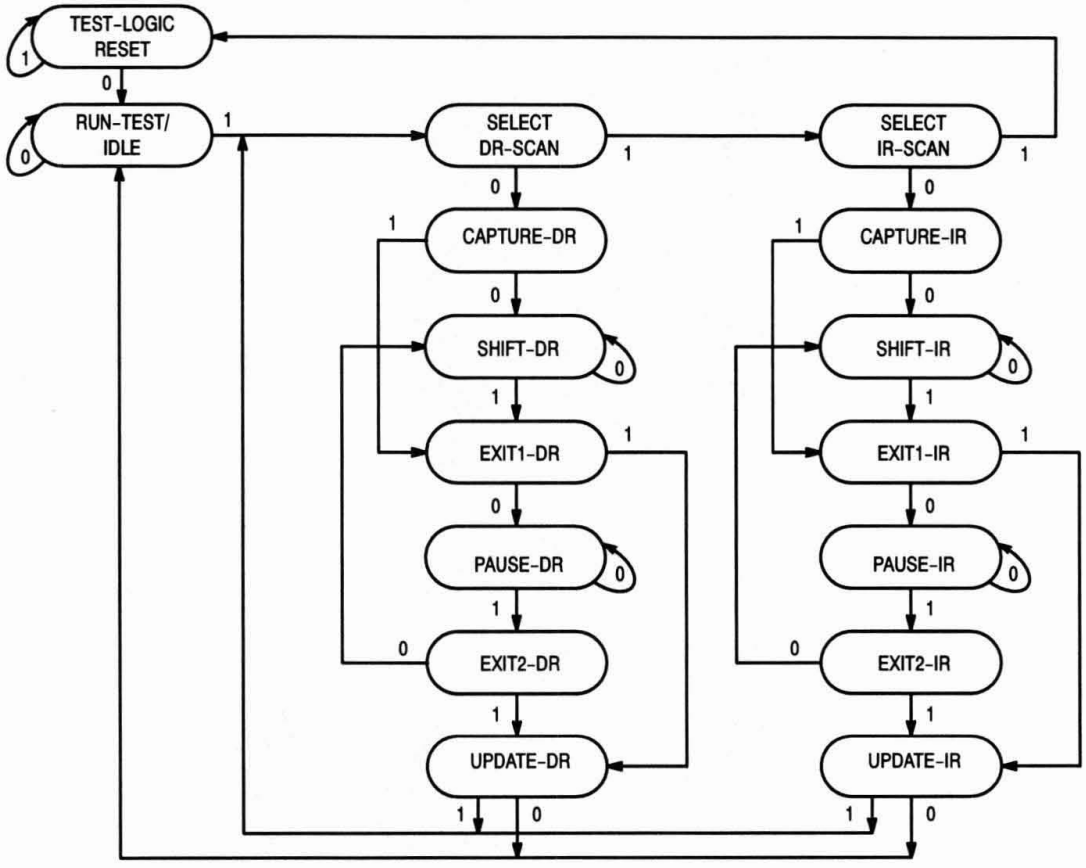
Instruction	Code*	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM outputs to High–Z state. *NOT 1149.1 COMPLIANT*
IDCODE	001**	Preloads ID register and places it between TDI and TDO. Does not affect RAM operation.
SAMPLE / PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect RAM operation. Does not implement 1149.1 Preload function. * NOT 1149.1 COMPLIANT *
BYPASS	111	Places bypass register between TDI and TDO. Does not affect RAM operation.
SAMPLE–Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM output drivers to High–Z.

* Instruction codes expressed in binary, MSB on left, LSB on right.
** Default instruction automatically loaded at power–up and in test–logic–reset state.

STANDARD (PRIVATE) INSTRUCTION CODES

Instruction	Code*	Description
NO OP	011	Do not use these instructions; they are reserved for future use.
NO OP	101	Do not use these instructions; they are reserved for future use.
NO OP	110	Do not use these instructions; they are reserved for future use.

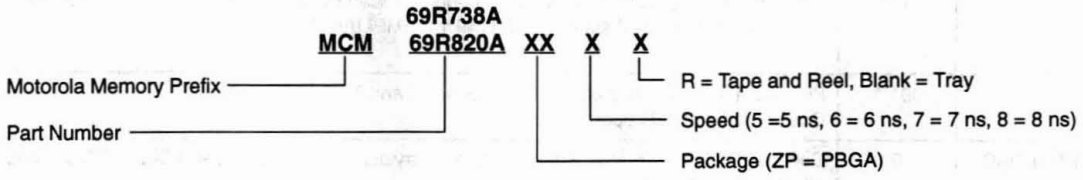
* Instruction codes expressed in binary, MSB on left, LSB on right.



NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 5. TAP Controller State Diagram

ORDERING INFORMATION
(Order by Full Part Number)


69R738A
MCM 69R820A XX X X
Motorola Memory Prefix
Part Number
R = Tape and Reel, Blank = Tray
Speed (5 =5 ns, 6 = 6 ns, 7 = 7 ns, 8 = 8 ns)
Package (ZP = PBGA)

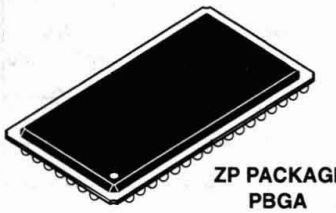
Full Part Numbers — MCM69R738AZP5 MCM69R738AZP6 MCM69R738AZP7 MCM69R738AZP8
MCM69R820AZP5 MCM69R820AZP6 MCM69R820AZP7 MCM69R820AZP8
MCM69R738AZP5R MCM69R738AZP6R MCM69R738AZP7R MCM69R738AZP8R
MCM69R820AZP5R MCM69R820AZP6R MCM69R820AZP7R MCM69R820AZP8R

MCM69R739A
MCM69R821A

Advance Information

Dual Clock 4M Late Write HSTL

256K x 18 or 128K x 36 Synchronous Memory



ZP PACKAGE
PBGA
CASE 999–01

The MCM69R739A/821A is a 4 megabit synchronous late write fast static RAM designed to provide high performance in secondary cache, ATM switch, Telecom, and other high speed memory applications. The MCM69R821A organized as 256K words by 18 bits, and the MCM69R739A organized as 128K words by 36 bits wide.

The differential K and C clock inputs control the timing of read/write operations of the RAM. At the rising edge of the K clock all addresses, write enables, and synchronous selects are registered. An internal buffer and special logic enable the memory to accept write data on the rising edge of the K clock a cycle after address and control signals. The outputs are enabled on the rising edge of the C clock which operates at the same frequency as the K clock; but shifted in time.

The RAM uses HSTL inputs and outputs. The adjustable input trip – point (V_{ref}) and output voltage (V_{DDQ}) gives the system designer greater flexibility in optimizing system performance.

The synchronous write and byte enables allow writing to individual bytes or the entire word.

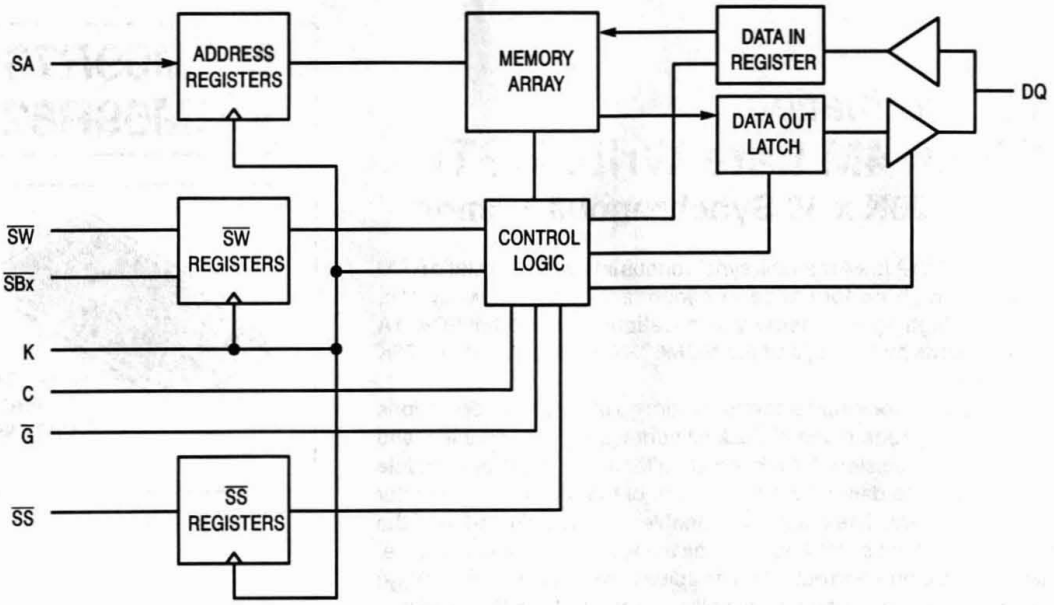
The impedance of the output buffers is programmable allowing the outputs to match the impedance of the circuit traces which reduces signal reflections.

- Byte Write Control
- 3.3 V Power Supply
- HSTL – I/O (JEDEC Standard JESD8–6 Class I Compatible)
- HSTL – User Selectable Input Trip–Point
- HSTL – Compatible Programmable Impedance Output Drivers
- Synchronous Operation
- Asynchronous Impedance Update
- Boundary Scan (JTAG) IEEE 1149.1 Compatible
- Differential Clock Inputs C and K provide separate Input and Output Clocks
- Optional x 18 or x 36 organization
- MCM69R739A/821A–4.2 = 4.2 ns
  MCM69R739A/821A–4.5 = 4.5 ns
  MCM69R739A/821A–5 = 5 ns
- 119 Bump, 50 mil (1.27 mm) Pitch, 14 mm x 22 mm Plastic Ball Grid Array (PBGA) Package

This document contains information on a new product. Specifications and information herein are subject to change without notice.

4/3/97

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENTS

TOP VIEW

MCM69R739A

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	SA	NC	SA	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQc	DQc	V_{SS}	ZQ	V_{SS}	DQb	DQb
E	DQc	DQc	V_{SS}	$\overline{SS}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{G}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{SBc}$	$\overline{C}$	$\overline{SBb}$	DQb	DQb
H	DQc	DQc	V_{SS}	C	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	V_{ref}	V_{DD}	V_{ref}	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	K	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{SBd}$	$\overline{K}$	$\overline{SBa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{SW}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
P	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
R	NC	SA	V_{DD}	V_{DD}	V_{DD}	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69R821A

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	SA	NC	SA	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQb	NC	V_{SS}	ZQ	V_{SS}	DQa	NC
E	NC	DQb	V_{SS}	$\overline{SS}$	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	$\overline{SBb}$	$\overline{C}$	V_{SS}	NC	DQa
H	DQb	NC	V_{SS}	C	V_{SS}	DQa	NC
J	V_{DDQ}	V_{DD}	V_{ref}	V_{DD}	V_{ref}	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	K	V_{SS}	NC	DQa
L	DQb	NC	V_{SS}	$\overline{K}$	$\overline{SBa}$	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{SW}$	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	SA	V_{SS}	DQa	NC
P	NC	DQb	V_{SS}	SA	V_{SS}	NC	DQa
R	NC	SA	V_{DD}	V_{DD}	V_{DD}	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69R739A PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4H	C	Input	Output Clock. Active high.
4G	$\overline{C}$	Input	Output Clock. Active low.
(a) 6K, 7K, 6L, 7L, 6M, 6N, 7N, 6P, 7P (b) 6D, 7D, 6E, 7E, 6F, 6G, 7G, 6H, 7H (c) 1D, 2D, 1E, 2E, 2F, 1G, 2G, 1H, 2H (d) 1K, 2K, 1L, 2L, 2M, 1N, 2N, 1P, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Active low.
4K	K	Input	Address, data in and control input register clock. Active high.
4L	$\overline{K}$	Input	Address, data in and control input register clock. Active low.
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 3T, 4T, 5T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 5G, 3G, 3L (a), (b), (c), (d)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
3J, 5J	V_{ref}	Supply	Input Reference: provides reference voltage for input buffers.
4D	ZQ	Input	Programmable Output Impedance: Programming pin.
7T	ZZ	Input	Reserved for future use. Must be grounded.
4C, 2J, 4J, 6J, 4R, 5R, 3R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 3H, 5H, 3K, 5K, 3M, 5M, 3N, 5N, 3P, 5P	V_{SS}	Supply	Ground.
4A, 1B, 2B, 4B, 6B, 7B, 1C, 7C, 1R, 7R, 1T, 2T, 6T, 6U	NC	—	No Connection: There is no connection to the chip.

MCM69R821A PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4H	C	Input	Output Clock. Active high.
4G	$\overline{C}$	Input	Output Clock. Active low.
(a) 6D, 7E, 6F, 7G, 6H, 7K, 6L, 6N, 7P (b) 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Active low.
4K	K	Input	Address, data in and control input register clock. Active high.
4L	$\overline{K}$	Input	Address, data in and control input register clock. Active low.
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 2T, 3T, 5T, 6T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 3G (a), (b)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
3J, 5J	V_{ref}	Supply	Input Reference: provides reference voltage for input buffers.
4D	ZQ	Input	Programmable Output Impedance: Programming pin.
7T	ZZ	Input	Reserved for future use. Must be grounded.
4C, 2J, 4J, 6J, 4R, 5R, 3R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P	V_{SS}	Supply	Ground.
4A, 1B, 2B, 4B, 6B, 7B, 1C, 7C, 2D, 7D, 1E, 6E, 2F, 1G, 6G, 2H, 7H, 1K, 6K, 2L, 7L, 6M, 2N, 7N, 1P, 6P, 1R, 7R, 1T, 4T, 6U	NC	—	No Connection: There is no connection to the chip.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to VSS)

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Output Supply Voltage	V_{DDQ}	– 0.5 to V_{DD} + 0.5	V
Voltage On Input only pins	V_{in}	– 0.5 to V_{DD} + 0.5	V
Voltage On I/O pins	$V_{INi/o}$	–0.5 to V_{DDQ} + 0.5	V
Input Current (per I/O)	I_{in}	± 50	mA
Output Current (per I/O)	I_{out}	± 70	mA
Junction Temperature Under Bias*	T_{Jbias}	+ 20 to + 110	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

*NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

3

PBGA PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (Still Air)		$R_{\theta JA}$	53	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Single Layer Board	$R_{\theta JA}$	38	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Four Layer Board	$R_{\theta JA}$	22	°C/W	
Junction to Board (Bottom)		$R_{\theta JB}$	14	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	5	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

($0°C \le T_A \le 70°C$, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (See Notes 1 through 4)

Parameter	Symbol	Min	Typical –4.2	Typical –4.5	Typical –5	Max	Unit	Notes
Input Reference DC Voltage	V_{ref} (dc)	0.6	—	—	—	1.1	V	11
Core Power Supply Voltage	V_{DD}	3.15	—	—	—	3.6	V	
Output Driver Supply Voltage	V_{DDQ}	1.4	—	—	—	1.6	V	
Active Power Supply Current (x18)	I_{DD1}	—	TBD	TBD	TBD	TBD	mA	5
Active Power Supply Current (x36)	I_{DD1}	—	TBD	TBD	TBD	TBD	mA	5
Quiescent Active Power Supply Current	I_{DD2}	—	TBD	TBD	TBD	TBD	mA	6, 10
Active Standby Power Supply Current	I_{SB1}	—	TBD	TBD	TBD	TBD	mA	7
Quiescent Standby Power Supply Current	I_{SB2}	—	TBD	TBD	TBD	TBD	mA	8, 10
Sleep Mode Power Supply Current	I_{SB3}	—	TBD	TBD	TBD	TBD	mA	9, 10

NOTES:

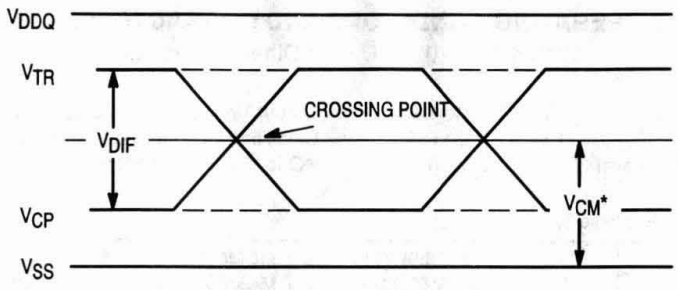
1. All data sheet parameters specified to full range of V_{DD} unless otherwise noted. All voltages are referenced to voltage applied to V_{SS} bumps.
2. Supply voltage applied to V_{DD} connections.
3. Supply voltage applied to V_{DDQ} connections.
4. All power supply currents measured with outputs open or deselected.
5. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered active, 50% read cycles.
6. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered active.
7. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered inactive.
8. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered inactive, ZZ low.
9. $V_{DD} = V_{DD}$ (Max), t_{KHKH} = dc, registered inactive, ZZ high.
10. 200 mV $\ge V_{in} \ge V_{DDQ} - 200$ mV.
11. Although considerable latitude in the selection of the nominal dc value (i.e., rms value) of V_{ref} is supported, the peak to peak ac component superimposed on V_{ref} may not exceed 5% of the dc component of V_{ref}.

DC INPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
DC Input Logic High	$V_{IH(dc)}$	$V_{ref} + 0.1$	$V_{DD} + 0.3$	V	
DC Input Logic Low	$V_{IL(dc)}$	– 0.3	$V_{ref} - 0.1$	V	1
Input Reference DC Voltage	V_{ref} (dc)	0.7	0.9	V	2
Input Leakage Current	$I_{lkg(1)}$	—	± 5	µA	3
Clock Input Signal Voltage	$V_{in(dc)}$	– 0.3	$V_{DD} + 0.3$	V	
Clock Input Differential Voltage	$V_{DIF(dc)}$	0.2	$V_{DD} + 0.6$	V	4
Clock Input Common Mode Voltage Range (See Figure 1)	V_{CM} (dc)	0.68	1.1	V	
Clock Input Crossing Point Voltage Range (See Figure 1)	V_X	0.68	1.1	V	

NOTES:

1. Inputs may undershoot to – 0.5 V (peak) for up to 20% t_{KHKH} (e.g., 2 ns at a clock cycle time of 10 ns).
2. Although considerable latitude in the selection of the nominal dc value (i.e., rms value) of V_{ref} is supported, the peak to peak ac component superimposed on V_{ref} may not exceed 5% of the dc component of V_{ref}.
3. $0 V \le V_{in} \le V_{DD}$ for all pins.
4. Minimum differential input voltage required for differential input clock operation.



*V_{CM}, the Common Mode Input Voltage, equals $V_{TR} - ((V_{TR} - V_{CP})/2)$.

Figure 1. Differential Inputs/Common Mode Input Voltage

3

DC OUTPUT BUFFER CHARACTERISTICS – PROGRAMMABLE IMPEDANCE PUSH–PULL OUTPUT BUFFER MODE

($0°C \le T_A \le 70°C$, Unless Otherwise Noted, See Notes 5 and 6)

Parameter	Symbol	Min	Max	Unit	Notes
Output Logic Low	V_{OL}	$V_{DDQ}/2 - 0.025$	$V_{DDQ}/2 + 0.025$	V	1
Output Logic High	V_{OH}	$V_{DDQ}/2 - 0.025$	$V_{DDQ}/2 + 0.025$	V	2
Light Load Output Logic Low	$V_{OL}1$	V_{SS}	0.2	V	3
Light Load Output Logic High	$V_{OH}1$	$V_{DDQ} - 0.2$	V_{DDQ}	V	4

NOTES:
1. $I_{OL} = (V_{DDQ}/2) / (RQ/5)$ for values of $RQ = 175\ \Omega \le RQ \le 350\ \Omega$.
2. $|I_{OH}| = (V_{DDQ}/2) / (RQ/5)$ for values of $RQ = 175\ \Omega \le RQ \le 350\ \Omega$.
3. $I_{OL} \le 100\ \mu A$
4. $|I_{OH}| \le 100\ \mu A$
5. The impedance controlled mode is expected to be used in point–to–point applications, driving high impedance inputs.
6. The ZQ pin is connected through RQ to V_{SS} for the controlled impedance mode.

DC OUTPUT BUFFER CHARACTERISTICS – MINIMUM IMPEDANCE PUSH–PULL OUTPUT BUFFER MODE

($0°C \le T_A \le 70°C$, ZQ = V_{DD}, See Notes 5 and 6)

Parameter	Symbol	Min.	Max.	Unit	Notes
Output Logic Low	$V_{OL}2$	V_{SS}	0.4	V	1
Output Logic High	$V_{OH}2$	$V_{DDQ} - 0.4$	V_{DDQ}	V	2
Light Load Output Logic Low	VOL_3	V_{SS}	0.2	V	3
Light Load Output Logic High	$V_{OH}3$	$V_{DDQ} - 0.2$	V_{DDQ}	V	4

NOTES:
1. $I_{OL} \le 16$ mA.
2. $|I_{OH}| \le 16$ mA.
3. $I_{OL} \le 100\ \mu A$.
4. $|I_{OH}| \le 100\ \mu A$.
5. The push–pull output mode is expected to be used in bussed applications and may be series or parallel terminated. Conforms to the JEDEC Standard JESD8–6 Class II.
6. The ZQ pin is connected to V_{DD} to enable the minimum impedance mode.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, $0°C \le T_A \le 70°C$, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	5	pF
Input/Output Capacitance	$C_{I/O}$	7	8	pF
CK, $\overline{CK}$ Capacitance	C_{CK}	4	5	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

($0°C \le T_A \le 70°C$, Unless Otherwise Noted)

Input Pulse Levels ..... 0.25 to 1.25 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 0.75 V
Output Timing Reference Level ..... 0.75 V
Clock Input Timing Reference Level ..... Differential Cross–Point
RQ for 50 Ω Impedance ..... 250 Ω

READ/WRITE CYCLE TIMING (See Note 3)

Parameter	Symbol	MCM69R739A–4.2 MCM69R821A–4.2		MCM69R739A–4.5 MCM69R821A–4.5		MCM69R739A–5 MCM69R821A–5		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	4.2	—	4.5	—	5	—	ns	
K Clock High Pulse Width	t_{KHKL}	1.7	—	2	—	2	—	ns	
K Clock Low Pulse Width	t_{KLKH}	1.5	—	1.75	—	2	—	ns	
C Clock High Pulse Width	t_{CHCL}	1.7		2		2		ns	
C Clock Low Pulse Width	t_{CLCH}	1.5		1.75		2		ns	
C Clock High to K Clock High Delay	t_{CHKH}	0.8		0.8		1		ns	
K Clock High to C Clock High Delay	t_{KHCH}	1.5		1.5		2		ns	
Clock High to Output Valid	t_{KHQV}	—	5.5	—	6.5	—	7.5	ns	1
C Clock High to Output Valid	t_{CHQV}		2.3		2.7		3	ns	1
C Clock High to Output Hold	t_{CHQX}	0.7		0.7		1		ns	2
Output Enable Low to Output Low–Z	t_{GLQX}	0.5	—	0.5	—	0.5	—	ns	2
Output Enable Low to Output Valid	t_{GLQV}	—	2.1	—	2.5	—	2.5	ns	1
Output Enable to Output Hold	t_{GHQX}	0.5	—	0.5	—	0.5	—	ns	2
Output Enable High to Output High–Z	t_{GHQZ}	—	2	—	2.3	—	2.5	ns	2
Setup Times: Address Data In Chip Select Write Enable Output Enable	t_{AVKH} t_{DVKH} t_{SVKH} t_{WVKH} t_{GVKH}	0.5	—	0.5	—	0.5	—	ns	
Hold Times: Address Chip Select Write Enable Output Enable	t_{KHAX} t_{KHSX} t_{KHWX} t_{KHGX}	1	—	1	—	1	—	ns	
Hold Time Data In	t_{KHDX}	0.8	—	1	—	1	—	ns	

NOTES:
1. Tested per AC Test Load diagram. See Figure 2.
2. Measured at ± 200 mV from steady state.
3. In no case may control input signals (e.g., $\overline{SS}$) be operated with pulse widths less than the minimum clock input pulse width specifications (e.g., t_{KHKL}) or at frequencies that exceed the applied K clock frequency.

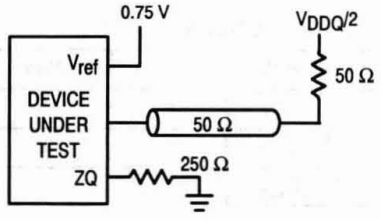


Figure 2. AC Test Load

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

AC INPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Note
AC Input Logic High (See Figure 4)	V_{IH} (ac)	V_{ref} + 200 mV		
AC Input Logic Low (See Figure 3 and 4)	V_{IL} (ac)		V_{ref} – 200 mV	1
Input Reference Peak to Peak ac Voltage	V_{ref}(ac)		5% V_{ref} (dc)	2
Clock Input Differential Voltage	V_{DIF} (ac)	400 mV	V_{DD} + 600 mV	3

NOTES:
1. Inputs may undershoot to – 0.5 V (peak) for up to 20% t_{KHKH} (e.g., 2 ns at a clock cycle time of 10 ns).
2. Although considerable latitude in the selection of the nominal dc value (i.e., rms value) of V_{ref} is supported, the peak to peak ac component superimposed on V_{ref} may not exceed 5% of the dc component of V_{ref}.
3. Minimum differential input voltage required for differential input clock operation.

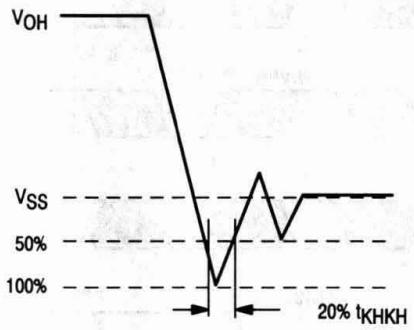


Figure 3. Undershoot Voltage

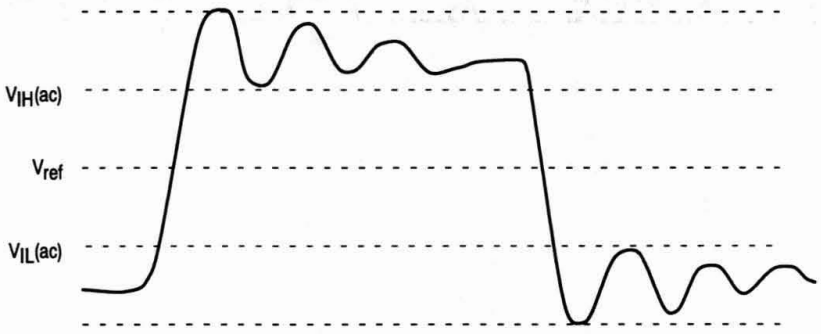
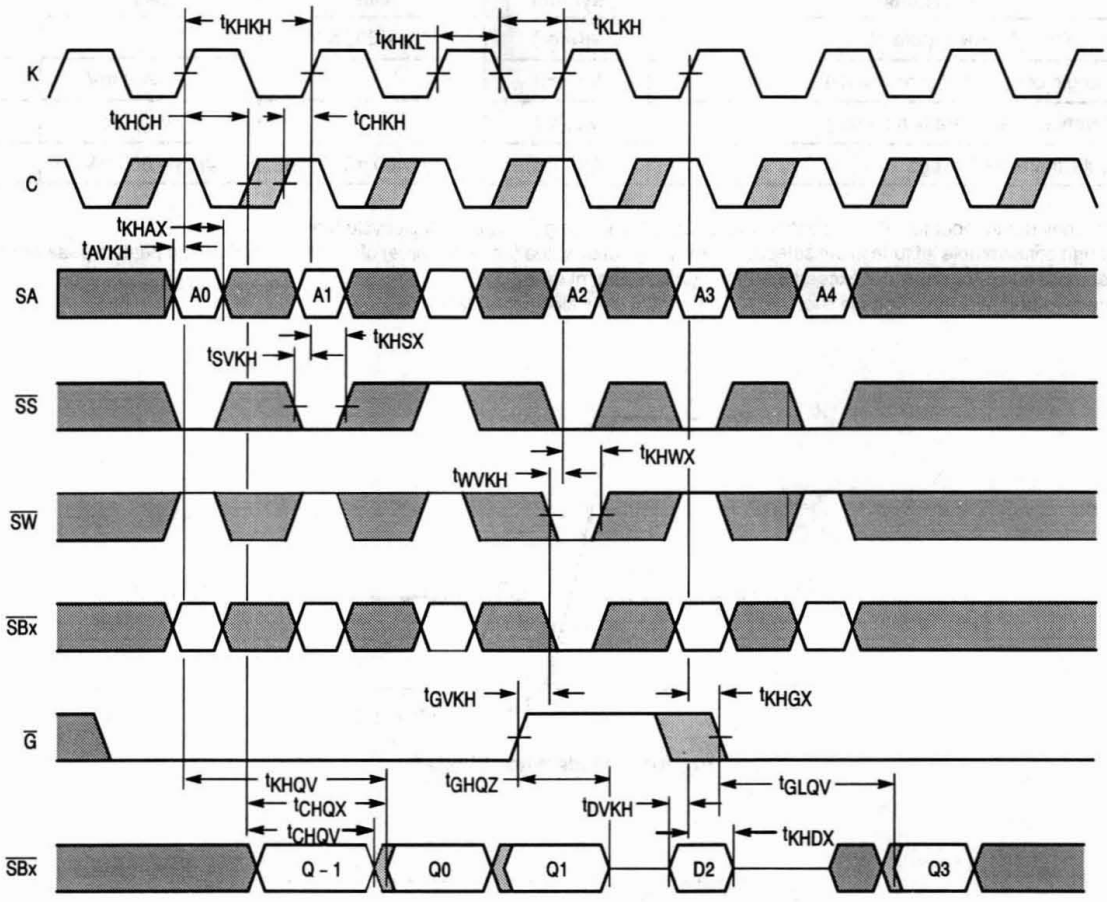
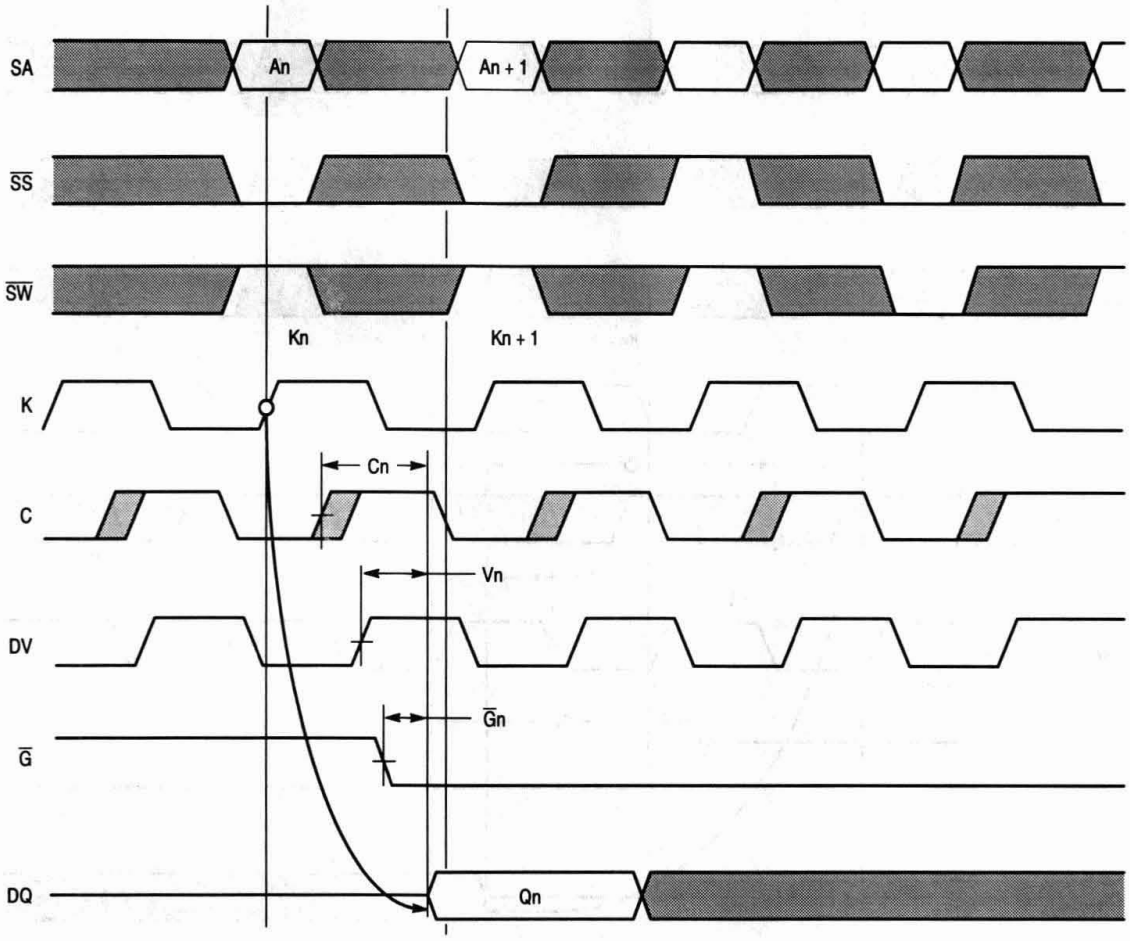


Figure 4. Differential Inputs/Common Mode Input Voltage

BASIC TIMING



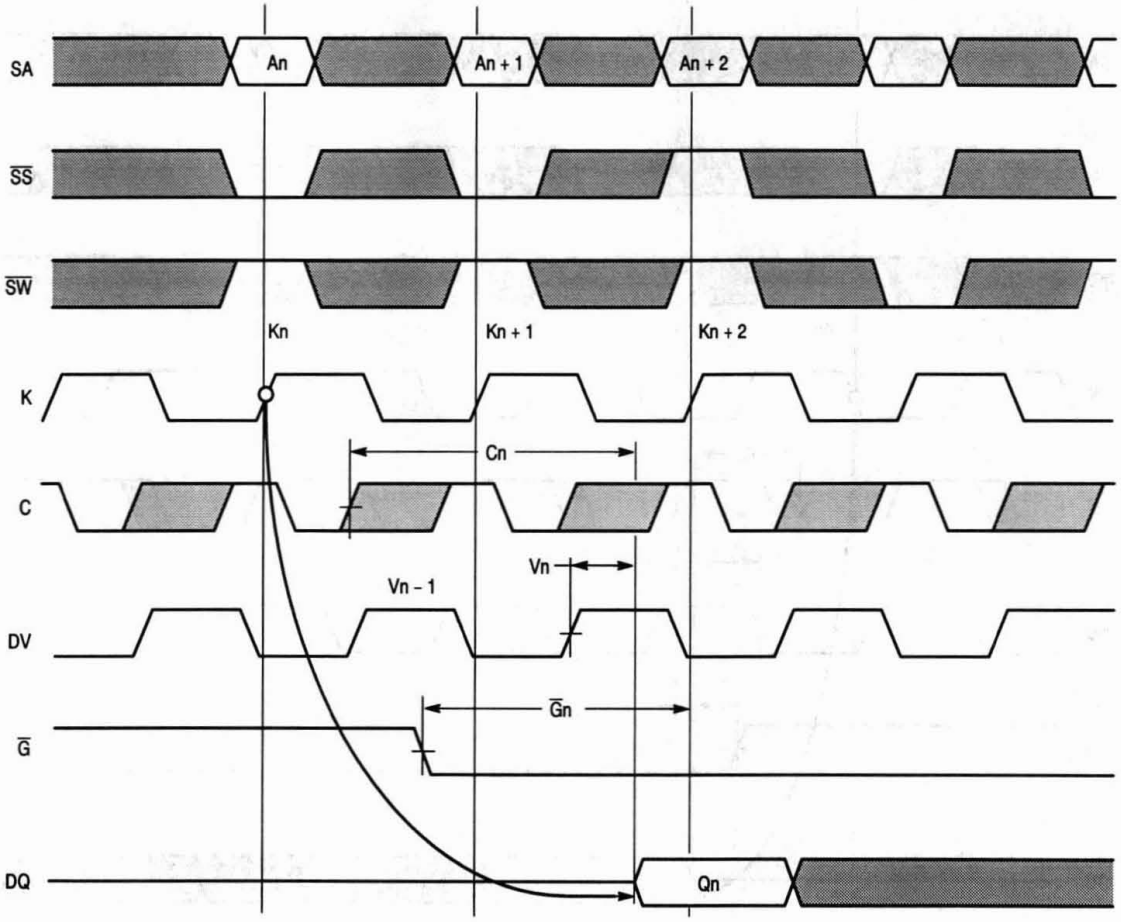
READ TIMING OUTPUT ENABLE ($t_{KHQV} < t_{KHKH}$)



NOTE:

1. The outputs are enabled by a combination of events, both internal and external.
2. DV is an internal signal and is not visible externally. It indicates when new valid data is available. Actual output enable occurs only after all three events; C clock, DV, $\overline{G}$ have occurred for cycle Kn. They do not have to occur in the order shown.

READ TIMING OUTPUT ENABLE ($t_{KHQV} > t_{KHKH}$)



NOTE:

1. The outputs are enabled by a combination of events, both internal and external.
2. DV is an internal signal and is not visible externally. It indicates when new valid data is available. Actual output enable occurs only after all three events; C clock, DV, $\overline{G}$ have occurred for cycle Kn. They do not have to occur in the order shown.

FUNCTIONAL OPERATION

GENERAL

All control signals except $\overline{G}$ are registered on the rising edge of the K clock. All signals must meet the setup and hold times shown in the AC Characteristics table.

OUTPUT ENABLE and $\overline{G}$

$\overline{G}$ asynchronously three–states the output buffers. However when going from three–state to a low–Z condition, the state and timing of K, C, $\overline{SW}$, $\overline{SS}$, and $\overline{G}$ determine when the data bus comes out of three–state. The Read Timing Output Enable Timing diagrams ($t_{KHQV} < t_{KHKH}$) and ($t_{KHQV} > t_{KHKH}$) show the conditions that must occur before the output is enabled.

If $\overline{SS}$ is high at the rising edge of K the device will be deselected at the next rising edge of the C clock, if it is not already deselected from a previous event.

READ OPERATION

The read operation is controlled by $\overline{G}$, K, C , $\overline{SW}$, and $\overline{SS}$. The K and C clock operate at the same frequency but are shifted in phase with each other. There is a minimum separation of the K and C clock as specified by t_{KHCH} and t_{CHKH}. The rising edge of the C clock allows valid data to be output and disables further changes in the output until the next rising edge of C clock.

WRITE OPERATION

$\overline{G}$ must be used to three–state the data bus for a write cycle. $\overline{SW}$ does not three–state the bus.

The write address is sampled on the first rising edge of K clock and write data is sampled on the following rising edge.

The late write feature is implemented with single stage write buffering. Write buffering is transparent to the user. A comparator monitors the address bus and, when necessary, routes buffer contents to the outputs to assure coherent operation. This occurs in all cases whether there is a byte write or a full word is written.

Data is transferred to the array at the next write cycle.

WRITE AND BYTE WRITE FUNCTIONS

Note that in the following discussion the term "byte" refers to nine bits of the RAM I/O bus. In all cases, the timing parameters described for synchronous write input ($\overline{SW}$) apply to each of the byte write enable inputs ($\overline{SBa}$, $\overline{SBb}$, etc.).

Byte write enable inputs have no effect on read cycles. This allows the system designer not interested in performing byte writes to connect the byte enable inputs to active low (V_{SS}). Reads of all bytes proceed normally and write cycles, activated via a low on $\overline{SW}$, and the rising edge of the K clock, write the entire RAM I/O width. This way the designer is spared having to drive multiple write input buffer loads.

Byte writes are performed using the byte write enable inputs in conjunction with the synchronous write input ($\overline{SW}$). It is important to note that writing any one byte will inhibit a read of all bytes at the current address. The RAM cannot simultaneously read one byte and write another at the same address. A write cycle initiated with none of the byte write enable inputs active is neither a read or a write. No write will occur.

PROGRAMMABLE IMPEDANCE OPERATION

The designer can program the RAMs output buffer impedance by terminating the ZQ pin to V_{SS} through a precision resistor (RQ). The value of RQ is five times the output impedance desired. For example, 250 Ω resistor will give an output impedance of 50 Ω.

Impedance updates occur continuously and the frequency of the update is based on the subdivided K clock. Note that if the K clock stops so does the impedance update.

The actual change in the impedance occurs in small increments and is monotonic. There are no significant disturbances that occur on the output because of this smooth update method.

The impedance update is not related to any particular type of cycle because the impedance is updated continuously and is based on the K clock. Updates occur regardless of whether the the device is performing a read, write or a deselect cycle and does not depend on the state of $\overline{G}$.

At power up, the output impedance defaults to approximately 50 ohms. It will take 4,000 to 16,000 cycles for the impedance to be completely updated if the programmed impedance is much higher or lower than 50 Ω.

The output buffers can also be programmed in a minimum impedance configuration by connecting ZQ to V_{DD}.

POWER UP AND INITIALIZATION

The following supply voltage application sequence is recommended: V_{SS}, V_{DD}, then V_{DDQ}. Please note, per the Absolute Maximum Ratings table, V_{DDQ} is not to exceed V_{DD} + 0.5 V, whatever the instantaneous value of V_{DD}. Once supplies have reached specification levels, a minimum dwell of 1.0 ms with C/K clock inputs cycling is required before beginning normal operations. At power up the output impedance will be set at approximately 50 Ω as stated above.

SERIAL BOUNDARY SCAN TEST ACCESS PORT OPERATION

OVERVIEW

The serial boundary scan test access port (TAP) on this RAM is designed to operate in a manner consistent with IEEE Standard 1149.1–1990 (commonly referred to as JTAG), but does not implement all of the functions required for 1149.1 compliance. Certain functions have been modified or eliminated because their implementation places extra delays in the RAMs critical speed path. Nevertheless, the RAM supports the standard TAP controller architecture. (The TAP controller is the state machine that controls the TAPs operation) and can be expected to function in a manner that does not conflict with the operation of devices with Standard 1149.1 compliant TAPs. The TAP operates using conventional JEDEC Standard 8–1B Low Voltage (3.3 V) TTL / CMOS logic level signaling.

DISABLING THE TEST ACCESS PORT

It is possible to use this device without utilizing the TAP. To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid level inputs. TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a 1 k resistor. TDO should be left unconnected.

TAP DC OPERATING CHARACTERISTICS

($0°C \le T_A \le 70°C$, Unless Otherwise Noted)

Parameter	Symbol	Min	Max	Unit	Note
Logic Input Logic High	$V_{IH}1$	2.0	V_{DD} + 0.3	V	
Logic Input Logic Low	$V_{IL}1$	– 0.3	0.8	V	
Logic Input Leakage Current	I_{lkg}	—	± 5	µA	1
Output Logic Low	$V_{OL}1$	—	0.2	V	2
Output Logic High	$V_{OH}1$	V_{DD} – 0.2	—	V	3
Output Logic Low	$V_{OL}2$	—	0.4	V	4
Output Logic High	$V_{OH}2$	2.4	—	V	5

NOTES:
1. 0 V ≤ Vin ≤ VDDQ for all logic input pins.
2. IOL1 ≤ 100 µA @ VOL = 0.2 V. Sampled, not 100% tested.
3. IIOH1I ≤ 100 µA @ VDDQ – 0.2 V. Sampled, not 100% tested.
4. IOL2 ≤ 8 mA @ VOL = 0.4 V.
5. IIOH2I ≤ 8 mA @ VOH = 2.4 V.

TAP AC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V

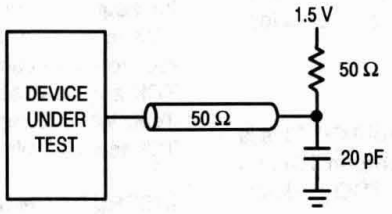
Output Test Load ..... 50 Ω Parallel Terminated T–line with 20 pF Receiver Input Capacitance
Test Load Termination Supply Voltage (VT) ..... 1.5 V

TAP CONTROLLER TIMING

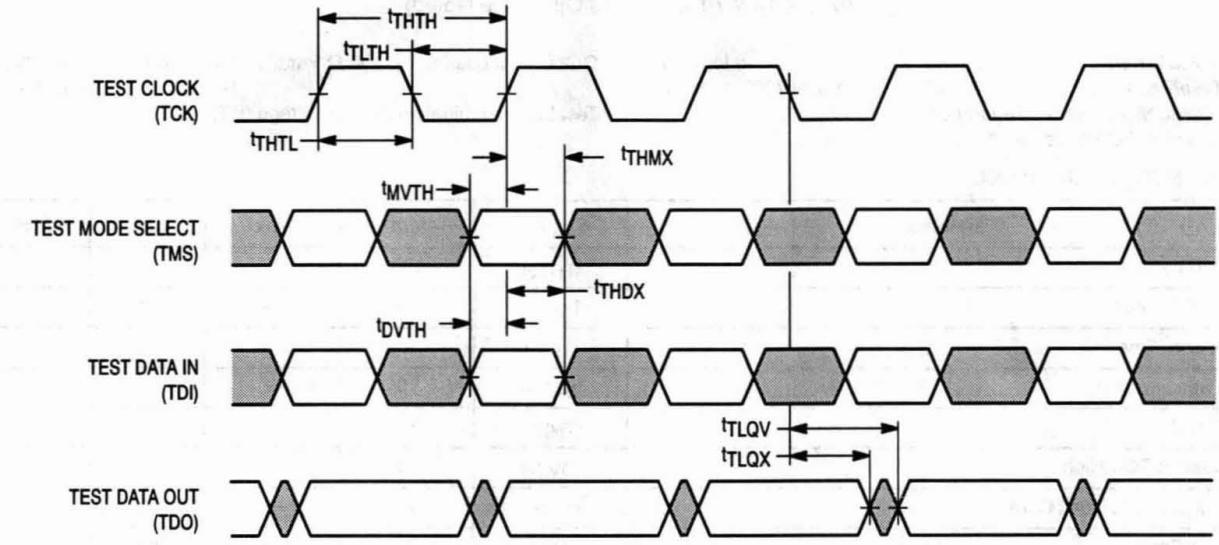
Parameter	Symbol	Min	Max	Unit	Notes
Cycle Time	t_{THTH}	100	—	ns	
Clock High Time	t_{THTL}	40	—	ns	
Clock Low Time	t_{TLTH}	40	—	ns	
TMS Setup	t_{MVTH}	10	—	ns	
TMS Hold	t_{THMX}	10	—	ns	
TDI Valid to TCK High	t_{DVTH}	10	—	ns	
TCK High to TDI Don't Care	t_{THDX}	10	—	ns	
Capture Setup	t_{CS}	10	—	ns	1
Capture Hold	t_{CH}	10	—	ns	1
TCK Low to TDO Unknown	t_{TLQX}	0	—	ns	
TCK Low to TDO Valid	t_{TLOV}	—	20	ns	

NOTES:
1. t_{CS} + t_{CH} defines the minimum pause in RAM I/O pad transitions to assure accurate pad data capture.

AC TEST LOAD



TAP CONTROLLER TIMING DIAGRAM



TEST ACCESS PORT PINS

TCK – TEST CLOCK (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

TMS – TEST MODE SELECT (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.

TDI – TEST DATA IN (INPUT)

The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (refer to Figure 6 TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.

TDO – TEST DATA OUT (OUTPUT)

Output that is active depending on the state of the TAP state machine (refer to Figure 6 TAP Controller State Diagram). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

TRST – TAP RESET

This device does not have a TRST pin. TRST is optional in IEEE 1149.1. The test–logic reset state is entered while TMS is held high for five rising edges of TCK. Power on reset circuitry is included internally. This type of reset does not affect the operation of the system logic. The reset affects test logic only.

TEST ACCESS PORT REGISTERS

OVERVIEW

The various TAP registers are selected (one at a time) via the sequences of ones and zeros input to the TMS pin as the TCK is strobed. Each of the TAPs registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on subsequent falling edge of TCK. When a register is selected it is "placed" between the TDI and TDO pins.

INSTRUCTION REGISTER

The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run test/idle or the various data register states. The instructions are three bits long. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power–up or whenever the controller is placed in test–logic–reset state.

BYPASS REGISTER

The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.

BOUNDARY SCAN REGISTER

The boundary scan register is identical in length to the number of active input and I/O connections on the RAM (not counting the TAP pins). This also includes a number of place holder locations (always set to a logic 1) reserved for density upgrade address pins. There are a total of 70 bits in the case of the x36 device and 51 bits in the case of the x18 device. The boundary scan register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture–DR state and then is placed between the TDI and TDO pins when the controller is moved to shift–DR state. Several TAP instructions can be used to activate the boundary scan register.

The Bump/Bit Scan Order tables describe which device bump connects to each boundary scan register location. The first column defines the bit's position in the boundary scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the input or I/O at the bump and the third column is the bump number.

IDENTIFICATION (ID) REGISTER

The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture–DR state with the IDCODE command loaded in the instruction register. The code is loaded from a 32 bit on–chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into shift–DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Presence Indicator

Bit #	0
Value	1

Motorola JEDEC ID Code (Compressed Format, per IEEE Standard 1149.1 – 1990

Bit #	11	10	9	8	7	6	5	4	3	2	1
Value	0	0	0	0	0	0	0	1	1	1	0

Reserved For Future Use

Bit #	17	16	15	14	13	12
Value	x	x	x	x	x	x

Device Width

Configuration	Bit #	22	21	20	19	18
128Kx36	Value	0	0	1	0	0
256Kx18	Value	0	0	0	1	1

Device Depth

Configuration	Bit #	27	26	25	24	23
128Kx36	Value	0	0	1	0	1
256Kx18	Value	0	0	1	1	0

Revision Number

Bit #	31	30	29	28
Value	x	x	x	x

Figure 5. ID Register Bit Meanings

MCM69R739A Bump/Bit Scan Order

BIT #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	SA	3B
2	SA	4P		37	NC	2B
3	SA	4T		38	SA	3A
4	SA	6R		39	SA	3C
5	SA	5T		40	SA	2C
6	ZZ	7T		41	SA	2A
7	DQa	6P		42	DQc	2D
8	DQa	7P		43	DQc	1D
9	DQa	6N		44	DQc	2E
10	DQa	7N		45	DQc	1E
11	DQa	6M		46	DQc	2F
12	DQa	6L		47	DQc	2G
13	DQa	7L		48	DQc	1G
14	DQa	6K		49	DQc	2H
15	DQa	7K		50	DQc	1H
16	$\overline{SBa}$	5L		51	$\overline{SBc}$	3G
17	$\overline{K}$	4L		52	ZQ	4D
18	K	4K		53	$\overline{SS}$	4E
19	$\overline{G}$	4F		54	$\overline{C}$	4G
20	$\overline{SBb}$	5G		55	C	4H
21	DQb	7H		56	$\overline{SW}$	4M
22	DQb	6H		57	$\overline{SBd}$	3L
23	DQb	7G		58	DQd	1K
24	DQb	6G		59	DQd	2K
25	DQb	6F		60	DQd	1L
26	DQb	7E		61	DQd	2L
27	DQb	6E		62	DQd	2M
28	DQb	7D		63	DQd	1N
29	DQb	6D		64	DQd	2N
30	SA	6A		65	DQd	1P
31	SA	6C		66	DQd	2P
32	SA	5C		67	SA	3T
33	SA	5A		68	SA	2R
34	NC	6B		69	SA	4N
35	SA	5B		70	M1	3R

MCM69R821A Bump/Bit Scan Order

Bit #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	$\overline{SBb}$	3G
2	SA	6T		37	ZQ	4D
3	SA	4P		38	$\overline{SS}$	4E
4	SA	6R		39	$\overline{C}$	4G
5	SA	5T		40	C	4H
6	ZZ	7T		41	$\overline{SW}$	4M
7	DQa	7P		42	DQb	2K
8	DQa	6N		43	DQb	1L
9	DQa	6L		44	DQb	2M
10	DQa	7K		45	DQb	1N
11	$\overline{SBa}$	5L		46	DQb	2P
12	$\overline{K}$	4L		47	SA	3T
13	K	4K		48	SA	2R
14	$\overline{G}$	4F		49	SA	4N
15	DQa	6H		50	SA	2T
16	DQa	7G		51	M1	3R
17	DQa	6F				
18	DQa	7E				
19	DQa	6D				
20	SA	6A				
21	SA	6C				
22	SA	5C				
23	SA	5A				
24	NC	6B				
25	SA	5B				
26	SA	3B				
27	NC	2B				
28	SA	3A				
29	SA	3C				
30	SA	2C				
31	SA	2A				
32	DQb	1D				
33	DQb	2E				
34	DQb	2G				
35	DQb	1H				

NOTES:

1. The NC pads listed in this table are indeed no connects, but are represented in the boundary scan register by a "place holder" bit that is forced to logic 1. These pads are reserved for use as address inputs on higher density RAMs that follow this pad out and scan order standard.
2. K, $\overline{K}$, C, $\overline{C}$ are sampled individually. $\overline{K}$, $\overline{C}$ is not simply a forced complement of the K, C input. In scan mode these differential inputs are referenced to V_{ref}, not each other.
3. ZQ, M1, and M2 are not ordinary inputs and may not respond to standard I/O logic levels. ZQ, M1, and M2 must be driven to within 100 mV of a V_{DD} or V_{SS} supply rail to ensure consistent results.
4. ZZ must remain at V_{IL} during boundary scan to ensure consistent results.

TAP CONTROLLER INSTRUCTION SET

OVERVIEW

There are two classes of instructions defined in the Standard 1149.1–1990; the standard (public) instructions, and device specific (private) instructions. Some public instructions, are mandatory for 1149.1 compliance. Optional public instructions must be implemented in prescribed ways.

Although the TAP controller in this device follows the 1149.1 conventions, it is not 1194.1 compliant because some of the mandatory instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads, but cannot be used to load address, data or control signals into the RAM or to preload the I/O buffers. In other words, the device will not perform Standard 1149.1 EXTEST, INTEST or the preload portion of the SAMPLE / PRELOAD command.

When the TAP controller is placed in capture–IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the shift–IR state the instruction register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to update–IR state. The TAP instruction sets for this device are listed in the following tables.

STANDARD (PUBLIC) INSTRUCTIONS

BYPASS

The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift–DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

Sample/preload is a Standard 1149.1 mandatory public instruction. When the sample / preload instruction is loaded in the Instruction register, moving the TAP controller into the capture–DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set–up plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register.

Moving the controller to shift–DR state then places the boundary scan register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the update–DR state with the SAMPLE / PRELOAD instruction loaded in the instruction register has the same effect as the pause–DR command. This functionality is not Standard 1149.1 compliant.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic 0s. EXTEST is not implemented in this device. Therefore this device is not 1149.1 compliant. Nevertheless, this RAMs TAP does respond to an all zeros instruction, as follows. With the EXTEST (000) instruction loaded in the instruction register the RAM responds just as it does in response to the SAMPLE/PRELOAD instruction described above, except the RAM outputs are forced to high–Z any time the instruction is loaded.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture–DR mode and places the ID register between the TDI and TDO pins in shift–DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test–logic–reset state.

THE DEVICE SPECIFIC (PUBLIC) INSTRUCTION

SAMPLE–Z

If the SAMPLE–Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high–Z) and the boundary scan register is connected between TDI and TDO when the TAP controller is moved to the shift–DR state.

THE DEVICE SPECIFIC (PRIVATE) INSTRUCTION

NOOP

Do not use these instructions; they are reserved for future use.

STANDARD (PUBLIC) INSTRUCTION CODES

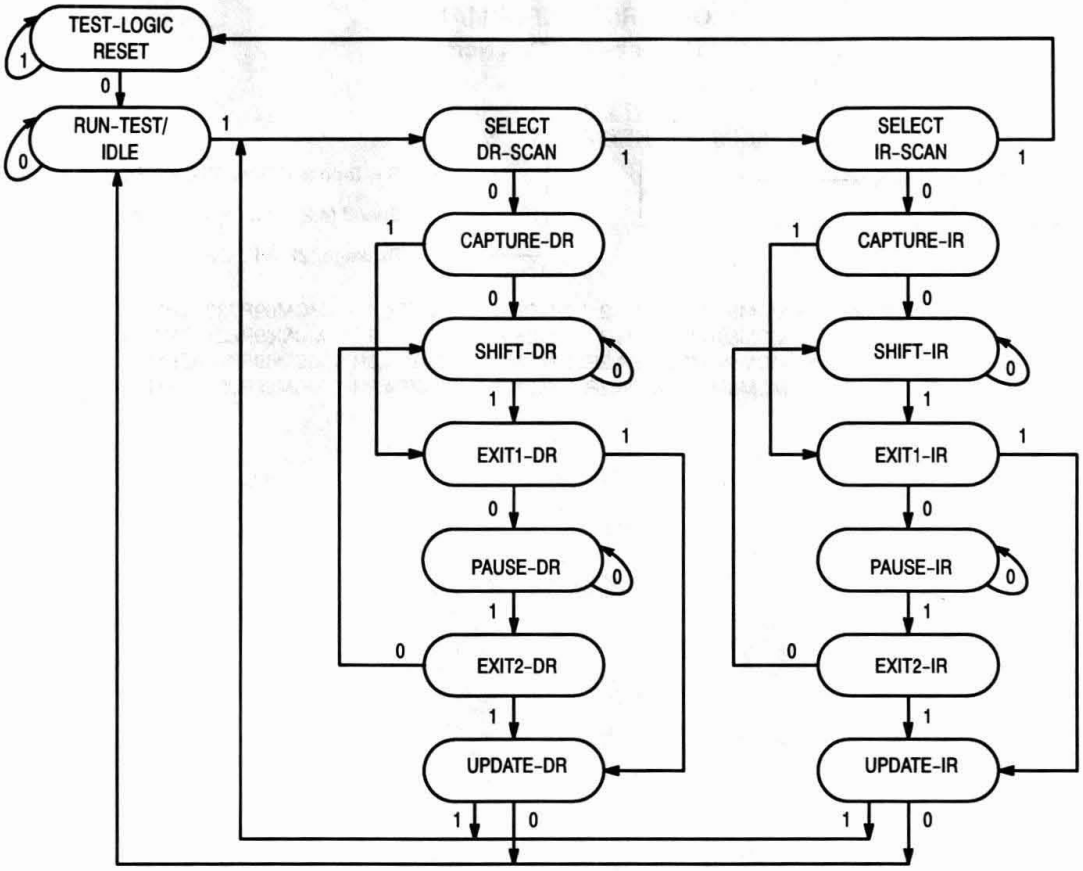
Instruction	Code*	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM outputs to High–Z state. *NOT 1149.1 COMPLIANT*
IDCODE	001**	Preloads ID register and places it between TDI and TDO. Does not affect RAM operation.
SAMPLE / PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect RAM operation. Does not implement 1149.1 Preload function. * NOT 1149.1 COMPLIANT *
BYPASS	111	Places bypass register between TDI and TDO. Does not affect RAM operation.
SAMPLE–Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM output drivers to High–Z.

* Instruction codes expressed in binary, MSB on left, LSB on right.
** Default instruction automatically loaded at power–up and in test–logic–reset state.

STANDARD (PRIVATE) INSTRUCTION CODES

Instruction	Code*	Description
NO OP	011	Do not use these instructions; they are reserved for future use.
NO OP	101	Do not use these instructions; they are reserved for future use.
NO OP	110	Do not use these instructions; they are reserved for future use.

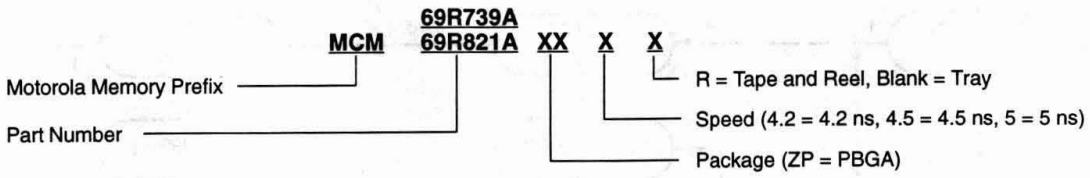
* Instruction codes expressed in binary, MSB on left, LSB on right.



NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 6. TAP Controller State Diagram

ORDERING INFORMATION
(Order by Full Part Number)



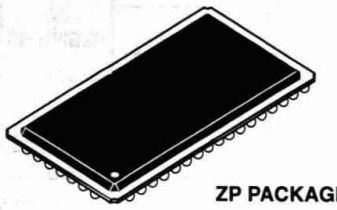
Full Part Numbers —

MCM69R739AZP4.2	MCM69R739AZP4.5	MCM69R739AZP5
MCM69R821AZP4.2	MCM69R821AZP4.5	MCM69R821AZP5
MCM69R739AZP4.2R	MCM69R739AZP4.5R	MCM69R739AZP5R
MCM69R821AZP4.2R	MCM69R821AZP4.5R	MCM69R821AZP5R

MCM69L736
MCM69L818

Advance Information

4M Late Write HSTL



ZP PACKAGE
PBGA
CASE 999–01

The MCM69L736/818 is a 4M synchronous late write fast static RAM designed to provide high performance in secondary cache and ATM switch, Telecom, and other high speed memory applications. The MCM69L818 (organized as 256K words by 18 bits) and the MCM69L736 (organized as 128K words by 36 bits) are fabricated in Motorola's high performance silicon gate BiCMOS technology.

The differential clock (CK) inputs control the timing of read/write operations of the RAM. At the rising edge of CK, all addresses, write enables, and synchronous selects are registered. An internal buffer and special logic enable the memory to accept write data on the rising edge of CK a cycle after address and control signals. Read data is available at the falling edge of CK.

The RAM uses HSTL inputs and outputs. The adjustable input trip–point (V_{ref}) and output voltage (V_{DDQ}) gives the system designer greater flexibility in optimizing system performance.

The synchronous write and byte enables allow writing to individual bytes or the entire word.

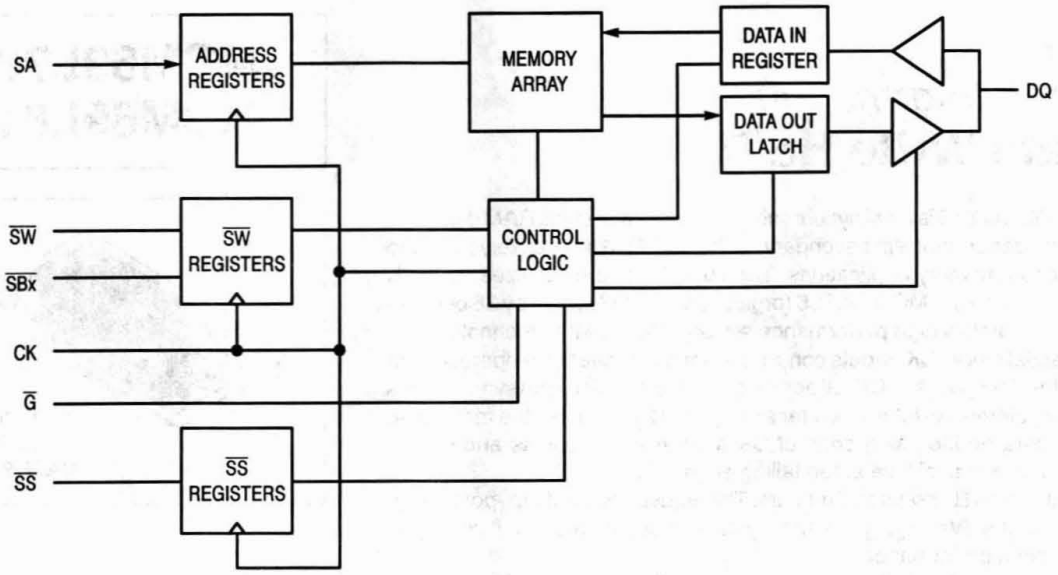
The impedance of the output buffers is programmable, allowing the outputs to match the impedance of the circuit traces which reduces signal reflections.

- Byte Write Control
- Single 3.3 V +10%, – 5% Operation
- HSTL — I/O (JEDEC Standard JESD8–6 Class I)
- HSTL — User Selectable Input Trip–Point
- HSTL — Compatible Programmable Impedance Output Drivers
- Register to Latch Synchronous Operation
- Asynchronous Output Enable
- Boundary Scan (JTAG) IEEE 1149.1 Compatible
- Differential Clock Inputs
- Optional x18 or x36 Organization
- MCM69L736/818–7 = 7 ns
  MCM69L736/818–8 = 8 ns
- 119 Bump, 50 mil (1.27 mm) Pitch, 14 mm x 22 mm Plastic Ball Grid Array (PBGA) Package

This document contains information on a new product. Specifications and information herein are subject to change without notice.

4/3/97

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENTS

TOP VIEW

MCM69L736

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	SA	NC	SA	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQc	DQc	V_{SS}	ZQ	V_{SS}	DQb	DQb
E	DQc	DQc	V_{SS}	$\overline{SS}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{G}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{SBc}$	NC	$\overline{SBb}$	DQb	DQb
H	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	V_{ref}	V_{DD}	V_{ref}	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CK	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{SBd}$	$\overline{CK}$	$\overline{SBa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{SW}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
P	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
R	NC	SA	V_{DD}	V_{DD}	V_{SS}	SA	NC
T	NC	NC	SA	SA	SA	NC	NC
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69L818

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	SA	NC	SA	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQb	NC	V_{SS}	ZQ	V_{SS}	DQa	NC
E	NC	DQb	V_{SS}	$\overline{SS}$	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	$\overline{SBb}$	NC	V_{SS}	NC	DQa
H	DQb	NC	V_{SS}	NC	V_{SS}	DQa	NC
J	V_{DDQ}	V_{DD}	V_{ref}	V_{DD}	V_{ref}	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	CK	V_{SS}	NC	DQa
L	DQb	NC	V_{SS}	$\overline{CK}$	$\overline{SBa}$	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{SW}$	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	SA	V_{SS}	DQa	NC
P	NC	DQb	V_{SS}	SA	V_{SS}	NC	DQa
R	NC	SA	V_{DD}	V_{DD}	V_{SS}	SA	NC
T	NC	SA	SA	NC	SA	SA	NC
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69L736 PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 3T, 4T, 5T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
4K	CK	Input	Address, data in, and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in, and control input register clock. Active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
5L, 5G, 3G, 3L (a), (b), (c), (d)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2U	TMS	Input	Test Mode Select (JTAG).
3U	TDI	Input	Test Data In (JTAG).
4U	TCK	Input	Test Clock (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
4D	ZQ	Input	Programmable Output Impedance: Programming pin.
(a) 6K, 7K, 6L, 7L, 6M, 6N, 7N, 6P, 7P (b) 6D, 7D, 6E, 7E, 6F, 6G, 7G, 6H, 7H (c) 1D, 2D, 1E, 2E, 2F, 1G, 2G, 1H, 2H (d) 1K, 2K, 1L, 2L, 2M, 1N, 2N, 1P, 2P	DQx	I/O	Synchronous Data I/O.
3J, 5J	V_{ref}	Supply	Input Reference: Provides reference voltage for input buffers.
4C, 2J, 4J, 6J, 4R, 3R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: Provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 3H, 5H, 3K, 5K, 3M, 5M, 3N, 5N, 3P, 5P, 5R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 4B, 6B, 7B, 1C, 7C, 4G, 4H, 1R, 7R, 1T, 2T, 6T, 7T, 6U	NC	—	No Connection: There is no connection to the chip.

MCM69L818 PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 2T, 3T, 5T, 6T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
4K	CK	Input	Address, data in, and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in, and control input register clock. Active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
5L, 3G (a), (b)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
2U	TMS	Input	Test Mode Select (JTAG).
3U	TDI	Input	Test Data In (JTAG).
4U	TCK	Input	Test Clock (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
4D	ZQ	Input	Programmable Output Impedance: Programming pin.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
(a) 6D, 7E, 6F, 7G, 6H, 7K, 6L, 6N, 7P (b) 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 2P	DQx	I/O	Synchronous Data I/O.
3J, 5J	V_{ref}	Supply	Input Reference: Provides reference voltage for input buffers.
4C, 2J, 4J, 6J, 4R, 3R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: Provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P, 5R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 4B, 6B, 7B, 1C, 7C, 2D, 7D, 1E, 6E, 2F, 1G, 4G, 6G, 2H, 4H, 7H, 1K, 6K, 2L, 7L, 6M, 2N, 7N, 1P, 6P, 1R, 7R, 1T, 4T, 7T, 6U	NC	—	No Connection: There is no connection to the chip.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS}, See Note 1)

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Output Supply Voltage	V_{DDQ}	– 0.5 to V_{DD} + 0.5	V
Voltage On Any Pin	V_{in}	– 0.5 to V_{DD} + 0.5	V
Input Current (per I/O)	I_{in}	± 50	mA
Output Current (per I/O)	I_{out}	± 70	mA
Power Dissipation (See Note 2)	P_D	—	W
Operating Temperature	T_A	0 to + 70	°C
Temperature Under Bias	T_{bias}	–10 to + 85	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability will be dependent upon package characteristics and use environment. See enclosed thermal impedance data.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

3

PBGA PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (Still Air)		$R_{\theta JA}$	53	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Single Layer Board	$R_{\theta JA}$	38	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Four Layer Board	$R_{\theta JA}$	22	°C/W	
Junction to Board (Bottom)		$R_{\theta JB}$	14	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	5	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (See Notes 1 through 4)

Parameter		Symbol	Min	Typ–7	Typ–8	Max	Unit	Notes
Core Power Supply Voltage		V_{DD}	3.15	—	—	3.6	V	
Output Driver Supply Voltage		V_{DDQ}	1.4	—	—	1.6	V	
Input Reference DC Voltage		V_{ref} (dc)	0.6	—	—	1.1	V	10
Active Power Supply Current	(x18) (x36)	I_{DD1}	— —	300 390	290 380	400 490	mA	5
Quiescent Active Power Supply Current		I_{DD2}	—	190	190	250	mA	6
Active Standby Power Supply Current		I_{SB1}	—	150	150	250	mA	7
Quiescent Standby Power Supply Current		I_{SB2}	—	130	130	230	mA	8

NOTES:

1. All data sheet parameters specified to full range of V_{DD} unless otherwise noted. All voltages are referenced to voltage applied to V_{SS} bumps.
2. Supply voltage applied to V_{DD} connections.
3. Supply voltage applied to V_{DDQ} connections when using the RAM in push–pull output configuration.
4. All power supply currents measured with outputs open or deselected.
5. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered active, 50% read cycles.
6. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered active.
7. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered inactive, ZZ low.
8. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered inactive, ZZ high.
9. 200 mV ≥ V_{in} ≥ V_{DDQ} – 200 mV.
10. Although considerable latitude in the selection of the nominal dc value (i.e., rms value) of V_{ref} is supported, the peak to peak ac component superimposed on V_{ref} may not exceed 5% of the dc component of V_{ref}.

DC INPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
DC Input Logic High	V_{IH} (dc)	V_{ref} + 0.1	V_{DD} + 0.3	V	
DC Input Logic Low	V_{IL} (dc)	– 0.3	V_{ref} – 0.1	V	1
Input Reference DC Voltage	V_{ref} (dc)	0.6	1.1	V	2
Input Leakage Current	$I_{lkg(1)}$	—	± 5	µA	3
Clock Input Signal Voltage	V_{in}	– 0.3	V_{DD} + 0.3	V	
Clock Input Differential Voltage	V_{DIF} (dc)	0.1	V_{DD} + 0.6	V	4
Clock Input Common Mode Voltage Range (See Figure 3)	V_{CM} (dc)	0.68	1.1	V	5
Clock Input Crossing Point Voltage Range	V_X	0.68	1.1	V	

NOTES:

1. Inputs may undershoot to – 0.5 V (peak) for up to 20% t_{KHKH} (e.g., 2 ns at a clock cycle time of 10 ns).
2. Although considerable latitude in the selection of the nominal dc value (i.e., rms value) of V_{ref} is supported, the peak–to–peak ac component superimposed on V_{ref} may not exceed 5% of the dc component of V_{ref}.
3. 0 V ≤ V_{in} ≤ V_{DDQ} for all pins.
4. Minimum instantaneous differential input voltage required for differential input clock operation.
5. Maximum rejectable common mode input voltage variation.

DC OUTPUT BUFFER CHARACTERISTICS – PROGRAMMABLE IMPEDANCE PUSH–PULL OUTPUT BUFFER MODE

($0°C \le T_A \le 70°C$, Unless Otherwise Noted, See Notes 5 and 6)

Parameter	Symbol	Min	Max	Unit	Notes
Output Logic Low	V_{OL}	$V_{DDQ}/2 - 0.025$	$V_{DDQ}/2 + 0.025$	V	1
Output Logic High	V_{OH}	$V_{DDQ}/2 - 0.025$	$V_{DDQ}/2 + 0.025$	V	2
Light Load Output Logic Low	$V_{OL}1$	V_{SS}	0.2	V	3
Light Load Output Logic High	$V_{OH}1$	$V_{DDQ} - 0.2$	V_{DDQ}	V	4

NOTES:
1. $I_{OL} = (V_{DDQ}/2)/(RQ/5)$ for values of $RQ = 175\ \Omega \le RQ \le 350\ \Omega$.
2. $|I_{OH}| = (V_{DDQ}/2)/(RQ/5)$ for values of $RQ = 175\ \Omega \le RQ \le 350\ \Omega$.
3. $I_{OL} \le 100\ \mu A$
4. $|I_{OH}| \le 100\ \mu A$
5. The impedance controlled mode is expected to be used in point–to–point applications, driving high impedance inputs.
6. The ZQ pin is connected through RQ to V_{SS} for the controlled impedance mode.

3

DC OUTPUT BUFFER CHARACTERISTICS — MINIMUM IMPEDANCE PUSH–PULL OUTPUT BUFFER MODE

($0°C \le T_A \le 70°C$, $ZQ = V_{DD}$) (See Notes 1 and 2)

Parameter	Symbol	Min	Max	Unit	Notes
Output Logic Low	$V_{OL}2$	V_{SS}	0.4	V	3
Output Logic High	$V_{OH}2$	$V_{DDQ} - 0.4$	V_{DDQ}	V	4
Light Load Output Logic Low	$V_{OL}3$	V_{SS}	0.2	V	5
Light Load Output Logic High	$V_{OH}3$	$V_{DDQ} - 0.2$	V_{DDQ}	V	6

NOTES:
1. The push–pull output mode is expected to be used in bussed applications and may be series or parallel terminated. Conforms to the JEDEC Standard JESD8–6 Class I.
2. The ZQ pin is connected to V_{DD} to enable the minimum impedance mode.
3. $I_{OL} \le 8$ mA.
4. $|I_{OH}| \le 8$ mA.
5. $I_{OL} \le 100\ \mu A$.
6. $|I_{OH}| \le 100\ \mu A$.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, $0°C \le T_A \le 70°C$, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	5	5	pF
Input/Output Capacitance	$C_{I/O}$	6	8	pF
CK, $\overline{CK}$ Capacitance	C_{CK}	6	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Input Pulse Levels	0.25 to 1.25 V
Input Rise/Fall Time	1 V/ns (20% to 80%)
Input Timing Measurement Reference Level	0.75 V
Output Timing Reference Level	0.75 V
Clock Input Timing Reference Level	Differential Cross–Point
RQ for 50 Ω Impedance	250 Ω

READ/WRITE CYCLE TIMING (See Note 1)

Parameter	Symbol	MCM69L736–7 MCM69L818–7 Min	MCM69L736–7 MCM69L818–7 Max	MCM69L736–8 MCM69L818–8 Min	MCM69L736–8 MCM69L818–8 Max	Unit	Notes
Cycle Time	t_{KHKH}	7	—	8	—	ns	
Clock High Pulse Width	t_{KHKL}	2.8	—	3.2	—	ns	
Clock Low Pulse Width	t_{KLKH}	2.8	—	3.2	—	ns	
Clock High to Output Valid	t_{KHQV}	—	8.5	—	9.5	ns	2
Clock Low to Output Valid	t_{KLQV}	—	3.5	—	4.0	ns	2
Clock Low to Output Hold	t_{KLQX}	0.5	—	0.5	—	ns	2
Clock Low to Output Low–Z	t_{KLQX1}	1.0	—	1.0	—	ns	3
Clock High to Output High–Z	t_{KHQZ}	—	3.5	—	4.0	ns	3
Output Enable Low to Output Low–Z	t_{GLQX}	0.5	—	0.5	—	ns	3
Output Enable Low to Output Valid	t_{GLQV}	—	3.5	—	4.0	ns	2
Output Enable to Output Hold	t_{GHQX}	1	—	1	—	ns	2
Output Enable High to Output High–Z	t_{GHQZ}	—	3.5	—	4.0	ns	3
Setup Times: Address, Data In, Chip Select, Write Enable	t_{AVKH}, t_{DVKH}, t_{SVKH}, t_{WVKH}	0.5	—	0.5	—	ns	
Hold Times: Address, Data In, Chip Select, Write Enable	t_{KHAX}, t_{KHDX}, t_{KHSX}, t_{KHWX}	1	—	1	—	ns	

NOTES:
1. Measured at ± 200 mV from steady state.
2. In no case may control input signals (e.g., $\overline{SS}$) be operated with pulse widths less than the minimum clock input pulse width specifications (e.g., t_{KHKL}) or at frequencies that exceed the applied CK frequency.
3. Tested per AC Test Load diagram. See Figure 1.

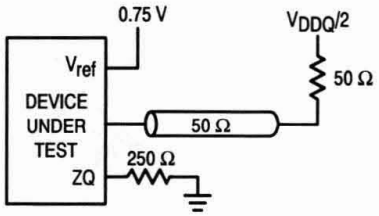


Figure 1. AC Test Load

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

AC INPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Notes
AC Input Logic High (See Figure 4)	V_{IH} (ac)	V_{ref} + 200 mV		
AC Input Logic Low (See Figures 2 and 4)	V_{IL} (ac)		V_{ref} – 200 mV	1
Input Reference Peak to Peak ac Voltage	V_{ref} (ac)		5% V_{ref} (dc)	2
Clock Input Differential Voltage	V_{dif} (ac)	400 mV	V_{DDQ} + 600 mV	3

NOTES:
1. Inputs may undershoot to – 0.5 V (peak) for up to 20% t_{KHKH} (e.g., 2 ns at a clock cycle time of 10 ns).
2. Although considerable latitude in the selection of the nominal dc value (i.e., rms value) of V_{ref} is supported, the peak to peak ac component superimposed on V_{ref} may not exceed 5% of the dc component of V_{ref}.
3. Minimum instantaneous differential input voltage required for differential input clock operation.

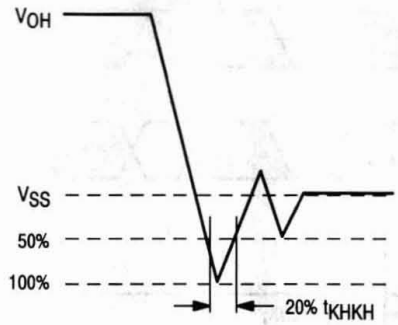
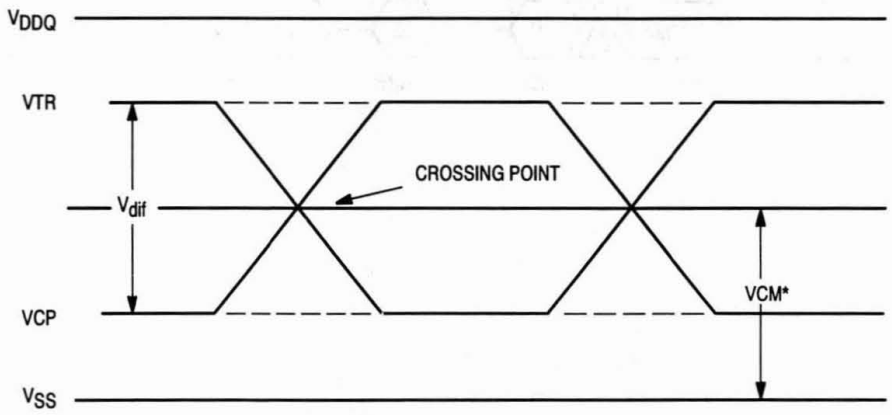


Figure 2. Undershoot Voltage



* VCM, the common mode input voltage, equals VTR – [(VTR – VCP)/2].

Figure 3. Differential Inputs/Common Mode Input Voltage

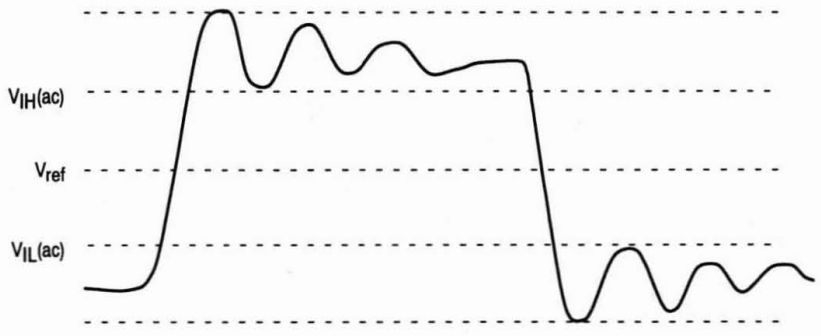
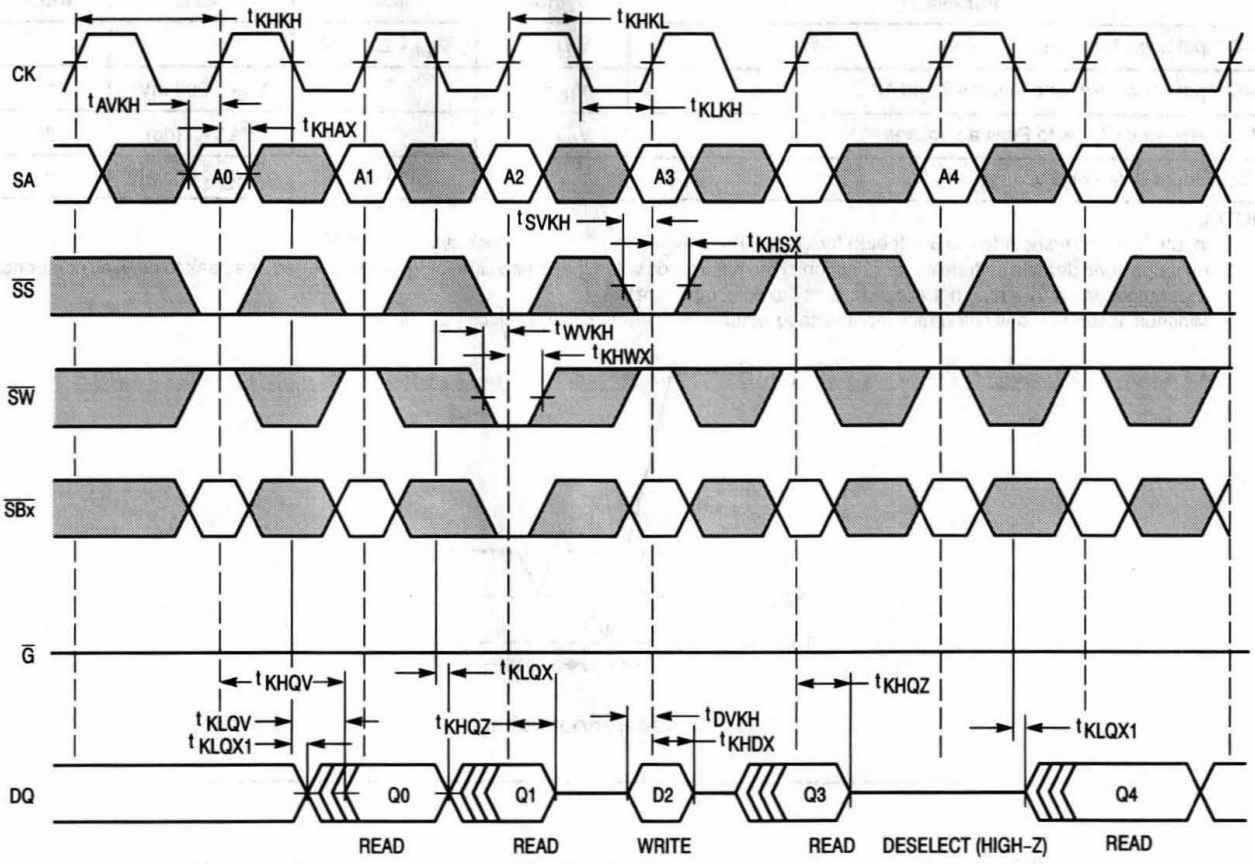
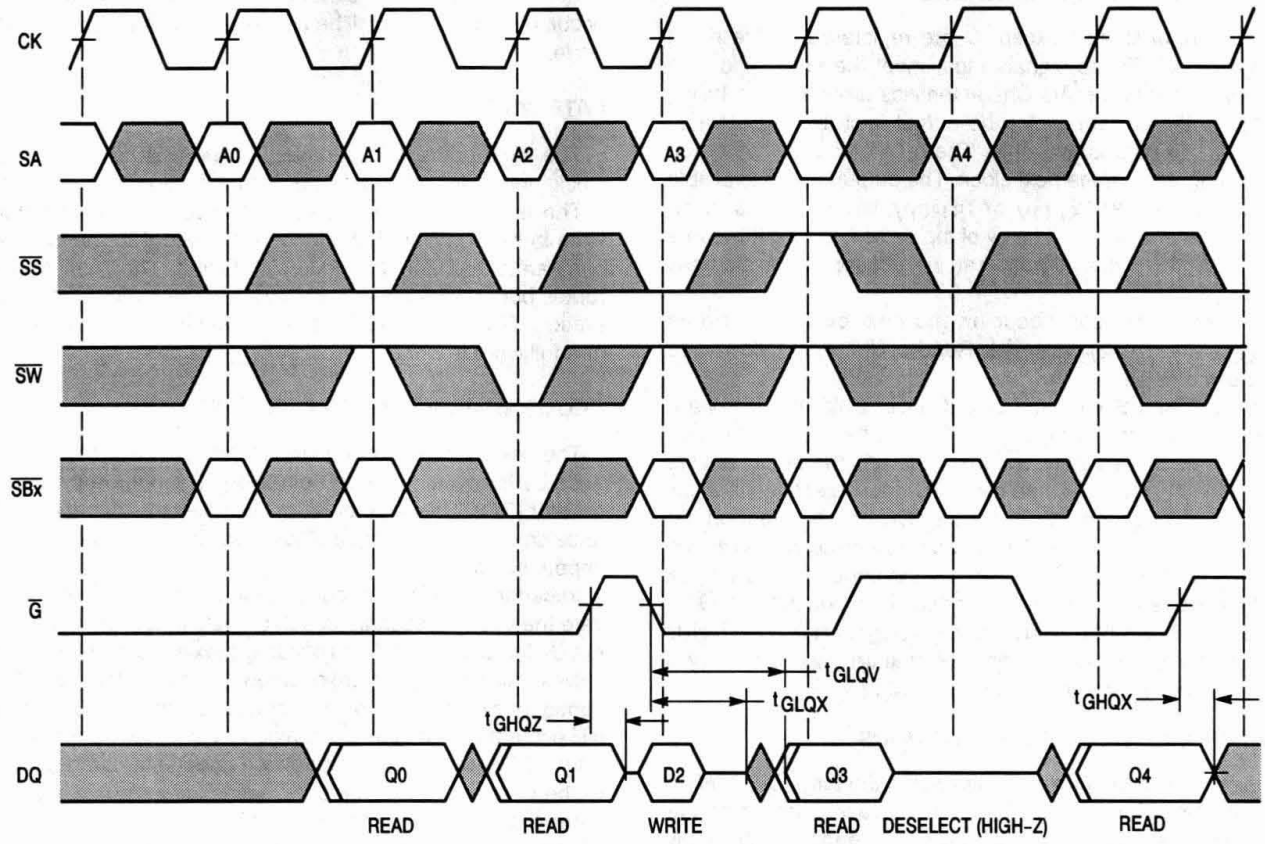


Figure 4. Differential Inputs/Common Mode Input Voltage

REGISTER LATCH READ–WRITE–READ CYCLES



REGISTER LATCH READ–WRITE–READ CYCLES
($\overline{G}$ Controlled)



FUNCTIONAL OPERATION

READ AND WRITE OPERATIONS

All control signals except $\overline{G}$ are registered on the rising edge of CK. These signals must meet the setup and hold times shown in the AC Characteristics table. On the falling edge of the current cycle, the output latch becomes transparent and data is available. The output data is latched on the rising edge of the next clock. The output data is available at the output at t_{KLQV} or t_{KHQV}, whichever is later. t_{KHQV} is the internal latency of the device. During this same cycle, a new read address can be applied to the address pins.

A write cycle can occur on the next cycle as long as t_{KLQX} and t_{DVKH} are met. Read cycles may follow write cycles immediately.

$\overline{G}$, $\overline{SS}$, and $\overline{SW}$ control output drive. Chip deselect via a high on $\overline{SS}$ at the rising edge of CK has its effect on the output drivers immediately. $\overline{SW}$ low deselects the output drivers immediately (on the same cycle). Output selecting via a low on $\overline{SS}$ and high on $\overline{SW}$ at a rising CK has its effect on the output drivers at t_{KLQX}. Output drive is also controlled directly by output enable ($\overline{G}$). $\overline{G}$ is an asynchronous input. No clock edges are required to enable or disable the output with $\overline{G}$.

Output data will be valid at t_{GLQV}, t_{KHQV}, or t_{KLQV}, which is even later. Outputs will begin driving at t_{KLQX1}. Outputs will hold previous data until t_{KLQX} or t_{GHQX}.

WRITE AND BYTE WRITE FUNCTIONS

Note that in the following discussion the term "byte" refers to nine bits of the RAM I/O bus. In all cases, the timing parameters described for synchronous write input ($\overline{SW}$) apply to each of the byte write enable inputs ($\overline{SBa}$, $\overline{SBb}$, etc.).

Byte write enable inputs have no effect on read cycles. This allows the system designer not interested in performing byte writes to connect the byte enable inputs to active low (V_{SS}). Reads of all bytes proceed normally and write cycles, activated via a low on $\overline{SW}$ and the rising edge of CK, write the entire RAM I/O width. This way the designer is spared having to drive multiple write input buffer loads.

Byte writes are performed using the byte write enable inputs in conjunction with the synchronous write input ($\overline{SW}$). It is important to note that writing any one byte will inhibit a read of all bytes at the current address. The RAM cannot simultaneously read one byte and write another at the same address. A write cycle initiated with none of the byte write enable inputs active is neither a read or a write. No write will occur, but the outputs will be deselected as in a normal write cycle.

LATE WRITE

The write address is sampled on the first rising edge of clock, and write data is sampled on the following rising edge.

The late write feature is implemented with single stage write buffering. Write buffering is transparent to the user. A comparator monitors the address bus and, when necessary, routes buffer contents to the outputs to ensure coherent operation. This occurs in all cases whether there is a byte write or a full word is written.

PROGRAMMABLE IMPEDANCE OPERATION

The designer can program the RAM's output buffer impedance by terminating the ZQ pin to V_{SS} through a precision resistor (RQ). The value of RQ is five times the output impedance desired. For example, 250 Ω resistor will give an output impedance of 50 Ω.

Impedance updates occur early in cycles that do not activate the outputs, such as deselect cycles (i.e., $\overline{SW}$, $\overline{SS}$), but not $\overline{G}$. Impedance updates occur approximately every 32 CK cycles. All clock cycles are counted. For example, after 3241 contiguous read cycles have occurred, an impedance update will occur the next time $\overline{SS}$ is high or $\overline{SW}$ is low at the rising edge of CK. In all cases impedance updates are transparent to the user and do not produce access time "push–outs" or other anomalous behavior in the RAM.

The output buffers can also be programmed in a minimum impedance configuration. The output buffers have an output impedance similar to standard LVTTL outputs but maintain V_{DDQ} and V_{SS} as the maximum output voltages.

POWER UP AND INITIALIZATION

Once supplies have reached specification levels, a minimum dwell of 1.0 µs with CK inputs cycling is required before beginning normal operations. At power up the output impedance will be set at approximately 50 Ω, however, in order to match the programmed impedance the part requires deselect cycles to occur.

SERIAL BOUNDARY SCAN TEST ACCESS PORT OPERATION

OVERVIEW

The serial boundary scan test access port (TAP) on this RAM is designed to operate in a manner consistent with IEEE 1149.1–1990 (commonly referred to as JTAG), but does not implement all of the functions required for 1149.1 compliance. Certain functions have been modified or eliminated because their implementation places extra delays in the RAMs critical speed path. Nevertheless, the RAM supports the standard TAP controller architecture. The TAP controller is the state machine that controls the TAP operation and can be expected to function in a manner that does not conflict with the operation of devices with IEEE 1149.1 compliant TAPs. The TAP operates using conventional JEDEC Standard 8–1B low voltage (3.3 V) TTL/CMOS logic level signaling.

DISABLING THE TEST ACCESS PORT

It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid–level inputs. TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic one, and may be left unconnected. But they may also be tied to V_{DD} through a 1 k resistor. TDO should be left unconnected.

3

TAP DC OPERATING CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Parameter	Symbol	Min	Max	Unit	Notes
Logic Input Logic High	$V_{IH}1$	2.0	V_{DD} + 0.3	V	
Logic Input Logic Low	$V_{IL}1$	– 0.3	0.8	V	
Logic Input Leakage Current	I_{lkg}	—	± 5	µA	1
CMOS Output Logic Low	$V_{OL}1$	—	0.2	V	2
CMOS Output Logic High	$V_{OH}1$	V_{DD} – 0.2	—	V	3
TTL Output Logic Low	$V_{OL}2$	—	0.4	V	4
TTL Output Logic High	$V_{OH}2$	2.4	—	V	5

NOTES:
1. 0 V ± V_{in} ± V_{DDQ} for all logic input pins.
2. $I_{OL}1$ ≤ 100 µA @ V_{OL} = 0.2 V. Sampled, not 100% tested.
3. $|I_{OH}1|$ ≤ 100 µA @ V_{DDQ} – 0.2 V. Sampled, not 100% tested.
4. $I_{OL}2$ ≤ 8 mA @ V_{OL} = 0.4 V.
5. $|I_{OH}2|$ ≤ 8 mA @ V_{OH} = 2.4 V.

TAP AC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V

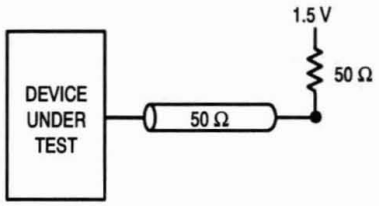
Output Test Load ..... 50 Ω Parallel Terminated T–line with 20 pF Receiver Input Capacitance
Test Load Termination Supply Voltage (V_T) ..... 1.5 V

TAP CONTROLLER TIMING

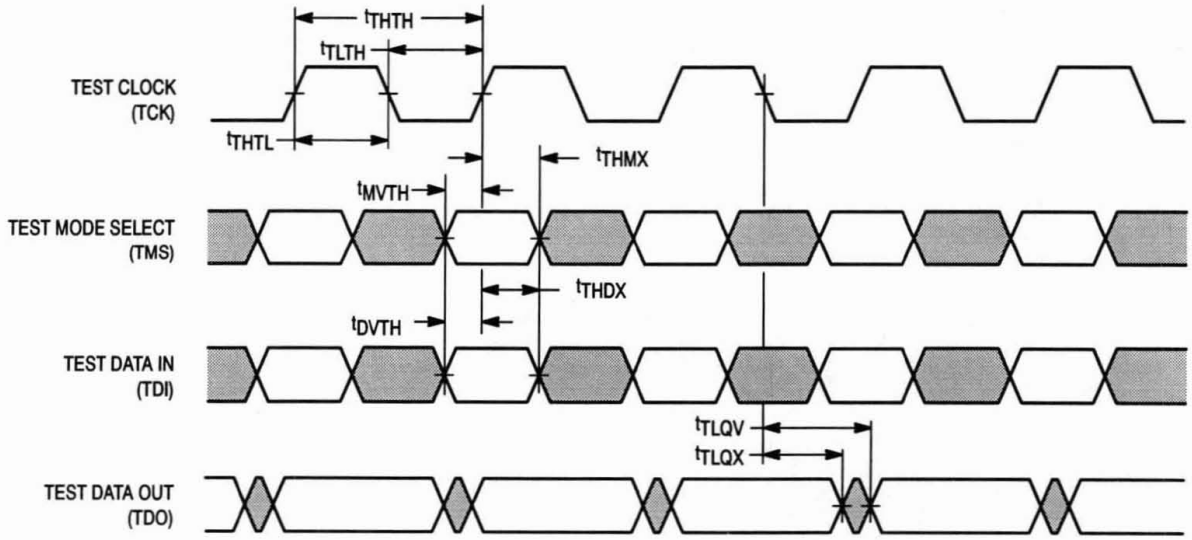
Parameter	Symbol	Min	Max	Unit	Notes
Cycle Time	t_{THTH}	100	—	ns	
Clock High Time	t_{THTL}	40	—	ns	
Clock Low Time	t_{TLTH}	40	—	ns	
TMS Setup	t_{MVTH}	10	—	ns	
TMS Hold	t_{THMX}	10	—	ns	
TDI Valid to TCK High	t_{DVTH}	10	—	ns	
TCK High to TDI Don't Care	t_{THDX}	10	—	ns	
Capture Setup	t_{CS}	10	—	ns	1
Capture Hold	t_{CH}	10	—	ns	1
TCK Low to TDO Unknown	t_{TLQX}	0	—	ns	
TCK Low to TDO Valid	t_{TLOV}	—	20	ns	

NOTE:
1. t_{CS} + t_{CH} defines the minimum pause in RAM I/O pad transitions to ensure accurate pad data capture.

AC TEST LOAD



TAP CONTROLLER TIMING DIAGRAM



TEST ACCESS PORT PINS

TCK — TEST CLOCK (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

TMS — TEST MODE SELECT (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.

TDI — TEST DATA IN (INPUT)

The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (see Figure 6). An undriven TDI pin will produce the same result as a logic one input level.

TDO — TEST DATA OUT (OUTPUT)

Output that is active depending on the state of the TAP state machine (see Figure 6). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

TRST — TAP RESET

This device does not have a TRST pin. TRST is optional in IEEE 1149.1. The test–logic reset state is entered while TMS is held high for five rising edges of TCK. Power on reset circuitry is included internally. This type of reset does not affect the operation of the system logic. The reset affects test logic only.

TEST ACCESS PORT REGISTERS

OVERVIEW

The various TAP registers are selected (one at a time) via the sequences of ones and zeros input to the TMS pin as the TCK is strobed. Each of the TAP registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on the subsequent falling edge of TCK. When a register is selected it is "placed" between the TDI and TDO pins.

INSTRUCTION REGISTER

The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run test/idle or the various data register states. The instructions are three bits long. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power–up or whenever the controller is placed in test–logic–reset state.

BYPASS REGISTER

The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.

BOUNDARY SCAN REGISTER

The boundary scan register is identical in length to the number of active input and I/O connections on the RAM (not counting the TAP pins). This also includes a number of place holder locations (always set to a logic one) reserved for density upgrade address pins. There are a total of 70 bits in the case of the x36 device and 51 bits in the case of the x18 device. The boundary scan register, under the control of the TAP controller, is loaded with the contents of the RAM I/O ring when the controller is in capture–DR state and then is placed between the TDI and TDO pins when the controller is moved to shift–DR state. Several TAP instructions can be used to activate the boundary scan register.

The Bump/Bit Scan Order tables describe which device bump connects to each boundary scan register location. The first column defines the bit's position in the boundary scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the input or I/O at the bump and the third column is the bump number.

IDENTIFICATION (ID) REGISTER

The ID register is a 32–bit register that is loaded with a device and vendor specific 32–bit code when the controller is put in capture–DR state with the IDCODE command loaded in the instruction register. The code is loaded from a 32–bit on–chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into shift–DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Presence Indicator

Bit No.	0
Value	1

Motorola JEDEC ID Code (Compressed Format, per IEEE Standard 1149.1 – 1990)

Bit No.	11	10	9	8	7	6	5	4	3	2	1
Value	0	0	0	0	0	0	0	1	1	1	0

Reserved For Future Use

Bit No.	17	16	15	14	13	12
Value	x	x	x	x	x	x

Device Width

Configuration	Bit No.	22	21	20	19	18
128K x 36	Value	0	0	1	0	0
256K x 18	Value	0	0	0	1	1

Device Depth

Configuration	Bit No.	27	26	25	24	23
128K x 36	Value	0	0	1	0	1
256K x 18	Value	0	0	1	1	0

Revision Number

Bit No.	31	30	29	28
Value	x	x	x	x

Figure 5. ID Register Bit Meanings

MCM69L736 Bump/Bit Scan Order

Bit No.	Signal Name	Bump ID		Bit No.	Signal Name	Bump ID
1	M2	5R		36	SA	3B
2	SA	4P		37	NC	2B
3	SA	4T		38	SA	3A
4	SA	6R		39	SA	3C
5	SA	5T		40	SA	2C
6	NC	7T		41	SA	2A
7	DQa	6P		42	DQc	2D
8	DQa	7P		43	DQc	1D
9	DQa	6N		44	DQc	2E
10	DQa	7N		45	DQc	1E
11	DQa	6M		46	DQc	2F
12	DQa	6L		47	DQc	2G
13	DQa	7L		48	DQc	1G
14	DQa	6K		49	DQc	2H
15	DQa	7K		50	DQc	1H
16	$\overline{SBa}$	5L		51	$\overline{SBc}$	3G
17	$\overline{CK}$	4L		52	ZQ	4D
18	CK	4K		53	$\overline{SS}$	4E
19	$\overline{G}$	4F		54	NC	4G
20	$\overline{SBb}$	5G		55	NC	4H
21	DQb	7H		56	$\overline{SW}$	4M
22	DQb	6H		57	$\overline{SBd}$	3L
23	DQb	7G		58	DQd	1K
24	DQb	6G		59	DQd	2K
25	DQb	6F		60	DQd	1L
26	DQb	7E		61	DQd	2L
27	DQb	6E		62	DQd	2M
28	DQb	7D		63	DQd	1N
29	DQb	6D		64	DQd	2N
30	SA	6A		65	DQd	1P
31	SA	6C		66	DQd	2P
32	SA	5C		67	SA	3T
33	SA	5A		68	SA	2R
34	NC	6B		69	SA	4N
35	SA	5B		70	M1	3R

MCM69L818 Bump/Bit Scan Order

Bit No.	Signal Name	Bump ID		Bit No.	Signal Name	Bump ID
1	M2	5R		36	SBb	3G
2	SA	6T		37	ZQ	4D
3	SA	4P		38	SS	4E
4	SA	6R		39	NC	4G
5	SA	5T		40	NC	4H
6	NC	7T		41	SW	4M
7	DQa	7P		42	DQb	2K
8	DQa	6N		43	DQb	1L
9	DQa	6L		44	DQb	2M
10	DQa	7K		45	DQb	1N
11	$\overline{SBa}$	5L		46	DQb	2P
12	$\overline{CK}$	4L		47	SA	3T
13	CK	4K		48	SA	2R
14	$\overline{G}$	4F		49	SA	4N
15	DQa	6H		50	SA	2T
16	DQa	7G		51	M1	3R
17	DQa	6F				
18	DQa	7E				
19	DQa	6D				
20	SA	6A				
21	SA	6C				
22	SA	5C				
23	SA	5A				
24	NC	6B				
25	SA	5B				
26	SA	3B				
27	NC	2B				
28	SA	3A				
29	SA	3C				
30	SA	2C				
31	SA	2A				
32	DQb	1D				
33	DQb	2E				
34	DQb	2G				
35	DQb	1H				

NOTES:

1. The NC pads listed in this table are indeed no connects, but are represented in the boundary scan register by a "place holder" bit that is forced to logic one. These pads are reserved for use as address inputs on higher density RAMs that follow this pad out and scan order standard.
2. CK and $\overline{CK}$, are sampled individually. $\overline{CK}$ is not simply a forced compliment of the CK input. In scan mode these differential inputs are referenced to V_{ref}, not each other.
3. ZQ, M1, and M2 are not ordinary inputs and may not respond to standard I/O logic levels. ZQ, M1, and M2 must be driven to within 100 mV of a V_{DD} or V_{SS} supply rail to ensure consistent results.

TAP CONTROLLER INSTRUCTION SET

OVERVIEW

There are two classes of instructions defined in IEEE Standard 1149.1–1990, the standard (public) instructions and device specific (private) instructions. Some public instructions are mandatory for IEEE 1149.1 compliance. Optional public instructions must be implemented in prescribed ways.

Although the TAP controller in this device follows the IEEE 1149.1 conventions, it is not IEEE 1194.1 compliant because some of the mandatory instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads, but cannot be used to load address, data, or control signals into the RAM or to preload the I/O buffers. In other words, the device will not perform IEEE 1149.1 EXTEST, INTEST, or the preload portion of the SAMPLE/PRELOAD command.

When the TAP controller is placed in capture–IR state, the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the shift–IR state, the instruction register is placed between TDI and TDO. In this state, the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to update–IR state. The TAP instruction sets for this device are listed in the following tables.

STANDARD (PUBLIC) INSTRUCTIONS

BYPASS

The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift–DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is an IEEE 1149.1 mandatory public instruction. When the SAMPLE/PRELOAD instruction is loaded in the instruction register, moving the TAP controller into the capture–DR state loads the data in the RAM's input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e., in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAP's input data capture set–up plus hold time (t_{CS} plus t_{CH}). The RAM's clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register.

Moving the controller to shift–DR state then places the boundary scan register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the update–DR state with the SAMPLE/PRELOAD instruction loaded in the instruction register has the same effect as the pause–DR command. This functionality is not IEEE 1149.1 compliant.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic zeros. EXTEST is not implemented in this device. Therefore, this device is not IEEE 1149.1 compliant. Nevertheless, this RAM TAP does respond to an all zeros instruction, as follows. With the EXTEST (000) instruction loaded in the instruction register, the RAM responds just as it does in response to the SAMPLE/PRELOAD instruction described above, except the RAM outputs are forced to High–Z any time the instruction is loaded.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture–DR mode and places the ID register between the TDI and TDO pins in shift–DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test–logic–reset state.

DEVICE SPECIFIC (PUBLIC) INSTRUCTION

SAMPLE–Z

If the SAMPLE–Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (High–Z) and the boundary scan register is connected between TDI and TDO when the TAP controller is moved to the shift–DR state.

DEVICE SPECIFIC (PRIVATE) INSTRUCTION

NO OP

Do not use these instructions; they are reserved for future use.

STANDARD (PUBLIC) INSTRUCTION CODES

Instruction	Code*	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM outputs to High–Z state. **NOT IEEE 1149.1 COMPLIANT.**
IDCODE	001**	Preloads ID register and places it between TDI and TDO. Does not affect RAM operation.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect RAM operation. Does not implement IEEE 1149.1 PRELOAD function. **NOT IEEE 1149.1 COMPLIANT.**
BYPASS	111	Places bypass register between TDI and TDO. Does not affect RAM operation.
SAMPLE–Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM output drivers to High–Z state.

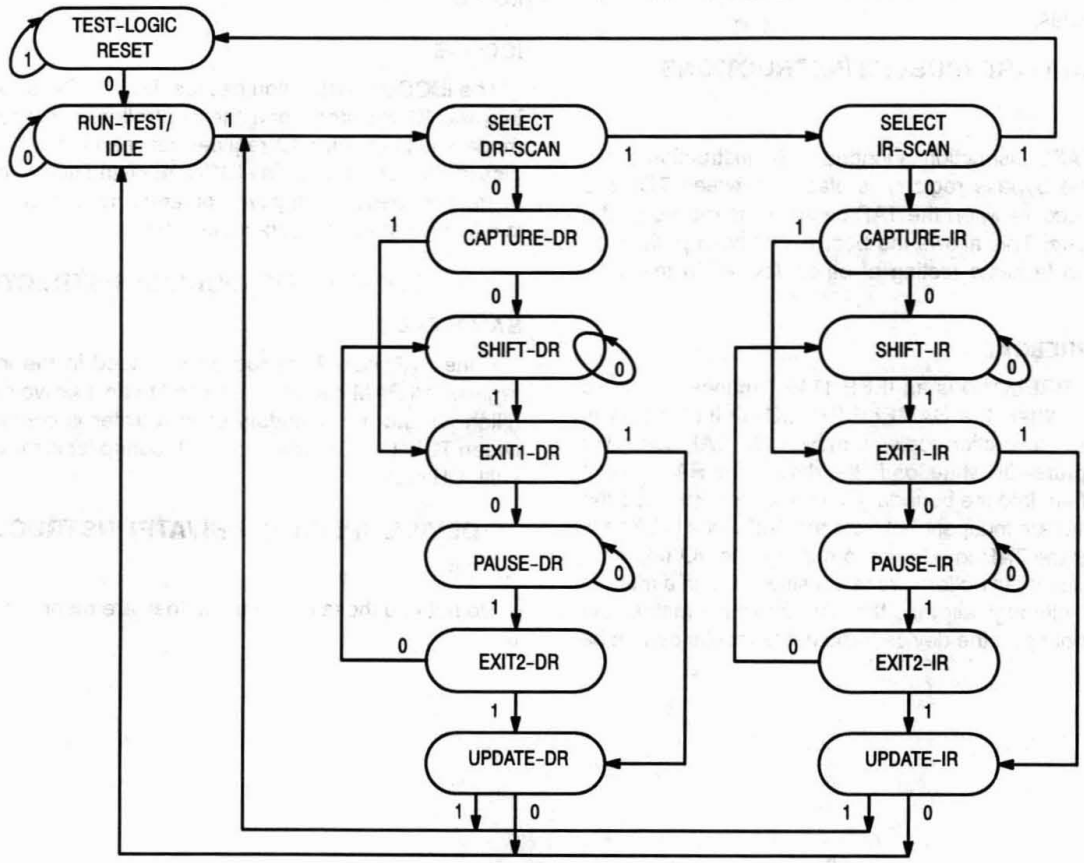
* Instruction codes expressed in binary; MSB on left, LSB on right.
** Default instruction automatically loaded at power–up and in test–logic–reset state.

3

STANDARD (PRIVATE) INSTRUCTION CODES

Instruction	Code*	Description
NO OP	011	Do not use these instructions; they are reserved for future use.
NO OP	101	Do not use these instructions; they are reserved for future use.
NO OP	110	Do not use these instructions; they are reserved for future use.

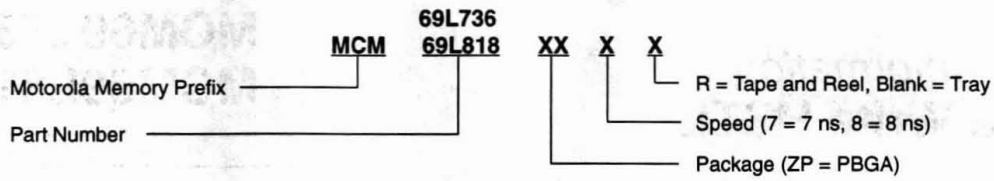
* Instruction codes expressed in binary; MSB on left, LSB on right.



NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 6. TAP Controller State Diagram

ORDERING INFORMATION
(Order by Full Part Number)



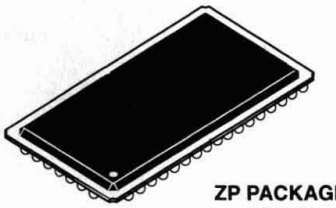
Full Part Numbers —	MCM69L736ZP7	MCM69L736ZP8
	MCM69L818ZP7	MCM69L818ZP8
	MCM69L736ZP7R	MCM69L736ZP8R
	MCM69L818ZP7R	MCM69L818ZP8R

3

MCM69L736A
MCM69L818A

Advance Information

4M Late Write HSTL



ZP PACKAGE
PBGA
CASE 999–01

The MCM69L736A/818A is a 4M synchronous late write fast static RAM designed to provide high performance in secondary cache and ATM switch, Telecom, and other high speed memory applications. The MCM69L818A (organized as 256K words by 18 bits) and the MCM69L736A (organized as 128K words by 36 bits) are fabricated in Motorola's high performance silicon gate BiCMOS technology.

The differential clock (CK) inputs control the timing of read/write operations of the RAM. At the rising edge of CK, all addresses, write enables, and synchronous selects are registered. An internal buffer and special logic enable the memory to accept write data on the rising edge of CK a cycle after address and control signals. Read data is available at the falling edge of CK.

The RAM uses HSTL inputs and outputs. The adjustable input trip–point (V_{ref}) and output voltage (V_{DDQ}) gives the system designer greater flexibility in optimizing system performance.

The synchronous write and byte enables allow writing to individual bytes or the entire word.

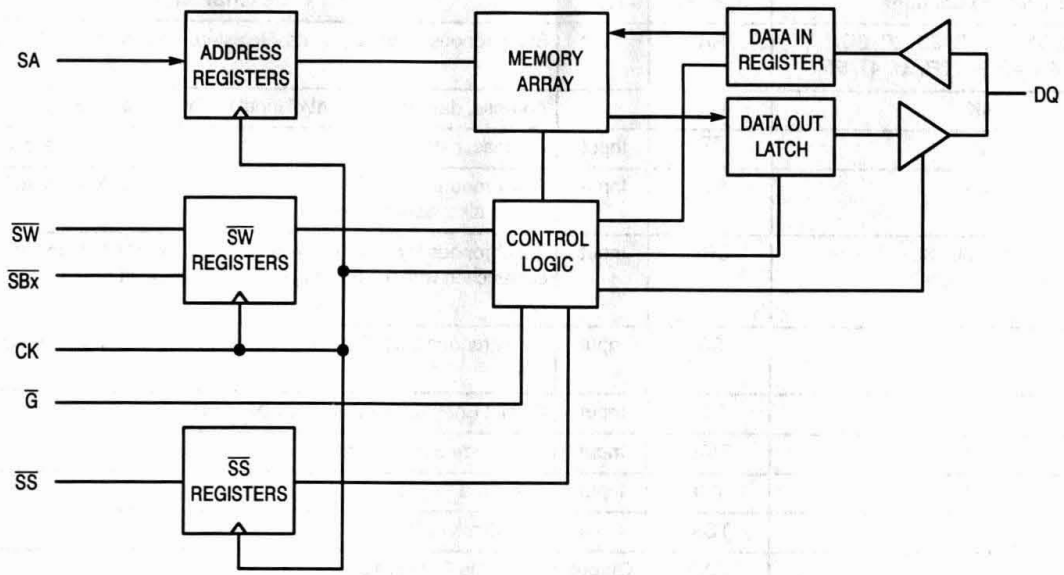
The impedance of the output buffers is programmable, allowing the outputs to match the impedance of the circuit traces which reduces signal reflections.

- Byte Write Control
- Single 3.3 V +10%, – 5% Operation
- HSTL — I/O (JEDEC Standard JESD8–6 Class I)
- HSTL — User Selectable Input Trip–Point
- HSTL — Compatible Programmable Impedance Output Drivers
- Register to Latch Synchronous Operation
- Asynchronous Output Enable
- Boundary Scan (JTAG) IEEE 1149.1 Compatible
- Differential Clock Inputs
- Optional x18 or x36 Organization
- MCM69L736A/818A–7.5 = 7.5 ns
  MCM69L736A/818A–8.5 = 8.5 ns
  MCM69L736A/818A–9.5 = 9.5 ns
  MCM69L736A/818A–10.5 = 10.5 ns
- 119 Bump, 50 mil (1.27 mm) Pitch, 14 mm x 22 mm Plastic Ball Grid Array (PBGA) Package

This document contains information on a new product. Specifications and information herein are subject to change without notice.

4/3/97

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENTS

TOP VIEW

MCM69L736A

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	SA	NC	SA	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQc	DQc	V_{SS}	ZQ	V_{SS}	DQb	DQb
E	DQc	DQc	V_{SS}	$\overline{SS}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{G}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{SBc}$	NC	$\overline{SBb}$	DQb	DQb
H	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	V_{ref}	V_{DD}	V_{ref}	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CK	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{SBd}$	$\overline{CK}$	$\overline{SBa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{SW}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
P	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
R	NC	SA	V_{DD}	V_{DD}	V_{SS}	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69L818A

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	SA	NC	SA	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQb	NC	V_{SS}	ZQ	V_{SS}	DQa	NC
E	NC	DQb	V_{SS}	$\overline{SS}$	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	$\overline{SBb}$	NC	V_{SS}	NC	DQa
H	DQb	NC	V_{SS}	NC	V_{SS}	DQa	NC
J	V_{DDQ}	V_{DD}	V_{ref}	V_{DD}	V_{ref}	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	CK	V_{SS}	NC	DQa
L	DQb	NC	V_{SS}	$\overline{CK}$	$\overline{SBa}$	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{SW}$	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	SA	V_{SS}	DQa	NC
P	NC	DQb	V_{SS}	SA	V_{SS}	NC	DQa
R	NC	SA	V_{DD}	V_{DD}	V_{SS}	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69L736A PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 3T, 4T, 5T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
4K	CK	Input	Address, data in, and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in, and control input register clock. Active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
5L, 5G, 3G, 3L (a), (b), (c), (d)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2U	TMS	Input	Test Mode Select (JTAG).
3U	TDI	Input	Test Data In (JTAG).
4U	TCK	Input	Test Clock (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
4D	ZQ	Input	Programmable Output Impedance: Programming pin.
7T	ZZ	Input	Reserved for future use. Must be grounded.
(a) 6K, 7K, 6L, 7L, 6M, 6N, 7N, 6P, 7P (b) 6D, 7D, 6E, 7E, 6F, 6G, 7G, 6H, 7H (c) 1D, 2D, 1E, 2E, 2F, 1G, 2G, 1H, 2H (d) 1K, 2K, 1L, 2L, 2M, 1N, 2N, 1P, 2P	DQx	I/O	Synchronous Data I/O.
3J, 5J	V_{ref}	Supply	Input Reference: Provides reference voltage for input buffers.
4C, 2J, 4J, 6J, 4R, 3R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: Provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 3H, 5H, 3K, 5K, 3M, 5M, 3N, 5N, 3P, 5P, 5R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 4B, 6B, 7B, 1C, 7C, 4G, 4H, 1R, 7R, 1T, 2T, 6T, 6U	NC	—	No Connection: There is no connection to the chip.

MCM69L818A PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 2T, 3T, 5T, 6T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
4K	CK	Input	Address, data in, and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in, and control input register clock. Active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
5L, 3G (a), (b)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
2U	TMS	Input	Test Mode Select (JTAG).
3U	TDI	Input	Test Data In (JTAG).
4U	TCK	Input	Test Clock (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
4D	ZQ	Input	Programmable Output Impedance: Programming pin.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
7T	ZZ	Input	Reserved for future use. Must be grounded.
(a) 6D, 7E, 6F, 7G, 6H, 7K, 6L, 6N, 7P (b) 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 2P	DQx	I/O	Synchronous Data I/O.
3J, 5J	V_{ref}	Supply	Input Reference: Provides reference voltage for input buffers.
4C, 2J, 4J, 6J, 4R, 3R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: Provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P, 5R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 4B, 6B, 7B, 1C, 7C, 2D, 7D, 1E, 6E, 2F, 1G, 4G, 6G, 2H, 4H, 7H, 1K, 6K, 2L, 7L, 6M, 2N, 7N, 1P, 6P, 1R, 7R, 1T, 4T, 6U	NC	—	No Connection: There is no connection to the chip.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS}, See Note 1)

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Output Supply Voltage	V_{DDQ}	– 0.5 to V_{DD} + 0.5	V
Voltage On Any Pin	V_{in}	– 0.5 to V_{DD} + 0.5	V
Input Current (per I/O)	I_{in}	± 50	mA
Output Current (per I/O)	I_{out}	± 70	mA
Power Dissipation (See Note 2)	P_D	—	W
Operating Temperature	T_A	0 to + 70	°C
Temperature Under Bias	T_{bias}	–10 to + 85	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability will be dependent upon package characteristics and use environment. See enclosed thermal impedance data.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

PBGA PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (Still Air)		$R_{\theta JA}$	53	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Single Layer Board	$R_{\theta JA}$	38	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Four Layer Board	$R_{\theta JA}$	22	°C/W	
Junction to Board (Bottom)		$R_{\theta JB}$	14	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	5	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

($0°C \le T_A \le 70°C$, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (See Notes 1 through 4)

Parameter	Symbol	Min	Typical –7.5	Typical –8.5	Typical –9.5	Typical –10.5	Max	Unit	Notes
Input Reference DC Voltage	V_{ref} (dc)	0.6	—	—	—	—	1.1	V	11
Core Power Supply Voltage	V_{DD}	3.15	—	—	—	—	3.6	V	
Output Driver Supply Voltage	V_{DDQ}	1.4	—	—	—	—	1.6	V	
Active Power Supply Current (x18) (x36)	I_{DD1}	— —	300 390	290 380	270 360	260 350	450 560	mA	5
Quiescent Active Power Supply Current)	I_{DD2}	—	190	190	190	190	250	mA	6, 10
Active Standby Power Supply Current	I_{SB1}	—	160	160	160	160	250	mA	7
Quiescent Standby Power Supply Current	I_{SB2}	—	140	140	140	140	230	mA	8, 10
Sleep Mode Power Supply Current	I_{SB3}	—	TBD	TBD	TBD	TBD	TBD	mA	9, 10

NOTES:

1. All data sheet parameters specified to full range of V_{DD} unless otherwise noted. All voltages are referenced to voltage applied to V_{SS} bumps.
2. Supply voltage applied to V_{DD} connections.
3. Supply voltage applied to V_{DDQ} connections.
4. All power supply currents measured with outputs open or deselected.
5. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered active, 50% read cycles.
6. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered active.
7. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered inactive.
8. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered inactive, ZZ low.
9. $V_{DD} = V_{DD}$ (Max), t_{KHKH} = dc, registered inactive, ZZ high.
10. $200 \text{ mV} \ge V_{in} \ge V_{DDQ} - 200 \text{ mV}$.
11. Although considerable latitude in the selection of the nominal dc value (i.e., rms value) of V_{ref} is supported, the peak to peak ac component superimposed on V_{ref} may not exceed 5% of the dc component of V_{ref}.

DC INPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
DC Input Logic High	V_{IH} (dc)	$V_{ref} + 0.1$	$V_{DD} + 0.3$	V	
DC Input Logic Low	V_{IL} (dc)	– 0.3	$V_{ref} - 0.1$	V	1
Input Reference DC Voltage	V_{ref} (dc)	0.6	1.1	V	2
Input Leakage Current	$I_{lkg(1)}$	—	± 5	µA	3
Clock Input Signal Voltage	V_{in}	– 0.3	$V_{DD} + 0.3$	V	
Clock Input Differential Voltage	V_{DIF} (dc)	0.1	$V_{DD} + 0.6$	V	4
Clock Input Common Mode Voltage Range (See Figure 3)	V_{CM} (dc)	0.68	1.1	V	5
Clock Input Crossing Point Voltage Range	V_X	0.68	1.1	V	

NOTES:

1. Inputs may undershoot to – 0.5 V (peak) for up to 20% t_{KHKH} (e.g., 2 ns at a clock cycle time of 10 ns).
2. Although considerable latitude in the selection of the nominal dc value (i.e., rms value) of V_{ref} is supported, the peak–to–peak ac component superimposed on V_{ref} may not exceed 5% of the dc component of V_{ref}.
3. $0 \text{ V} \le V_{in} \le V_{DDQ}$ for all pins.
4. Minimum instantaneous differential input voltage required for differential input clock operation.
5. Maximum rejectable common mode input voltage variation.

DC OUTPUT BUFFER CHARACTERISTICS – PROGRAMMABLE IMPEDANCE PUSH–PULL OUTPUT BUFFER MODE

($0°C \le T_A \le 70°C$, Unless Otherwise Noted, See Notes 5 and 6)

Parameter	Symbol	Min	Max	Unit	Notes
Output Logic Low	V_{OL}	$V_{DDQ}/2 - 0.025$	$V_{DDQ}/2 + 0.025$	V	1
Output Logic High	V_{OH}	$V_{DDQ}/2 - 0.025$	$V_{DDQ}/2 + 0.025$	V	2
Light Load Output Logic Low	$V_{OL}1$	V_{SS}	0.2	V	3
Light Load Output Logic High	$V_{OH}1$	$V_{DDQ} - 0.2$	V_{DDQ}	V	4

NOTES:
1. $I_{OL} = (V_{DDQ}/2)/(RQ/5)$ for values of $RQ = 175\ \Omega \le RQ \le 350\ \Omega$.
2. $|I_{OH}| = (V_{DDQ}/2)/(RQ/5)$ for values of $RQ = 175\ \Omega \le RQ \le 350\ \Omega$.
3. $I_{OL} \le 100\ \mu A$.
4. $|I_{OH}| \le 100\ \mu A$.
5. The impedance controlled mode is expected to be used in point–to–point applications, driving high impedance inputs.
6. The ZQ pin is connected through RQ to V_{SS} for the controlled impedance mode.

3

DC OUTPUT BUFFER CHARACTERISTICS — MINIMUM IMPEDANCE PUSH–PULL OUTPUT BUFFER MODE

($0°C \le T_A \le 70°C$, $ZQ = V_{DD}$) (See Notes 1 and 2)

Parameter	Symbol	Min	Max	Unit	Notes
Output Logic Low	$V_{OL}2$	V_{SS}	0.4	V	3
Output Logic High	$V_{OH}2$	$V_{DDQ} - 0.4$	V_{DDQ}	V	4
Light Load Output Logic Low	$V_{OL}3$	V_{SS}	0.2	V	5
Light Load Output Logic High	$V_{OH}3$	$V_{DDQ} - 0.2$	V_{DDQ}	V	6

NOTES:
1. The push–pull output mode is expected to be used in bussed applications and may be series or parallel terminated. Conforms to the JEDEC Standard JESD8–6 Class I.
2. The ZQ pin is connected to V_{DD} to enable the minimum impedance mode.
3. $I_{OL} \le 8$ mA.
4. $|I_{OH}| \le 8$ mA.
5. $I_{OL} \le 100\ \mu A$.
6. $|I_{OH}| \le 100\ \mu A$.

CAPACITANCE ($f = 1.0$ MHz, $dV = 3.0$ V, $0°C \le T_A \le 70°C$, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	5	pF
Input/Output Capacitance	$C_{I/O}$	7	8	pF
CK, $\overline{CK}$ Capacitance	C_{CK}	4	5	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0.25 to 1.25 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 0.75 V
Output Timing Reference Level ..... 0.75 V
Clock Input Timing Reference Level ..... Differential Cross–Point
RQ for 50 Ω Impedance ..... 250 Ω

READ/WRITE CYCLE TIMING (See Note 3)

Parameter	Symbol	MCM69L736A–7.5 MCM69L818A–7.5		MCM69L736A–8.5 MCM69L818A–8.5		MCM69L736A–9.5 MCM69L818A–9.5		MCM69L736A–10.5 MCM69L818A–10.5		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	7	—	8	—	9	—	10	—	ns	
Clock High Pulse Width	t_{KHKL}	2.8	—	3.2	—	3.6	—	4	—	ns	
Clock Low Pulse Width	t_{KLKH}	2.8	—	3.2	—	3.6	—	4	—	ns	
Clock High to Output Valid	t_{KHQV}	—	7.5	—	8.5	—	9.5	—	10.5	ns	2
Clock Low to Output Valid	t_{KLQV}	—	3.5	—	4	—	4	—	4	ns	2
Clock Low to Output Hold	t_{KLQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	2
Clock Low to Output Low–Z	t_{KLQX1}	1	—	1	—	1	—	1	—	ns	3
Clock High to Output High–Z	t_{KHQZ}	—	3.5	—	4	—	4	—	4	ns	3
Output Enable Low to Output Low–Z	t_{GLQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	3
Output Enable Low to Output Valid	t_{GLQV}	—	3.5	—	4	—	4	—	4	ns	2
Output Enable to Output Hold	t_{GHQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	2
Output Enable High to Output High–Z	t_{GHQZ}	—	3.5	—	4	—	4	—	4	ns	3
Setup Times: Address, Data In, Chip Select, Write Enable	t_{AVKH} t_{DVKH} t_{SVKH} t_{WVKH}	0.5	—	0.5	—	0.5	—	0.5	—	ns	
Hold Times: Address, Data In, Chip Select, Write Enable	t_{KHAX} t_{KHDX} t_{KHSX} t_{KHWX}	1	—	1	—	1	—	1	—	ns	

NOTES:
1. Measured at ± 200 mV from steady state.
2. In no case may control input signals (e.g., $\overline{SS}$) be operated with pulse widths less than the minimum clock input pulse width specifications (e.g., t_{KHKL}) or at frequencies that exceed the applied K clock frequency.
3. Tested per AC Test Load diagram. See Figure 1.

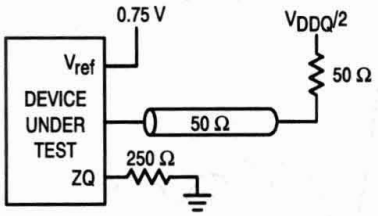


Figure 1. AC Test Load

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

AC INPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Notes
AC Input Logic High (See Figure 4)	V_{IH} (ac)	V_{ref} + 200 mV		
AC Input Logic Low (See Figures 2 and 4)	V_{IL} (ac)		V_{ref} – 200 mV	1
Input Reference Peak to Peak ac Voltage	V_{ref} (ac)		5% V_{ref} (dc)	2
Clock Input Differential Voltage	V_{dif} (ac)	400 mV	V_{DDQ} + 600 mV	3

NOTES:
1. Inputs may undershoot to – 0.5 V (peak) for up to 20% t_{KHKH} (e.g., 2 ns at a clock cycle time of 10 ns).
2. Although considerable latitude in the selection of the nominal dc value (i.e., rms value) of V_{ref} is supported, the peak to peak ac component superimposed on V_{ref} may not exceed 5% of the dc component of V_{ref}.
3. Minimum instantaneous differential input voltage required for differential input clock operation.

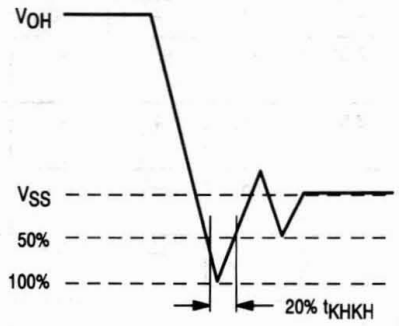
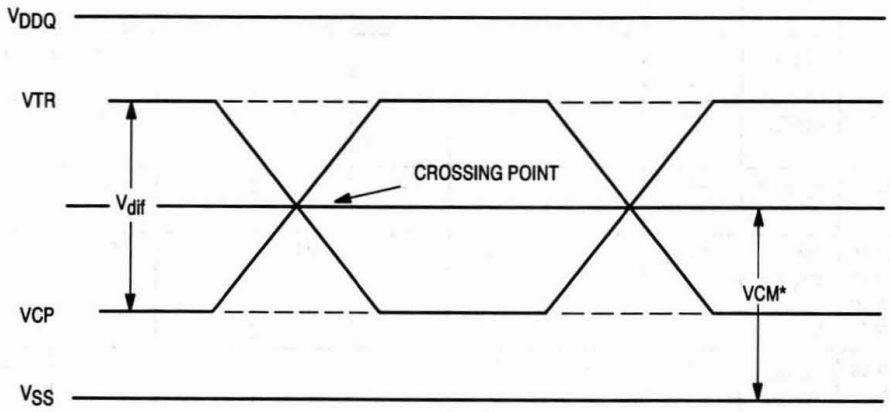


Figure 2. Undershoot Voltage



* VCM, the common mode input voltage, equals VTR – [(VTR – VCP)/2].

Figure 3. Differential Inputs/Common Mode Input Voltage

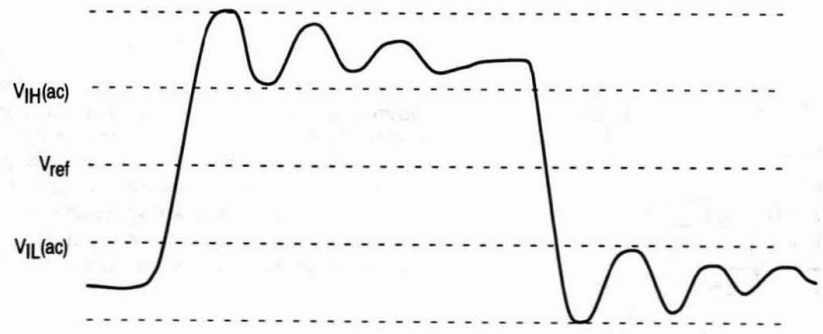
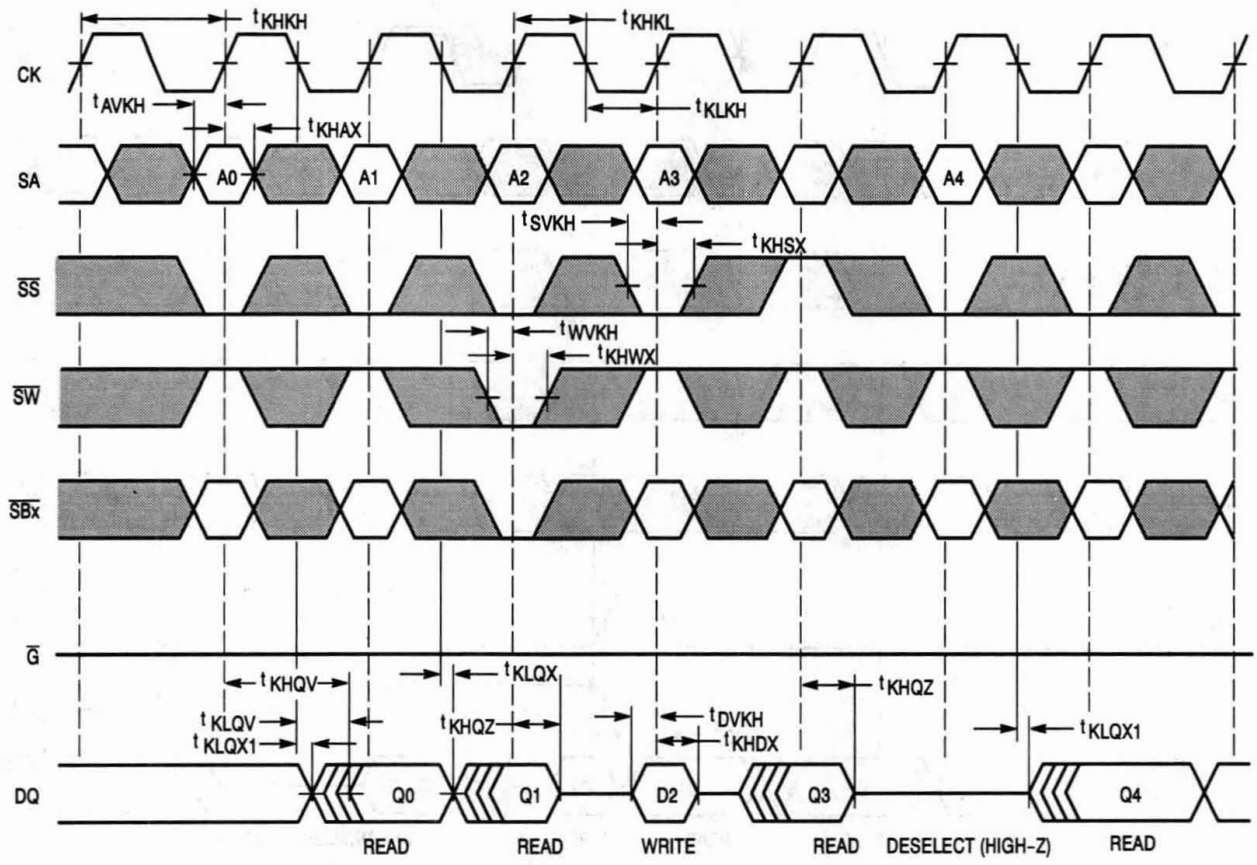
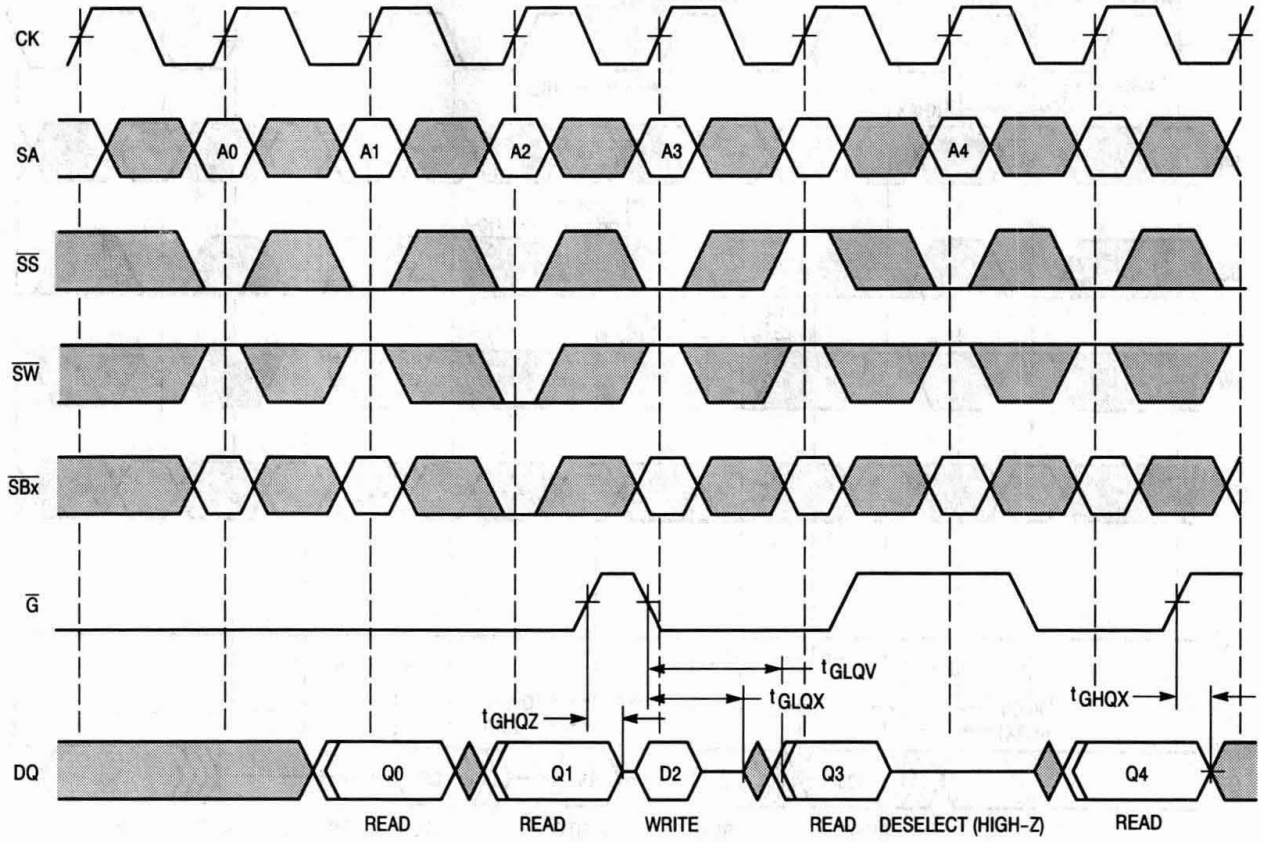


Figure 4. Differential Inputs/Common Mode Input Voltage

REGISTER LATCH READ–WRITE–READ CYCLES



REGISTER LATCH READ–WRITE–READ CYCLES
($\overline{G}$ Controlled)



FUNCTIONAL OPERATION

READ AND WRITE OPERATIONS

All control signals except $\overline{G}$ are registered on the rising edge of CK. These signals must meet the setup and hold times shown in the AC Characteristics table. On the falling edge of the current cycle, the output latch becomes transparent and data is available. The output data is latched on the rising edge of the next clock. The output data is available at the output at t_{KLQV} or t_{KHQV}, whichever is later. t_{KHQV} is the internal latency of the device. During this same cycle, a new read address can be applied to the address pins.

A write cycle can occur on the next cycle as long as t_{KLQX} and t_{DVKH} are met. Read cycles may follow write cycles immediately.

$\overline{G}$, $\overline{SS}$, and $\overline{SW}$ control output drive. Chip deselect via a high on $\overline{SS}$ at the rising edge of CK has its effect on the output drivers immediately. $\overline{SW}$ low deselects the output drivers immediately (on the same cycle). Output selecting via a low on $\overline{SS}$ and high on $\overline{SW}$ at a rising CK has its effect on the output drivers at t_{KLQX}. Output drive is also controlled directly by output enable ($\overline{G}$). $\overline{G}$ is an asynchronous input. No clock edges are required to enable or disable the output with $\overline{G}$.

Output data will be valid at t_{GLQV}, t_{KHQV}, or t_{KLQV}, which is even later. Outputs will begin driving at t_{KLQX1}. Outputs will hold previous data until t_{KLQX} or t_{GHQX}.

WRITE AND BYTE WRITE FUNCTIONS

Note that in the following discussion the term "byte" refers to nine bits of the RAM I/O bus. In all cases, the timing parameters described for synchronous write input ($\overline{SW}$) apply to each of the byte write enable inputs ($\overline{SBa}$, $\overline{SBb}$, etc.).

Byte write enable inputs have no effect on read cycles. This allows the system designer not interested in performing byte writes to connect the byte enable inputs to active low (V_{SS}). Reads of all bytes proceed normally and write cycles, activated via a low on $\overline{SW}$ and the rising edge of CK, write the entire RAM I/O width. This way the designer is spared having to drive multiple write input buffer loads.

Byte writes are performed using the byte write enable inputs in conjunction with the synchronous write input ($\overline{SW}$). It is important to note that writing any one byte will inhibit a read of all bytes at the current address. The RAM cannot simultaneously read one byte and write another at the same address. A write cycle initiated with none of the byte write enable inputs active is neither a read or a write. No write will occur, but the outputs will be deselected as in a normal write cycle.

LATE WRITE

The write address is sampled on the first rising edge of clock, and write data is sampled on the following rising edge.

The late write feature is implemented with single stage write buffering. Write buffering is transparent to the user. A comparator monitors the address bus and, when necessary, routes buffer contents to the outputs to ensure coherent operation. This occurs in all cases whether there is a byte write or a full word is written.

PROGRAMMABLE IMPEDANCE OPERATION

The designer can program the RAMs output buffer impedance by terminating the $\overline{ZQ}$ pin to V_{SS} through a precision resistor (RQ). The value of RQ is five times the output impedance desired. For example, 250 Ω resistor will give an output impedance of 50 Ω.

Impedance updates occur continuously and the frequency of the update is based on the subdivided K clock. Note that if the K clock stops so does the impedance update.

The actual change in the impedance occurs in small increments and is monotonic. There are no significant disturbances that occur on the output because of this smooth update method.

The impedance update is not related to any particular type of cycle because the impedance is updated continuously and is based on the K clock. Updates occur regardless of whether the the device is performing a read, write or a deselect cycle and does not depend on the state of $\overline{G}$.

At power up, the output impedance defaults to approximately 50 ohms. It will take 4,000 to 16,000 cycles for the impedance to be completely updated if the programmed impedance is much higher or lower than 50 Ω.

The output buffers can also be programmed in a minimum impedance configuration by connecting ZQ to V_{DD}.

POWER UP AND INITIALIZATION

Once supplies have reached specification levels, a minimum dwell of 1.0 µs with CK inputs cycling is required before beginning normal operations. At power up the output impedance will be set at approximately 50 Ω, however, in order to match the programmed impedance the part requires deselect cycles to occur.

SERIAL BOUNDARY SCAN TEST ACCESS PORT OPERATION

OVERVIEW

The serial boundary scan test access port (TAP) on this RAM is designed to operate in a manner consistent with IEEE 1149.1–1990 (commonly referred to as JTAG), but does not implement all of the functions required for 1149.1 compliance. Certain functions have been modified or eliminated because their implementation places extra delays in the RAMs critical speed path. Nevertheless, the RAM supports the standard TAP controller architecture. The TAP controller is the state machine that controls the TAP operation and can be expected to function in a manner that does not conflict with the operation of devices with IEEE 1149.1 compliant TAPs. The TAP operates using conventional JEDEC Standard 8–1B low voltage (3.3 V) TTL/CMOS logic level signaling.

DISABLING THE TEST ACCESS PORT

It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid–level inputs. TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic one, and may be left unconnected. But they may also be tied to V_{DD} through a 1 k resistor. TDO should be left unconnected.

TAP DC OPERATING CHARACTERISTICS

($0°C \le T_A \le 70°C$, Unless Otherwise Noted)

Parameter	Symbol	Min	Max	Unit	Notes
Logic Input Logic High	$V_{IH}1$	2.0	V_{DD} + 0.3	V	
Logic Input Logic Low	$V_{IL}1$	– 0.3	0.8	V	
Logic Input Leakage Current	I_{lkg}	—	± 5	µA	1
CMOS Output Logic Low	$V_{OL}1$	—	0.2	V	2
CMOS Output Logic High	$V_{OH}1$	V_{DD} – 0.2	—	V	3
TTL Output Logic Low	$V_{OL}2$	—	0.4	V	4
TTL Output Logic High	$V_{OH}2$	2.4	—	V	5

NOTES:
1. $0 V \pm V_{in} \pm V_{DDQ}$ for all logic input pins.
2. $I_{OL}1 \le 100$ µA @ $V_{OL} = 0.2$ V. Sampled, not 100% tested.
3. $|I_{OH}1| \le 100$ µA @ $V_{DDQ} - 0.2$ V. Sampled, not 100% tested.
4. $I_{OL}2 \le 8$ mA @ $V_{OL} = 0.4$ V.
5. $|I_{OH}2| \le 8$ mA @ $V_{OH} = 2.4$ V.

TAP AC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V

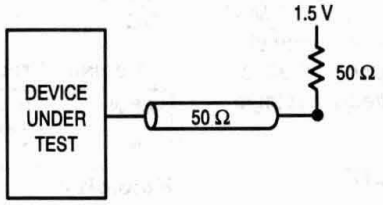
Output Test Load ..... 50 Ω Parallel Terminated T–line with 20 pF Receiver Input Capacitance
Test Load Termination Supply Voltage (V_T) ..... 1.5 V

TAP CONTROLLER TIMING

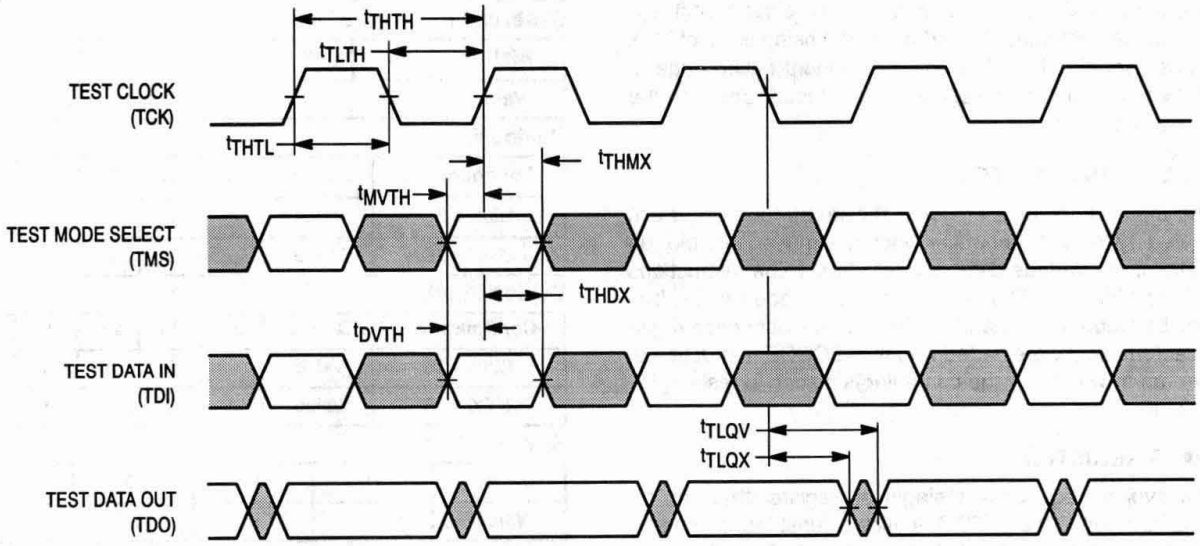
Parameter	Symbol	Min	Max	Unit	Notes
Cycle Time	t_{THTH}	100	—	ns	
Clock High Time	t_{THTL}	40	—	ns	
Clock Low Time	t_{TLTH}	40	—	ns	
TMS Setup	t_{MVTH}	10	—	ns	
TMS Hold	t_{THMX}	10	—	ns	
TDI Valid to TCK High	t_{DVTH}	10	—	ns	
TCK High to TDI Don't Care	t_{THDX}	10	—	ns	
Capture Setup	t_{CS}	10	—	ns	1
Capture Hold	t_{CH}	10	—	ns	1
TCK Low to TDO Unknown	t_{TLQX}	0	—	ns	
TCK Low to TDO Valid	t_{TLOV}	—	20	ns	

NOTE:
1. t_{CS} + t_{CH} defines the minimum pause in RAM I/O pad transitions to ensure accurate pad data capture.

AC TEST LOAD



TAP CONTROLLER TIMING DIAGRAM



TEST ACCESS PORT PINS

TCK — TEST CLOCK (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

TMS — TEST MODE SELECT (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.

TDI — TEST DATA IN (INPUT)

The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (see Figure 6). An undriven TDI pin will produce the same result as a logic one input level.

TDO — TEST DATA OUT (OUTPUT)

Output that is active depending on the state of the TAP state machine (see Figure 6). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

TRST — TAP RESET

This device does not have a TRST pin. TRST is optional in IEEE 1149.1. The test–logic reset state is entered while TMS is held high for five rising edges of TCK. Power on reset circuitry is included internally. This type of reset does not affect the operation of the system logic. The reset affects test logic only.

TEST ACCESS PORT REGISTERS

OVERVIEW

The various TAP registers are selected (one at a time) via the sequences of ones and zeros input to the TMS pin as the TCK is strobed. Each of the TAP registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on the subsequent falling edge of TCK. When a register is selected it is "placed" between the TDI and TDO pins.

INSTRUCTION REGISTER

The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run test/idle or the various data register states. The instructions are three bits long. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power–up or whenever the controller is placed in test–logic–reset state.

BYPASS REGISTER

The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.

BOUNDARY SCAN REGISTER

The boundary scan register is identical in length to the number of active input and I/O connections on the RAM (not counting the TAP pins). This also includes a number of place holder locations (always set to a logic one) reserved for density upgrade address pins. There are a total of 70 bits in the case of the x36 device and 51 bits in the case of the x18 device. The boundary scan register, under the control of the TAP controller, is loaded with the contents of the RAM I/O ring when the controller is in capture–DR state and then is placed between the TDI and TDO pins when the controller is moved to shift–DR state. Several TAP instructions can be used to activate the boundary scan register.

The Bump/Bit Scan Order tables describe which device bump connects to each boundary scan register location. The first column defines the bit's position in the boundary scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the input or I/O at the bump and the third column is the bump number.

IDENTIFICATION (ID) REGISTER

The ID register is a 32–bit register that is loaded with a device and vendor specific 32–bit code when the controller is put in capture–DR state with the IDCODE command loaded in the instruction register. The code is loaded from a 32–bit on–chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into shift–DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Presence Indicator

Bit No.	0
Value	1

Motorola JEDEC ID Code (Compressed Format, per IEEE Standard 1149.1 – 1990)

Bit No.	11	10	9	8	7	6	5	4	3	2	1
Value	0	0	0	0	0	0	0	1	1	1	0

Reserved For Future Use

Bit No.	17	16	15	14	13	12
Value	x	x	x	x	x	x

Device Width

Configuration	Bit No.	22	21	20	19	18
128K x 36	Value	0	0	1	0	0
256K x 18	Value	0	0	0	1	1

Device Depth

Configuration	Bit No.	27	26	25	24	23
128K x 36	Value	0	0	1	0	1
256K x 18	Value	0	0	1	1	0

Revision Number

Bit No.	31	30	29	28
Value	x	x	x	x

Figure 5. ID Register Bit Meanings

MCM69L736A Bump/Bit Scan Order

Bit No.	Signal Name	Bump ID		Bit No.	Signal Name	Bump ID
1	M2	5R		36	SA	3B
2	SA	4P		37	NC	2B
3	SA	4T		38	SA	3A
4	SA	6R		39	SA	3C
5	SA	5T		40	SA	2C
6	ZZ	7T		41	SA	2A
7	DQa	6P		42	DQc	2D
8	DQa	7P		43	DQc	1D
9	DQa	6N		44	DQc	2E
10	DQa	7N		45	DQc	1E
11	DQa	6M		46	DQc	2F
12	DQa	6L		47	DQc	2G
13	DQa	7L		48	DQc	1G
14	DQa	6K		49	DQc	2H
15	DQa	7K		50	DQc	1H
16	$\overline{SBa}$	5L		51	$\overline{SBc}$	3G
17	$\overline{CK}$	4L		52	ZQ	4D
18	CK	4K		53	$\overline{SS}$	4E
19	$\overline{G}$	4F		54	NC	4G
20	$\overline{SBb}$	5G		55	NC	4H
21	DQb	7H		56	$\overline{SW}$	4M
22	DQb	6H		57	$\overline{SBd}$	3L
23	DQb	7G		58	DQd	1K
24	DQb	6G		59	DQd	2K
25	DQb	6F		60	DQd	1L
26	DQb	7E		61	DQd	2L
27	DQb	6E		62	DQd	2M
28	DQb	7D		63	DQd	1N
29	DQb	6D		64	DQd	2N
30	SA	6A		65	DQd	1P
31	SA	6C		66	DQd	2P
32	SA	5C		67	SA	3T
33	SA	5A		68	SA	2R
34	NC	6B		69	SA	4N
35	SA	5B		70	M1	3R

MCM69L818A Bump/Bit Scan Order

Bit No.	Signal Name	Bump ID		Bit No.	Signal Name	Bump ID
1	M2	5R		36	SBb	3G
2	SA	6T		37	ZQ	4D
3	SA	4P		38	SS	4E
4	SA	6R		39	NC	4G
5	SA	5T		40	NC	4H
6	ZZ	7T		41	SW	4M
7	DQa	7P		42	DQb	2K
8	DQa	6N		43	DQb	1L
9	DQa	6L		44	DQb	2M
10	DQa	7K		45	DQb	1N
11	$\overline{SBa}$	5L		46	DQb	2P
12	$\overline{CK}$	4L		47	SA	3T
13	CK	4K		48	SA	2R
14	$\overline{G}$	4F		49	SA	4N
15	DQa	6H		50	SA	2T
16	DQa	7G		51	M1	3R
17	DQa	6F				
18	DQa	7E				
19	DQa	6D				
20	SA	6A				
21	SA	6C				
22	SA	5C				
23	SA	5A				
24	NC	6B				
25	SA	5B				
26	SA	3B				
27	NC	2B				
28	SA	3A				
29	SA	3C				
30	SA	2C				
31	SA	2A				
32	DQb	1D				
33	DQb	2E				
34	DQb	2G				
35	DQb	1H				

NOTES:

1. The NC pads listed in this table are indeed no connects, but are represented in the boundary scan register by a "place holder" bit that is forced to logic one. These pads are reserved for use as address inputs on higher density RAMs that follow this pad out and scan order standard.
2. CK and $\overline{CK}$, are sampled individually. $\overline{CK}$ is not simply a forced complement of the CK input. In scan mode these differential inputs are referenced to V_{ref}, not each other.
3. ZQ, M1, and M2 are not ordinary inputs and may not respond to standard I/O logic levels. ZQ, M1, and M2 must be driven to within 100 mV of a V_{DD} or V_{SS} supply rail to ensure consistent results.
4. ZZ must remain at V_{IL} during boundary scan to ensure consistent results.

TAP CONTROLLER INSTRUCTION SET

OVERVIEW

There are two classes of instructions defined in IEEE Standard 1149.1–1990, the standard (public) instructions and device specific (private) instructions. Some public instructions are mandatory for IEEE 1149.1 compliance. Optional public instructions must be implemented in prescribed ways.

Although the TAP controller in this device follows the IEEE 1149.1 conventions, it is not IEEE 1194.1 compliant because some of the mandatory instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads, but cannot be used to load address, data, or control signals into the RAM or to preload the I/O buffers. In other words, the device will not perform IEEE 1149.1 EXTEST, INTEST, or the preload portion of the SAMPLE/PRELOAD command.

When the TAP controller is placed in capture–IR state, the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the shift–IR state, the instruction register is placed between TDI and TDO. In this state, the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to update–IR state. The TAP instruction sets for this device are listed in the following tables.

STANDARD (PUBLIC) INSTRUCTIONS

BYPASS

The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift–DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is an IEEE 1149.1 mandatory public instruction. When the SAMPLE/PRELOAD instruction is loaded in the instruction register, moving the TAP controller into the capture–DR state loads the data in the RAM's input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e., in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAP's input data capture set–up plus hold time (t_{CS} plus t_{CH}). The RAM's clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register.

Moving the controller to shift–DR state then places the boundary scan register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the update–DR state with the SAMPLE/PRELOAD instruction loaded in the instruction register has the same effect as the pause–DR command. This functionality is not IEEE 1149.1 compliant.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic zeros. EXTEST is not implemented in this device. Therefore, this device is not IEEE 1149.1 compliant. Nevertheless, this RAM TAP does respond to an all zeros instruction, as follows. With the EXTEST (000) instruction loaded in the instruction register, the RAM responds just as it does in response to the SAMPLE/PRELOAD instruction described above, except the RAM outputs are forced to High–Z any time the instruction is loaded.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture–DR mode and places the ID register between the TDI and TDO pins in shift–DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test–logic–reset state.

DEVICE SPECIFIC (PUBLIC) INSTRUCTION

SAMPLE–Z

If the SAMPLE–Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (High–Z) and the boundary scan register is connected between TDI and TDO when the TAP controller is moved to the shift–DR state.

DEVICE SPECIFIC (PRIVATE) INSTRUCTION

NO OP

Do not use these instructions; they are reserved for future use.

STANDARD (PUBLIC) INSTRUCTION CODES

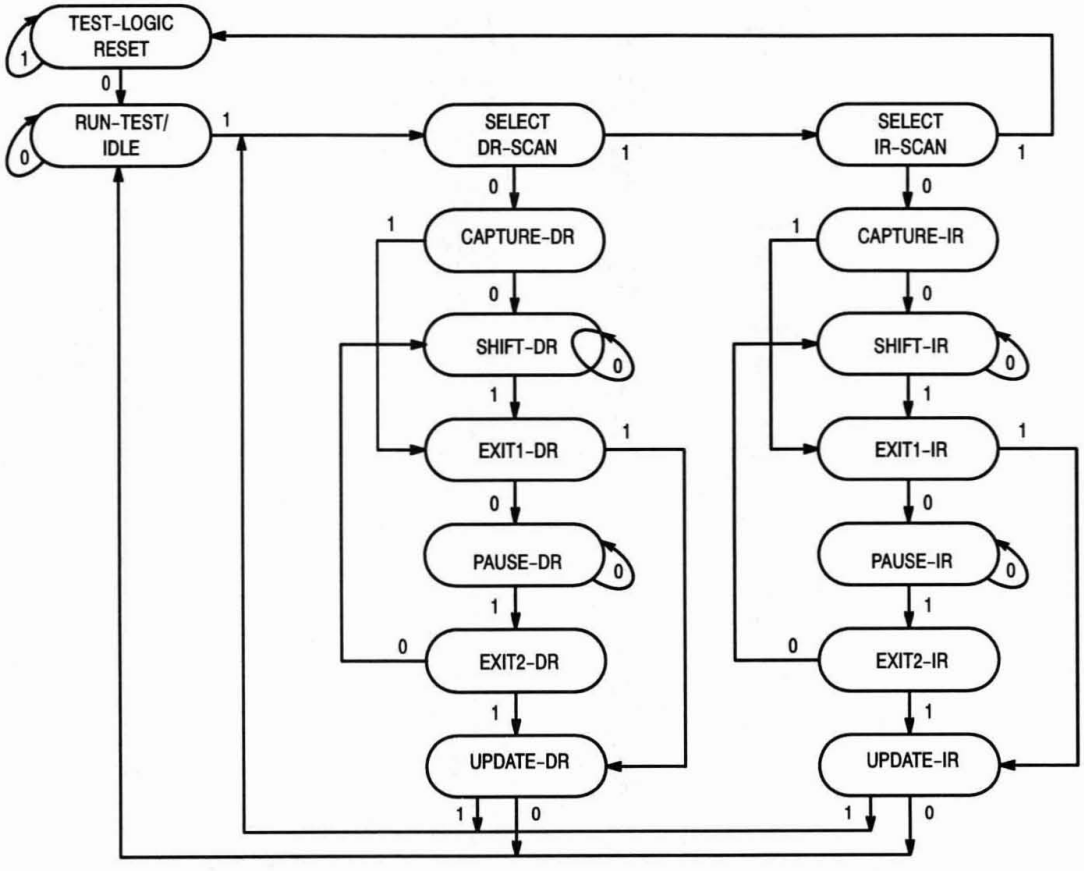
Instruction	Code*	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM outputs to High–Z state. **NOT IEEE 1149.1 COMPLIANT.**
IDCODE	001**	Preloads ID register and places it between TDI and TDO. Does not affect RAM operation.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect RAM operation. Does not implement IEEE 1149.1 PRELOAD function. **NOT IEEE 1149.1 COMPLIANT.**
BYPASS	111	Places bypass register between TDI and TDO. Does not affect RAM operation.
SAMPLE–Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM output drivers to High–Z state.

* Instruction codes expressed in binary; MSB on left, LSB on right.
** Default instruction automatically loaded at power–up and in test–logic–reset state.

STANDARD (PRIVATE) INSTRUCTION CODES

Instruction	Code*	Description
NO OP	011	Do not use these instructions; they are reserved for future use.
NO OP	101	Do not use these instructions; they are reserved for future use.
NO OP	110	Do not use these instructions; they are reserved for future use.

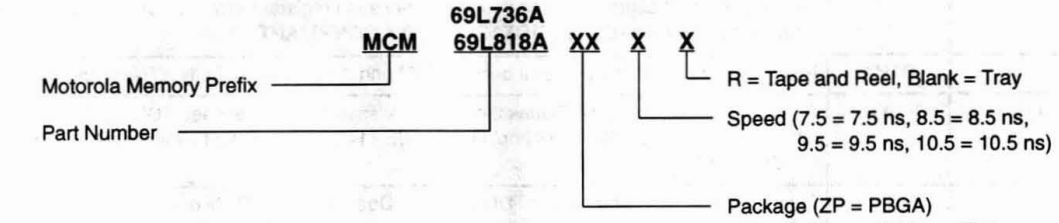
* Instruction codes expressed in binary; MSB on left, LSB on right.



NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 6. TAP Controller State Diagram

ORDERING INFORMATION
(Order by Full Part Number)


69L736A
MCM 69L818A XX X X
Motorola Memory Prefix
Part Number
R = Tape and Reel, Blank = Tray
Speed (7.5 = 7.5 ns, 8.5 = 8.5 ns,
9.5 = 9.5 ns, 10.5 = 10.5 ns)
Package (ZP = PBGA)

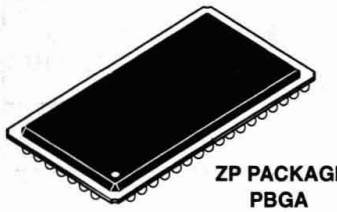
Full Part Numbers —	MCM69L736AZP7.5	MCM69L736AZP8.5	MCM69L736AZP9.5	MCM69L736AZP10.5
	MCM69L818AZP7.5	MCM69L818AZP8.5	MCM69L818AZP9.5	MCM69L818AZP10.5
	MCM69L736AZP7.5R	MCM69L736AZP8.5R	MCM69L736AZP9.5R	MCM69L736AZP10.5R
	MCM69L818AZP7.5R	MCM69L818AZP8.5R	MCM69L818AZP9.5R	MCM69L818AZP10.5R

3

MCM69L737
MCM69L819

Advance Information

4M Late Write LVTTL



ZP PACKAGE
PBGA
CASE 999–01

The MCM69L737/819 is a 4 megabit synchronous late write fast static RAM designed to provide high performance in secondary cache and ATM switch, Telecom, and other high speed memory applications. The MCM69L819 organized as 256K words by 18 bits, and the MCM69L737 organized as 128K words by 36 bits wide are fabricated in Motorola's high performance silicon gate BiCMOS technology.

The differential CK clock inputs control the timing of read/write operations of the RAM. At the rising edge of the CK clock all addresses, write enables, and synchronous selects are registered. An internal buffer and special logic enable the memory to accept write data on the rising edge of the CK clock a cycle after address and control signals. Read data is available at the falling edge of the CK clock.

The RAM uses LVTTL 3.3 V inputs and outputs.

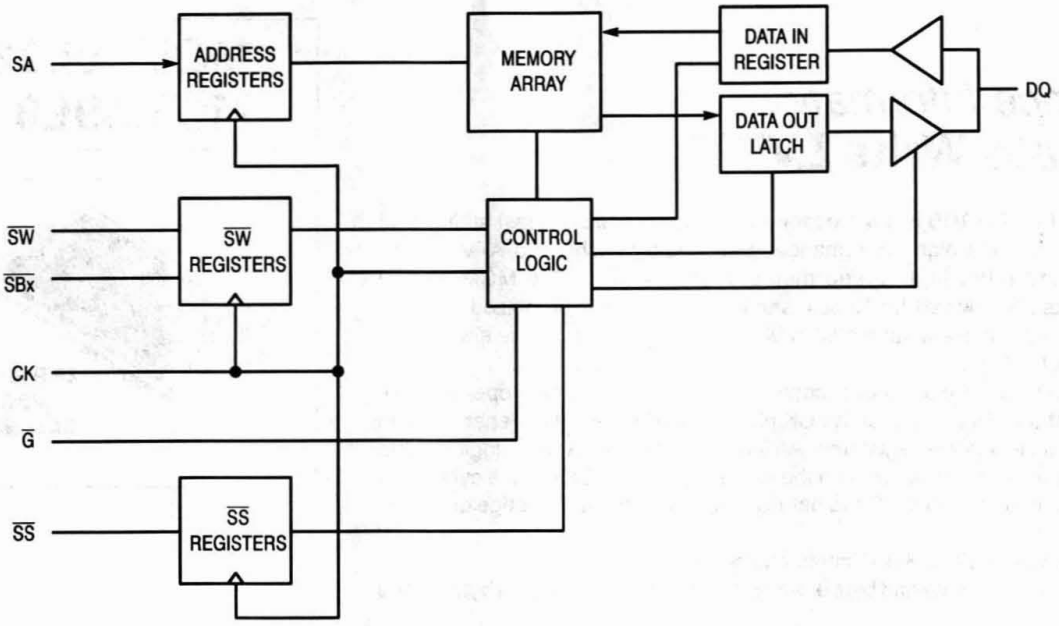
The synchronous write and byte enables allow writing to individual bytes or the entire word.

- Byte Write Control
- Single 3.3 V +10%, – 5% Operation
- LVTTL 3.3 V I/O (V_{DDQ})
- Register to Latch Synchronous Operation
- Asynchronous Output Enable
- Boundary Scan (JTAG) IEEE 1149.1 Compatible
- Differential Clock Inputs
- Optional x 18 or x 36 organization
- MCM69L737/819–8 = 8 ns
  MCM69L737/819–9 = 9 ns
- 119 Bump, 50 mil (1.27 mm) Pitch, 14 mm x 22 mm Plastic Ball Grid Array (PBGA) Package

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 1
4/3/97

FUNCTIONAL BLOCK DIAGRAM



3

PIN ASSIGNMENTS

TOP VIEW

MCM69L737

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	SA	NC	SA	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
E	DQc	DQc	V_{SS}	$\overline{SS}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{G}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{SBc}$	NC	$\overline{SBb}$	DQb	DQb
H	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CK	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{SBd}$	$\overline{CK}$	$\overline{SBa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{SW}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
P	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
R	NC	SA	V_{DD}	V_{DD}	V_{SS}	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69L819

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	SA	NC	SA	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQb	NC	V_{SS}	NC	V_{SS}	DQa	NC
E	NC	DQb	V_{SS}	$\overline{SS}$	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	$\overline{SBb}$	NC	V_{SS}	NC	DQa
H	DQb	NC	V_{SS}	NC	V_{SS}	DQa	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	CK	V_{SS}	NC	DQa
L	DQb	NC	V_{SS}	$\overline{CK}$	$\overline{SBa}$	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{SW}$	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	SA	V_{SS}	DQa	NC
P	NC	DQb	V_{SS}	SA	V_{SS}	NC	DQa
R	NC	SA	V_{DD}	V_{DD}	V_{SS}	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69L737 PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6K, 7K, 6L, 7L, 6M, 6N, 7N, 6P, 7P (b) 6D, 7D, 6E, 7E, 6F, 6G, 7G, 6H, 7H (c) 1D, 2D, 1E, 2E, 2F, 1G, 2G, 1H, 2H (d) 1K, 2K, 1L, 2L, 2M, 1N, 2N, 1P, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 3T, 4T, 5T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 5G, 3G, 3L (a), (b), (c), (d)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
7T	ZZ	Input	Enables sleep mode.
4C, 2J, 4J, 6J, 4R, 3R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 3H, 5H, 3K, 5K, 3M, 5M, 3N, 5N, 3P, 5P, 5R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 4B, 6B, 7B, 1C, 7C, 4D, 4G, 4H, 3J, 5J, 1R, 7R, 1T, 2T, 6T, 6U	NC	—	No Connection: There is no connection to the chip. Note: 3J and 5J are tied common.

MCM69L819 PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6D, 7E, 6F, 7G, 6H, 7K, 6L, 6N, 7P (b) 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 2T, 3T, 5T, 6T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 3G (a), (b)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
7T	ZZ	Input	Enables sleep mode.
4C, 2J, 4J, 6J, 4R, 3R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P, 5R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 4B, 6B, 7B, 1C, 7C, 2D, 4D, 7D, 1E, 6E, 2F, 1G, 4G, 6G, 2H, 4H, 7H, 3J, 5J, 1K, 6K, 2L, 7L, 6M, 2N, 7N, 1P, 6P, 1R, 7R, 1T, 4T, 6U	NC	—	No Connection: There is no connection to the chip. Note: 3J and 5J are tied common.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS}, See Note 1)

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Output Supply Voltage	V_{DDQ}	– 0.5 to V_{DD} + 0.5	V
Voltage On Any Pin	V_{in}	– 0.5 to V_{DD} + 0.5	V
Input Current (per I/O)	I_{in}	± 50	mA
Output Current (per I/O)	I_{out}	± 70	mA
Power Dissipation (See Note 2)	P_D	—	W
Operating Temperature	T_A	0 to + 70	°C
Temperature Under Bias	T_{bias}	–10 to + 85	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability will be dependent upon package characteristics and use environment. See enclosed thermal impedance data.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

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PBGA PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (Still Air)		$R_{\theta JA}$	53	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Single Layer Board	$R_{\theta JA}$	38	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Four Layer Board	$R_{\theta JA}$	22	°C/W	
Junction to Board (Bottom)		$R_{\theta JB}$	14	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	5	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

($0°C \le T_A \le 70°C$, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (See Notes 1 through 4)

Parameter		Symbol	Min	Typical –8	Typical –9	Max	Unit	Notes
Core Power Supply Voltage		V_{DD}	3.15	—	—	3.6	V	
Output Driver Supply Voltage		V_{DDQ}	3.15	—	—	3.6	V	
Active Power Supply Current	(x18) (x36)	I_{DD1}	— —	320 370	300 350	420 470	mA	5
Quiescent Active Power Supply Current		I_{DD2}	—	180	180	250	mA	6, 10
Active Standby Power Supply Current		I_{SB1}	—	160	160	250	mA	7
Quiescent Standby Powe Supply Current		I_{SB2}	—	140	140	230	mA	8, 10
Sleep Mode Power Supply Current		I_{SB3}	—	30	30	50	mA	9, 10

NOTES:
1. All data sheet parameters specified to full range of V_{DD} unless otherwise noted. All voltages are referenced to voltage applied to V_{SS} bumps.
2. Supply voltage applied to V_{DD} connections.
3. Supply voltage applied to V_{DDQ} connections.
4. All power supply currents measured with outputs open or deselected.
5. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered active, 50% read cycles.
6. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered active.
7. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered inactive.
8. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered inactive, ZZ low.
9. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered inactive, ZZ high.
10. $200 \text{ mV} \ge V_{in} \ge V_{DDQ} - 200 \text{ mV}$.

DC INPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
DC Input Logic High	V_{IH} (dc)	2.0	$V_{DD} + 0.3$	V	
DC Input Logic Low	V_{IL} (dc)	– 0.3	0.8	V	1
Input Leakage Current	I_{lkg}	—	± 5	µA	2
Clock Input Leakage Current	I_{clkg}	—	± 8	µA	2
Clock Input Signal Voltage	V_{in}	– 0.3	$V_{DD} + 0.3$	V	
Clock Input Differential Voltage	V_{DIF} (dc)	0.2	$V_{DD} + 0.6$	V	3
Clock Input Common Mode Voltage Range (See Figure 3)	V_{CM} (dc)	1.1	2.1	V	4

NOTES:
1. Inputs may undershoot to – 0.5 V (peak) for up to 20% t_{KHKH} (e.g., 2 ns at a clock cycle time of 10 ns).
2. $0 \text{ V} \le V_{in} \le V_{DD}$.
3. Minimum instantaneous differential input voltage required for differential input clock operation.
4. Maximum rejectable common mode input voltage variation.

DC OUTPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
Output Leakage Current	I_{lkg}	– 1.0	1.0	µA	
Output Low Voltage	V_{OL}	—	0.4	V	1
Output High Voltage	V_{OH}	2.4	—	V	2

NOTES:
1. $I_{OL} = 8.0$ mA.
2. $I_{OH} = -8.0$ mA.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, $0°C \le T_A \le 70°C$, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	5	5	pF
Input/Output Capacitance	$C_{I/O}$	6	8	pF
CK, $\overline{CK}$ Capacitance	C_{CK}	6	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V
Clock Input Timing Reference Level ..... Differential Cross–Point

REGISTER LATCH READ/WRITE CYCLE TIMING (See Notes 2 and 3)

Parameter	Symbol	MCM69L737–8 MCM69L819–8		MCM69L737–9 MCM69L819–9		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{KHKH}	8	—	9	—	ns	
Clock High Pulse Width	t_{KHKL}	3.2	—	3.6	—	ns	
Clock Low Pulse Width	t_{KLKH}	3.2	—	3.6	—	ns	
Clock High to Output Valid	t_{KHQV}	—	9.5	—	10.5	ns	
Clock Low to Output Valid	t_{KLQV}	—	3.5	—	3.5	ns	
Clock Low to Output Hold	t_{KLQX}	0.5	—	0.5	—	ns	
Clock Low to Output Low–Z	t_{KLQX1}	0.5	—	0.5	—	ns	1
Clock High to Output High–Z	t_{KHQZ}	—	4	—	4.5	ns	
Output Enable Low to Output Low–Z	t_{GLQX}	0.5	—	0.5	—	ns	1
Output Enable Low to Output Valid	t_{GLQV}	—	4	—	4.5	ns	
Output Enable to Output Hold	t_{GHQX}	0.5	—	0.5	—	ns	
Output Enable High to Output High–Z	t_{GHQZ}	—	4	—	4.5	ns	1
Setup Times: Address / Data In / Chip Select / Write Enable	t_{AVKH} / t_{DVKH} / t_{SVKH} / t_{WVKH}	0.5	—	0.5	—	ns	
Hold Times: Address / Data In / Chip Select / Write Enable	t_{KHAX} / t_{KHDX} / t_{KHSX} / t_{KHWX}	1	—	1	—	ns	

NOTES:
1. Tested per AC Test Load diagram. See Figure 1.
2. Measured at ± 200 mV from steady state.
3. In no case may control input signals (e.g., $\overline{SS}$) be operated with pulse widths less than the minimum clock input pulse width specifications (e.g., t_{KHKL}) or at frequencies that exceed the applied CK clock frequency.

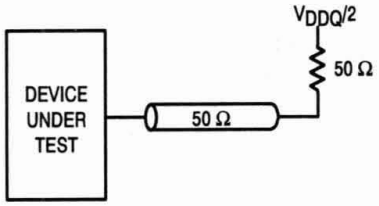


Figure 1. AC Test Load

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

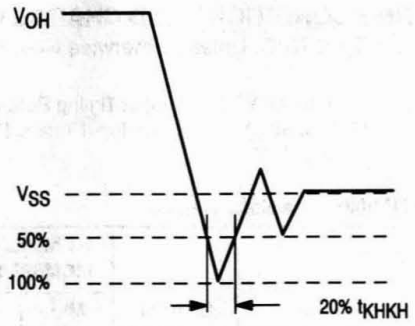
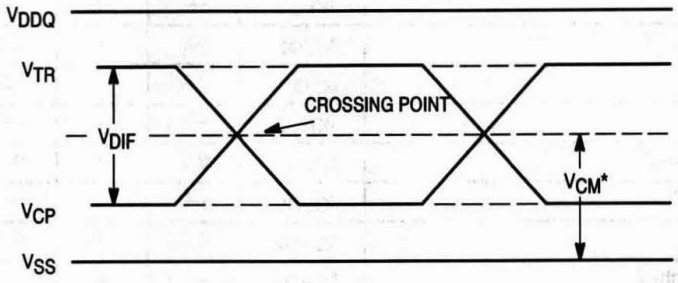


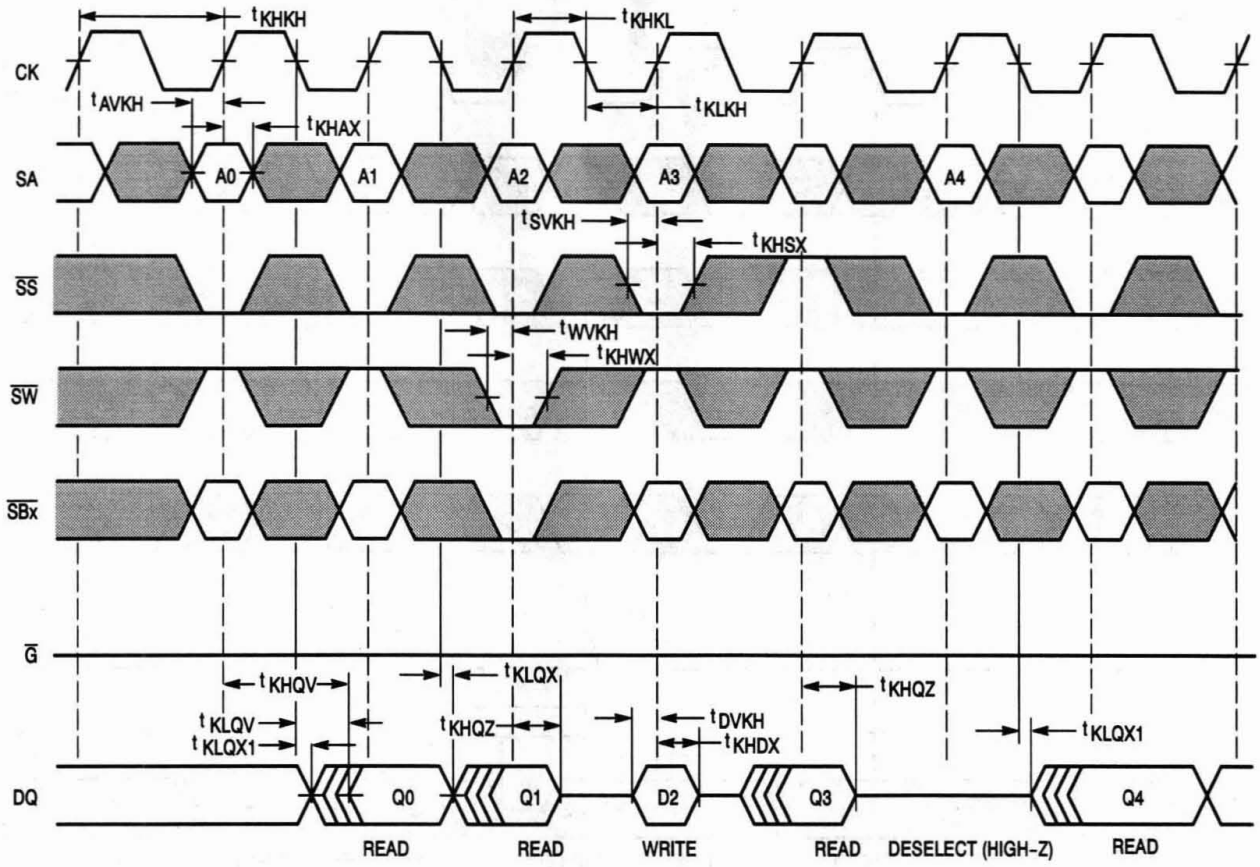
Figure 2. Undershoot Voltage



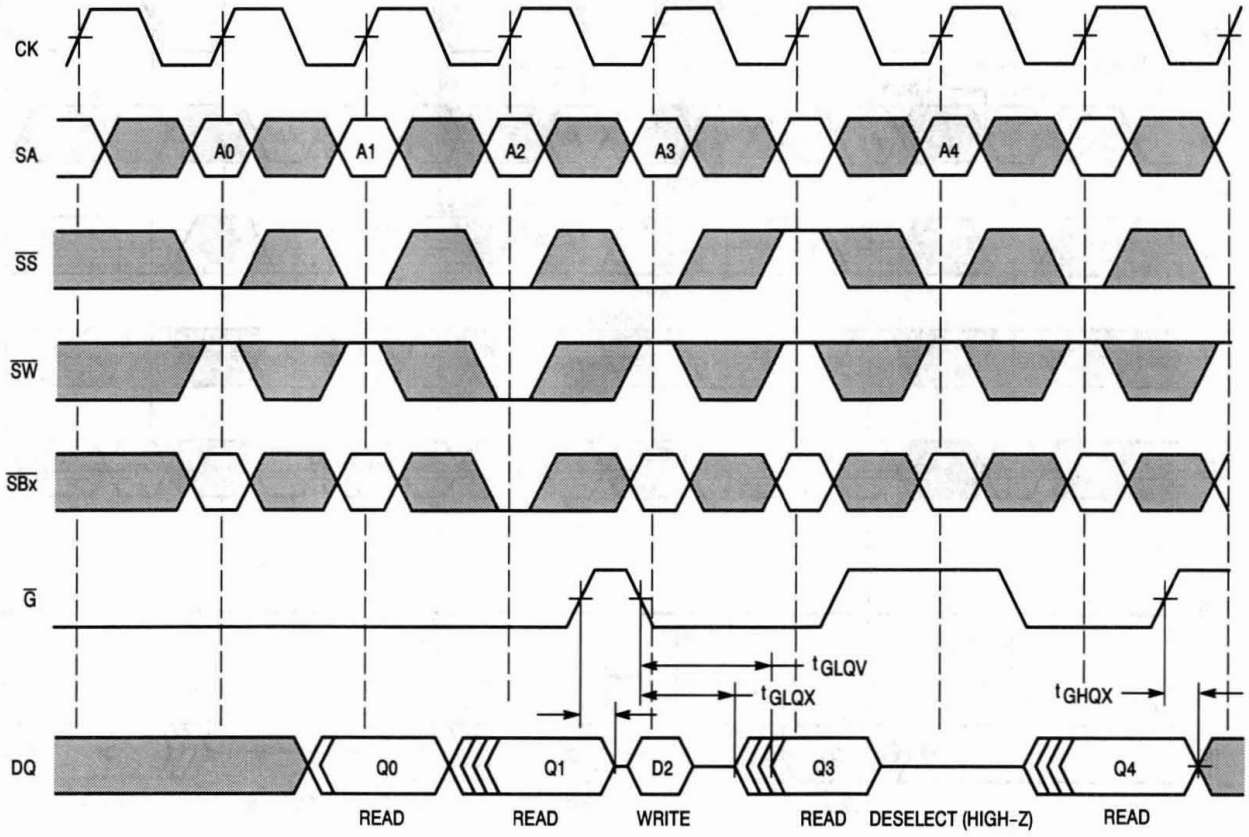
*V_{CM}, the Common Mode Input Voltage, equals $V_{TR} - ((V_{TR} - V_{CP})/2)$.

Figure 3. Differential Inputs/Common Mode Input Voltage

REGISTER LATCH READ–WRITE–READ CYCLES



REGISTER LATCH READ–WRITE–READ CYCLES
($\overline{G}$ Controlled)



FUNCTIONAL OPERATION

READ AND WRITE OPERATIONS

All control signals except $\overline{G}$ are registered on the rising edge of the CK clock. These signals must meet the setup and hold times shown in the AC Characteristics table. On the falling edge of the current cycle, the output latch becomes transparent and data is available. The output data is latched on the rising edge of the next clock. The output data is available at the output at t_{KLQV} or t_{KHQV} whichever is later. t_{KHQV} is the internal latency of the device. During this same cycle a new read address can be applied to the address pins.

A write cycle can occur on the next cycle as long as t_{KLQX} and t_{DVKH} are met. Read cycles may follow write cycles immediately.

$\overline{G}$, $\overline{SS}$, and $\overline{SW}$ control output drive. Chip deselect via a high on $\overline{SS}$ at the rising edge of the CK clock has its effect on the output drivers immediately. $\overline{SW}$ low deselects the output drivers immediately (on the same cycle). Output selecting via a low on $\overline{SS}$ and high on $\overline{SW}$ at a rising CK clock has its effect on the output drivers at t_{KLQX}. Output drive is also controlled directly by output enable, $\overline{G}$. $\overline{G}$ is an asynchronous input. No clock edges are required to enable or disable the output with $\overline{G}$.

Output data will be valid the latter of t_{GLQV}, t_{KHQV}, or t_{KLQV}. Outputs will begin driving at t_{KLQX1}. Outputs will hold previous data until t_{KLQX} or t_{GHQX}.

WRITE AND BYTE WRITE FUNCTIONS

Note that in the following discussion the term "byte" refers to nine bits of the RAM I/O bus. In all cases, the timing parameters described for synchronous write input ($\overline{SW}$) apply to each of the byte write enable inputs ($\overline{SBa}$, $\overline{SBb}$, etc.).

Byte write enable inputs have no effect on read cycles. This allows the system designer not interested in performing byte writes to connect the byte enable inputs to active low (V_{SS}). Reads of all bytes proceed normally and write cycles, activated via a low on $\overline{SW}$, and the rising edge of the CK clock, write the entire RAM I/O width. This way the designer is spared having to drive multiple write input buffer loads.

Byte writes are performed using the byte write enable inputs in conjunction with the synchronous write input ($\overline{SW}$). It is important to note that writing any one byte will inhibit a read of all bytes at the current address. The RAM cannot simultaneously read one byte and write another at the same address. A write cycle initiated with none of the byte write enable inputs active is neither a read or a write. No write will occur, but the outputs will be deselected as in a normal write cycle.

LATE WRITE

The write address is sampled on the first rising edge of clock and write data is sampled on the following rising edge.

The late write feature is implemented with single stage write buffering. Write buffering is transparent to the user. A comparator monitors the address bus and, when necessary, routes buffer contents to the outputs to assure coherent operation. This occurs in all cases whether there is a byte write or a full word is written.

POWER UP AND INITIALIZATION

Please note, per the Absolute Maximum Ratings table, V_{DDQ} is not to exceed V_{DD} + 0.5 V, whatever the instantaneous value of V_{DD}. Once supplies have reached specification levels, a minimum dwell of 1.0 µs with CK clock inputs cycling is required before beginning normal operations.

SERIAL BOUNDARY SCAN TEST ACCESS PORT OPERATION

OVERVIEW

The serial boundary scan test access port (TAP) on this RAM is designed to operate in a manner consistent with IEEE Standard 1149.1–1990 (commonly referred to as JTAG), but does not implement all of the functions required for 1149.1 compliance. Certain functions have been modified or eliminated because their implementation places extra delays in the RAMs critical speed path. Nevertheless, the RAM supports the standard TAP controller architecture. (The TAP controller is the state machine that controls the TAPs operation) and can be expected to function in a manner that does not conflict with the operation of devices with Standard 1149.1 compliant TAPs. The TAP operates using conventional JEDEC Standard 8–1B Low Voltage (3.3 V) TTL / CMOS logic level signaling.

DISABLING THE TEST ACCESS PORT

It is possible to use this device without utilizing the TAP. To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid level inputs. TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a 1 k resistor. TDO should be left unconnected.

TAP DC OPERATING CHARACTERISTICS

($0°C \le T_A \le 70°C$, Unless Otherwise Noted)

Parameter	Symbol	Min	Max	Unit	Note
Logic Input Logic High	$V_{IH}1$	2.0	V_{DD} + 0.3	V	
Logic Input Logic Low	$V_{IL}1$	– 0.3	0.8	V	
Logic Input Leakage Current	I_{lkg}	—	± 5	µA	1
CMOS Output Logic Low	$V_{OL}1$	—	0.2	V	2
CMOS Output Logic High	$V_{OH}1$	V_{DD} – 0.2	—	V	3
TTL Output Logic Low	$V_{OL}2$	—	0.4	V	4
TTL Output Logic High	$V_{OH}2$	2.4	—	V	5

NOTES:
1. $0 V \le V_{in} \le V_{DDQ}$ for all logic input pins.
2. $I_{OL}1 \le 100$ µA. Sampled, not 100% tested.
3. $|I_{OH}1| \le 100$ µA. Sampled, not 100% tested.
4. $I_{OL}2 \le 8$ mA.
5. $|I_{OH}2| \le 8$ mA.

TAP AC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V

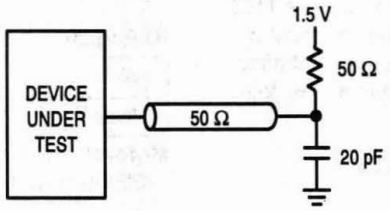
Output Test Load ..... 50 Ω Parallel Terminated T–line with 20 pF Receiver Input Capacitance
Test Load Termination Supply Voltage (V_T) ..... 1.5 V

TAP CONTROLLER TIMING

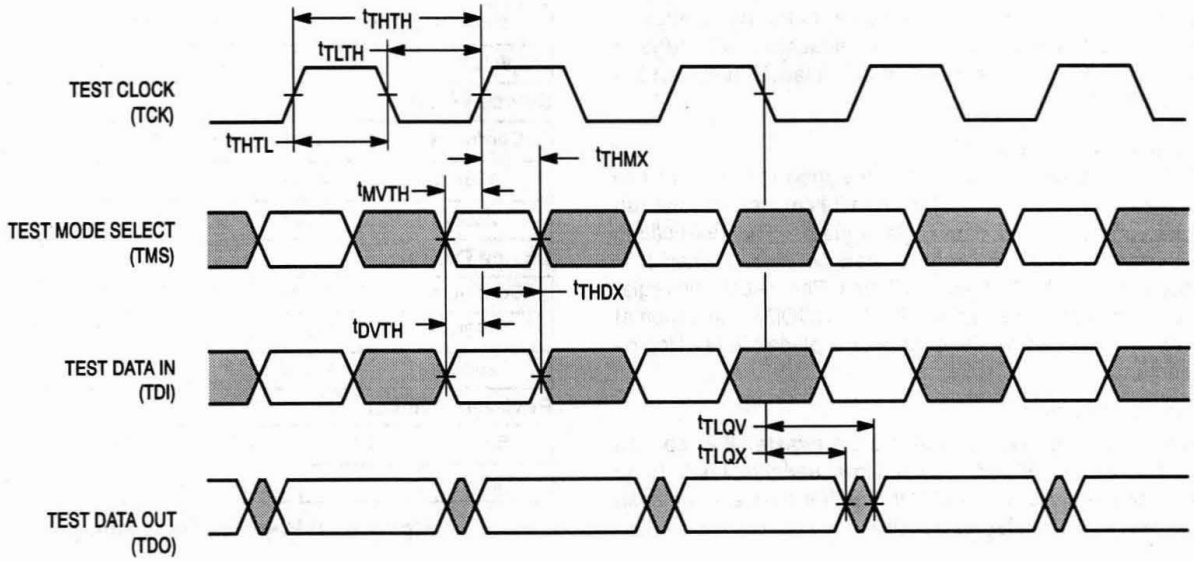
Parameter	Symbol	Min	Max	Unit	Notes
Cycle Time	t_{THTH}	100	—	ns	
Clock High Time	t_{THTL}	40	—	ns	
Clock Low Time	t_{TLTH}	40	—	ns	
TMS Setup	t_{MVTH}	10	—	ns	
TMS Hold	t_{THMX}	10	—	ns	
TDI Valid to TCK High	t_{DVTH}	10	—	ns	
TCK High to TDI Don't Care	t_{THDX}	10	—	ns	
Capture Setup	t_{CS}	10	—	ns	1
Capture Hold	t_{CH}	10	—	ns	1
TCK Low to TDO Unknown	t_{TLQX}	0	—	ns	
TCK Low to TDO Valid	t_{TLOV}	—	20	ns	

NOTES:
1. t_{CS} + t_{CH} defines the minimum pause in RAM I/O pad transitions to assure accurate pad data capture.

AC TEST LOAD



TAP CONTROLLER TIMING DIAGRAM



TEST ACCESS PORT PINS

TCK – TEST CLOCK (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

TMS – TEST MODE SELECT (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.

TDI – TEST DATA IN (INPUT)

The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (refer to Figure 5 TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.

TDO – TEST DATA OUT (OUTPUT)

Output that is active depending on the state of the TAP state machine (refer to Figure 5 TAP Controller State Diagram). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

TRST – TAP RESET

This device does not have a TRST pin. TRST is optional in **IEEE 1149.1.** The test–logic reset state is entered while TMS is held high for five rising edges of TCK. Power on reset circuitry is included internally. This type of reset does not affect the operation of the system logic. The reset affects test logic only.

TEST ACCESS PORT REGISTERS

OVERVIEW

The various TAP registers are selected (one at a time) via the sequences of ones and zeros input to the TMS pin as the TCK is strobed. Each of the TAPs registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on subsequent falling edge of TCK. When a register is selected it is "placed" between the TDI and TDO pins.

INSTRUCTION REGISTER

The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run test/idle or the various data register states. The instructions are three bits long. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power–up or whenever the controller is placed in test–logic–reset state.

BYPASS REGISTER

The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.

BOUNDARY SCAN REGISTER

The boundary scan register is identical in length to the number of active input and I/O connections on the RAM (not counting the TAP pins). This also includes a number of place holder locations (always set to a logic 1) reserved for density upgrade address pins. There are a total of 70 bits in the case of the x36 device and 51 bits in the case of the x18 device. The boundary scan register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture–DR state and then is placed between the TDI and TDO pins when the controller is moved to shift–DR state. Several TAP instructions can be used to activate the boundary scan register.

The Bump/Bit Scan Order tables describe which device bump connects to each boundary scan register location. The first column defines the bit's position in the boundary scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the input or I/O at the bump and the third column is the bump number.

IDENTIFICATION (ID) REGISTER

The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture–DR state with the IDCODE command loaded in the instruction register. The code is loaded from a 32 bit on–chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into shift–DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Presence Indicator

Bit #	0
Value	1

Motorola JEDEC ID Code (Compressed Format, per IEEE Standard 1149.1 – 1990

Bit #	11	10	9	8	7	6	5	4	3	2	1
Value	0	0	0	0	0	0	0	1	1	1	0

Reserved For Future Use

Bit #	17	16	15	14	13	12
Value	x	x	x	x	x	x

Device Width

Configuration	Bit #	22	21	20	19	18
128Kx36	Value	0	0	1	0	0
256Kx18	Value	0	0	0	1	1

Device Depth

Configuration	Bit #	27	26	25	24	23
128Kx36	Value	0	0	1	0	1
256Kx18	Value	0	0	1	1	0

Revision Number

Bit #	31	30	29	28
Value	x	x	x	x

Figure 4. ID Register Bit Meanings

MCM69L737 Bump/Bit Scan Order

BIT #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	SA	3B
2	SA	4P		37	NC	2B
3	SA	4T		38	SA	3A
4	SA	6R		39	SA	3C
5	SA	5T		40	SA	2C
6	ZZ	7T		41	SA	2A
7	DQa	6P		42	DQc	2D
8	DQa	7P		43	DQc	1D
9	DQa	6N		44	DQc	2E
10	DQa	7N		45	DQc	1E
11	DQa	6M		46	DQc	2F
12	DQa	6L		47	DQc	2G
13	DQa	7L		48	DQc	1G
14	DQa	6K		49	DQc	2H
15	DQa	7K		50	DQc	1H
16	$\overline{SBa}$	5L		51	$\overline{SBc}$	3G
17	$\overline{CK}$	4L		52	NC	4D
18	CK	4K		53	$\overline{SS}$	4E
19	$\overline{G}$	4F		54	NC	4G
20	$\overline{SBb}$	5G		55	NC	4H
21	DQb	7H		56	$\overline{SW}$	4M
22	DQb	6H		57	$\overline{SBd}$	3L
23	DQb	7G		58	DQd	1K
24	DQb	6G		59	DQd	2K
25	DQb	6F		60	DQd	1L
26	DQb	7E		61	DQd	2L
27	DQb	6E		62	DQd	2M
28	DQb	7D		63	DQd	1N
29	DQb	6D		64	DQd	2N
30	SA	6A		65	DQd	1P
31	SA	6C		66	DQd	2P
32	SA	5C		67	SA	3T
33	SA	5A		68	SA	2R
34	NC	6B		69	SA	4N
35	SA	5B		70	M1	3R

MCM69L819 Bump/Bit Scan Order

Bit #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	$\overline{SBb}$	3G
2	SA	6T		37	NC	4D
3	SA	4P		38	$\overline{SS}$	4E
4	SA	6R		39	NC	4G
5	SA	5T		40	NC	4H
6	ZZ	7T		41	$\overline{SW}$	4M
7	DQa	7P		42	DQb	2K
8	DQa	6N		43	DQb	1L
9	DQa	6L		44	DQb	2M
10	DQa	7K		45	DQb	1N
11	$\overline{SBa}$	5L		46	DQb	2P
12	$\overline{CK}$	4L		47	SA	3T
13	CK	4K		48	SA	2R
14	$\overline{G}$	4F		49	SA	4N
15	DQa	6H		50	SA	2T
16	DQa	7G		51	M1	3R
17	DQa	6F				
18	DQa	7E				
19	DQa	6D				
20	SA	6A				
21	SA	6C				
22	SA	5C				
23	SA	5A				
24	NC	6B				
25	SA	5B				
26	SA	3B				
27	NC	2B				
28	SA	3A				
29	SA	3C				
30	SA	2C				
31	SA	2A				
32	DQb	1D				
33	DQb	2E				
34	DQb	2G				
35	DQb	1H				

NOTES:

1. The NC pads listed in this table are indeed no connects, but are represented in the boundary scan register by a "place holder" bit that is forced to logic 1. These pads are reserved for use as address inputs on higher density RAMs that follow this pad out and scan order standard.
2. CK, $\overline{CK}$, are sampled individually. $\overline{CK}$ is not simply a forced complement of the CK input. In scan mode these differential inputs are referenced to each other.
3. M1 and M2 are not ordinary inputs and may not respond to standard I/O logic levels. M1 and M2 must be driven to within 100 mV of a V_{DD} or V_{SS} supply rail to ensure consistent results.
4. ZZ must remain at V_{IL} during boundary scan to ensure consistent results.

TAP Controller Instruction Set

OVERVIEW

There are two classes of instructions defined in the Standard 1149.1–1990; the standard (public) instructions, and device specific (private) instructions. Some public instructions, are mandatory for 1149.1 compliance. Optional public instructions must be implemented in prescribed ways.

Although the TAP controller in this device follows the 1149.1 conventions, it is not 1194.1 compliant because some of the mandatory instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads, but cannot be used to load address, data or control signals into the RAM or to preload the I/O buffers. In other words, the device will not perform Standard 1149.1 EXTEST, INTEST or the preload portion of the SAMPLE / PRELOAD command.

When the TAP controller is placed in capture–IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the shift–IR state the instruction register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to update–IR state. The TAP instruction sets for this device are listed in the following tables.

STANDARD (PUBLIC) INSTRUCTIONS

BYPASS

The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift–DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

Sample/preload is a Standard 1149.1 mandatory public instruction. When the sample / preload instruction is loaded in the Instruction register, moving the TAP controller into the capture–DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set–up plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register.

Moving the controller to shift–DR state then places the boundary scan register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the update–DR state with the SAMPLE / PRELOAD instruction loaded in the instruction register has the same effect as the pause–DR command. This functionality is not Standard 1149.1 compliant.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic 0s. EXTEST is not implemented in this device. Therefore this device is not 1149.1 compliant. Nevertheless, this RAMs TAP does respond to an all zeros instruction, as follows. With the EXTEST (000) instruction loaded in the instruction register the RAM responds just as it does in response to the SAMPLE / PRELOAD instruction described above, except the RAM outputs are forced to high–Z any time the instruction is loaded.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture–DR mode and places the ID register between the TDI and TDO pins in shift–DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test–logic–reset state.

THE DEVICE SPECIFIC (PUBLIC) INSTRUCTION

SAMPLE–Z

If the SAMPLE–Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high–Z) and the boundary scan register is connected between TDI and TDO when the TAP controller. is moved to the shift–DR state.

THE DEVICE SPECIFIC (PRIVATE) INSTRUCTION

NOOP

Do not use these instructions; they are reserved for future use.

STANDARD (PUBLIC) INSTRUCTION CODES

Instruction	Code*	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM outputs to High–Z state. *NOT 1149.1 COMPLIANT*
IDCODE	001**	Preloads ID register and places it between TDI and TDO. Does not affect RAM operation.
SAMPLE / PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect RAM operation. Does not implement 1149.1 Preload function. * NOT 1149.1 COMPLIANT *
BYPASS	111	Places bypass register between TDI and TDO. Does not affect RAM operation.
SAMPLE–Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM output drivers to High–Z.

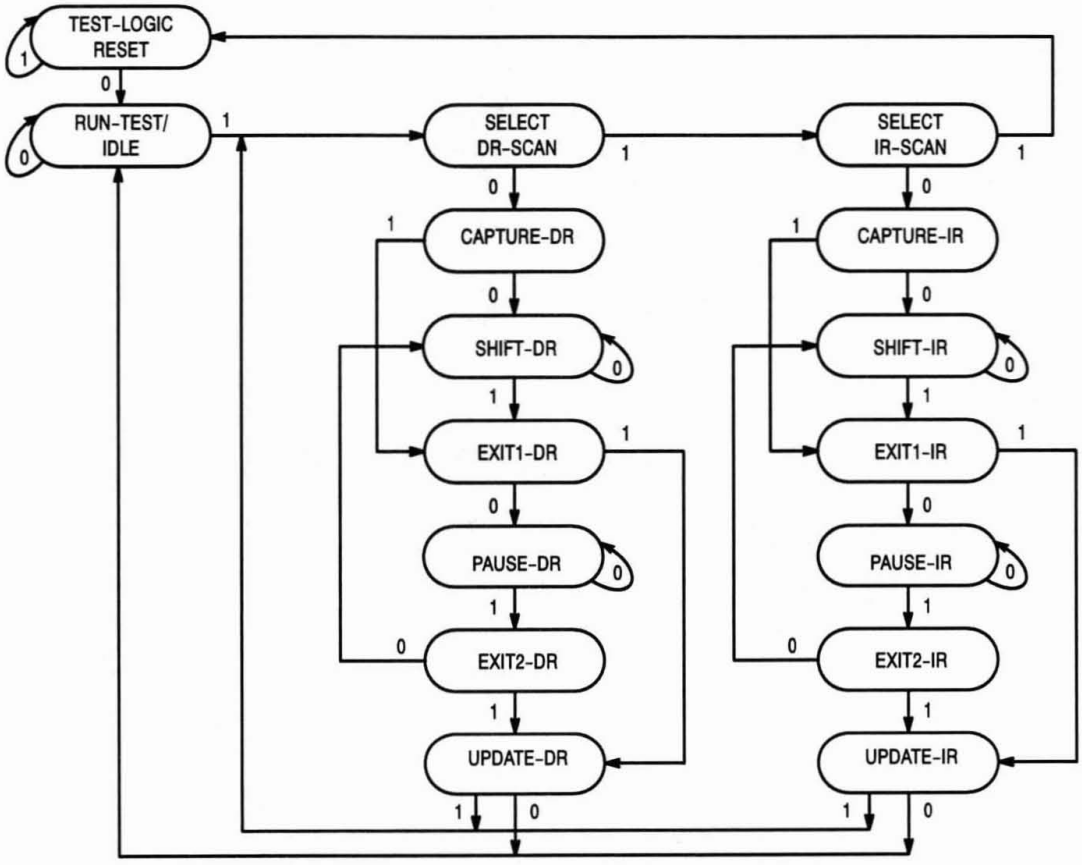
* Instruction codes expressed in binary, MSB on left, LSB on right.
** Default instruction automatically loaded at power–up and in test–logic–reset state.

3

STANDARD (PRIVATE) INSTRUCTION CODES

Instruction	Code*	Description
NO OP	011	Do not use these instructions; they are reserved for future use.
NO OP	101	Do not use these instructions; they are reserved for future use.
NO OP	110	Do not use these instructions; they are reserved for future use.

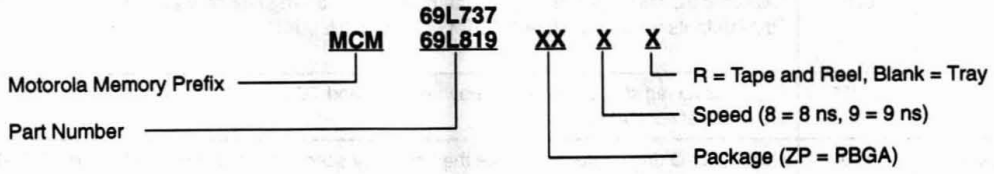
* Instruction codes expressed in binary, MSB on left, LSB on right.



NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 5. TAP Controller State Diagram

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers —	MCM69L737ZP8	MCM69L737ZP9
	MCM69L819ZP8	MCM69L819ZP9
	MCM69L737ZP8R	MCM69L737ZP9R
	MCM69L819ZP8R	MCM69L819ZP9R

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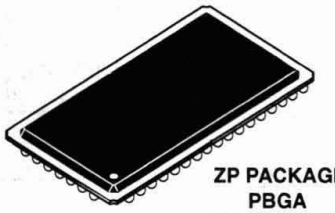
MCM69L737A
MCM69L819A

Advance Information

4M Late Write LVTTL



ZP PACKAGE
PBGA
CASE 999–01

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The MCM69L737A/819A is a 4 megabit synchronous late write fast static RAM designed to provide high performance in secondary cache and ATM switch, Telecom, and other high speed memory applications. The MCM69L819A organized as 256K words by 18 bits, and the MCM69L737A organized as 128K words by 36 bits wide are fabricated in Motorola's high performance silicon gate BiCMOS technology.

The differential CK clock inputs control the timing of read/write operations of the RAM. At the rising edge of the CK clock all addresses, write enables, and synchronous selects are registered. An internal buffer and special logic enable the memory to accept write data on the rising edge of the CK clock a cycle after address and control signals. Read data is available at the falling edge of the CK clock.

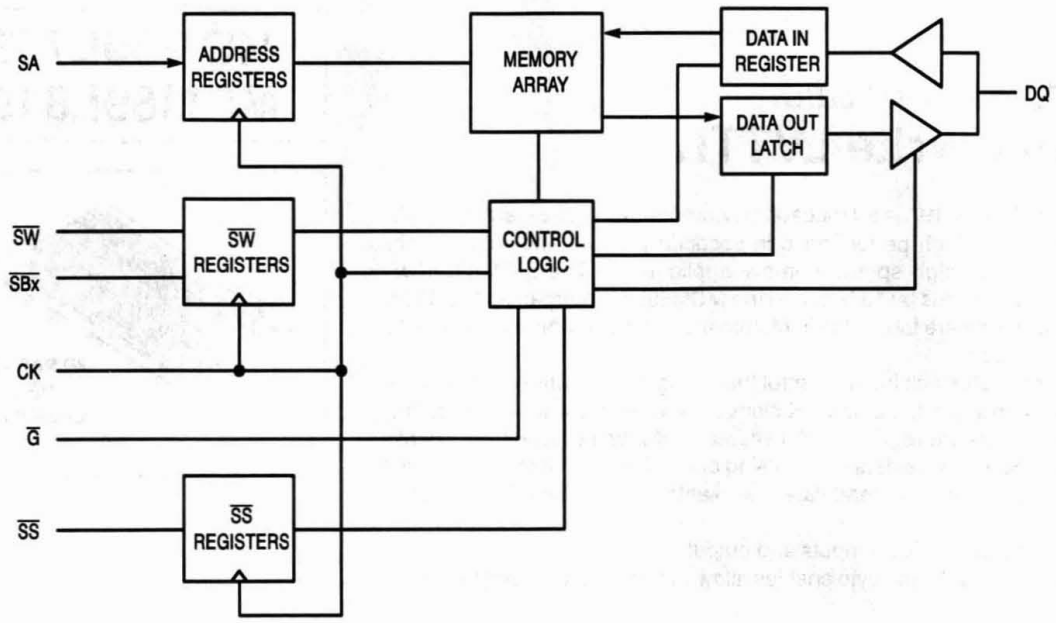
The RAM uses LVTTL 3.3 V inputs and outputs.

The synchronous write and byte enables allow writing to individual bytes or the entire word.

- Byte Write Control
- Single 3.3 V + 10%, – 5% Operation
- LVTTL 3.3 V I/O (V_{DDQ})
- Register to Latch Synchronous Operation
- Asynchronous Output Enable
- Boundary Scan (JTAG) IEEE 1149.1 Compatible
- Differential Clock Inputs
- Optional x 18 or x 36 organization
- MCM69L737A/819A–7.5 = 7.5 ns
  MCM69L737A/819A–8.5 = 8.5 ns
  MCM69L737A/819A–9.5 = 9.5 ns
  MCM69L737A/819A–10.5 = 10.5 ns
- 119 Bump, 50 mil (1.27 mm) Pitch, 14 mm x 22 mm Plastic Ball Grid Array (PBGA) Package

This document contains information on a new product. Specifications and information herein are subject to change without notice.
4/3/97

FUNCTIONAL BLOCK DIAGRAM



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PIN ASSIGNMENTS

TOP VIEW

MCM69L737A

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	SA	NC	SA	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
E	DQc	DQc	V_{SS}	$\overline{SS}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{G}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{SBc}$	NC	$\overline{SBb}$	DQb	DQb
H	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CK	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{SBd}$	$\overline{CK}$	$\overline{SBa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{SW}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
P	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
R	NC	SA	V_{DD}	V_{DD}	V_{SS}	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69L819A

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	SA	NC	SA	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQb	NC	V_{SS}	NC	V_{SS}	DQa	NC
E	NC	DQb	V_{SS}	$\overline{SS}$	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	$\overline{SBb}$	NC	V_{SS}	NC	DQa
H	DQb	NC	V_{SS}	NC	V_{SS}	DQa	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	CK	V_{SS}	NC	DQa
L	DQb	NC	V_{SS}	$\overline{CK}$	$\overline{SBa}$	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{SW}$	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	SA	V_{SS}	DQa	NC
P	NC	DQb	V_{SS}	SA	V_{SS}	NC	DQa
R	NC	SA	V_{DD}	V_{DD}	V_{SS}	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69L737A PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6K, 7K, 6L, 7L, 6M, 6N, 7N, 6P, 7P (b) 6D, 7D, 6E, 7E, 6F, 6G, 7G, 6H, 7H (c) 1D, 2D, 1E, 2E, 2F, 1G, 2G, 1H, 2H (d) 1K, 2K, 1L, 2L, 2M, 1N, 2N, 1P, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 3T, 4T, 5T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 5G, 3G, 3L (a), (b), (c), (d)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
7T	ZZ	Input	Enables sleep mode.
4C, 2J, 4J, 6J, 4R, 3R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 3H, 5H, 3K, 5K, 3M, 5M, 3N, 5N, 3P, 5P, 5R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 4B, 6B, 7B, 1C, 7C, 4D, 4G, 4H, 3J, 5J, 1R, 7R, 1T, 2T, 6T, 6U	NC	—	No Connection: There is no connection to the chip. Note: 3J and 5J are tied common.

MCM69L819A PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6D, 7E, 6F, 7G, 6H, 7K, 6L, 6N, 7P (b) 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 2T, 3T, 5T, 6T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 3G (a), (b)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
7T	ZZ	Input	Enables sleep mode.
4C, 2J, 4J, 6J, 4R, 3R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P, 5R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 4B, 6B, 7B, 1C, 7C, 2D, 4D, 7D, 1E, 6E, 2F, 1G, 4G, 6G, 2H, 4H, 7H, 3J, 5J, 1K, 6K, 2L, 7L, 6M, 2N, 7N, 1P, 6P, 1R, 7R, 1T, 4T, 6U	NC	—	No Connection: There is no connection to the chip. Note: 3J and 5J are tied common.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS}, See Note 1)

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Output Supply Voltage	V_{DDQ}	– 0.5 to V_{DD} + 0.5	V
Voltage On Any Pin	V_{in}	– 0.5 to V_{DD} + 0.5	V
Input Current (per I/O)	I_{in}	± 50	mA
Output Current (per I/O)	I_{out}	± 70	mA
Power Dissipation (See Note 2)	P_D	—	W
Operating Temperature	T_A	0 to + 70	°C
Temperature Under Bias	T_{bias}	–10 to + 85	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability will be dependent upon package characteristics and use environment. See enclosed thermal impedance data.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

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PBGA PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (Still Air)		$R_{\theta JA}$	53	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Single Layer Board	$R_{\theta JA}$	38	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Four Layer Board	$R_{\theta JA}$	22	°C/W	
Junction to Board (Bottom)		$R_{\theta JB}$	14	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	5	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (See Notes 1 through 4)

Parameter	Symbol	Min	Typical –7.5	Typical –8.5	Typical –9.5	Typical –10.5	Max	Unit	Notes
Core Power Supply Voltage	V_{DD}	3.15	—	—	—	—	3.6	V	
Output Driver Supply Voltage	V_{DDQ}	3.15	—	—	—	—	3.6	V	
Active Power Supply Current (x18) (x36)	I_{DD1}	— —	330 390	320 370	300 350	280 330	480 550	mA	5
Quiescent Active Power Supply Current	I_{DD2}	—	180	180	180	180	250	mA	6, 10
Active Standby Power Supply Current	I_{SB1}	—	170	170	170	170	250	mA	7
Quiescent Standby Power Supply Current	I_{SB2}	—	150	150	150	150	230	mA	8, 10
Sleep Mode Power Supply Current	I_{SB3}	—	30	30	30	30	50	mA	9, 10

NOTES:
1. All data sheet parameters specified to full range of V_{DD} unless otherwise noted. All voltages are referenced to voltage applied to V_{SS} bumps.
2. Supply voltage applied to V_{DD} connections.
3. Supply voltage applied to V_{DDQ} connections.
4. All power supply currents measured with outputs open or deselected.
5. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered active, 50% read cycles.
6. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered active.
7. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered inactive.
8. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered inactive, ZZ low.
9. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered inactive, ZZ high.
10. 200 mV ≥ V_{in} ≥ V_{DDQ} – 200 mV.

DC INPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
DC Input Logic High	V_{IH} (dc)	2.0	V_{DD} + 0.3	V	
DC Input Logic Low	V_{IL} (dc)	– 0.3	0.8	V	1
Input Leakage Current	I_{lkg}	—	± 5	µA	2
Clock Input Leakage Current	I_{clkg}	—	± 8	µA	2
Clock Input Signal Voltage	V_{in}	– 0.3	V_{DD} + 0.3	V	
Clock Input Differential Voltage	V_{DIF} (dc)	0.2	V_{DD} + 0.6	V	3
Clock Input Common Mode Voltage Range (See Figure 3)	V_{CM} (dc)	1.1	2.1	V	4

NOTES:
1. Inputs may undershoot to –0.5 V (peak) for up to 20% t_{KHKH} (e.g., 2 ns at a clock cycle time of 10 ns).
2. 0 V ≤ V_{in} ≤ V_{DD}.
3. Minimum instantaneous differential input voltage required for differential input clock operation.
4. Maximum rejectable common mode input voltage variation.

DC OUTPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
Output Leakage Current	I_{lkg}	–1.0	1.0	µA	
Output Low Voltage	V_{OL}	—	0.4	V	1
Output High Voltage	V_{OH}	2.4	—	V	2

NOTES:
1. I_{OL} = 8.0 mA.
2. I_{OH} = – 8.0 mA.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, 0°C ≤ T_A ≤ 70°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	5	pF
Input/Output Capacitance	$C_{I/O}$	7	8	pF
CK, $\overline{CK}$ Capacitance	C_{CK}	4	5	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

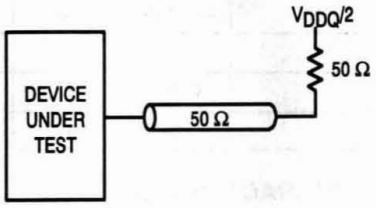
(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V
Clock Input Timing Reference Level ..... Differential Cross–Point
Clock Input Pulse Level ..... 1.8 V to 2.1 V

READ/WRITE CYCLE TIMING (See Note 3)

Parameter	Symbol	MCM69L736A–7.5 MCM69L818A–7.5		MCM69L736A–8.5 MCM69L818A–8.5		MCM69L736A–9.5 MCM69L818A–9.5		MCM69L736A–10.5 MCM69L818A–10.5		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	7	—	8	—	9	—	10	—	ns	
Clock High Pulse Width	t_{KHKL}	2.8	—	3.2	—	3.6	—	4	—	ns	
Clock Low Pulse Width	t_{KLKH}	2.8	—	3.2	—	3.6	—	4	—	ns	
Clock High to Output Valid	t_{KHQV}	—	7.5	—	8.5	—	9.5	—	10.5	ns	2
Clock Low to Output Valid	t_{KLQV}	—	3.5	—	4	—	4	—	4	ns	2
Clock Low to Output Hold	t_{KLQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	2
Clock Low to Output Low–Z	t_{KLQX1}	1	—	1	—	1	—	1	—	ns	3
Clock High to Output High–Z	t_{KHQZ}	—	3.5	—	4	—	4	—	4	ns	3
Output Enable Low to Output Low–Z	t_{GLQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	3
Output Enable Low to Output Valid	t_{GLQV}	—	3.5	—	4	—	4	—	4	ns	2
Output Enable to Output Hold	t_{GHQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	2
Output Enable High to Output High–Z	t_{GHQZ}	—	3.5	—	4	—	4	—	4	ns	3
Setup Times: Address Data In Chip Select Write Enable	t_{AVKH} t_{DVKH} t_{SVKH} t_{WVKH}	0.5	—	0.5	—	0.5	—	0.5	—	ns	
Hold Times: Address Data In Chip Select Write Enable	t_{KHAX} t_{KHDX} t_{KHSX} t_{KHWX}	1	—	1	—	1	—	1	—	ns	

NOTES:
1. Measured at ± 200 mV from steady state.
2. In no case may control input signals (e.g., $\overline{SS}$) be operated with pulse widths less than the minimum clock input pulse width specifications (e.g., t_{KHKL}) or at frequencies that exceed the applied K clock frequency.
3. Tested per AC Test Load diagram. See Figure 1.



TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Figure 1. AC Test Load

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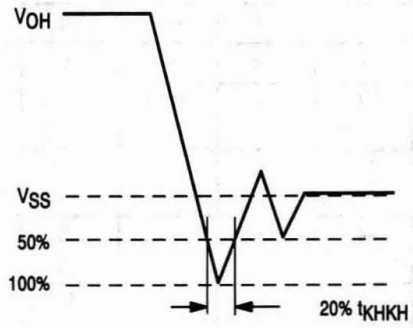
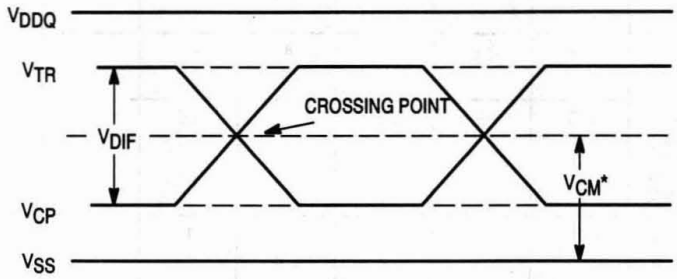


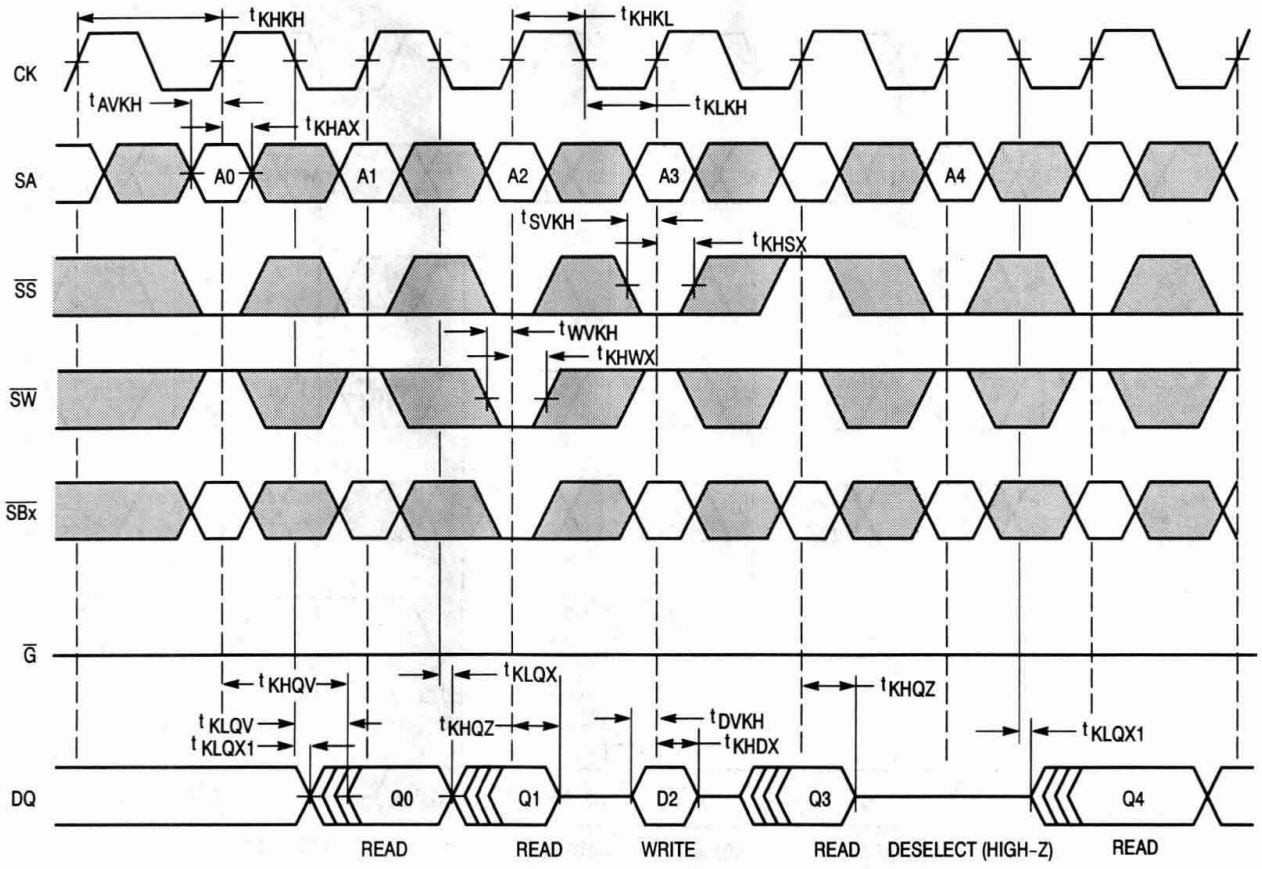
Figure 2. Undershoot Voltage



*V_{CM}, the Common Mode Input Voltage, equals $V_{TR} - ((V_{TR} - V_{CP})/2)$.

Figure 3. Differential Inputs/Common Mode Input Voltage

REGISTER LATCH READ–WRITE–READ CYCLES



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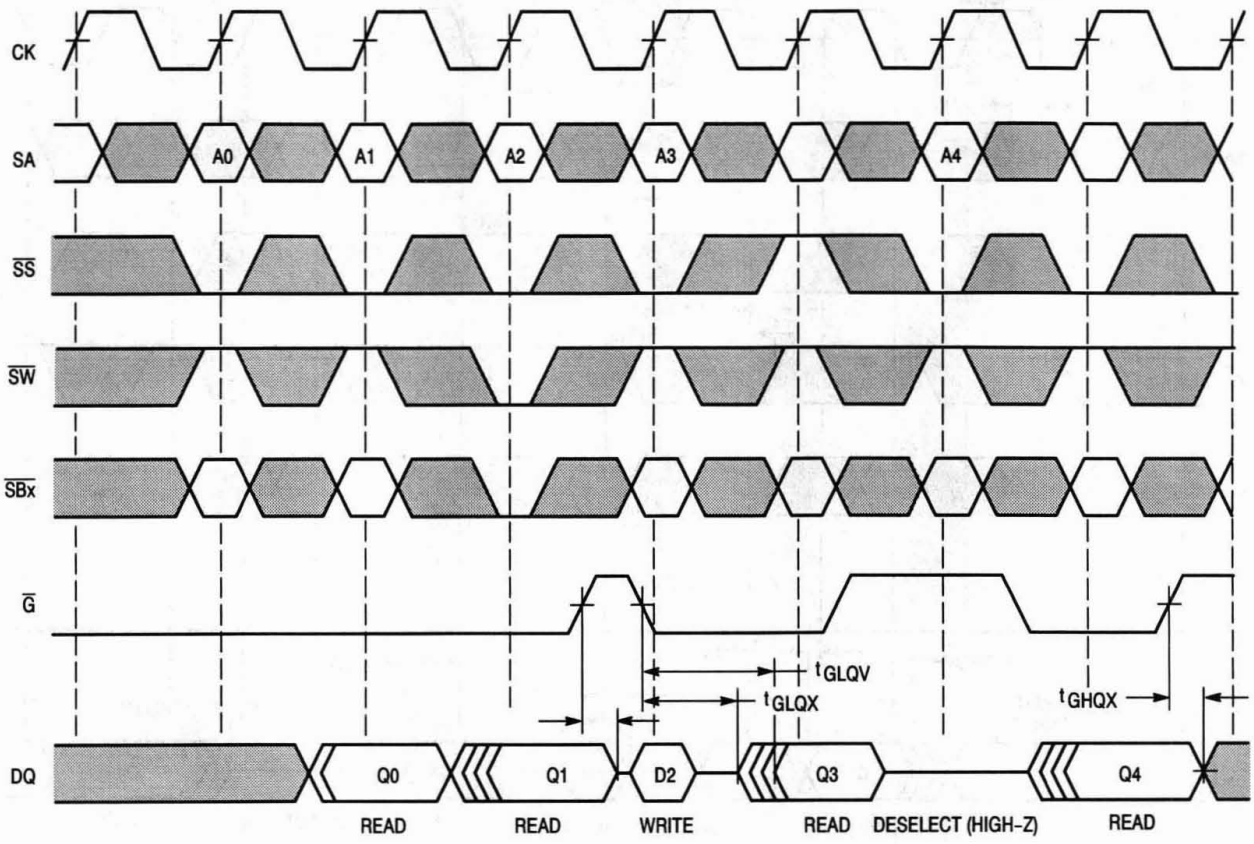
REGISTER LATCH READ–WRITE–READ CYCLES
($\overline{G}$ Controlled)



FUNCTIONAL OPERATION

READ AND WRITE OPERATIONS

All control signals except $\overline{G}$ are registered on the rising edge of the CK clock. These signals must meet the setup and hold times shown in the AC Characteristics table. On the falling edge of the current cycle, the output latch becomes transparent and data is available. The output data is latched on the rising edge of the next clock. The output data is available at the output at t_{KLQV} or t_{KHQV} whichever is later. t_{KHQV} is the internal latency of the device. During this same cycle a new read address can be applied to the address pins.

A write cycle can occur on the next cycle as long as t_{KLQX} and t_{DVKH} are met. Read cycles may follow write cycles immediately.

$\overline{G}$, $\overline{SS}$, and $\overline{SW}$ control output drive. Chip deselect via a high on $\overline{SS}$ at the rising edge of the CK clock has its effect on the output drivers immediately. $\overline{SW}$ low deselects the output drivers immediately (on the same cycle). Output selecting via a low on $\overline{SS}$ and high on $\overline{SW}$ at a rising CK clock has its effect on the output drivers at t_{KLQX}. Output drive is also controlled directly by output enable, $\overline{G}$. $\overline{G}$ is an asynchronous input. No clock edges are required to enable or disable the output with $\overline{G}$.

Output data will be valid the latter of t_{GLQV}, t_{KHQV}, or t_{KLQV}. Outputs will begin driving at t_{KLQX1}. Outputs will hold previous data until t_{KLQX} or t_{GHQX}.

WRITE AND BYTE WRITE FUNCTIONS

Note that in the following discussion the term "byte" refers to nine bits of the RAM I/O bus. In all cases, the timing parameters described for synchronous write input ($\overline{SW}$) apply to each of the byte write enable inputs ($\overline{SBa}$, $\overline{SBb}$, etc.).

Byte write enable inputs have no effect on read cycles. This allows the system designer not interested in performing byte writes to connect the byte enable inputs to active low (V_{SS}). Reads of all bytes proceed normally and write cycles, activated via a low on $\overline{SW}$, and the rising edge of the CK clock, write the entire RAM I/O width. This way the designer is spared having to drive multiple write input buffer loads.

Byte writes are performed using the byte write enable inputs in conjunction with the synchronous write input ($\overline{SW}$). It is important to note that writing any one byte will inhibit a read of all bytes at the current address. The RAM cannot simultaneously read one byte and write another at the same address. A write cycle initiated with none of the byte write enable inputs active is neither a read or a write. No write will occur, but the outputs will be deselected as in a normal write cycle.

LATE WRITE

The write address is sampled on the first rising edge of clock and write data is sampled on the following rising edge.

The late write feature is implemented with single stage write buffering. Write buffering is transparent to the user. A comparator monitors the address bus and, when necessary, routes buffer contents to the outputs to assure coherent operation. This occurs in all cases whether there is a byte write or a full word is written.

POWER UP AND INITIALIZATION

Please note, per the Absolute Maximum Ratings table, V_{DDQ} is not to exceed V_{DD} + 0.5 V, whatever the instantaneous value of V_{DD}. Once supplies have reached specification levels, a minimum dwell of 1.0 µs with CK clock inputs cycling is required before beginning normal operations.

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SERIAL BOUNDARY SCAN TEST ACCESS PORT OPERATION

OVERVIEW

The serial boundary scan test access port (TAP) on this RAM is designed to operate in a manner consistent with IEEE Standard 1149.1–1990 (commonly referred to as JTAG), but does not implement all of the functions required for 1149.1 compliance. Certain functions have been modified or eliminated because their implementation places extra delays in the RAMs critical speed path. Nevertheless, the RAM supports the standard TAP controller architecture. (The TAP controller is the state machine that controls the TAPs operation) and can be expected to function in a manner that does not conflict with the operation of devices with Standard 1149.1 compliant TAPs. The TAP operates using conventional JEDEC Standard 8–1B Low Voltage (3.3 V) TTL / CMOS logic level signaling.

DISABLING THE TEST ACCESS PORT

It is possible to use this device without utilizing the TAP. To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid level inputs. TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a 1 k resistor. TDO should be left unconnected.

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TAP DC OPERATING CHARACTERISTICS

($0°C \le T_A \le 70°C$, Unless Otherwise Noted)

Parameter	Symbol	Min	Max	Unit	Note
Logic Input Logic High	$V_{IH}1$	2.0	V_{DD} + 0.3	V	
Logic Input Logic Low	$V_{IL}1$	– 0.3	0.8	V	
Logic Input Leakage Current	I_{lkg}	—	± 5	µA	1
CMOS Output Logic Low	$V_{OL}1$	—	0.2	V	2
CMOS Output Logic High	$V_{OH}1$	V_{DD} – 0.2	—	V	3
TTL Output Logic Low	$V_{OL}2$	—	0.4	V	4
TTL Output Logic High	$V_{OH}2$	2.4	—	V	5

NOTES:
1. $0 V \le V_{in} \le V_{DDQ}$ for all logic input pins.
2. $I_{OL}1 \le 100$ µA. Sampled, not 100% tested.
3. $|I_{OH}1| \le 100$ µA. Sampled, not 100% tested.
4. $I_{OL}2 \le 8$ mA.
5. $|I_{OH}2| \le 8$ mA.

TAP AC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V

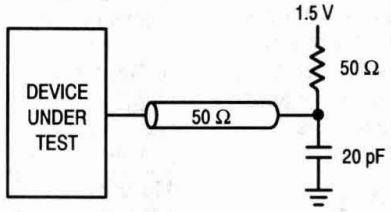
Output Test Load ..... 50 Ω Parallel Terminated T–line with 20 pF Receiver Input Capacitance
Test Load Termination Supply Voltage (V_T) ..... 1.5 V

TAP CONTROLLER TIMING

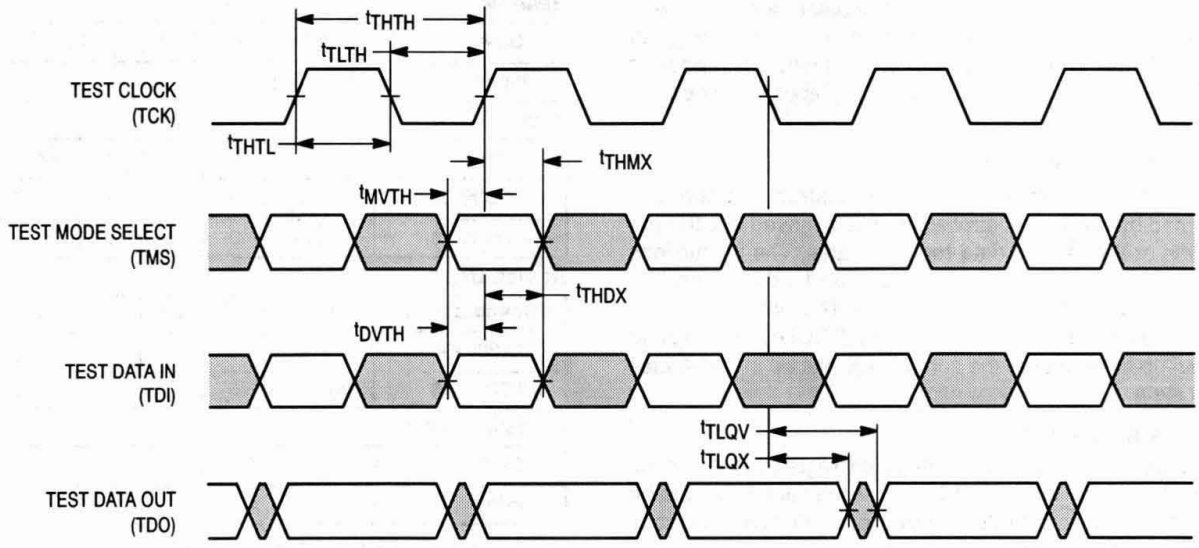
Parameter	Symbol	Min	Max	Unit	Notes
Cycle Time	t_{THTH}	100	—	ns	
Clock High Time	t_{THTL}	40	—	ns	
Clock Low Time	t_{TLTH}	40	—	ns	
TMS Setup	t_{MVTH}	10	—	ns	
TMS Hold	t_{THMX}	10	—	ns	
TDI Valid to TCK High	t_{DVTH}	10	—	ns	
TCK High to TDI Don't Care	t_{THDX}	10	—	ns	
Capture Setup	t_{CS}	10	—	ns	1
Capture Hold	t_{CH}	10	—	ns	1
TCK Low to TDO Unknown	t_{TLQX}	0	—	ns	
TCK Low to TDO Valid	t_{TLOV}	—	20	ns	

NOTES:
1. t_{CS} + t_{CH} defines the minimum pause in RAM I/O pad transitions to assure accurate pad data capture.

AC TEST LOAD



TAP CONTROLLER TIMING DIAGRAM



TEST ACCESS PORT PINS

TCK – TEST CLOCK (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

TMS – TEST MODE SELECT (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.

TDI – TEST DATA IN (INPUT)

The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (refer to Figure 5 TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.

TDO – TEST DATA OUT (OUTPUT)

Output that is active depending on the state of the TAP state machine (refer to Figure 5 TAP Controller State Diagram). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

TRST – TAP RESET

This device does not have a TRST pin. TRST is optional in **IEEE 1149.1.** The test–logic reset state is entered while TMS is held high for five rising edges of TCK. Power on reset circuitry is included internally. This type of reset does not affect the operation of the system logic. The reset affects test logic only.

TEST ACCESS PORT REGISTERS

OVERVIEW

The various TAP registers are selected (one at a time) via the sequences of ones and zeros input to the TMS pin as the TCK is strobed. Each of the TAPs registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on subsequent falling edge of TCK. When a register is selected it is "placed" between the TDI and TDO pins.

INSTRUCTION REGISTER

The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run test/idle or the various data register states. The instructions are three bits long. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power–up or whenever the controller is placed in test–logic–reset state.

BYPASS REGISTER

The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.

BOUNDARY SCAN REGISTER

The boundary scan register is identical in length to the number of active input and I/O connections on the RAM (not counting the TAP pins). This also includes a number of place holder locations (always set to a logic 1) reserved for density upgrade address pins. There are a total of 70 bits in the case of the x36 device and 51 bits in the case of the x18 device. The boundary scan register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture–DR state and then is placed between the TDI and TDO pins when the controller is moved to shift–DR state. Several TAP instructions can be used to activate the boundary scan register.

The Bump/Bit Scan Order tables describe which device bump connects to each boundary scan register location. The first column defines the bit's position in the boundary scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the input or I/O at the bump and the third column is the bump number.

IDENTIFICATION (ID) REGISTER

The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture–DR state with the IDCODE command loaded in the instruction register. The code is loaded from a 32 bit on–chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into shift–DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Presence Indicator

Bit #	0
Value	1

Motorola JEDEC ID Code (Compressed Format, per IEEE Standard 1149.1 – 1990

Bit #	11	10	9	8	7	6	5	4	3	2	1
Value	0	0	0	0	0	0	0	1	1	1	0

Reserved For Future Use

Bit #	17	16	15	14	13	12
Value	x	x	x	x	x	x

Device Width

Configuration	Bit #	22	21	20	19	18
128Kx36	Value	0	0	1	0	0
256Kx18	Value	0	0	0	1	1

Device Depth

Configuration	Bit #	27	26	25	24	23
128Kx36	Value	0	0	1	0	1
256Kx18	Value	0	0	1	1	0

Revision Number

Bit #	31	30	29	28
Value	x	x	x	x

Figure 4. ID Register Bit Meanings

MCM69L737A Bump/Bit Scan Order

BIT #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	SA	3B
2	SA	4P		37	NC	2B
3	SA	4T		38	SA	3A
4	SA	6R		39	SA	3C
5	SA	5T		40	SA	2C
6	ZZ	7T		41	SA	2A
7	DQa	6P		42	DQc	2D
8	DQa	7P		43	DQc	1D
9	DQa	6N		44	DQc	2E
10	DQa	7N		45	DQc	1E
11	DQa	6M		46	DQc	2F
12	DQa	6L		47	DQc	2G
13	DQa	7L		48	DQc	1G
14	DQa	6K		49	DQc	2H
15	DQa	7K		50	DQc	1H
16	$\overline{SBa}$	5L		51	$\overline{SBc}$	3G
17	$\overline{CK}$	4L		52	NC	4D
18	CK	4K		53	$\overline{SS}$	4E
19	$\overline{G}$	4F		54	NC	4G
20	$\overline{SBb}$	5G		55	NC	4H
21	DQb	7H		56	$\overline{SW}$	4M
22	DQb	6H		57	$\overline{SBd}$	3L
23	DQb	7G		58	DQd	1K
24	DQb	6G		59	DQd	2K
25	DQb	6F		60	DQd	1L
26	DQb	7E		61	DQd	2L
27	DQb	6E		62	DQd	2M
28	DQb	7D		63	DQd	1N
29	DQb	6D		64	DQd	2N
30	SA	6A		65	DQd	1P
31	SA	6C		66	DQd	2P
32	SA	5C		67	SA	3T
33	SA	5A		68	SA	2R
34	NC	6B		69	SA	4N
35	SA	5B		70	M1	3R

MCM69L819A Bump/Bit Scan Order

Bit #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	$\overline{SBb}$	3G
2	SA	6T		37	NC	4D
3	SA	4P		38	$\overline{SS}$	4E
4	SA	6R		39	NC	4G
5	SA	5T		40	NC	4H
6	ZZ	7T		41	$\overline{SW}$	4M
7	DQa	7P		42	DQb	2K
8	DQa	6N		43	DQb	1L
9	DQa	6L		44	DQb	2M
10	DQa	7K		45	DQb	1N
11	$\overline{SBa}$	5L		46	DQb	2P
12	$\overline{CK}$	4L		47	SA	3T
13	CK	4K		48	SA	2R
14	$\overline{G}$	4F		49	SA	4N
15	DQa	6H		50	SA	2T
16	DQa	7G		51	M1	3R
17	DQa	6F				
18	DQa	7E				
19	DQa	6D				
20	SA	6A				
21	SA	6C				
22	SA	5C				
23	SA	5A				
24	NC	6B				
25	SA	5B				
26	SA	3B				
27	NC	2B				
28	SA	3A				
29	SA	3C				
30	SA	2C				
31	SA	2A				
32	DQb	1D				
33	DQb	2E				
34	DQb	2G				
35	DQb	1H				

NOTES:

1. The NC pads listed in this table are indeed no connects, but are represented in the boundary scan register by a "place holder" bit that is forced to logic 1. These pads are reserved for use as address inputs on higher density RAMs that follow this pad out and scan order standard.
2. CK, $\overline{CK}$, are sampled individually. $\overline{CK}$ is not simply a forced complement of the CK input. In scan mode these differential inputs are referenced to each other.
3. M1 and M2 are not ordinary inputs and may not respond to standard I/O logic levels. M1 and M2 must be driven to within 100 mV of a V_{DD} or V_{SS} supply rail to ensure consistent results.
4. ZZ must remain at V_{IL} during boundary scan to ensure consistent results.

TAP Controller Instruction Set

OVERVIEW

There are two classes of instructions defined in the Standard 1149.1–1990; the standard (public) instructions, and device specific (private) instructions. Some public instructions, are mandatory for 1149.1 compliance. Optional public instructions must be implemented in prescribed ways.

Although the TAP controller in this device follows the 1149.1 conventions, it is not 1194.1 compliant because some of the mandatory instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads, but cannot be used to load address, data or control signals into the RAM or to preload the I/O buffers. In other words, the device will not perform Standard 1149.1 EXTEST, INTEST or the preload portion of the SAMPLE / PRELOAD command.

When the TAP controller is placed in capture–IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the shift–IR state the instruction register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to update–IR state. The TAP instruction sets for this device are listed in the following tables.

STANDARD (PUBLIC) INSTRUCTIONS

BYPASS

The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift–DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

Sample/preload is a Standard 1149.1 mandatory public instruction. When the sample / preload instruction is loaded in the Instruction register, moving the TAP controller into the capture–DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set–up plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register.

Moving the controller to shift–DR state then places the boundary scan register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the update–DR state with the SAMPLE / PRELOAD instruction loaded in the instruction register has the same effect as the pause–DR command. This functionality is not Standard 1149.1 compliant.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic 0s. EXTEST is not implemented in this device. Therefore this device is not 1149.1 compliant. Nevertheless, this RAMs TAP does respond to an all zeros instruction, as follows. With the EXTEST (000) instruction loaded in the instruction register the RAM responds just as it does in response to the SAMPLE / PRELOAD instruction described above, except the RAM outputs are forced to high–Z any time the instruction is loaded.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture–DR mode and places the ID register between the TDI and TDO pins in shift–DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test–logic–reset state.

THE DEVICE SPECIFIC (PUBLIC) INSTRUCTION

SAMPLE–Z

If the SAMPLE–Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high–Z) and the boundary scan register is connected between TDI and TDO when the TAP controller. is moved to the shift–DR state.

THE DEVICE SPECIFIC (PRIVATE) INSTRUCTION

NOOP

Do not use these instructions; they are reserved for future use.

STANDARD (PUBLIC) INSTRUCTION CODES

Instruction	Code*	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM outputs to High–Z state. *NOT 1149.1 COMPLIANT*
IDCODE	001**	Preloads ID register and places it between TDI and TDO. Does not affect RAM operation.
SAMPLE / PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect RAM operation. Does not implement 1149.1 Preload function. * NOT 1149.1 COMPLIANT *
BYPASS	111	Places bypass register between TDI and TDO. Does not affect RAM operation.
SAMPLE–Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM output drivers to High–Z.

* Instruction codes expressed in binary, MSB on left, LSB on right.
** Default instruction automatically loaded at power–up and in test–logic–reset state.

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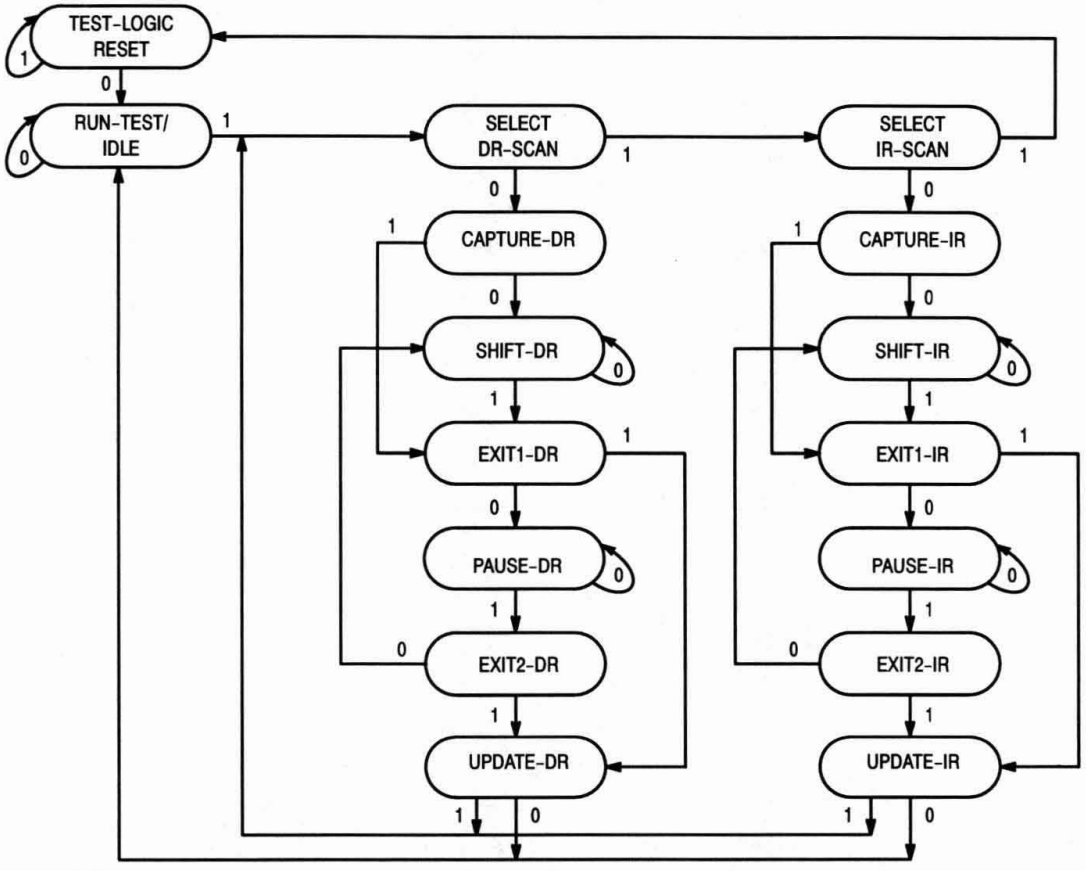
STANDARD (PRIVATE) INSTRUCTION CODES

Instruction	Code*	Description
NO OP	011	Do not use these instructions; they are reserved for future use.
NO OP	101	Do not use these instructions; they are reserved for future use.
NO OP	110	Do not use these instructions; they are reserved for future use.

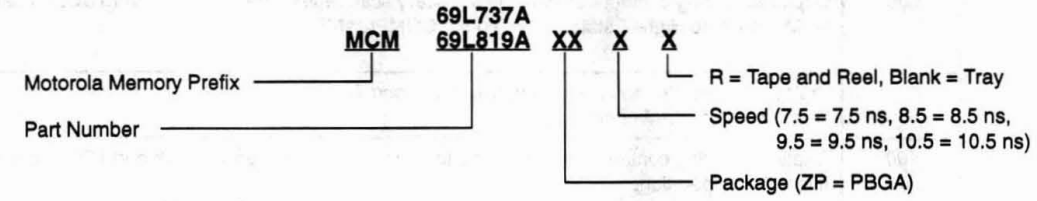
* Instruction codes expressed in binary, MSB on left, LSB on right.



NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 5. TAP Controller State Diagram

ORDERING INFORMATION
(Order by Full Part Number)


MCM 69L737A 69L819A XX X X
Motorola Memory Prefix
Part Number
R = Tape and Reel, Blank = Tray
Speed (7.5 = 7.5 ns, 8.5 = 8.5 ns, 9.5 = 9.5 ns, 10.5 = 10.5 ns)
Package (ZP = PBGA)

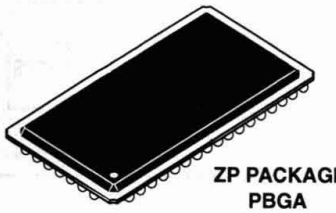
Full Part Numbers —	MCM69L737AZP7.5	MCM69L737AZP8.5	MCM69L737AZP9.5	MCM69L737AZP10.5
	MCM69L819AZP7.5	MCM69L819AZP8.5	MCM69L819AZP9.5	MCM69L819AZP10.5
	MCM69L737AZP7.5R	MCM69L737AZP8.5R	MCM69L737AZP9.5R	MCM69L737AZP10.5R
	MCM69L819AZP7.5R	MCM69L819AZP8.5R	MCM69L819AZP9.5R	MCM69L819AZP10.5R

3

MCM69L738
MCM69L820

Advance Information

4M Late Write 2.5 V I/O



ZP PACKAGE
PBGA
CASE 999–01

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The MCM69L738/820 is a 4 megabit synchronous late write fast static RAM designed to provide high performance in secondary cache and ATM switch, Telecom, and other high speed memory applications. The MCM69L820 organized as 256K words by 18 bits, and the MCM69L738 organized as 128K words by 36 bits wide are fabricated in Motorola's high performance silicon gate BiCMOS technology.

The differential CK clock inputs control the timing of read/write operations of the RAM. At the rising edge of the CK clock all addresses, write enables, and synchronous selects are registered. An internal buffer and special logic enable the memory to accept write data on the rising edge of the CK clock a cycle after address and control signals. Read data is available at the falling edge of the CK clock.

The RAM use 2.5 V inputs and outputs.

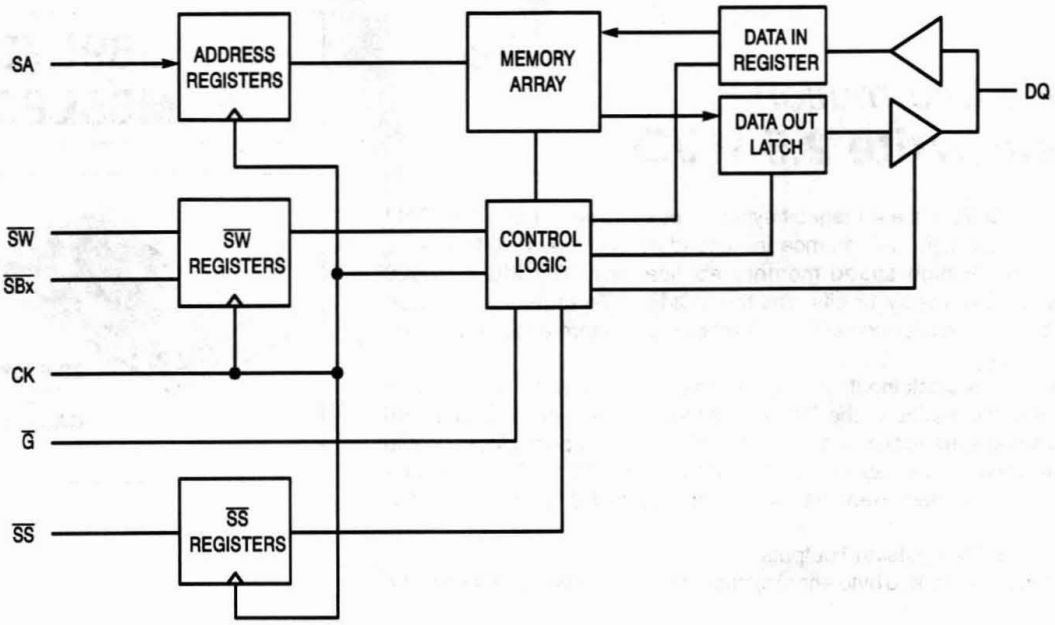
The synchronous write and byte enables allow writing to individual bytes or the entire word.

- Byte Write Control
- 3.3 V + 10%, – 5% Operation
- 2.5 V I/O (V_{DDQ})
- Register to Latch Synchronous Operation
- Asynchronous Output Enable
- Boundary Scan (JTAG) IEEE 1149.1 Compatible
- Differential Clock Inputs (PECL)
- Optional x 18 or x 36 organization
- MCM69L738/820–8 = 8 ns
  MCM69L738/820–9 = 9 ns
- 119 Bump, 50 mil (1.27 mm) Pitch, 14 mm x 22 mm Plastic Ball Grid Array (PBGA) Package

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 1
4/3/97

FUNCTIONAL BLOCK DIAGRAM



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PIN ASSIGNMENTS

TOP VIEW

MCM69L738

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	SA	NC	SA	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
E	DQc	DQc	V_{SS}	$\overline{SS}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{G}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{SBc}$	NC	$\overline{SBb}$	DQb	DQb
H	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CK	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{SBd}$	$\overline{CK}$	$\overline{SBa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{SW}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
P	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
R	NC	SA	V_{DD}	V_{DD}	V_{SS}	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69L820

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	SA	NC	SA	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQb	NC	V_{SS}	NC	V_{SS}	DQa	NC
E	NC	DQb	V_{SS}	$\overline{SS}$	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	$\overline{SBb}$	NC	V_{SS}	NC	DQa
H	DQb	NC	V_{SS}	NC	V_{SS}	DQa	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	CK	V_{SS}	NC	DQa
L	DQb	NC	V_{SS}	$\overline{CK}$	$\overline{SBa}$	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{SW}$	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	SA	V_{SS}	DQa	NC
P	NC	DQb	V_{SS}	SA	V_{SS}	NC	DQa
R	NC	SA	V_{DD}	V_{DD}	V_{SS}	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69L738 PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6K, 7K, 6L, 7L, 6M, 6N, 7N, 6P, 7P (b) 6D, 7D, 6E, 7E, 6F, 6G, 7G, 6H, 7H (c) 1D, 2D, 1E, 2E, 2F, 1G, 2G, 1H, 2H (d) 1K, 2K, 1L, 2L, 2M, 1N, 2N, 1P, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 3T, 4T, 5T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 5G, 3G, 3L (a), (b), (c), (d)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
7T	ZZ	Input	Enables sleep mode.
4C, 2J, 4J, 6J, 4R, 3R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 3H, 5H, 3K, 5K, 3M, 5M, 3N, 5N, 3P, 5P, 5R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 4B, 6B, 7B, 1C, 7C, 4D, 4G, 4H, 3J, 5J, 1R, 7R, 1T, 2T, 6T, 6U	NC	—	No Connection: There is no connection to the chip. Note: 3J and 5J are tied common.

MCM69L820 PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6D, 7E, 6F, 7G, 6H, 7K, 6L, 6N, 7P (b) 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 2T, 3T, 5T, 6T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 3G (a), (b)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
7T	ZZ	Input	Enables sleep mode.
4C, 2J, 4J, 6J, 4R, 3R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P, 5R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 4B, 6B, 7B, 1C, 7C, 2D, 4D, 7D, 1E, 6E, 2F, 1G, 4G, 6G, 2H, 4H, 7H, 3J, 5J, 1K, 6K, 2L, 7L, 6M, 2N, 7N, 1P, 6P, 1R, 7R, 1T, 4T, 6U	NC	—	No Connection: There is no connection to the chip. Note: 3J and 5J are tied common.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS}, See Note 1)

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Output Supply Voltage	V_{DDQ}	– 0.5 to V_{DD} + 0.5	V
Voltage On Any Pin	V_{in}	– 0.5 to V_{DD} + 0.5	V
Input Current (per I/O)	I_{in}	± 50	mA
Output Current (per I/O)	I_{out}	± 70	mA
Power Dissipation (See Note 2)	P_D	—	W
Operating Temperature	T_A	0 to + 70	°C
Temperature Under Bias	T_{bias}	–10 to + 85	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability will be dependent upon package characteristics and use environment. See enclosed thermal impedance data.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

3

PBGA PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (Still Air)		$R_{\theta JA}$	53	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Single Layer Board	$R_{\theta JA}$	38	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Four Layer Board	$R_{\theta JA}$	22	°C/W	
Junction to Board (Bottom)		$R_{\theta JB}$	14	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	5	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

($0°C \le T_A \le 70°C$, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (See Notes 1 through 4)

Parameter		Symbol	Min	Typical –8	Typical –9	Max	Unit	Notes
Core Power Supply Voltage		V_{DD}	3.15	—	—	3.6	V	
Output Driver Supply Voltage		V_{DDQ}	2.3	—	—	2.7	V	
Active Power Supply Current	(x18) (x36)	I_{DD1}	— —	320 370	300 350	420 470	mA	5
Quiescent Active Power Supply Current		I_{DD2}	—	180	180	250	mA	6, 10
Active Standby Power Supply Current		I_{SB1}	—	160	160	250	mA	7
Quiescent Standby Power Supply Current		I_{SB2}	—	140	140	230	mA	8, 10
Sleep Mode Power Supply Current		I_{SB3}	—	30	30	50	mA	9, 10

NOTES:
1. All data sheet parameters specified to full range of V_{DD} unless otherwise noted. All voltages are referenced to voltage applied to V_{SS} bumps.
2. Supply voltage applied to V_{DD} connections.
3. Supply voltage applied to V_{DDQ} connections.
4. All power supply currents measured with outputs open or deselected.
5. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered active, 50% read cycles.
6. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered active.
7. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered inactive.
8. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered inactive, $\overline{ZZ}$ low.
9. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered inactive, $\overline{ZZ}$ high.
10. $200 \text{ mV} \ge V_{in} \ge V_{DDQ} - 200 \text{ mV}$.

DC INPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
DC Input Logic High	V_{IH} (dc)	1.7	$V_{DD} + 0.3$	V	
DC Input Logic Low	V_{IL} (dc)	– 0.3	0.7	V	1
Input Leakage Current	I_{lkg}	—	± 5	µA	2
Clock Input Leakage Current	I_{clkg}	—	± 8	µA	2
Clock Input Signal Voltage	V_{in}	– 0.3	$V_{DD} + 0.3$	V	
Clock Input Differential Voltage	V_{DIF}(dc)	0.2	$V_{DD} + 0.6$	V	3
Clock Input Common Mode Voltage Range (See Figure 3)	V_{CM}(dc)	1.1	2.1	V	4

NOTES:
1. Inputs may undershoot to – 0.5 V (peak) for up to 20% t_{KHKH} (e.g., 2 ns at a clock cycle time of 10 ns).
2. $0 \text{ V} \le V_{in} \le V_{DD}$ for all pins.
3. Minimum instantaneous differential input voltage required for differential input clock operation.
4. Maximum rejectable common mode input voltage variation.

DC OUTPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
Output Leakage Current	I_{lkg}	–1.0	1.0	µA	
Output Low Voltage	V_{OL}	—	0.7	V	1
Output High Voltage	V_{OH}	1.7	—	V	2

NOTES:
1. $I_{OL} = 8.0$ mA.
2. $I_{OH} = -8.0$ mA.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, $0°C \le T_A \le 70°C$, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	5	5	pF
Input/Output Capacitance	$C_{I/O}$	6	8	pF
CK, $\overline{CK}$ Capacitance	C_{CK}	6	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

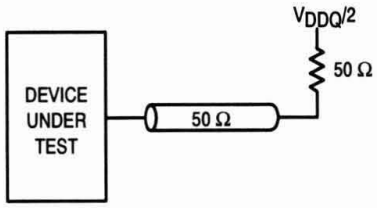
($0°C \le T_A \le 70°C$, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 2.5 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.25 V
Output Timing Reference Level ..... 1.25 V
Clock Input Timing Reference Level ..... Differential Cross–Point

REGISTER LATCH READ/WRITE CYCLE TIMING (See Notes 2 and 3)

Parameter	Symbol	MCM69L738–8 MCM69L820–8		MCM69L738–9 MCM69L820–9		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{KHKH}	8	—	9	—	ns	
Clock High Pulse Width	t_{KHKL}	3.2	—	3.6	—	ns	
Clock Low Pulse Width	t_{KLKH}	3.2	—	3.6	—	ns	
Clock High to Output Valid	t_{KHQV}	—	9.5	—	10.5	ns	
Clock Low to Output Valid	t_{KLQV}	—	3.5	—	3.5	ns	
Clock Low to Output Hold	t_{KLQX}	0.5	—	0.5	—	ns	
Clock Low to Output Low–Z	t_{KLQX1}	0.5	—	0.5	—	ns	1
Clock High to Output High–Z	t_{KHQZ}	—	3.5	—	3.5	ns	
Output Enable Low to Output Low–Z	t_{GLQX}	0.5	—	0.5	—	ns	1
Output Enable Low to Output Valid	t_{GLQV}	—	3.5	—	3.5	ns	
Output Enable to Output Hold	t_{GHQX}	0.5	—	0.5	—	ns	
Output Enable High to Output High–Z	t_{GHQZ}	—	3.5	—	3.5	ns	1
Setup Times: Address Data In Chip Select Write Enable	t_{AVKH} t_{DVKH} t_{SVKH} t_{WVKH}	0.5	—	0.5	—	ns	
Hold Times: Address Data In Chip Select Write Enable	t_{KHAX} t_{KHDX} t_{KHSX} t_{KHWX}	1	—	1	—	ns	

NOTES:
1. Tested per AC Test Load diagram. See Figure 1.
2. Measured at ± 200 mV from steady state.
3. In no case may control input signals (e.g., $\overline{SS}$) be operated with pulse widths less than the minimum clock input pulse width specifications (e.g., t_{KHKL}) or at frequencies that exceed the applied CK clock frequency.



TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Figure 1. AC Test Load

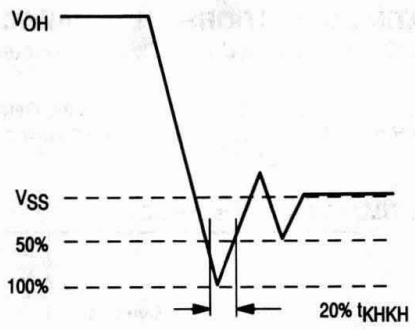
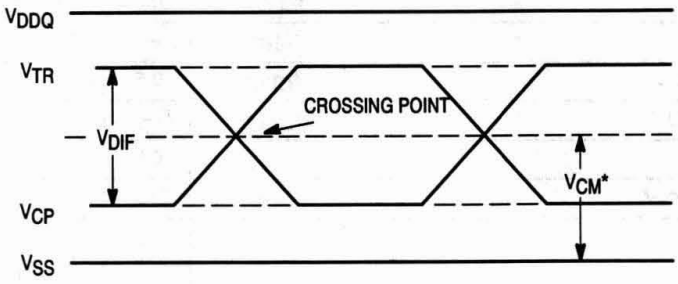


Figure 2. Undershoot Voltage

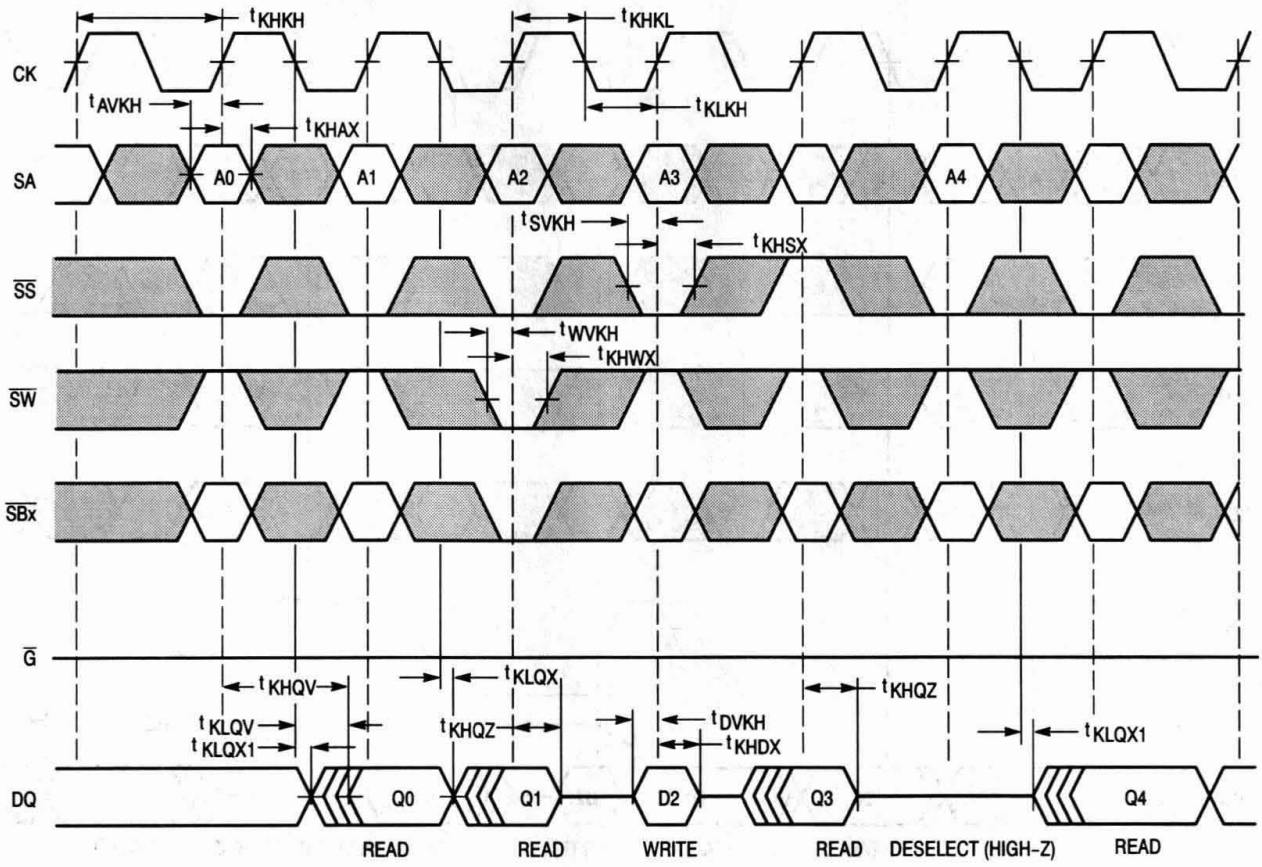
3



*V_{CM}, the Common Mode Input Voltage, equals $V_{TR} - ((V_{TR} - V_{CP})/2)$.

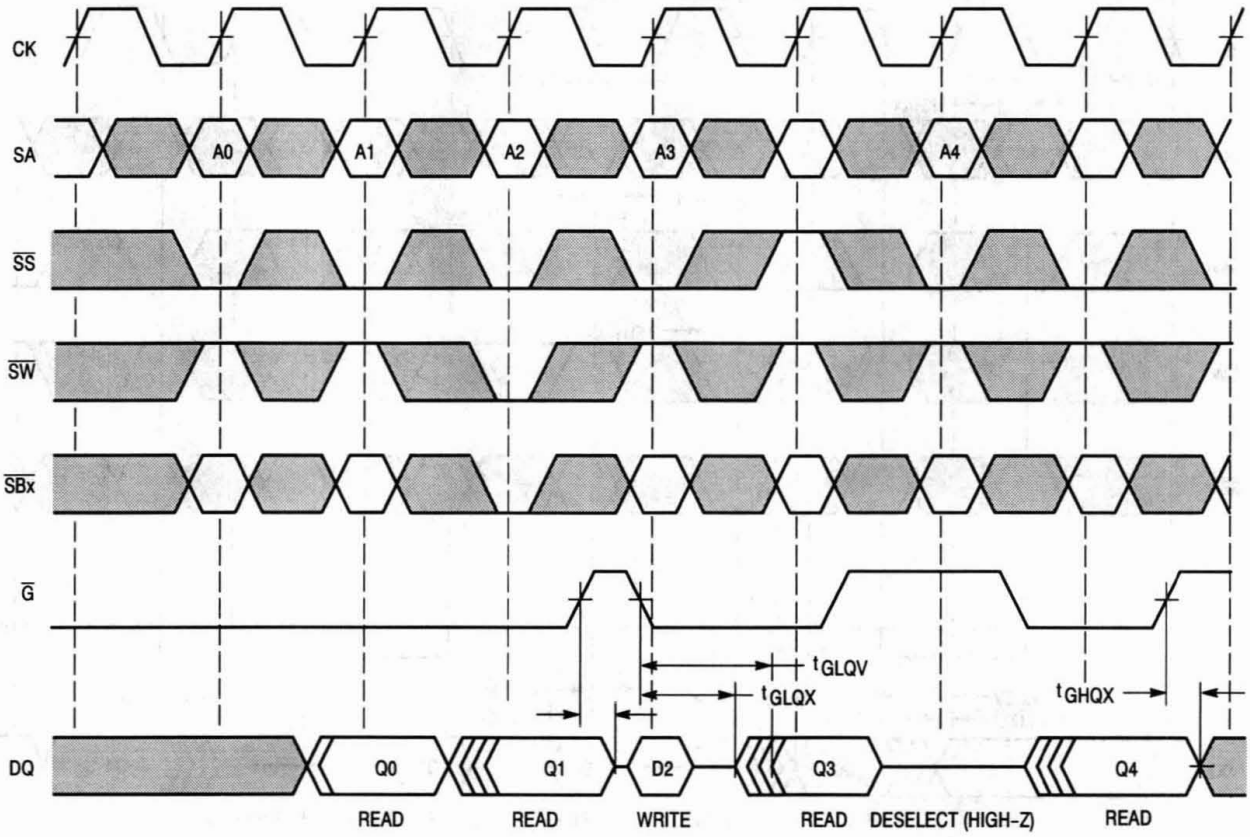
Figure 3. Differential Inputs/Common Mode Input Voltage

REGISTER LATCH READ–WRITE–READ CYCLES



3

REGISTER LATCH READ–WRITE–READ CYCLES
($\overline{G}$ Controlled)



FUNCTIONAL OPERATION

READ AND WRITE OPERATIONS

All control signals except $\overline{G}$ are registered on the rising edge of the CK clock. These signals must meet the setup and hold times shown in the AC Characteristics table. On the falling edge of the current cycle, the output latch becomes transparent and data is available. The output data is latched on the rising edge of the next clock. The output data is available at the output at t_{KLQV} or t_{KHQV}, whichever is later. t_{KHQV} is the internal latency of the device. During this same cycle a new read address can be applied to the address pins.

A write cycle can occur on the next cycle as long as t_{KLQX} and t_{DVKH} are met. Read cycles may follow write cycles immediately.

$\overline{G}$, $\overline{SS}$, and $\overline{SW}$ control output drive. Chip deselect via a high on $\overline{SS}$ at the rising edge of the CK clock has its effect on the output drivers immediately. $\overline{SW}$ low deselects the output drivers immediately (on the same cycle). Output selecting via a low on $\overline{SS}$ and high on $\overline{SW}$ at a rising CK clock has its effect on the output drivers at t_{KLQX}. Output drive is also controlled directly by output enable, $\overline{G}$. $\overline{G}$ is an asynchronous input. No clock edges are required to enable or disable the output with $\overline{G}$.

Output data will be valid the later of t_{GLQV}, t_{KHQV}, or t_{KLQV}. Outputs will begin driving at t_{KLQX1}. Outputs will hold previous data until t_{KLQX} or t_{GHQX}.

WRITE AND BYTE WRITE FUNCTIONS

Note that in the following discussion the term "byte" refers to nine bits of the RAM I/O bus. In all cases, the timing parameters described for synchronous write input ($\overline{SW}$) apply to each of the byte write enable inputs ($\overline{SBa}$, $\overline{SBb}$, etc.).

Byte write enable inputs have no effect on read cycles. This allows the system designer not interested in performing byte writes to connect the byte enable inputs to active low (V_{SS}). Reads of all bytes proceed normally and write cycles, activated via a low on $\overline{SW}$, and the rising edge of the CK clock, write the entire RAM I/O width. This way the designer is spared having to drive multiple write input buffer loads.

Byte writes are performed using the byte write enable inputs in conjunction with the synchronous write input ($\overline{SW}$). It is important to note that writing any one byte will inhibit a read of all bytes at the current address. The RAM cannot simultaneously read one byte and write another at the same address. A write cycle initiated with none of the byte write enable inputs active is neither a read or a write. No write will occur, but the outputs will be deselected as in a normal write cycle.

LATE WRITE

The write address is sampled on the first rising edge of clock and write data is sampled on the following rising edge.

The late write feature is implemented with single stage write buffering. Write buffering is transparent to the user. A comparator monitors the address bus and, when necessary, routes buffer contents to the outputs to assure coherent operation. This occurs in all cases whether there is a byte write or a full word is written.

POWER UP AND INITIALIZATION

Please note, per the Absolute Maximum Ratings table, V_{DDQ} is not to exceed V_{DD} + 0.5 V, whatever the instantaneous value of V_{DD}. Once supplies have reached specification levels, a minimum dwell of 1.0 µs with CK clock inputs cycling is required before beginning normal operations.

3

SERIAL BOUNDARY SCAN TEST ACCESS PORT OPERATION

OVERVIEW

The serial boundary scan test access port (TAP) on this RAM is designed to operate in a manner consistent with IEEE Standard 1149.1–1990 (commonly referred to as JTAG), but does not implement all of the functions required for 1149.1 compliance. Certain functions have been modified or eliminated because their implementation places extra delays in the RAMs critical speed path. Nevertheless, the RAM supports the standard TAP controller architecture. (The TAP controller is the state machine that controls the TAPs operation) and can be expected to function in a manner that does not conflict with the operation of devices with Standard 1149.1 compliant TAPs. The TAP operates using conventional JEDEC Standard 8–1B Low Voltage (3.3 V) TTL / CMOS logic level signaling.

DISABLING THE TEST ACCESS PORT

It is possible to use this device without utilizing the TAP. To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid level inputs. TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a 1 k resistor. TDO should be left unconnected.

3

TAP DC OPERATING CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Parameter	Symbol	Min	Max	Unit	Note
Logic Input Logic High	$V_{IH}1$	2.0	V_{DD} + 0.3	V	
Logic Input Logic Low	$V_{IL}1$	– 0.3	0.8	V	
Logic Input Leakage Current	I_{lkg}	—	± 5	µA	1
CMOS Output Logic Low	$V_{OL}1$	—	0.2	V	2
CMOS Output Logic High	$V_{OH}1$	V_{DD} – 0.2	—	V	3
TTL Output Logic Low	$V_{OL}2$	—	0.4	V	4
TTL Output Logic High	$V_{OH}2$	2.4	—	V	5

NOTES:

1. 0 V ≤ V_{in} ≤ V_{DDQ} for all logic input pins.
2. $I_{OL}1$ ≤ 100 µA @ V_{OL} = 0.2 V. Sampled, not 100% tested.
3. $|I_{OH}1|$ ≤ 100 µA @ V_{DDQ} – 0.2 V. Sampled, not 100% tested.
4. $I_{OL}2$ ≤ 8 mA @ V_{OL} = 0.4 V
5. $|I_{OH}2|$ ≤ 8 mA @ V_{OH} = 2.4 V

TAP AC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V

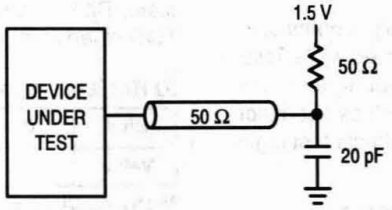
Output Test Load ..... 50 Ω Parallel Terminated T–line with 20 pF Receiver Input Capacitance
Test Load Termination Supply Voltage (V_T) ..... 1.5 V

TAP CONTROLLER TIMING

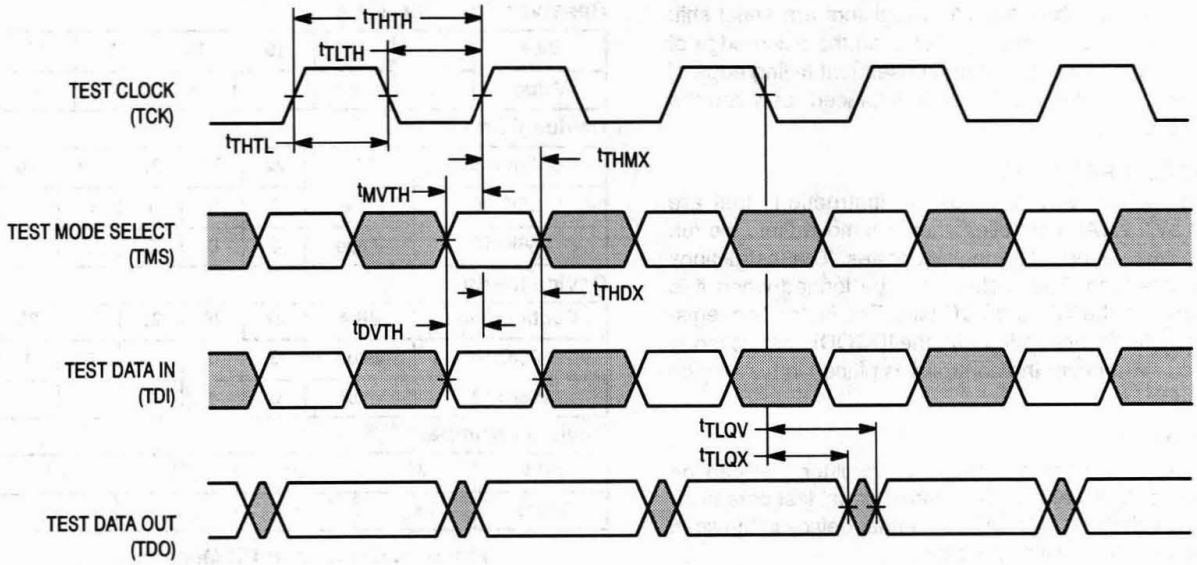
Parameter	Symbol	Min	Max	Unit	Notes
Cycle Time	t_{THTH}	100	—	ns	
Clock High Time	t_{THTL}	40	—	ns	
Clock Low Time	t_{TLTH}	40	—	ns	
TMS Setup	t_{MVTH}	10	—	ns	
TMS Hold	t_{THMX}	10	—	ns	
TDI Valid to TCK High	t_{DVTH}	10	—	ns	
TCK High to TDI Don't Care	t_{THDX}	10	—	ns	
Capture Setup	t_{CS}	10	—	ns	1
Capture Hold	t_{CH}	10	—	ns	1
TCK Low to TDO Unknown	t_{TLQX}	0	—	ns	
TCK Low to TDO Valid	t_{TLOV}	—	20	ns	

NOTES:
1. t_{CS} + t_{CH} defines the minimum pause in RAM I/O pad transitions to assure accurate pad data capture.

AC TEST LOAD



TAP CONTROLLER TIMING DIAGRAM



TEST ACCESS PORT PINS

TCK – TEST CLOCK (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

TMS – TEST MODE SELECT (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.

TDI – TEST DATA IN (INPUT)

The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (refer to Figure 5 TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.

TDO – TEST DATA OUT (OUTPUT)

Output that is active depending on the state of the TAP state machine (refer to Figure 5 TAP Controller State Diagram). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

TRST – TAP RESET

This device does not have a TRST pin. TRST is optional in **IEEE 1149.1.** The test–logic reset state is entered while TMS is held high for five rising edges of TCK. Power on reset circuitry is included internally. This type of reset does not affect the operation of the system logic. The reset affects test logic only.

TEST ACCESS PORT REGISTERS

OVERVIEW

The various TAP registers are selected (one at a time) via the sequences of ones and zeros input to the TMS pin as the TCK is strobed. Each of the TAPs registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on subsequent falling edge of TCK. When a register is selected it is "placed" between the TDI and TDO pins.

INSTRUCTION REGISTER

The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run test/idle or the various data register states. The instructions are three bits long. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power–up or whenever the controller is placed in test–logic–reset state.

BYPASS REGISTER

The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.

BOUNDARY SCAN REGISTER

The boundary scan register is identical in length to the number of active input and I/O connections on the RAM (not counting the TAP pins). This also includes a number of place holder locations (always set to a logic 1) reserved for density upgrade address pins. There are a total of 70 bits in the case of the x36 device and 51 bits in the case of the x18 device. The boundary scan register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture–DR state and then is placed between the TDI and TDO pins when the controller is moved to shift–DR state. Several TAP instructions can be used to activate the boundary scan register.

The Bump/Bit Scan Order tables describe which device bump connects to each boundary scan register location. The first column defines the bit's position in the boundary scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the input or I/O at the bump and the third column is the bump number.

IDENTIFICATION (ID) REGISTER

The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture–DR state with the IDCODE command loaded in the instruction register. The code is loaded from a 32 bit on–chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into shift–DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Presence Indicator

Bit #	0
Value	1

Motorola JEDEC ID Code (Compressed Format, per IEEE Standard 1149.1 – 1990

Bit #	11	10	9	8	7	6	5	4	3	2	1
Value	0	0	0	0	0	0	0	1	1	1	0

Reserved For Future Use

Bit #	17	16	15	14	13	12
Value	x	x	x	x	x	x

Device Width

Configuration	Bit #	22	21	20	19	18
128Kx36	Value	0	0	1	0	0
256Kx18	Value	0	0	0	1	1

Device Depth

Configuration	Bit #	27	26	25	24	23
128Kx36	Value	0	0	1	0	1
256Kx18	Value	0	0	1	1	0

Revision Number

Bit #	31	30	29	28
Value	x	x	x	x

Figure 4. ID Register Bit Meanings

MCM69L738 Bump/Bit Scan Order

BIT #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	SA	3B
2	SA	4P		37	NC	2B
3	SA	4T		38	SA	3A
4	SA	6R		39	SA	3C
5	SA	5T		40	SA	2C
6	ZZ	7T		41	SA	2A
7	DQa	6P		42	DQc	2D
8	DQa	7P		43	DQc	1D
9	DQa	6N		44	DQc	2E
10	DQa	7N		45	DQc	1E
11	DQa	6M		46	DQc	2F
12	DQa	6L		47	DQc	2G
13	DQa	7L		48	DQc	1G
14	DQa	6K		49	DQc	2H
15	DQa	7K		50	DQc	1H
16	$\overline{SBa}$	5L		51	$\overline{SBc}$	3G
17	$\overline{CK}$	4L		52	NC	4D
18	CK	4K		53	$\overline{SS}$	4E
19	$\overline{G}$	4F		54	NC	4G
20	$\overline{SBb}$	5G		55	NC	4H
21	DQb	7H		56	$\overline{SW}$	4M
22	DQb	6H		57	$\overline{SBd}$	3L
23	DQb	7G		58	DQd	1K
24	DQb	6G		59	DQd	2K
25	DQb	6F		60	DQd	1L
26	DQb	7E		61	DQd	2L
27	DQb	6E		62	DQd	2M
28	DQb	7D		63	DQd	1N
29	DQb	6D		64	DQd	2N
30	SA	6A		65	DQd	1P
31	SA	6C		66	DQd	2P
32	SA	5C		67	SA	3T
33	SA	5A		68	SA	2R
34	NC	6B		69	SA	4N
35	SA	5B		70	M1	3R

MCM69L820 Bump/Bit Scan Order

Bit #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	$\overline{SBb}$	3G
2	SA	6T		37	NC	4D
3	SA	4P		38	$\overline{SS}$	4E
4	SA	6R		39	NC	4G
5	SA	5T		40	NC	4H
6	ZZ	7T		41	$\overline{SW}$	4M
7	DQa	7P		42	DQb	2K
8	DQa	6N		43	DQb	1L
9	DQa	6L		44	DQb	2M
10	DQa	7K		45	DQb	1N
11	$\overline{SBa}$	5L		46	DQb	2P
12	$\overline{CK}$	4L		47	SA	3T
13	CK	4K		48	SA	2R
14	$\overline{G}$	4F		49	SA	4N
15	DQa	6H		50	SA	2T
16	DQa	7G		51	M1	3R
17	DQa	6F				
18	DQa	7E				
19	DQa	6D				
20	SA	6A				
21	SA	6C				
22	SA	5C				
23	SA	5A				
24	NC	6B				
25	SA	5B				
26	SA	3B				
27	NC	2B				
28	SA	3A				
29	SA	3C				
30	SA	2C				
31	SA	2A				
32	DQb	1D				
33	DQb	2E				
34	DQb	2G				
35	DQb	1H				

NOTES:

1. The NC pads listed in this table are indeed no connects, but are represented in the boundary scan register by a "place holder" bit that is forced to logic 1. These pads are reserved for use as address inputs on higher density RAMs that follow this pad out and scan order standard.
2. CK, $\overline{CK}$, are sampled individually. $\overline{CK}$ is not simply a forced complement of the CK input. In scan mode these differential inputs are referenced to each other.
3. M1 and M2 are not ordinary inputs and may not respond to standard I/O logic levels. M1 and M2 must be driven to within 100 mV of a V_{DD} or V_{SS} supply rail to ensure consistent results.
4. ZZ must remain at V_{IL} during boundary scan to ensure consistent results.

TAP Controller Instruction Set

OVERVIEW

There are two classes of instructions defined in the Standard 1149.1–1990; the standard (public) instructions, and device specific (private) instructions. Some public instructions, are mandatory for 1149.1 compliance. Optional public instructions must be implemented in prescribed ways.

Although the TAP controller in this device follows the 1149.1 conventions, it is not 1194.1 compliant because some of the mandatory instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads, but cannot be used to load address, data or control signals into the RAM or to preload the I/O buffers. In other words, the device will not perform Standard 1149.1 EXTEST, INTEST or the preload portion of the SAMPLE / PRELOAD command.

When the TAP controller is placed in capture–IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the shift–IR state the instruction register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to update–IR state. The TAP instruction sets for this device are listed in the following tables.

STANDARD (PUBLIC) INSTRUCTIONS

BYPASS

The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift–DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

Sample/preload is a Standard 1149.1 mandatory public instruction. When the sample / preload instruction is loaded in the Instruction register, moving the TAP controller into the capture–DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set–up plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register.

Moving the controller to shift–DR state then places the boundary scan register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the update–DR state with the SAMPLE / PRELOAD instruction loaded in the instruction register has the same effect as the pause–DR command. This functionality is not Standard 1149.1 compliant.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic 0s. EXTEST is not implemented in this device. Therefore this device is not 1149.1 compliant. Nevertheless, this RAMs TAP does respond to an all zeros instruction, as follows. With the EXTEST (000) instruction loaded in the instruction register the RAM responds just as it does in response to the SAMPLE / PRELOAD instruction described above, except the RAM outputs are forced to high–Z any time the instruction is loaded.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture–DR mode and places the ID register between the TDI and TDO pins in shift–DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test–logic–reset state.

THE DEVICE SPECIFIC (PUBLIC) INSTRUCTION

SAMPLE–Z

If the SAMPLE–Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high–Z) and the boundary scan register is connected between TDI and TDO when the TAP controller. is moved to the shift–DR state.

THE DEVICE SPECIFIC (PRIVATE) INSTRUCTION

NOOP

Do not use these instructions; they are reserved for future use.

STANDARD (PUBLIC) INSTRUCTION CODES

Instruction	Code*	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM outputs to High–Z state. *NOT 1149.1 COMPLIANT*
IDCODE	001**	Preloads ID register and places it between TDI and TDO. Does not affect RAM operation.
SAMPLE / PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect RAM operation. Does not implement 1149.1 Preload function. * NOT 1149.1 COMPLIANT *
BYPASS	111	Places bypass register between TDI and TDO. Does not affect RAM operation.
SAMPLE–Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM output drivers to High–Z.

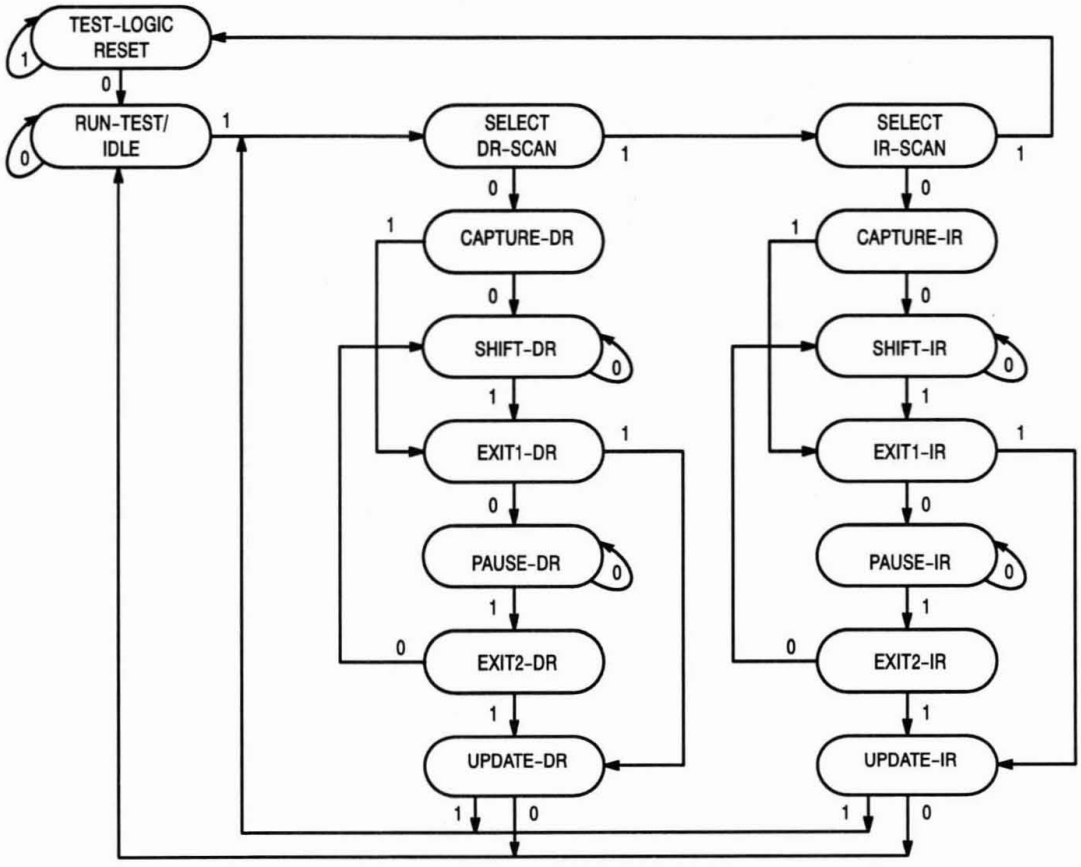
* Instruction codes expressed in binary, MSB on left, LSB on right.
** Default instruction automatically loaded at power–up and in test–logic–reset state.

3

STANDARD (PRIVATE) INSTRUCTION CODES

Instruction	Code*	Description
NO OP	011	Do not use these instructions; they are reserved for future use.
NO OP	101	Do not use these instructions; they are reserved for future use.
NO OP	110	Do not use these instructions; they are reserved for future use.

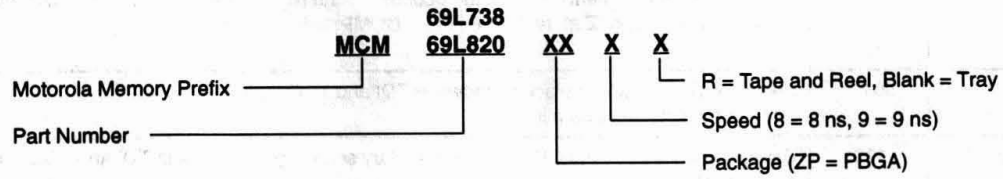
* Instruction codes expressed in binary, MSB on left, LSB on right.



NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 5. TAP Controller State Diagram

ORDERING INFORMATION
(Order by Full Part Number)



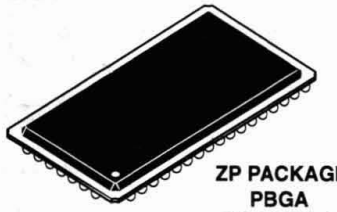
Full Part Numbers —	MCM69L738ZP8	MCM69L738ZP9
	MCM69L820ZP8	MCM69L820ZP9
	MCM69L738ZP8R	MCM69L738ZP9R
	MCM69L820ZP8R	MCM69L820ZP9R

3

MCM69L738A
MCM69L820A

Advance Information

4M Late Write 2.5 V I/O



ZP PACKAGE
PBGA
CASE 999–01

The MCM69L738A/820A is a 4 megabit synchronous late write fast static RAM designed to provide high performance in secondary cache and ATM switch, Telecom, and other high speed memory applications. The MCM69L820A organized as 256K words by 18 bits, and the MCM69L738A organized as 128K words by 36 bits wide are fabricated in Motorola's high performance silicon gate BiCMOS technology.

The differential CK clock inputs control the timing of read/write operations of the RAM. At the rising edge of the CK clock all addresses, write enables, and synchronous selects are registered. An internal buffer and special logic enable the memory to accept write data on the rising edge of the CK clock a cycle after address and control signals. Read data is available at the falling edge of the CK clock.

The RAM use 2.5 V inputs and outputs.

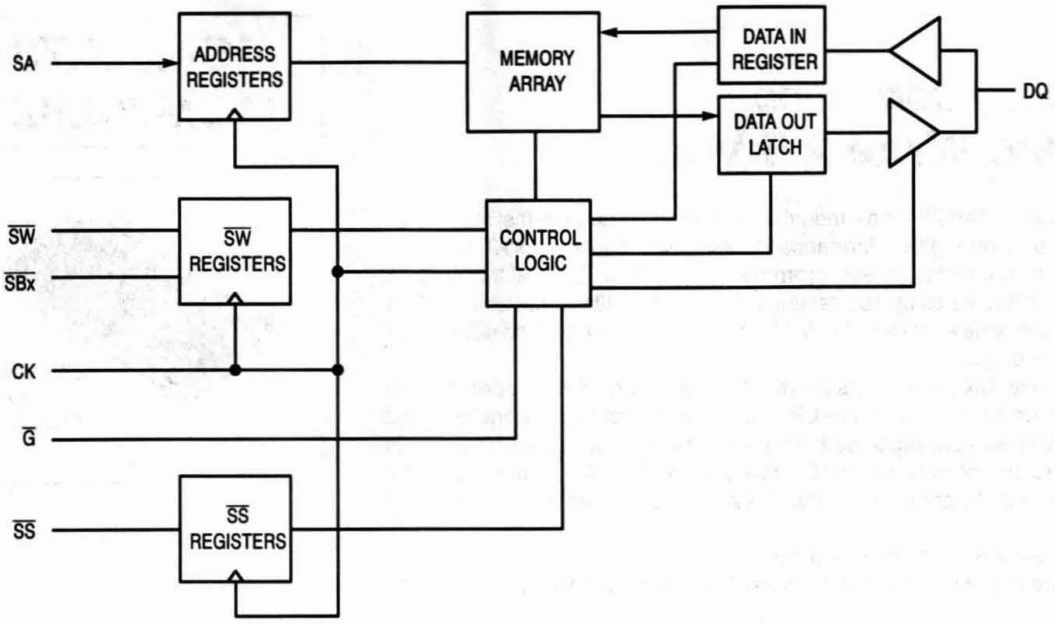
The synchronous write and byte enables allow writing to individual bytes or the entire word.

- Byte Write Control
- 3.3 V + 10%, – 5% Operation
- 2.5 V I/O (V_{DDQ})
- Register to Latch Synchronous Operation
- Asynchronous Output Enable
- Boundary Scan (JTAG) IEEE 1149.1 Compatible
- Differential Clock Inputs
- Optional x 18 or x 36 organization
- MCM69L738A/820A–7.5 = 7.5 ns
  MCM69L738A/820A–8.5 = 8.5 ns
  MCM69L738A/820A–9.5 = 9.5 ns
  MCM69L738A/820A–10.5 = 10.5 ns
- 119 Bump, 50 mil (1.27 mm) Pitch, 14 mm x 22 mm Plastic Ball Grid Array (PBGA) Package

This document contains information on a new product. Specifications and information herein are subject to change without notice.

4/3/97

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENTS

TOP VIEW

MCM69L738A

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	SA	NC	SA	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
E	DQc	DQc	V_{SS}	$\overline{SS}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{G}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{SBc}$	NC	$\overline{SBb}$	DQb	DQb
H	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CK	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{SBd}$	$\overline{CK}$	$\overline{SBa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{SW}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
P	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
R	NC	SA	V_{DD}	V_{DD}	V_{SS}	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69L820A

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	SA	NC	SA	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQb	NC	V_{SS}	NC	V_{SS}	DQa	NC
E	NC	DQb	V_{SS}	$\overline{SS}$	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	$\overline{SBb}$	NC	V_{SS}	NC	DQa
H	DQb	NC	V_{SS}	NC	V_{SS}	DQa	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	CK	V_{SS}	NC	DQa
L	DQb	NC	V_{SS}	$\overline{CK}$	$\overline{SBa}$	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{SW}$	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	SA	V_{SS}	DQa	NC
P	NC	DQb	V_{SS}	SA	V_{SS}	NC	DQa
R	NC	SA	V_{DD}	V_{DD}	V_{SS}	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69L738A PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6K, 7K, 6L, 7L, 6M, 6N, 7N, 6P, 7P (b) 6D, 7D, 6E, 7E, 6F, 6G, 7G, 6H, 7H (c) 1D, 2D, 1E, 2E, 2F, 1G, 2G, 1H, 2H (d) 1K, 2K, 1L, 2L, 2M, 1N, 2N, 1P, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 3T, 4T, 5T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 5G, 3G, 3L (a), (b), (c), (d)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
7T	ZZ	Input	Enables sleep mode.
4C, 2J, 4J, 6J, 4R, 3R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 3H, 5H, 3K, 5K, 3M, 5M, 3N, 5N, 3P, 5P, 5R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 4B, 6B, 7B, 1C, 7C, 4D, 4G, 4H, 3J, 5J, 1R, 7R, 1T, 2T, 6T, 6U	NC	—	No Connection: There is no connection to the chip. Note: 3J and 5J are tied common.

MCM69L820A PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6D, 7E, 6F, 7G, 6H, 7K, 6L, 6N, 7P (b) 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 2T, 3T, 5T, 6T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 3G (a), (b)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
7T	ZZ	Input	Enables sleep mode.
4C, 2J, 4J, 6J, 4R, 3R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P, 5R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 4B, 6B, 7B, 1C, 7C, 2D, 4D, 7D, 1E, 6E, 2F, 1G, 4G, 6G, 2H, 4H, 7H, 3J, 5J, 1K, 6K, 2L, 7L, 6M, 2N, 7N, 1P, 6P, 1R, 7R, 1T, 4T, 6U	NC	—	No Connection: There is no connection to the chip. Note: 3J and 5J are tied common.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS}, See Note 1)

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Output Supply Voltage	V_{DDQ}	– 0.5 to V_{DD} + 0.5	V
Voltage On Any Pin	V_{in}	– 0.5 to V_{DD} + 0.5	V
Input Current (per I/O)	I_{in}	± 50	mA
Output Current (per I/O)	I_{out}	± 70	mA
Power Dissipation (See Note 2)	P_D	—	W
Operating Temperature	T_A	0 to + 70	°C
Temperature Under Bias	T_{bias}	–10 to + 85	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability will be dependent upon package characteristics and use environment. See enclosed thermal impedance data.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

3

PBGA PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (Still Air)		$R_{\theta JA}$	53	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Single Layer Board	$R_{\theta JA}$	38	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Four Layer Board	$R_{\theta JA}$	22	°C/W	
Junction to Board (Bottom)		$R_{\theta JB}$	14	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	5	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (See Notes 1 through 4)

Parameter	Symbol	Min	Typical –7.5	Typical –8.5	Typical –9.5	Typical –10.5	Max	Unit	Notes
Core Power Supply Voltage	V_{DD}	3.15	—	—	—	—	3.6	V	
Output Driver Supply Voltage	V_{DDQ}	2.3	—	—	—	—	2.7	V	
Active Power Supply Current (x18) (x36)	I_{DD1}	— —	330 390	320 370	300 350	280 330	490 550	mA	5
Quiescent Active Power Supply Current	I_{DD2}	—	180	180	180	180	250	mA	6, 10
Active Standby Power Supply Current	I_{SB1}	—	170	170	170	170	250	mA	7
Quiescent Standby Power Supply Current	I_{SB2}	—	150	150	150	150	230	mA	8, 10
Sleep Mode Power Supply Current	I_{SB3}	—	30	30	30	30	50	mA	9, 10

NOTES:
1. All data sheet parameters specified to full range of V_{DD} unless otherwise noted. All voltages are referenced to voltage applied to V_{SS} bumps.
2. Supply voltage applied to V_{DD} connections.
3. Supply voltage applied to V_{DDQ} connections.
4. All power supply currents measured with outputs open or deselected.
5. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered active, 50% read cycles.
6. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered active.
7. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered inactive.
8. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered inactive. ZZ low.
9. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered inactive, ZZ high.
10. 200 mV ≥ V_{in} ≥ V_{DDQ} – 200 mV.

DC INPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
DC Input Logic High	V_{IH} (dc)	1.7	V_{DD} + 0.3	V	
DC Input Logic Low	V_{IL} (dc)	– 0.3	0.7	V	1
Input Leakage Current	I_{lkg}	—	± 5	µA	2
Clock Input Leakage Current	I_{clkg}	—	± 8	µA	2
Clock Input Signal Voltage	V_{in}	– 0.3	V_{DD} + 0.3	V	
Clock Input Differential Voltage	V_{DIF}(dc)	0.2	V_{DD} + 0.6	V	3
Clock Input Common Mode Voltage Range (See Figure 3)	V_{CM}(dc)	1.1	2.1	V	4

NOTES:
1. Inputs may undershoot to – 0.5 V (peak) for up to 20% t_{KHKH} (e.g., 2 ns at a clock cycle time of 10 ns).
2. 0 V ≤ V_{in} ≤ V_{DD} for all pins.
3. Minimum instantaneous differential input voltage required for differential input clock operation.
4. Maximum rejectable common mode input voltage variation.

DC OUTPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
Output Leakage Current	I_{lkg}	–1.0	1.0	µA	
Output Low Voltage	V_{OL}	—	0.7	V	1
Output High Voltage	V_{OH}	1.7	—	V	2

NOTES:
1. I_{OL} = 8.0 mA.
2. I_{OH} = – 8.0 mA.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, 0°C ≤ T_A ≤ 70°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	5	5	pF
Input/Output Capacitance	$C_{I/O}$	6	8	pF
CK, $\overline{CK}$ Capacitance	C_{CK}	6	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

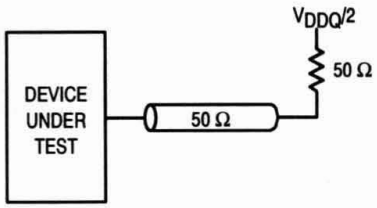
(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 2.5 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.25 V
Output Timing Reference Level ..... 1.25 V
Clock Input Timing Reference Level ..... Differential Cross–Point
Clock Input Pulse Level ..... 1.8 V to 2.1 V

READ/WRITE CYCLE TIMING (See Notes 2 and 3)

Parameter	Symbol	MCM69L536–7.5 MCM69L618–7.5		MCM69L536–8.5 MCM69L618–8.5		MCM69L536–9.5 MCM69L618–9.5		MCM69L536–10.5 MCM69L618–10.5		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	7	—	8	—	9	—	10	—	ns	
Clock High Pulse Width	t_{KHKL}	2.8	—	3.2	—	3.6	—	4	—	ns	
Clock Low Pulse Width	t_{KLKH}	2.8	—	3.2	—	3.6	—	4	—	ns	
Clock High to Output Valid	t_{KHQV}	—	7.5	—	8.5	—	9.5	—	10.5	ns	
Clock Low to Output Valid	t_{KLQV}	—	3.5	—	4	—	4	—	4	ns	
Clock Low to Output Hold	t_{KLQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	
Clock Low to Output Low–Z	t_{KLQX1}	1	—	1	—	1	—	1	—	ns	1
Clock High to Output High–Z	t_{KHQZ}	—	3.5	—	4	—	4	—	4	ns	
Output Enable Low to Output Low–Z	t_{GLQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	1
Output Enable Low to Output Valid	t_{GLQV}	—	3.5	—	4	—	4	—	4	ns	
Output Enable to Output Hold	t_{GHQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	
Output Enable High to Output High–Z	t_{GHQZ}	—	3.5	—	4	—	4	—	4	ns	1
Setup Times: Address, Data In, Chip Select, Write Enable	t_{AVKH}, t_{DVKH}, t_{SVKH}, t_{WVKH}	0.5	—	0.5	—	0.5	—	0.5	—	ns	
Hold Times: Address, Data In, Chip Select, Write Enable	t_{KHAX}, t_{KHDX}, t_{KHSX}, t_{KHWX}	1	—	1	—	1	—	1	—	ns	

NOTES:
1. Tested per AC Test Load diagram. See Figure 1.
2. Measured at ± 200 mV from steady state.
3. In no case may control input signals (e.g., $\overline{SS}$) be operated with pulse widths less than the minimum clock input pulse width specifications (e.g., t_{KHKL}) or at frequencies that exceed the applied K clock frequency.



TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Figure 1. AC Test Load

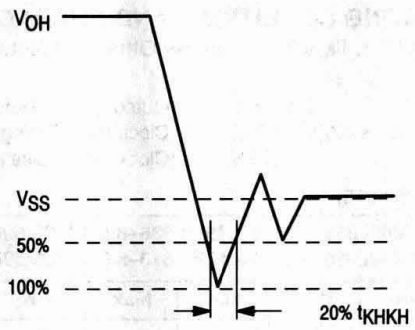
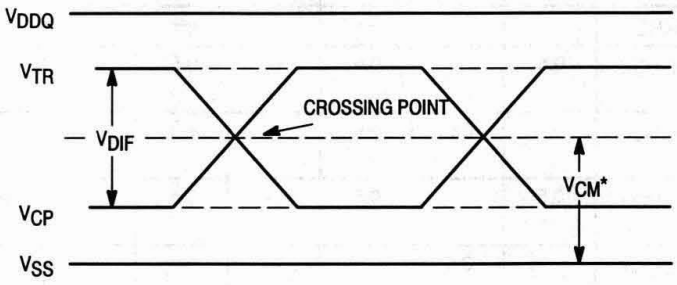


Figure 2. Undershoot Voltage

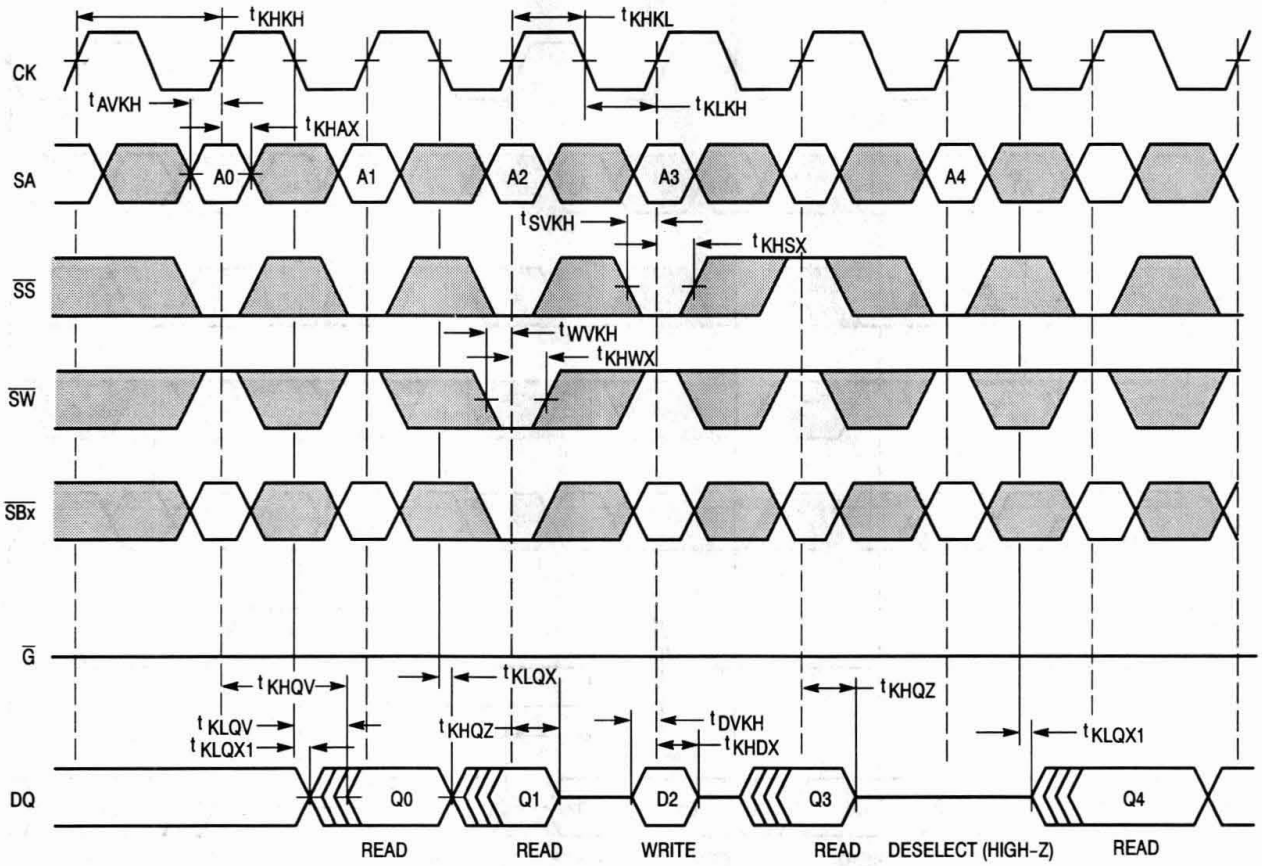
3



*V_{CM}, the Common Mode Input Voltage, equals $V_{TR} - ((V_{TR} - V_{CP})/2)$.

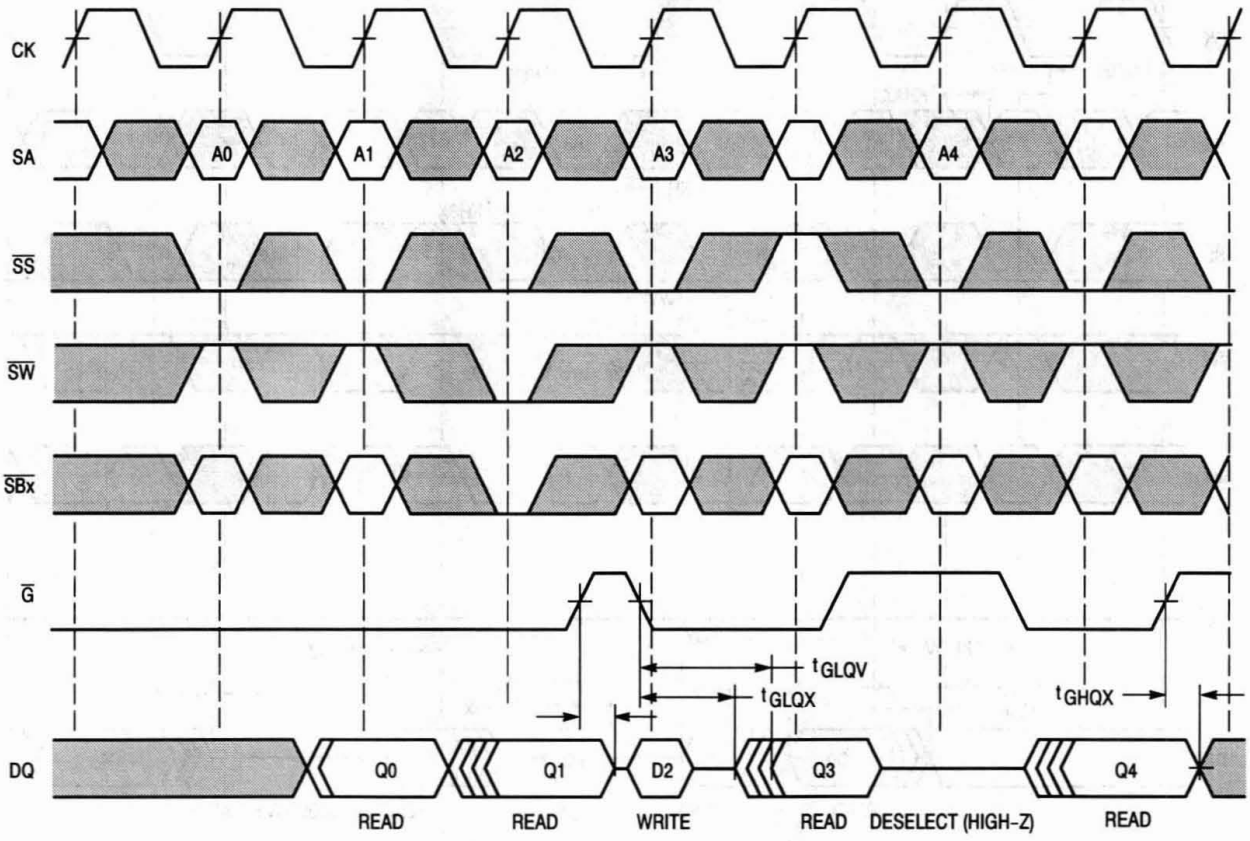
Figure 3. Differential Inputs/Common Mode Input Voltage

REGISTER LATCH READ–WRITE–READ CYCLES



3

REGISTER LATCH READ–WRITE–READ CYCLES
($\overline{G}$ Controlled)



FUNCTIONAL OPERATION

READ AND WRITE OPERATIONS

All control signals except $\overline{G}$ are registered on the rising edge of the CK clock. These signals must meet the setup and hold times shown in the AC Characteristics table. On the falling edge of the current cycle, the output latch becomes transparent and data is available. The output data is latched on the rising edge of the next clock. The output data is available at the output at t_{KLQV} or t_{KHQV}, whichever is later. t_{KHQV} is the internal latency of the device. During this same cycle a new read address can be applied to the address pins.

A write cycle can occur on the next cycle as long as t_{KLQX} and t_{DVKH} are met. Read cycles may follow write cycles immediately.

$\overline{G}$, $\overline{SS}$, and $\overline{SW}$ control output drive. Chip deselect via a high on $\overline{SS}$ at the rising edge of the CK clock has its effect on the output drivers immediately. $\overline{SW}$ low deselects the output drivers immediately (on the same cycle). Output selecting via a low on $\overline{SS}$ and high on $\overline{SW}$ at a rising CK clock has its effect on the output drivers at t_{KLQX}. Output drive is also controlled directly by output enable, $\overline{G}$. $\overline{G}$ is an asynchronous input. No clock edges are required to enable or disable the output with $\overline{G}$.

Output data will be valid the later of t_{GLQV}, t_{KHQV}, or t_{KLQV}. Outputs will begin driving at t_{KLQX1}. Outputs will hold previous data until t_{KLQX} or t_{GHQX}.

WRITE AND BYTE WRITE FUNCTIONS

Note that in the following discussion the term "byte" refers to nine bits of the RAM I/O bus. In all cases, the timing parameters described for synchronous write input ($\overline{SW}$) apply to each of the byte write enable inputs ($\overline{SBa}$, $\overline{SBb}$, etc.).

Byte write enable inputs have no effect on read cycles. This allows the system designer not interested in performing byte writes to connect the byte enable inputs to active low (V_{SS}). Reads of all bytes proceed normally and write cycles, activated via a low on $\overline{SW}$, and the rising edge of the CK clock, write the entire RAM I/O width. This way the designer is spared having to drive multiple write input buffer loads.

Byte writes are performed using the byte write enable inputs in conjunction with the synchronous write input ($\overline{SW}$). It is important to note that writing any one byte will inhibit a read of all bytes at the current address. The RAM cannot simultaneously read one byte and write another at the same address. A write cycle initiated with none of the byte write enable inputs active is neither a read or a write. No write will occur, but the outputs will be deselected as in a normal write cycle.

LATE WRITE

The write address is sampled on the first rising edge of clock and write data is sampled on the following rising edge.

The late write feature is implemented with single stage write buffering. Write buffering is transparent to the user. A comparator monitors the address bus and, when necessary, routes buffer contents to the outputs to assure coherent operation. This occurs in all cases whether there is a byte write or a full word is written.

POWER UP AND INITIALIZATION

Please note, per the Absolute Maximum Ratings table, V_{DDQ} is not to exceed V_{DD} + 0.5 V, whatever the instantaneous value of V_{DD}. Once supplies have reached specification levels, a minimum dwell of 1.0 µs with CK clock inputs cycling is required before beginning normal operations.

3

SERIAL BOUNDARY SCAN TEST ACCESS PORT OPERATION

OVERVIEW

The serial boundary scan test access port (TAP) on this RAM is designed to operate in a manner consistent with IEEE Standard 1149.1–1990 (commonly referred to as JTAG), but does not implement all of the functions required for 1149.1 compliance. Certain functions have been modified or eliminated because their implementation places extra delays in the RAMs critical speed path. Nevertheless, the RAM supports the standard TAP controller architecture. (The TAP controller is the state machine that controls the TAPs operation) and can be expected to function in a manner that does not conflict with the operation of devices with Standard 1149.1 compliant TAPs. The TAP operates using conventional JEDEC Standard 8–1B Low Voltage (3.3 V) TTL / CMOS logic level signaling.

DISABLING THE TEST ACCESS PORT

It is possible to use this device without utilizing the TAP. To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid level inputs. TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a 1 k resistor. TDO should be left unconnected.

3

TAP DC OPERATING CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Parameter	Symbol	Min	Max	Unit	Note
Logic Input Logic High	$V_{IH}1$	2.0	V_{DD} + 0.3	V	
Logic Input Logic Low	$V_{IL}1$	– 0.3	0.8	V	
Logic Input Leakage Current	I_{lkg}	—	± 5	µA	1
CMOS Output Logic Low	$V_{OL}1$	—	0.2	V	2
CMOS Output Logic High	$V_{OH}1$	V_{DD} – 0.2	—	V	3
TTL Output Logic Low	$V_{OL}2$	—	0.4	V	4
TTL Output Logic High	$V_{OH}2$	2.4	—	V	5

NOTES:
1. 0 V ≤ V_{in} ≤ V_{DDQ} for all logic input pins.
2. $I_{OL}1$ ≤ 100 µA @ V_{OL} = 0.2 V. Sampled, not 100% tested.
3. $I_{OH}1$ ≤ 100 µA @ V_{DDQ} – 0.2 V. Sampled, not 100% tested.
4. $I_{OL}2$ ≤ 8 mA @ V_{OL} = 0.4 V.
5. $I_{OH}2$ ≤ 8 mA @ V_{OH} = 2.4 V.

TAP AC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V

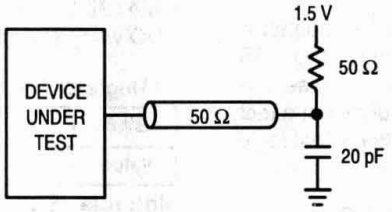
Output Test Load ..... 50 Ω Parallel Terminated T–line with 20 pF Receiver Input Capacitance
Test Load Termination Supply Voltage (V_T) ..... 1.5 V

TAP CONTROLLER TIMING

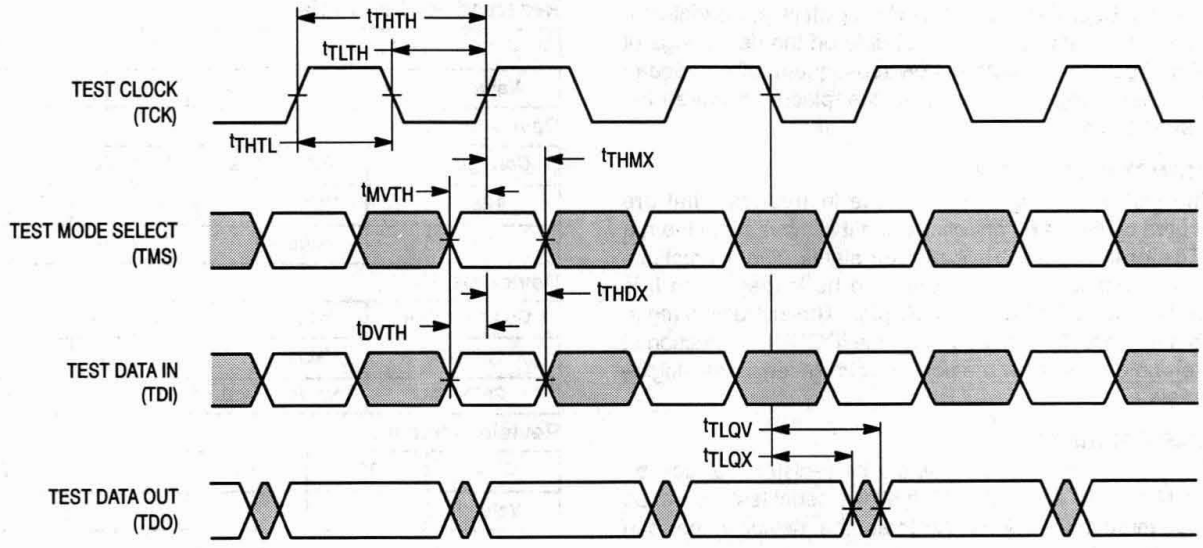
Parameter	Symbol	Min	Max	Unit	Notes
Cycle Time	t_{THTH}	100	—	ns	
Clock High Time	t_{THTL}	40	—	ns	
Clock Low Time	t_{TLTH}	40	—	ns	
TMS Setup	t_{MVTH}	10	—	ns	
TMS Hold	t_{THMX}	10	—	ns	
TDI Valid to TCK High	t_{DVTH}	10	—	ns	
TCK High to TDI Don't Care	t_{THDX}	10	—	ns	
Capture Setup	t_{CS}	10	—	ns	1
Capture Hold	t_{CH}	10	—	ns	1
TCK Low to TDO Unknown	t_{TLQX}	0	—	ns	
TCK Low to TDO Valid	t_{TLOV}	—	20	ns	

NOTES:
1. t_{CS} + t_{CH} defines the minimum pause in RAM I/O pad transitions to assure accurate pad data capture.

AC TEST LOAD



TAP CONTROLLER TIMING DIAGRAM



TEST ACCESS PORT PINS

TCK – TEST CLOCK (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

TMS – TEST MODE SELECT (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.

TDI – TEST DATA IN (INPUT)

The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (refer to Figure 5 TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.

TDO – TEST DATA OUT (OUTPUT)

Output that is active depending on the state of the TAP state machine (refer to Figure 5 TAP Controller State Diagram). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

TRST – TAP RESET

This device does not have a TRST pin. TRST is optional in **IEEE 1149.1.** The test–logic reset state is entered while TMS is held high for five rising edges of TCK. Power on reset circuitry is included internally. This type of reset does not affect the operation of the system logic. The reset affects test logic only.

TEST ACCESS PORT REGISTERS

OVERVIEW

The various TAP registers are selected (one at a time) via the sequences of ones and zeros input to the TMS pin as the TCK is strobed. Each of the TAPs registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on subsequent falling edge of TCK. When a register is selected it is "placed" between the TDI and TDO pins.

INSTRUCTION REGISTER

The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run test/idle or the various data register states. The instructions are three bits long. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power–up or whenever the controller is placed in test–logic–reset state.

BYPASS REGISTER

The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.

BOUNDARY SCAN REGISTER

The boundary scan register is identical in length to the number of active input and I/O connections on the RAM (not counting the TAP pins). This also includes a number of place holder locations (always set to a logic 1) reserved for density upgrade address pins. There are a total of 70 bits in the case of the x36 device and 51 bits in the case of the x18 device. The boundary scan register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture–DR state and then is placed between the TDI and TDO pins when the controller is moved to shift–DR state. Several TAP instructions can be used to activate the boundary scan register.

The Bump/Bit Scan Order tables describe which device bump connects to each boundary scan register location. The first column defines the bit's position in the boundary scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the input or I/O at the bump and the third column is the bump number.

IDENTIFICATION (ID) REGISTER

The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture–DR state with the IDCODE command loaded in the instruction register. The code is loaded from a 32 bit on–chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into shift–DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Presence Indicator

Bit #	0
Value	1

Motorola JEDEC ID Code (Compressed Format, per IEEE Standard 1149.1 – 1990

Bit #	11	10	9	8	7	6	5	4	3	2	1
Value	0	0	0	0	0	0	0	1	1	1	0

Reserved For Future Use

Bit #	17	16	15	14	13	12
Value	x	x	x	x	x	x

Device Width

Configuration	Bit #	22	21	20	19	18
128Kx36	Value	0	0	1	0	0
256Kx18	Value	0	0	0	1	1

Device Depth

Configuration	Bit #	27	26	25	24	23
128Kx36	Value	0	0	1	0	1
256Kx18	Value	0	0	1	1	0

Revision Number

Bit #	31	30	29	28
Value	x	x	x	x

Figure 4. ID Register Bit Meanings

MCM69L738A Bump/Bit Scan Order

BIT #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	SA	3B
2	SA	4P		37	NC	2B
3	SA	4T		38	SA	3A
4	SA	6R		39	SA	3C
5	SA	5T		40	SA	2C
6	ZZ	7T		41	SA	2A
7	DQa	6P		42	DQc	2D
8	DQa	7P		43	DQc	1D
9	DQa	6N		44	DQc	2E
10	DQa	7N		45	DQc	1E
11	DQa	6M		46	DQc	2F
12	DQa	6L		47	DQc	2G
13	DQa	7L		48	DQc	1G
14	DQa	6K		49	DQc	2H
15	DQa	7K		50	DQc	1H
16	$\overline{SBa}$	5L		51	$\overline{SBc}$	3G
17	$\overline{CK}$	4L		52	NC	4D
18	CK	4K		53	$\overline{SS}$	4E
19	$\overline{G}$	4F		54	NC	4G
20	$\overline{SBb}$	5G		55	NC	4H
21	DQb	7H		56	$\overline{SW}$	4M
22	DQb	6H		57	$\overline{SBd}$	3L
23	DQb	7G		58	DQd	1K
24	DQb	6G		59	DQd	2K
25	DQb	6F		60	DQd	1L
26	DQb	7E		61	DQd	2L
27	DQb	6E		62	DQd	2M
28	DQb	7D		63	DQd	1N
29	DQb	6D		64	DQd	2N
30	SA	6A		65	DQd	1P
31	SA	6C		66	DQd	2P
32	SA	5C		67	SA	3T
33	SA	5A		68	SA	2R
34	NC	6B		69	SA	4N
35	SA	5B		70	M1	3R

MCM69L820A Bump/Bit Scan Order

Bit #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	$\overline{SBb}$	3G
2	SA	6T		37	NC	4D
3	SA	4P		38	$\overline{SS}$	4E
4	SA	6R		39	NC	4G
5	SA	5T		40	NC	4H
6	ZZ	7T		41	$\overline{SW}$	4M
7	DQa	7P		42	DQb	2K
8	DQa	6N		43	DQb	1L
9	DQa	6L		44	DQb	2M
10	DQa	7K		45	DQb	1N
11	$\overline{SBa}$	5L		46	DQb	2P
12	$\overline{CK}$	4L		47	SA	3T
13	CK	4K		48	SA	2R
14	$\overline{G}$	4F		49	SA	4N
15	DQa	6H		50	SA	2T
16	DQa	7G		51	M1	3R
17	DQa	6F				
18	DQa	7E				
19	DQa	6D				
20	SA	6A				
21	SA	6C				
22	SA	5C				
23	SA	5A				
24	NC	6B				
25	SA	5B				
26	SA	3B				
27	NC	2B				
28	SA	3A				
29	SA	3C				
30	SA	2C				
31	SA	2A				
32	DQb	1D				
33	DQb	2E				
34	DQb	2G				
35	DQb	1H				

NOTES:

1. The NC pads listed in this table are indeed no connects, but are represented in the boundary scan register by a "place holder" bit that is forced to logic 1. These pads are reserved for use as address inputs on higher density RAMs that follow this pad out and scan order standard.
2. CK, $\overline{CK}$, are sampled individually. $\overline{CK}$ is not simply a forced complement of the CK input. In scan mode these differential inputs are referenced to each other.
3. M1 and M2 are not ordinary inputs and may not respond to standard I/O logic levels. M1 and M2 must be driven to within 100 mV of a V_{DD} or V_{SS} supply rail to ensure consistent results.
4. ZZ must remain at V_{IL} during boundary scan to ensure consistent results.

TAP Controller Instruction Set

OVERVIEW

There are two classes of instructions defined in the Standard 1149.1–1990; the standard (public) instructions, and device specific (private) instructions. Some public instructions, are mandatory for 1149.1 compliance. Optional public instructions must be implemented in prescribed ways.

Although the TAP controller in this device follows the 1149.1 conventions, it is not 1194.1 compliant because some of the mandatory instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads, but cannot be used to load address, data or control signals into the RAM or to preload the I/O buffers. In other words, the device will not perform Standard 1149.1 EXTEST, INTEST or the preload portion of the SAMPLE / PRELOAD command.

When the TAP controller is placed in capture–IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the shift–IR state the instruction register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to update–IR state. The TAP instruction sets for this device are listed in the following tables.

STANDARD (PUBLIC) INSTRUCTIONS

BYPASS

The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift–DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

Sample/preload is a Standard 1149.1 mandatory public instruction. When the sample / preload instruction is loaded in the Instruction register, moving the TAP controller into the capture–DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set–up plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register.

Moving the controller to shift–DR state then places the boundary scan register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the update–DR state with the SAMPLE / PRELOAD instruction loaded in the instruction register has the same effect as the pause–DR command. This functionality is not Standard 1149.1 compliant.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic 0s. EXTEST is not implemented in this device. Therefore this device is not 1149.1 compliant. Nevertheless, this RAMs TAP does respond to an all zeros instruction, as follows. With the EXTEST (000) instruction loaded in the instruction register the RAM responds just as it does in response to the SAMPLE / PRELOAD instruction described above, except the RAM outputs are forced to high–Z any time the instruction is loaded.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture–DR mode and places the ID register between the TDI and TDO pins in shift–DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test–logic–reset state.

THE DEVICE SPECIFIC (PUBLIC) INSTRUCTION

SAMPLE–Z

If the SAMPLE–Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high–Z) and the boundary scan register is connected between TDI and TDO when the TAP controller. is moved to the shift–DR state.

THE DEVICE SPECIFIC (PRIVATE) INSTRUCTION

NOOP

Do not use these instructions; they are reserved for future use.

STANDARD (PUBLIC) INSTRUCTION CODES

Instruction	Code*	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM outputs to High–Z state. *NOT 1149.1 COMPLIANT*
IDCODE	001**	Preloads ID register and places it between TDI and TDO. Does not affect RAM operation.
SAMPLE / PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect RAM operation. Does not implement 1149.1 Preload function. * NOT 1149.1 COMPLIANT *
BYPASS	111	Places bypass register between TDI and TDO. Does not affect RAM operation.
SAMPLE–Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM output drivers to High–Z.

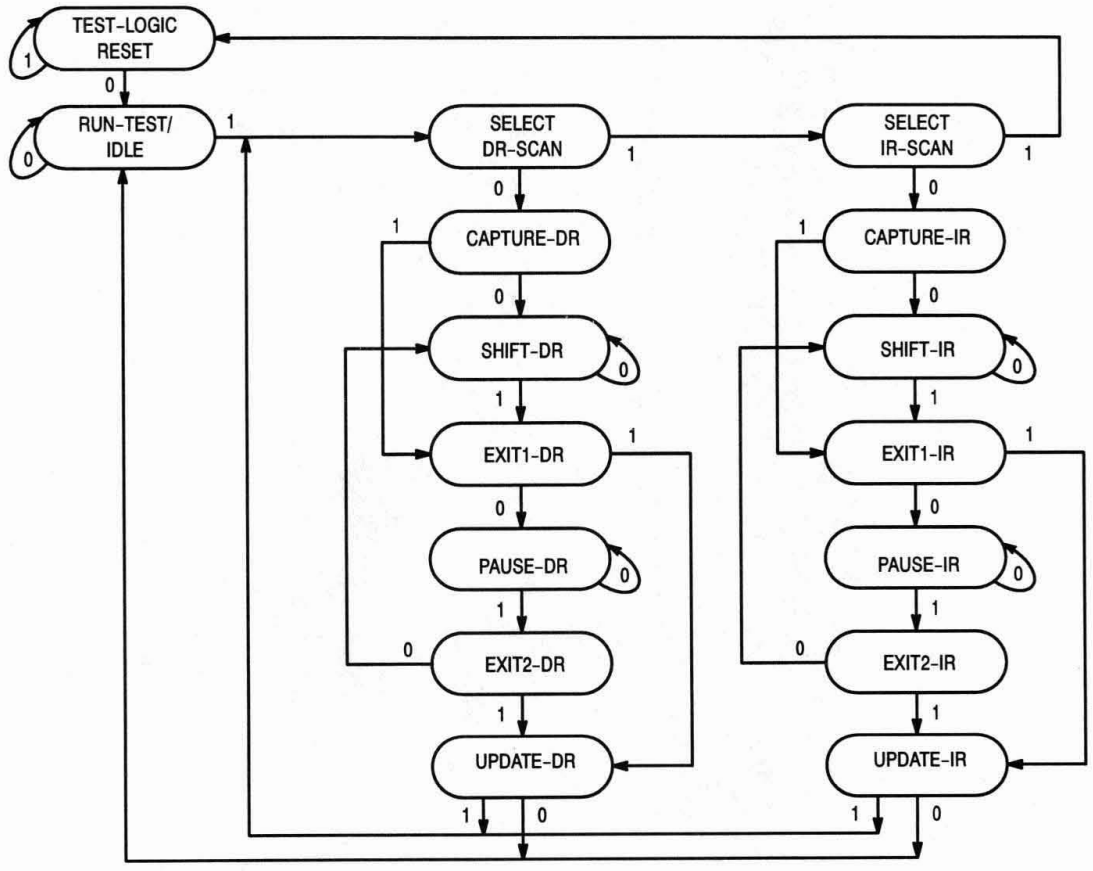
* Instruction codes expressed in binary, MSB on left, LSB on right.
** Default instruction automatically loaded at power–up and in test–logic–reset state.

3

STANDARD (PRIVATE) INSTRUCTION CODES

Instruction	Code*	Description
NO OP	011	Do not use these instructions; they are reserved for future use.
NO OP	101	Do not use these instructions; they are reserved for future use.
NO OP	110	Do not use these instructions; they are reserved for future use.

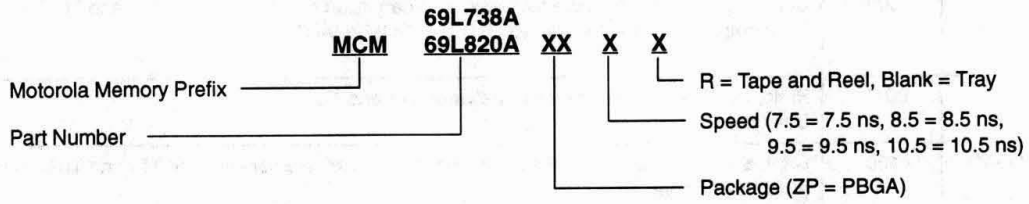
* Instruction codes expressed in binary, MSB on left, LSB on right.



NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 5. TAP Controller State Diagram

ORDERING INFORMATION
(Order by Full Part Number)



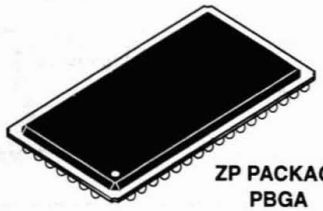
Full Part Numbers —	MCM69L738AZP7.5	MCM69L738AZP8.5	MCM69L738AZP9.5	MCM69L738AZP10.5
	MCM69L820AZP7.5	MCM69L820AZP8.5	MCM69L820AZP9.5	MCM69L820AZP10.5
	MCM69L738AZP7.5R	MCM69L738AZP8.5R	MCM69L738AZP9.5R	MCM69L738AZP10.5R
	MCM69L820AZP7.5R	MCM69L820AZP8.5R	MCM69L820AZP9.5R	MCM69L820AZP10.5R

3

MCM69R536
MCM69R618

Advance Information

1M Late Write HSTL



ZP PACKAGE
PBGA
CASE 999–01

The MCM69R536/618 is a 1 megabit synchronous late write fast static RAM designed to provide high performance in secondary cache, ATM switch, Telecom, and other high speed memory applications. The MCM69R618 organized as 64K words by 18 bits, and the MCM69R536 organized as 32K words by 36 bits wide are fabricated in Motorola's high performance silicon gate BiCMOS technology.

The differential CK clock inputs control the timing of read/write operations of the RAM. At the rising edge of the CK clock all addresses, write enables, and synchronous selects are registered. An internal buffer and special logic enable the memory to accept write data on the rising edge of the CK clock a cycle after address and control signals. Read data is driven on the rising edge of the CK clock also.

The RAM uses HSTL inputs and outputs. The adjustable input trip – point (V_{ref}) and output voltage (V_{DDQ}) gives the system designer greater flexibility in optimizing system performance.

The synchronous write and byte enables allow writing to individual bytes or the entire word.

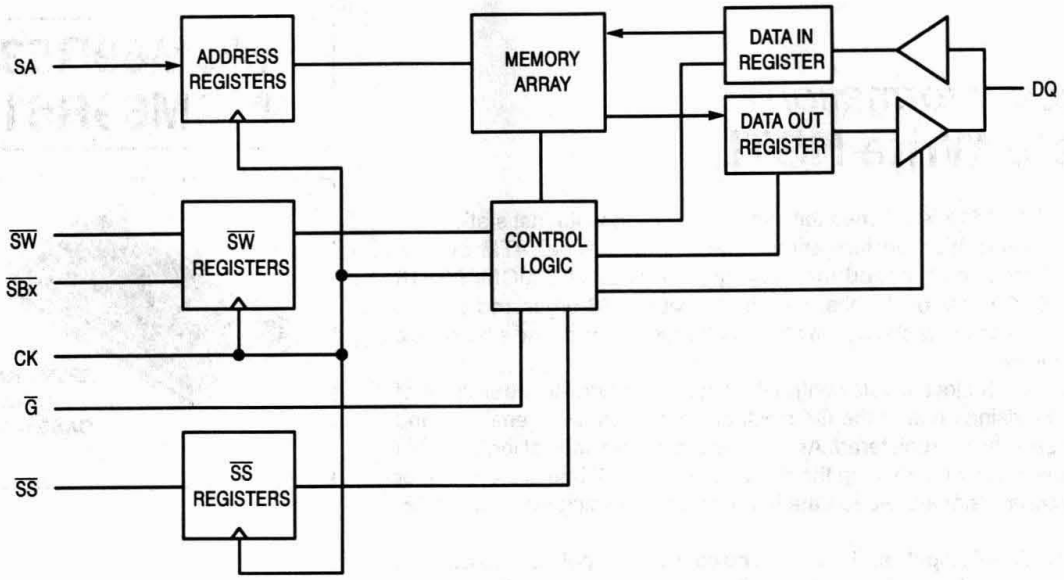
The impedance of the output buffers is programmable allowing the outputs to match the impedance of the circuit traces which reduces signal reflections.

- Byte Write Control
- Single 3.3 V + 10%, – 5% Operation
- HSTL – I/O (JEDEC Standard JESD8–6 Class II Compatible)
- HSTL – User Selectable Input Trip–Point
- HSTL – Compatible Programmable Impedance Output Drivers
- Register to Register Synchronous Operation
- Asynchronous Output Enable
- Boundary Scan (JTAG) IEEE 1149.1 Compatible
- Differential Clock Inputs
- Optional x 18 or x 36 organization
- MCM69R536/618 – 5 = 5 ns
  MCM69R536/618 – 6 = 6 ns
  MCM69R536/618 – 7 = 7 ns
  MCM69R536/618 – 8 = 8 ns
- 119 Bump, 50 mil (1.27 mm) Pitch, 14 mm x 22 mm Plastic Ball Grid Array (PBGA) Package

This document contains information on a new product. Specifications and information herein are subject to change without notice.

4/2/97

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENTS

TOP VIEW

MCM69R536

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	NC	NC	NC	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQc	DQc	V_{SS}	ZQ	V_{SS}	DQb	DQb
E	DQc	DQc	V_{SS}	$\overline{SS}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{G}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{SBc}$	NF	$\overline{SBb}$	DQb	DQb
H	DQc	DQc	V_{SS}	NF	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	V_{ref}	V_{DD}	V_{ref}	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CK	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{SBd}$	$\overline{CK}$	$\overline{SBa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{SW}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
P	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
R	NC	SA	V_{SS}	V_{DD}	V_{DD}	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69R618

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	NC	NC	NC	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQb	NC	V_{SS}	ZQ	V_{SS}	DQa	NC
E	NC	DQb	V_{SS}	$\overline{SS}$	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	$\overline{SBb}$	NF	V_{SS}	NC	DQa
H	DQb	NC	V_{SS}	NF	V_{SS}	DQa	NC
J	V_{DDQ}	V_{DD}	V_{ref}	V_{DD}	V_{ref}	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	CK	V_{SS}	NC	DQa
L	DQb	NC	V_{SS}	$\overline{CK}$	$\overline{SBa}$	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{SW}$	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	SA	V_{SS}	DQa	NC
P	NC	DQb	V_{SS}	SA	V_{SS}	NC	DQa
R	NC	SA	V_{SS}	V_{DD}	V_{DD}	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69R536 PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6K, 7K, 6L, 7L, 6M, 6N, 7N, 6P, 7P (b) 6D, 7D, 6E, 7E, 6F, 6G, 7G, 6H, 7H (c) 1D, 2D, 1E, 2E, 2F, 1G, 2G, 1H, 2H (d) 1K, 2K, 1L, 2L, 2M, 1N, 2N, 1P, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 3T, 4T, 5T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 5G, 3G, 3L (a), (b), (c), (d)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
3J, 5J	V_{ref}	Supply	Input Reference: provides reference voltage for input buffers.
4D	ZQ	Input	Programmable Output Impedance: Programming pin.
7T	ZZ	Input	Reserved for future use. Must be grounded.
4C, 2J, 4J, 6J, 4R, 5R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 3H, 5H, 3K, 5K, 3M, 5M, 3N, 5N, 3P, 5P, 3R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 3B, 4B, 5B, 6B, 7B, 1C, 7C, 1R, 7R, 1T, 2T, 6T, 6U	NC	—	No Connection: There is no connection to the chip.
4G, 4H	NF	—	No Function: There is an internal connection to the chip, but the pin has no function on this device.

MCM69R618 PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6D, 7E, 6F, 7G, 6H, 7K, 6L, 6N, 7P (b) 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 2T, 3T, 5T, 6T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 3G (a), (b)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
3J, 5J	V_{ref}	Supply	Input Reference: provides reference voltage for input buffers.
4D	ZQ	Input	Programmable Output Impedance: Programming pin.
7T	ZZ	Input	Reserved for future use. Must be grounded.
4C, 2J, 4J, 6J, 4R, 5R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P, 3R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 3B, 4B, 5B, 6B, 7B, 1C, 7C, 2D, 7D, 1E, 6E, 2F, 1G, 6G, 2H, 7H, 1K, 6K, 2L, 7L, 6M, 2N, 7N, 1P, 6P, 1R, 7R, 1T, 4T, 6U	NC	—	No Connection: There is no connection to the chip.
4G, 4H	NF	—	No Function: There is an internal connection to the chip, but the pin has no function on this device.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS}, See Note 1)

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Output Supply Voltage	V_{DDQ}	– 0.5 to V_{DD} + 0.5	V
Voltage On Any Pin	V_{in}	– 0.5 to V_{DD} + 0.5	V
Input Current (per I/O)	I_{in}	± 50	mA
Output Current (per I/O)	I_{out}	± 70	mA
Power Dissipation (See Note 2)	P_D	—	W
Operating Temperature	T_A	0 to + 70	°C
Temperature Under Bias	T_{bias}	–10 to + 85	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability will be dependent upon package characteristics and use environment. See enclosed thermal impedance data.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

3

PBGA PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (Still Air)		$R_{\theta JA}$	59	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Single Layer Board	$R_{\theta JA}$	44	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Four Layer Board	$R_{\theta JA}$	28	°C/W	
Junction to Board (Bottom)		$R_{\theta JB}$	18	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, pwer dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

($0°C \le T_A \le 70$ °C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (See Notes 1 through 4)

Parameter		Symbol	Min	Typical –5	Typical –6	Typical –7	Typical –8	Max	Unit	Notes
Input Reference DC Voltage		V_{ref} (dc)	0.6	—	—	—	—	1.1	V	11
Core Power Supply Voltage		V_{DD}	3.15	—	—	—	—	3.6	V	
Output Driver Supply Voltage		V_{DDQ}	1.4	—	—	—	—	1.6	V	
Active Power Supply Current	(x18) (x36)	I_{DD1}	— —	TBD TBD	TBD TBD	TBD TBD	TBD TBD	TBD TBD	mA	5
Quiescent Active Power Supply Current	(x18) (x36)	I_{DD2}	— —	TBD TBD	TBD TBD	TBD TBD	TBD TBD	TBD	mA	6, 10
Active Standby Power Supply Current	(x18) (x36)	I_{SB1}	— —	TBD TBD	TBD TBD	TBD TBD	TBD TBD	TBD	mA	7
Quiescent Standby Power Supply Current	(x18) (x36)	I_{SB2}	— —	TBD TBD	TBD TBD	TBD TBD	TBD TBD	TBD	mA	8, 10
Sleep Mode Power Supply Current		I_{SB3}	—	TBD	TBD	TBD	TBD	TBD	mA	9, 10

NOTES:

1. All data sheet parameters specified to full range of V_{DD} unless otherwise noted. All voltages are referenced to voltage applied to V_{SS} bumps.
2. Supply voltage applied to V_{DD} connections.
3. Supply voltage applied to V_{DDQ} connections.
4. All power supply currents measured with outputs open or deselected.
5. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered active, 50% read cycles.
6. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered active.
7. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered inactive.
8. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered inactive, ZZ low.
9. $V_{DD} = V_{DD}$ (Max), t_{KHKH} = dc, registered inactive, ZZ high.
10. 200 mV $\ge V_{in} \ge V_{DDQ} - 200$ mV.
11. Although considerable latitude in the selection of the nominal dc value (i.e., rms value) of V_{ref} is supported, the peak to peak ac component superimposed on V_{ref} may not exceed 5% of the dc component of V_{ref}.

DC INPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
DC Input Logic High	V_{IH} (dc)	$V_{ref} + 0.1$	$V_{DD} + 0.3$	V	
DC Input Logic Low (See Figure 2)	V_{IL} (dc)	– 0.3	$V_{ref} - 0.1$	V	1
Input Leakage Current	I_{lkg}	—	± 5	µA	2
Clock Input Signal Voltage	V_{in}	– 0.3	$V_{DD} + 0.3$	V	
Clock Input Differential Voltage	V_{DIF} (dc)	0.2	$V_{DD} + 0.6$	V	3
Clock Input Common Mode Voltage Range (See Figure 3)	V_{CM} (dc)	0.68	1.1	V	4
Clock Input Crossing Point Voltage Range (See Figure 3)	V_X	0.68	1.1	V	

NOTES:

1. Inputs may undershoot to –0.5 V (peak) for up to 20% t_{KHKH} (e.g., 2 ns at a clock cycle time of 10 ns).
2. $0 V \le V_{in} \le V_{DDQ}$ for all pins.
3. Minimum differential input voltage required for differential input clock operation.
4. Maximum rejectable common mode input voltage variation.

DC OUTPUT BUFFER CHARACTERISTICS – PROGRAMMABLE IMPEDANCE PUSH–PULL OUTPUT BUFFER MODE

($0°C \le T_A \le 70°C$, Unless Otherwise Noted, See Notes 5 and 6)

Parameter	Symbol	Min	Max	Unit	Notes
Output Logic Low	V_{OL}	$V_{DDQ}/2 - 0.025$	$V_{DDQ}/2 + 0.025$	V	1
Output Logic High	V_{OH}	$V_{DDQ}/2 - 0.025$	$V_{DDQ}/2 + 0.025$	V	2
Light Load Output Logic Low	$V_{OL}1$	V_{SS}	0.2	V	3
Light Load Output Logic High	$V_{OH}1$	$V_{DDQ} - 0.2$	V_{DDQ}	V	4

NOTES:
1. $I_{OL} = (V_{DDQ}/2)/(RQ/5)$ for values of $RQ = 175\ \Omega \le RQ \le 350\ \Omega$.
2. $|I_{OH}| = (V_{DDQ}/2)/(RQ/5)$ for values of $RQ = 175\ \Omega \le RQ \le 350\ \Omega$.
3. $I_{OL} \le 100\ \mu A$.
4. $|I_{OH}| \le 100\ \mu A$.
5. The impedance controlled mode is expected to be used in point–to–point applications, driving high impedance inputs.
6. The ZQ pin is connected through RQ to V_{SS} for the controlled impedance mode.

3

DC OUTPUT BUFFER CHARACTERISTICS – MINIMUM IMPEDANCE PUSH–PULL OUTPUT BUFFER MODE

($0°C \le T_A \le 70°C$, $ZQ = V_{DD}$, See Notes 5 and 6)

Parameter	Symbol	Min.	Max.	Unit	Notes
Output Logic Low	$V_{OL}2$	V_{SS}	0.4	V	1
Output Logic High	$V_{OH}2$	$V_{DDQ} - 0.4$	V_{DDQ}	V	2
Light Load Output Logic Low	$V_{OL}3$	V_{SS}	0.2	V	3
Light Load Output Logic High	$V_{OH}3$	$V_{DDQ} - 0.2$	V_{DDQ}	V	4

NOTES:
1. $I_{OL} \le 16$ mA.
2. $|I_{OH}| \le 16$ mA.
3. $I_{OL} \le 100\ \mu A$.
4. $|I_{OH}| \le 100\ \mu A$.
5. The push–pull output mode is expected to be used in bussed applications and may be series or parallel terminated. Conforms to the JEDEC Standard JESD8–6 Class II.
6. The ZQ pin is connected to V_{DD} to enable the minimum impedance mode.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, $0°C \le T_A \le 70°C$, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	5	pF
Input/Output Capacitance	$C_{I/O}$	7	8	pF
CK, $\overline{CK}$ Capacitance	C_{CK}	4	5	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T_A ≤ 70 °C, Unless Otherwise Noted)

Input Pulse Levels ..... 0.25 to 1.25 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 0.75 V
Output Timing Reference Level ..... 0.75 V
Clock Input Timing Reference Level ..... Differential Cross–Point
ZQ for 50 Ω Impedance ..... 250 Ω

READ/WRITE CYCLE TIMING (See Note 3)

Parameter	Symbol	MCM69R536–5 MCM69R618–5		MCM69R536–6 MCM69R618–6		MCM69R536–7 MCM69R618–7		MCM69R536–8 MCM69R618–8		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	5	—	6	—	7	—	8	—	ns	
Clock High Pulse Width	t_{KHKL}	2.4	—	2.4	—	2.8	—	3.2	—	ns	
Clock Low Pulse Width	t_{KLKH}	2.4	—	2.4	—	2.8	—	3.2	—	ns	
Clock High to Output Low–Z	t_{KHQX1}	1	—	1	—	1	—	1	—	ns	2
Clock High to Output Valid	t_{KHQV}	—	2.5	—	3	—	3.5	—	4	ns	1
Clock High to Output Hold	t_{KHQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	2
Clock High to Output High–Z	t_{KHQZ}	—	2.5	—	3	—	3.5	—	4	ns	2
Output Enable Low to Output Low–Z	t_{GLQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	2
Output Enable Low to Output Valid	t_{GLQV}	—	2.5	—	3	—	3.5	—	4	ns	2
Output Enable to Output Hold	t_{GHQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	2
Output Enable High to Output High–Z	t_{GHQZ}	—	2.5	—	3	—	3.5	—	4	ns	2
Setup Times: Address Data In Chip Select Write Enable	t_{AVKH} t_{DVKH} t_{SVKH} t_{WVKH}	0.5	—	0.5	—	0.5	—	0.5	—	ns	
Hold Times: Address Data In Chip Select Write Enable	t_{KHAX} t_{KHDX} t_{KHSX} t_{KHWX}	1	—	1	—	1	—	1	—	ns	

NOTES:
1. Tested per AC Test Load diagram. See Figure 1.
2. Measured at ± 200 mV from steady state.
3. In no case may control input signals (e.g., $\overline{SS}$) be operated with pulse widths less than the minimum clock input pulse width specifications (e.g., t_{KHKL}) or at frequencies that exceed the applied K clock frequency.

AC INPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Note
AC Input Logic High (See Figure 4)	V_{IH} (ac)	V_{ref} + 200 mV		
AC Input Logic Low (See Figure 2 and 4)	V_{IL} (ac)		V_{ref} – 200 mV	1
Input Reference Peak to Peak ac Voltage	V_{ref} (ac)		5% V_{ref} (dc)	2
Clock Input Differential Voltage	V_{dif} (ac)	400 mV	V_{DDQ} + 600 mV	3

NOTES:
1. Inputs may undershoot to – 0.5 V (peak) for up to 20% t_{KHKH} (e.g., 2 ns at a clock cycle time of 10 ns).
2. Although considerable latitude in the selection of the nominal dc value (i.e., rms value) of V_{ref} is supported, the peak to peak ac component superimposed on V_{ref} may not exceed 5% of the dc component of V_{ref}.
3. Minimum differential input voltage required for differential input clock operation.

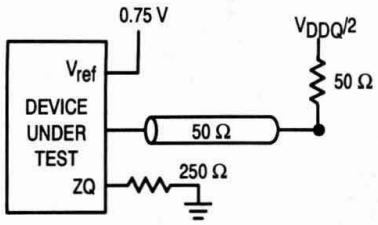


Figure 1. AC Test Load

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

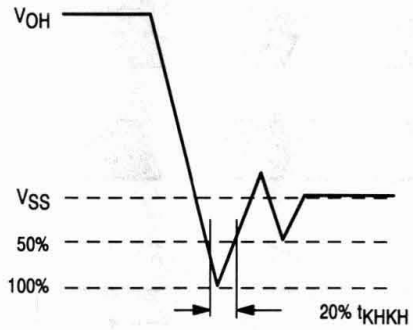
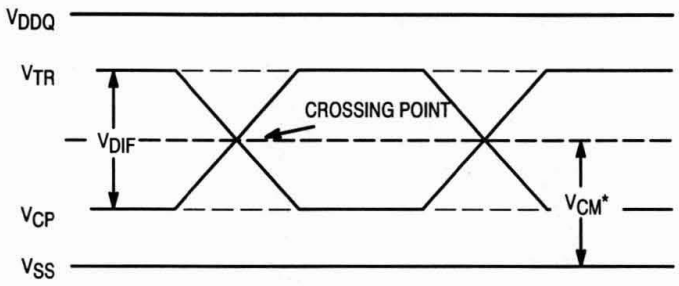


Figure 2. Undershoot Voltage



*V_{CM}, the Common Mode Input Voltage, equals $V_{TR} - ((V_{TR} - V_{CP})/2)$.

Figure 3. Differential Inputs/Common Mode Input Voltage

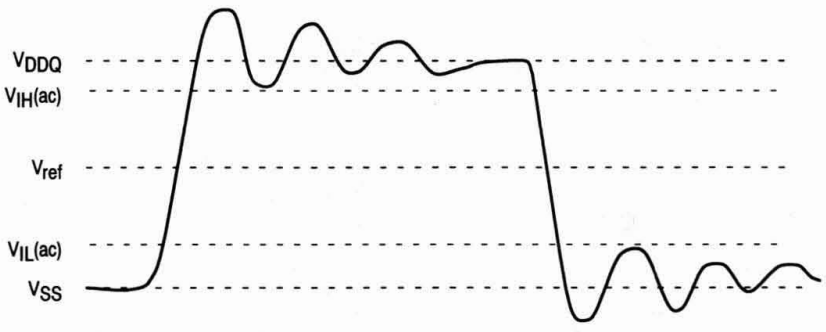
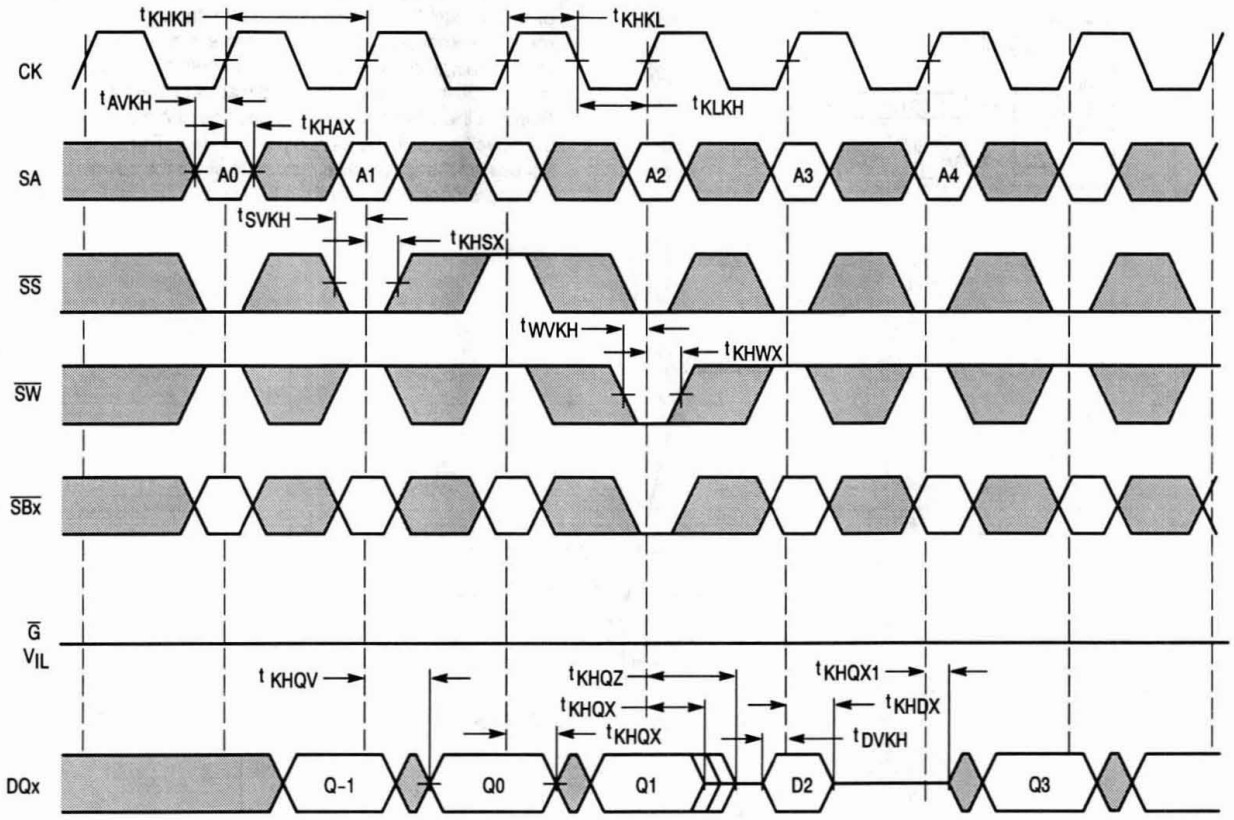
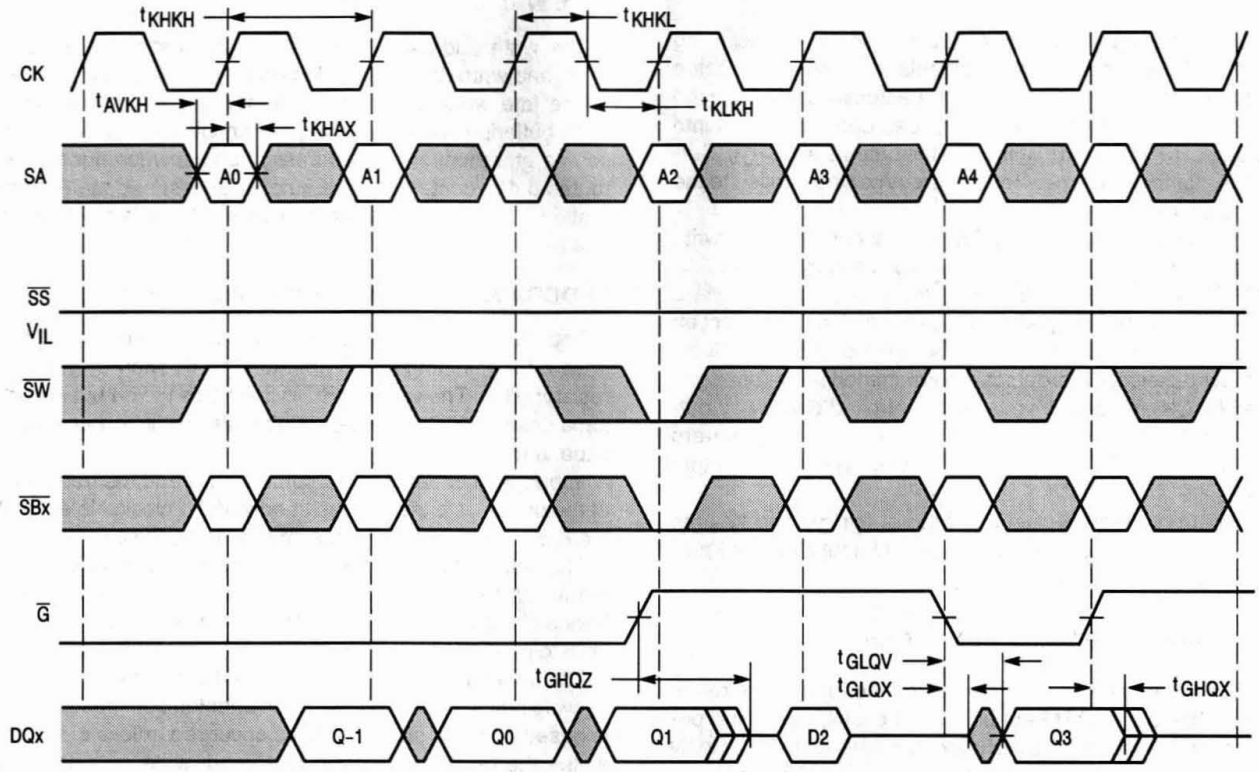


Figure 4. AC Input Conditions

REGISTER/REGISTER READ–WRITE–READ CYCLES



REGISTER/REGISTER READ–WRITE–READ
($\overline{G}$ Controlled)



3

FUNCTIONAL OPERATION

READ AND WRITE OPERATIONS

All control signals except $\overline{G}$ are registered on the rising edge of the CK clock. These signals must meet the setup and hold times shown in the AC Characteristics table. On the rising edge of the following clock, read data is clocked into the output register and available at the outputs at t_{KHQV}. During this same cycle a new read address can be applied to the address pins.

A deselect cycle (dead cycle) must occur prior to a write cycle. Read cycles may follow write cycles immediately.

$\overline{G}$, $\overline{SS}$, and $\overline{SW}$ control output drive. Chip deselect via a high on $\overline{SS}$ at the rising edge of the CK clock has its effect on the output drivers after the next rising edge of the CK clock. $\overline{SW}$ low deselects the output drivers immediately (as registered by CK). Output drive is also controlled directly by output enable, $\overline{G}$. No clock edges are required to generate output disable with $\overline{G}$. $\overline{G}$ asynchronously enables the output drivers.

Output data will be valid the latter of t_{GLQV} and t_{KHQV}. Outputs will begin driving at t_{KHQX1}. Outputs will hold previous data until t_{KHQX} or t_{GHQX}.

WRITE AND BYTE WRITE FUNCTIONS

Note that in the following discussion the term "byte" refers to nine bits of the RAM I/O bus. In all cases, the timing parameters described for synchronous write input ($\overline{SW}$) apply to each of the byte write enable inputs ($\overline{SBa}$, $\overline{SBb}$, etc.).

Byte write enable inputs have no effect on read cycles. This allows the system designer not interested in performing byte writes to connect the byte enable inputs to active low (V_{SS}). Reads of all bytes proceed normally and write cycles, activated via a low on $\overline{SW}$, and the rising edge of the CK clock, write the entire RAM I/O width. This way the designer is spared having to drive multiple write input buffer loads.

Byte writes are performed using the byte write enable inputs in conjunction with the synchronous write input ($\overline{SW}$). It is important to note that writing any one byte will inhibit a read of all bytes at the current address. The RAM cannot simultaneously read one byte and write another at the same address. A write cycle initiated with none of the byte write enable inputs active is neither a read or a write. No write will occur, but the outputs will be deselected as in a normal write cycle.

LATE WRITE

The write address is sampled on the first rising edge of clock and write data is sampled on the following rising edge.

The late write feature is implemented with single stage write buffering. Write buffering is transparent to the user. A comparator monitors the address bus and, when necessary, routes buffer contents to the outputs to assure coherent operation. This occurs in all cases whether there is a byte write or a full word is written.

PROGRAMMABLE IMPEDANCE OPERATION

The designer can program the RAMs output buffer impedance by terminating the $\overline{ZQ}$ pin to V_{SS} through a precision resistor (RQ). The value of RQ is five times the output impedance desired. For example, 250 Ω resistor will give an output impedance of 50 Ω.

Impedance updates occur continuously and the frequency of the update is based on the subdivided K clock. Note that if the K clock stops so does the impedance update.

The actual change in the impedance occurs in small increments and is monotonic. There are no significant disturbances that occur on the output because of this smooth update method.

The impedance update is not related to any particular type of cycle because the impedance is updated continuously and is based on the K clock. Updates occur regardless of whether the the device is performing a read, write or a deselect cycle and does not depend on the state of $\overline{G}$.

At power up, the output impedance defaults to approximately 50 ohms. It will take 4,000 to 16,000 cycles for the impedance to be completely updated if the programmed impedance is much higher or lower than 50 Ω.

The output buffers can also be programmed in a minimum impedance configuration by connecting ZQ to V_{DD}.

POWER UP AND INITIALIZATION

Once supplies have reached specification levels, a minimum dwell of 1.0 ms with CK clock inputs cycling is required before beginning normal operations. At power up the output impedance will be set at approximately 50 Ω as stated above.

SERIAL BOUNDARY SCAN TEST ACCESS PORT OPERATION

OVERVIEW

The serial boundary scan test access port (TAP) on this RAM is designed to operate in a manner consistent with IEEE Standard 1149.1–1990 (commonly referred to as JTAG), but does not implement all of the functions required for 1149.1 compliance. Certain functions have been modified or eliminated because their implementation places extra delays in the RAMs critical speed path. Nevertheless, the RAM supports the standard TAP controller architecture. (The TAP controller is the state machine that controls the TAPs operation) and can be expected to function in a manner that does not conflict with the operation of devices with Standard 1149.1 compliant TAPs. The TAP operates using conventional JEDEC Standard 8–1B Low Voltage (3.3 V) TTL / CMOS logic level signaling.

DISABLING THE TEST ACCESS PORT

It is possible to use this device without utilizing the TAP. To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid level inputs. TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a 1 k resistor. TDO should be left unconnected.

3

TAP DC OPERATING CHARACTERISTICS

($0°C \le T_A \le 70°C$, Unless Otherwise Noted)

Parameter	Symbol	Min	Max	Unit	Note
Logic Input Logic High	$V_{IH}1$	2.0	V_{DD} + 0.3	V	
Logic Input Logic Low	$V_{IL}1$	– 0.3	0.8	V	
Logic Input Leakage Current	I_{lkg}	—	± 5	µA	1
Output Logic Low	$V_{OL}1$	—	0.2	V	2
Output Logic High	$V_{OH}1$	V_{DD} – 0.2	—	V	3
Output Logic Low	$V_{OL}2$	—	0.4	V	4
Output Logic High	$V_{OH}2$	2.4	—	V	5

NOTES:
1. $0 V \le V_{in} \le V_{DD}$ for all logic input pins.
2. $I_{OL}1 \le 100$ µA @ $V_{OL} = 0.2$ V. Sampled, not 100% tested.
3. $|I_{OH}1| \le 100$ µA @ $V_{DDQ} - 0.2$ V. Sampled, not 100% tested.
4. $I_{OL}2 \le 8$ mA @ $V_{OL} = 0.4$ V.
5. $|I_{OH}2| \le 8$ mA @ $V_{OH} = 2.4$ V.

TAP AC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T_A ≤ 70 °C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V

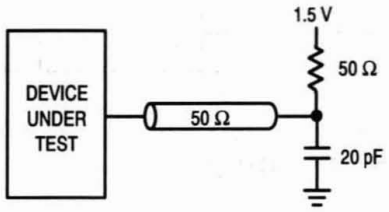
Output Test Load ..... 50 Ω Parallel Terminated T–line with 20 pF Receiver Input Capacitance
Test Load Termination Supply Voltage (V_T) ..... 1.5 V

TAP CONTROLLER TIMING

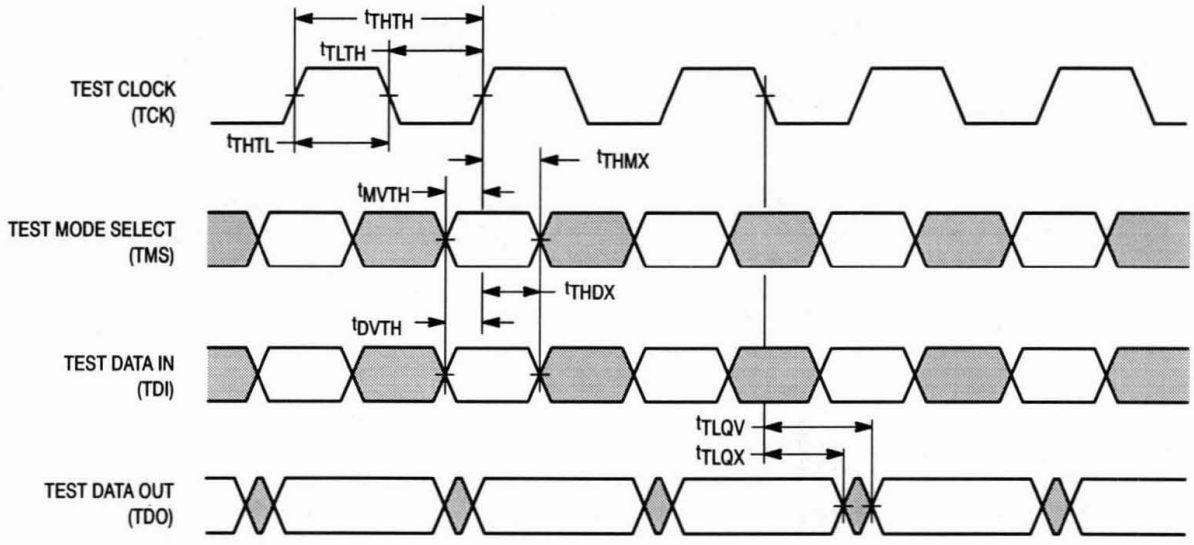
Parameter	Symbol	Min	Max	Unit	Notes
Cycle Time	t_{THTH}	100	—	ns	
Clock High Time	t_{THTL}	40	—	ns	
Clock Low Time	t_{TLTH}	40	—	ns	
TMS Setup	t_{MVTH}	10	—	ns	
TMS Hold	t_{THMX}	10	—	ns	
TDI Valid to TCK High	t_{DVTH}	10	—	ns	
TCK High to TDI Don't Care	t_{THDX}	10	—	ns	
Capture Setup	t_{CS}	10	—	ns	1
Capture Hold	t_{CH}	10	—	ns	1
TCK Low to TDO Unknown	t_{TLQX}	0	—	ns	
TCK Low to TDO Valid	t_{TLOV}	—	20	ns	

NOTES:
1. t_{CS} + t_{CH} defines the minimum pause in RAM I/O pad transitions to assure accurate pad data capture.

AC TEST LOAD



TAP CONTROLLER TIMING DIAGRAM



TEST ACCESS PORT PINS

TCK – TEST CLOCK (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

TMS – TEST MODE SELECT (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.

TDI – TEST DATA IN (INPUT)

The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (refer to Figure 6 TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.

TDO – TEST DATA OUT (OUTPUT)

Output that is active depending on the state of the TAP state machine (refer to Figure 6 TAP Controller State Diagram). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

TRST – TAP RESET

This device does not have a TRST pin. TRST is optional in **IEEE 1149.1.** The test–logic reset state is entered while TMS is held high for five rising edges of TCK. Power on reset circuitry is included internally. This type of reset does not affect the operation of the system logic. The reset affects test logic only.

TEST ACCESS PORT REGISTERS

OVERVIEW

The various TAP registers are selected (one at a time) via the sequences of ones and zeros input to the TMS pin as the TCK is strobed. Each of the TAPs registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on subsequent falling edge of TCK. When a register is selected it is "placed" between the TDI and TDO pins.

INSTRUCTION REGISTER

The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run test/idle or the various data register states. The instructions are three bits long. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power–up or whenever the controller is placed in test–logic–reset state.

BYPASS REGISTER

The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.

BOUNDARY SCAN REGISTER

The boundary scan register is identical in length to the number of active input and I/O connections on the RAM (not counting the TAP pins). This also includes a number of place holder locations (always set to a logic 1) reserved for density upgrade address pins. There are a total of 70 bits in the case of the x36 device and 51 bits in the case of the x18 device. The boundary scan register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture–DR state and then is placed between the TDI and TDO pins when the controller is moved to shift–DR state. Several TAP instructions can be used to activate the boundary scan register.

The Bump/Bit Scan Order tables describe which device bump connects to each boundary scan register location. The first column defines the bit's position in the boundary scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the input or I/O at the bump and the third column is the bump number.

IDENTIFICATION (ID) REGISTER

The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture–DR state with the IDCODE command loaded in the instruction register. The code is loaded from a 32 bit on–chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into shift–DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Presence Indicator

Bit #	0
Value	1

Motorola JEDEC ID Code (Compressed Format, per IEEE Standard 1149.1 – 1990

Bit #	11	10	9	8	7	6	5	4	3	2	1
Value	0	0	0	0	0	0	0	1	1	1	0

Reserved For Future Use

Bit #	17	16	15	14	13	12
Value	x	x	x	x	x	x

Device Width

Configuration	Bit #	22	21	20	19	18
32Kx36	Value	0	0	1	0	0
64Kx18	Value	0	0	0	1	1

Device Depth

Configuration	Bit #	27	26	25	24	23
32Kx36	Value	0	0	0	1	1
64Kx18	Value	0	0	1	0	0

Revision Number

Bit #	31	30	29	28
Value	x	x	x	x

Figure 5. ID Register Bit Meanings

MCM69R536 Bump/Bit Scan Order

BIT #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	NC	3B
2	SA	4P		37	NC	2B
3	SA	4T		38	SA	3A
4	SA	6R		39	SA	3C
5	SA	5T		40	SA	2C
6	ZZ	7T		41	SA	2A
7	DQa	6P		42	DQc	2D
8	DQa	7P		43	DQc	1D
9	DQa	6N		44	DQc	2E
10	DQa	7N		45	DQc	1E
11	DQa	6M		46	DQc	2F
12	DQa	6L		47	DQc	2G
13	DQa	7L		48	DQc	1G
14	DQa	6K		49	DQc	2H
15	DQa	7K		50	DQc	1H
16	$\overline{SBa}$	5L		51	$\overline{SBc}$	3G
17	$\overline{CK}$	4L		52	ZQ	4D
18	CK	4K		53	$\overline{SS}$	4E
19	$\overline{G}$	4F		54	NF	4G
20	$\overline{SBb}$	5G		55	NF	4H
21	DQb	7H		56	$\overline{SW}$	4M
22	DQb	6H		57	$\overline{SBd}$	3L
23	DQb	7G		58	DQd	1K
24	DQb	6G		59	DQd	2K
25	DQb	6F		60	DQd	1L
26	DQb	7E		61	DQd	2L
27	DQb	6E		62	DQd	2M
28	DQb	7D		63	DQd	1N
29	DQb	6D		64	DQd	2N
30	SA	6A		65	DQd	1P
31	SA	6C		66	DQd	2P
32	SA	5C		67	SA	3T
33	SA	5A		68	SA	2R
34	NC	6B		69	SA	4N
35	NC	5B		70	M1	3R

MCM69R618 Bump/Bit Scan Order

Bit #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	$\overline{SBb}$	3G
2	SA	6T		37	ZQ	4D
3	SA	4P		38	$\overline{SS}$	4E
4	SA	6R		39	NF	4G
5	SA	5T		40	NF	4H
6	ZZ	7T		41	$\overline{SW}$	4M
7	DQa	7P		42	DQb	2K
8	DQa	6N		43	DQb	1L
9	DQa	6L		44	DQb	2M
10	DQa	7K		45	DQb	1N
11	$\overline{SBa}$	5L		46	DQb	2P
12	$\overline{CK}$	4L		47	SA	3T
13	CK	4K		48	SA	2R
14	$\overline{G}$	4F		49	SA	4N
15	DQa	6H		50	SA	2T
16	DQa	7G		51	M1	3R
17	DQa	6F				
18	DQa	7E				
19	DQa	6D				
20	SA	6A				
21	SA	6C				
22	SA	5C				
23	SA	5A				
24	NC	6B				
25	NC	5B				
26	NC	3B				
27	NC	2B				
28	SA	3A				
29	SA	3C				
30	SA	2C				
31	SA	2A				
32	DQb	1D				
33	DQb	2E				
34	DQb	2G				
35	DQb	1H				

NOTES:

1. The NC pads listed in this table are indeed no connects, but are represented in the boundary scan register by a "place holder" bit that is forced to logic 1. These pads are reserved for use as address inputs on higher density RAMs that follow this pad out and scan order standard.
2. CK, $\overline{CK}$, are sampled individually. $\overline{CK}$ is not simply a forced complement of the CK input. In scan mode these differential inputs are referenced to V_{ref}, not each other.
3. ZQ, M1, and M2 are not ordinary inputs and may not respond to standard I/O logic levels. ZQ, M1, and M2 must be driven to within 100 mV of a V_{DD} or V_{SS} supply rail to ensure consistent results.
4. ZZ must remain at V_{IL} during boundary scan to ensure consistent results.

TAP Controller Instruction Set

OVERVIEW

There are two classes of instructions defined in the Standard 1149.1–1990; the standard (public) instructions, and device specific (private) instructions. Some public instructions, are mandatory for 1149.1 compliance. Optional public instructions must be implemented in prescribed ways.

Although the TAP controller in this device follows the 1149.1 conventions, it is not 1194.1 compliant because some of the mandatory instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads, but cannot be used to load address, data or control signals into the RAM or to preload the I/O buffers. In other words, the device will not perform Standard 1149.1 EXTEST, INTEST or the preload portion of the SAMPLE / PRELOAD command.

When the TAP controller is placed in capture–IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the shift–IR state the instruction register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to update–IR state. The TAP instruction sets for this device are listed in the following tables.

STANDARD (PUBLIC) INSTRUCTIONS

BYPASS

The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift–DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

Sample/preload is a Standard 1149.1 mandatory public instruction. When the sample / preload instruction is loaded in the Instruction register, moving the TAP controller into the capture–DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set–up plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register.

Moving the controller to shift–DR state then places the boundary scan register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the update–DR state with the SAMPLE / PRELOAD instruction loaded in the instruction register has the same effect as the pause–DR command. This functionality is not Standard 1149.1 compliant.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic 0s. EXTEST is not implemented in this device. Therefore this device is not 1149.1 compliant. Nevertheless, this RAMs TAP does respond to an all zeros instruction, as follows. With the EXTEST (000) instruction loaded in the instruction register the RAM responds just as it does in response to the SAMPLE / PRELOAD instruction described above, except the RAM outputs are forced to high–Z any time the instruction is loaded.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture–DR mode and places the ID register between the TDI and TDO pins in shift–DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test–logic–reset state.

THE DEVICE SPECIFIC (PUBLIC) INSTRUCTION

SAMPLE–Z

If the SAMPLE–Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high–Z) and the boundary scan register is connected between TDI and TDO when the TAP controller is moved to the shift–DR state.

THE DEVICE SPECIFIC (PRIVATE) INSTRUCTION

NOOP

Do not use these instructions; they are reserved for future use.

STANDARD (PUBLIC) INSTRUCTION CODES

Instruction	Code*	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM outputs to High–Z state. *NOT 1149.1 COMPLIANT*
IDCODE	001**	Preloads ID register and places it between TDI and TDO. Does not affect RAM operation.
SAMPLE / PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect RAM operation. Does not implement 1149.1 Preload function. * NOT 1149.1 COMPLIANT *
BYPASS	111	Places bypass register between TDI and TDO. Does not affect RAM operation.
SAMPLE–Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM output drivers to High–Z.

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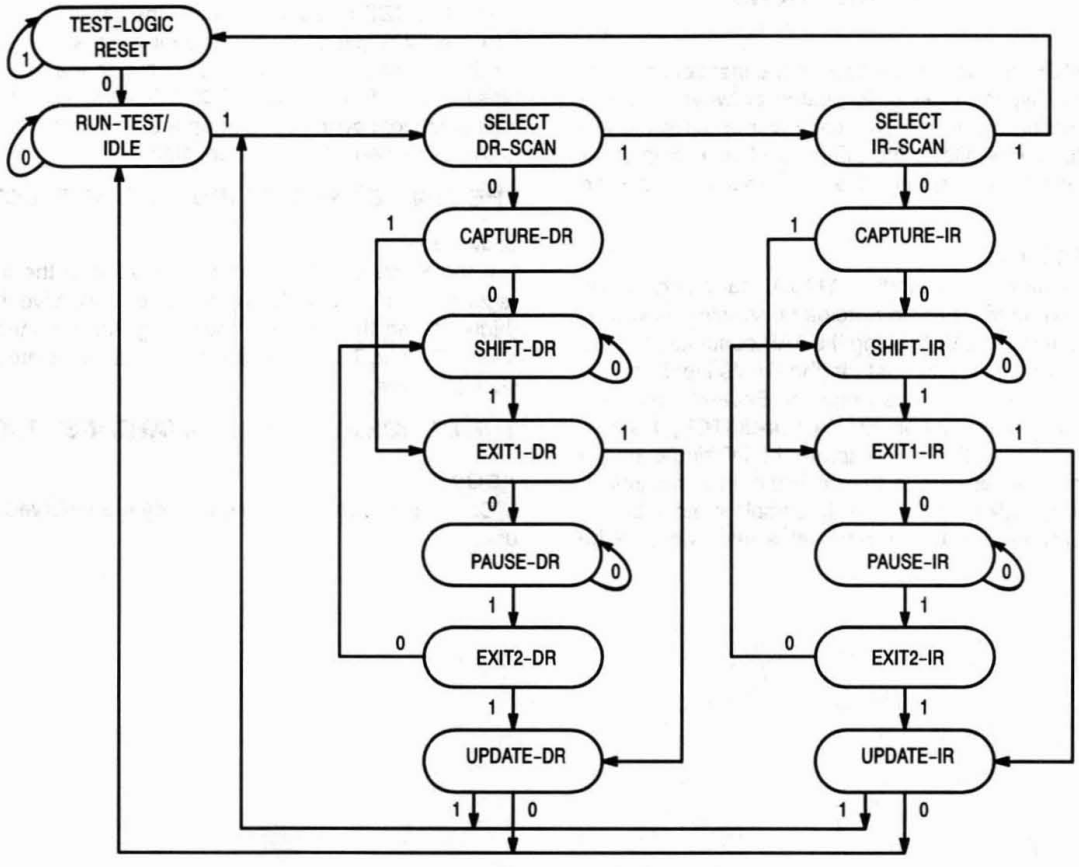
* Instruction codes expressed in binary, MSB on left, LSB on right.
** Default instruction automatically loaded at power–up and in test–logic–reset state.

STANDARD (PRIVATE) INSTRUCTION CODES

Instruction	Code*	Description
NO OP	011	Do not use these instructions; they are reserved for future use.
NO OP	101	Do not use these instructions; they are reserved for future use.
NO OP	110	Do not use these instructions; they are reserved for future use.

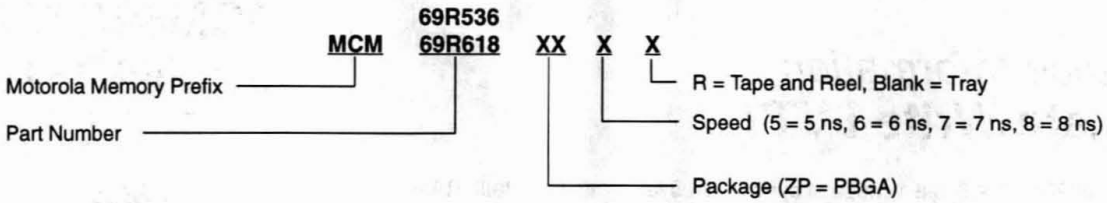
* Instruction codes expressed in binary, MSB on left, LSB on right.



NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 6. TAP Controller State Diagram

ORDERING INFORMATION
(Order by Full Part Number)


69R536
MCM 69R618 XX X X
Motorola Memory Prefix
Part Number
R = Tape and Reel, Blank = Tray
Speed (5 = 5 ns, 6 = 6 ns, 7 = 7 ns, 8 = 8 ns)
Package (ZP = PBGA)

Full Part Numbers —	MCM69R536ZP5	MCM69R536ZP6	MCM69R536ZP7	MCM69R536ZP8
	MCM69R618ZP5	MCM69R618ZP6	MCM69R618ZP7	MCM69R618ZP8
	MCM69R536ZP5R	MCM69R536ZP6R	MCM69R536ZP7R	MCM69R536ZP8R
	MCM69R618ZP5R	MCM69R618ZP6R	MCM69R618ZP7R	MCM69R618ZP8R

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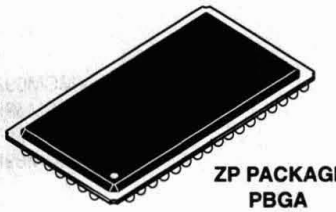
MCM69R537
MCM69R619

Advance Information

1M Late Write LVTTL



ZP PACKAGE
PBGA
CASE 999–01

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The MCM69R537/619 is a 1 megabit synchronous late write fast static RAM designed to provide high performance in secondary cache, ATM switch, Telecom, and other high speed memory applications. The MCM69R619 organized as 64K words by 18 bits, and the MCM69R537 organized as 32K words by 36 bits wide are fabricated in Motorola's high performance silicon gate BiCMOS technology.

The differential CK clock inputs control the timing of read/write operations of the RAM. At the rising edge of the CK clock all addresses, write enables, and synchronous selects are registered. An internal buffer and special logic enable the memory to accept write data on the rising edge of the CK clock a cycle after address and control signals. Read data is driven on the rising edge of the CK clock also.

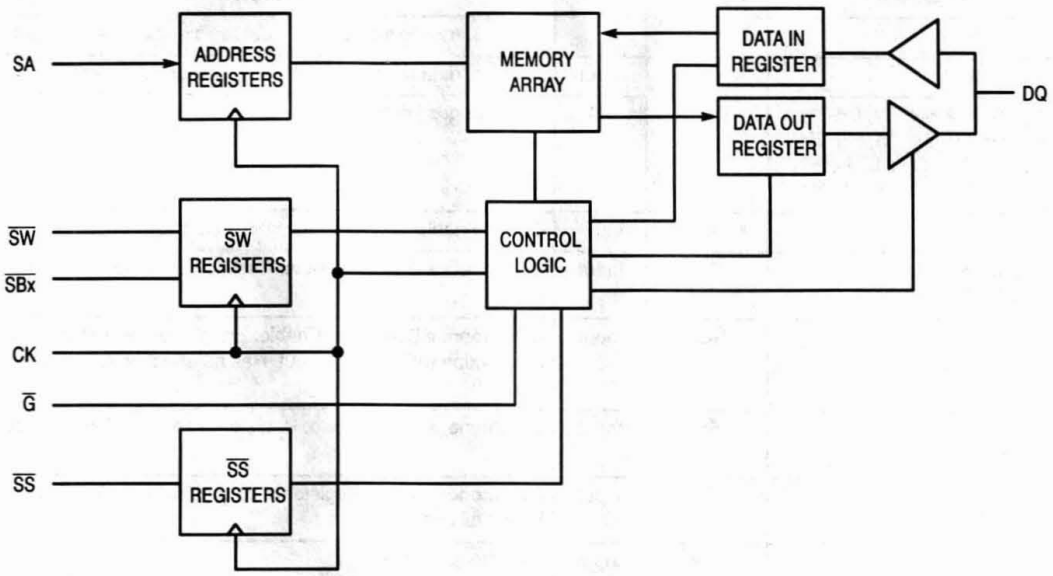
The synchronous write and byte enables allow writing to individual bytes or the entire word.

- Byte Write Control
- Single 3.3 V + 10%, – 5% Operation
- LVTTL 3.3 V I/O (V_{DDQ})
- Register to Register Synchronous Operation
- Asynchronous Output Enable
- Boundary Scan (JTAG) IEEE 1149.1 Compatible
- Differential Clock Inputs
- Optional x 18 or x 36 organization
- MCM69R537/618 – 5 = 5 ns
  MCM69R537/618 – 6 = 6 ns
  MCM69R537/618 – 7 = 7 ns
  MCM69R537/618 – 8 = 8 ns
- 119 Bump, 50 mil (1.27 mm) Pitch, 14 mm x 22 mm Plastic Ball Grid Array (PBGA) Package

This document contains information on a new product. Specifications and information herein are subject to change without notice.

4/2/97

FUNCTIONAL BLOCK DIAGRAM



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PIN ASSIGNMENTS

TOP VIEW

MCM69R537

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	NC	NC	NC	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
E	DQc	DQc	V_{SS}	$\overline{SS}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{G}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{SBc}$	NF	$\overline{SBb}$	DQb	DQb
H	DQc	DQc	V_{SS}	NF	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CK	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{SBd}$	$\overline{CK}$	$\overline{SBa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{SW}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
P	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
R	NC	SA	V_{SS}	V_{DD}	V_{DD}	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69R619

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	NC	NC	NC	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQb	NC	V_{SS}	NC	V_{SS}	DQa	NC
E	NC	DQb	V_{SS}	$\overline{SS}$	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	$\overline{SBb}$	NF	V_{SS}	NC	DQa
H	DQb	NC	V_{SS}	NF	V_{SS}	DQa	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	CK	V_{SS}	NC	DQa
L	DQb	NC	V_{SS}	$\overline{CK}$	$\overline{SBa}$	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{SW}$	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	SA	V_{SS}	DQa	NC
P	NC	DQb	V_{SS}	SA	V_{SS}	NC	DQa
R	NC	SA	V_{SS}	V_{DD}	V_{DD}	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69R537 PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6K, 7K, 6L, 7L, 6M, 6N, 7N, 6P, 7P (b) 6D, 7D, 6E, 7E, 6F, 6G, 7G, 6H, 7H (c) 1D, 2D, 1E, 2E, 2F, 1G, 2G, 1H, 2H (d) 1K, 2K, 1L, 2L, 2M, 1N, 2N, 1P, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 3T, 4T, 5T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 5G, 3G, 3L (a), (b), (c), (d)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
7T	ZZ	Input	Sleep mode, active high.
4C, 2J, 4J, 6J, 4R, 5R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 3H, 5H, 3K, 5K, 3M, 5M, 3N, 5N, 3P, 5P, 3R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 3B, 4B, 5B, 6B, 7B, 1C, 7C, 4D, 3J, 5J, 1R, 7R, 1T, 2T, 6T, 6U	NC	—	No Connection: There is no connection to the chip.
4G, 4H	NF	—	No Function: There is an internal connection to the chip, but the pin has no function on this device.

MCM69R619 PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6D, 7E, 6F, 7G, 6H, 7K, 6L, 6N, 7P (b) 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 2T, 3T, 5T, 6T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 3G (a), (b)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
7T	ZZ	Input	Sleep mode, active high.
4C, 2J, 4J, 6J, 4R, 5R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P, 3R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 3B, 4B, 5B, 6B, 7B, 1C, 7C, 2D, 4D, 7D, 1E, 6E, 2F, 1G, 6G, 2H, 7H, 3J, 5J, 1K, 6K, 2L, 7L, 6M, 2N, 7N, 1P, 6P, 1R, 7R, 1T, 4T, 6U	NC	—	No Connection: There is no connection to the chip.
4G, 4H	NF	—	No Function: There is an internal connection to the chip, but the pin has no function on this device.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS}, See Note 1)

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Output Supply Voltage	V_{DDQ}	– 0.5 to V_{DD} + 0.5	V
Voltage On Any Pin	V_{in}	– 0.5 to V_{DD} + 0.5	V
Input Current (per I/O)	I_{in}	± 50	mA
Output Current (per I/O)	I_{out}	± 70	mA
Power Dissipation (See Note 2)	P_D	—	W
Operating Temperature	T_A	0 to + 70	°C
Temperature Under Bias	T_{bias}	–10 to + 85	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability will be dependent upon package characteristics and use environment. See enclosed thermal impedance data.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

PBGA PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (Still Air)		$R_{\theta JA}$	59	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Single Layer Board	$R_{\theta JA}$	44	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Four Layer Board	$R_{\theta JA}$	28	°C/W	
Junction to Board (Bottom)		$R_{\theta JB}$	18	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, pwer dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

($0°C \le T_A \le 70°C$, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (See Notes 1 through 4)

Parameter		Symbol	Min	Typical –5	Typical –6	Typical –7	Typical –8	Max	Unit	Notes
Core Power Supply Voltage		V_{DD}	3.15	—	—	—	—	3.6	V	
Output Driver Supply Voltage		V_{DDQ}	1.4	—	—	—	—	1.6	V	
Active Power Supply Current	(x18) (x36)	I_{DD1}	— —	TBD TBD	TBD TBD	TBD TBD	TBD TBD	TBD TBD	mA	5
Quiescent Active Power Supply Current	(x18) (x36)	I_{DD2}	— —	TBD TBD	TBD TBD	TBD TBD	TBD TBD	TBD	mA	6, 10
Active Standby Power Supply Current	(x18) (x36)	I_{SB1}	— —	TBD TBD	TBD TBD	TBD TBD	TBD TBD	TBD	mA	7
Quiescent Standby Power Supply Current	(x18) (x36)	I_{SB2}	— —	TBD TBD	TBD TBD	TBD TBD	TBD TBD	TBD	mA	8, 10
Sleep Mode Power Supply Current		I_{SB3}	—	TBD	TBD	TBD	TBD	TBD	mA	9, 10

NOTES:
1. All data sheet parameters specified to full range of V_{DD} unless otherwise noted. All voltages are referenced to voltage applied to V_{SS} bumps.
2. Supply voltage applied to V_{DD} connections.
3. Supply voltage applied to V_{DDQ} connections.
4. All power supply currents measured with outputs open or deselected.
5. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered active, 50% read cycles.
6. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered active.
7. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered inactive.
8. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered inactive, ZZ low.
9. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered inactive, ZZ high.
10. 200 mV $\ge V_{in} \ge V_{DDQ} - 200$ mV.

DC INPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
DC Input Logic High	V_{IH} (dc)	2.0	$V_{DD} + 0.3$	V	
DC Input Logic Low	V_{IL} (dc)	– 0.3	0.8	V	1
Input Leakage Current	I_{lkg}	—	± 5	µA	2
Clock Input Leakage Current	I_{clkg}	—	± 8	µA	2
Clock Input Signal Voltage	V_{in}	– 0.3	$V_{DD} + 0.3$	V	
Clock Input Differential Voltage	V_{DIF} (dc)	0.2	$V_{DD} + 0.6$	V	3
Clock Input Common Mode Voltage Range (See Figure 3)	V_{CM} (dc)	1.1	2.1	V	4

NOTES:
1. Inputs may undershoot to – 0.5 V (peak) for up to 20% t_{KHKH} (e.g., 2 ns at a clock cycle time of 10 ns).
2. $0 V \le V_{in} \le V_{DD}$.
3. Minimum instantaneous differential input voltage required for differential input clock operation.
4. Maximum rejectable common mode input voltage variation.

DC OUTPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
Output Leakage Current	I_{lkg}	–1.0	1.0	µA	
Output Low Voltage	V_{OL}	—	0.4	V	1
Output High Voltage	V_{OH}	2.4	—	V	2

NOTES:
1. I_{OL} = 8.0 mA.
2. I_{OH} = – 8.0 mA.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, 0°C ≤ T_A ≤ 70°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	5	pF
Input/Output Capacitance	$C_{I/O}$	7	8	pF
CK, $\overline{CK}$ Capacitance	C_{CK}	4	5	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

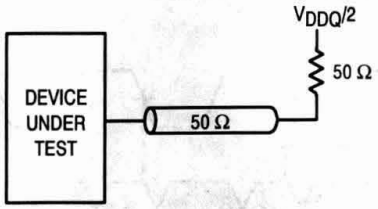
(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V
Clock Input Timing Reference Level ..... Differential Cross–Point
Clock Input Timing Pulse Level ..... 1.8 V to 2.1 V

READ/WRITE CYCLE TIMING (See Note 3)

Parameter	Symbol	MCM69R537–5 MCM69R619–5		MCM69R537–6 MCM69R619–6		MCM69R537–7 MCM69R619–7		MCM69R537–8 MCM69R619–8		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	5	—	6	—	7	—	8	—	ns	
Clock High Pulse Width	t_{KHKL}	2.4	—	2.4	—	2.8	—	3.2	—	ns	
Clock Low Pulse Width	t_{KLKH}	2.4	—	2.4	—	2.8	—	3.2	—	ns	
Clock High to Output Low–Z	t_{KHQX1}	1	—	1	—	1	—	1	—	ns	2
Clock High to Output Valid	t_{KHQV}	—	2.5	—	3	—	3.5	—	4	ns	1
Clock High to Output Hold	t_{KHQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	2
Clock High to Output High–Z	t_{KHQZ}	—	2.5	—	3	—	3.5	—	4	ns	2
Output Enable Low to Output Low–Z	t_{GLQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	2
Output Enable Low to Output Valid	t_{GLQV}	—	2.5	—	3	—	3.5	—	4	ns	2
Output Enable to Output Hold	t_{GHQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	2
Output Enable High to Output High–Z	t_{GHQZ}	—	2.5	—	3	—	3.5	—	4	ns	2
Setup Times: Address Data In Chip Select Write Enable	t_{AVKH} t_{DVKH} t_{SVKH} t_{WVKH}	0.5	—	0.5	—	0.5	—	0.5	—	ns	
Hold Times: Address Data In Chip Select Write Enable	t_{KHAX} t_{KHDX} t_{KHSX} t_{KHWX}	1	—	1	—	1	—	1	—	ns	

NOTES:
1. Tested per AC Test Load diagram. See Figure 1.
2. Measured at ± 200 mV from steady state.
3. In no case may control input signals (e.g., $\overline{SS}$) be operated with pulse widths less than the minimum clock input pulse width specifications (e.g., t_{KHKL}) or at frequencies that exceed the applied K clock frequency.



TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Figure 1. Test Load

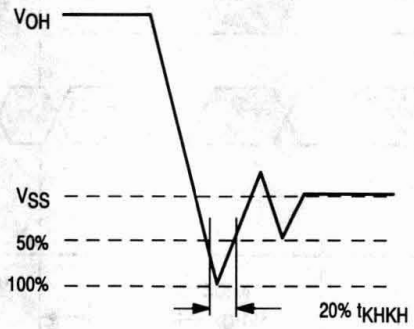
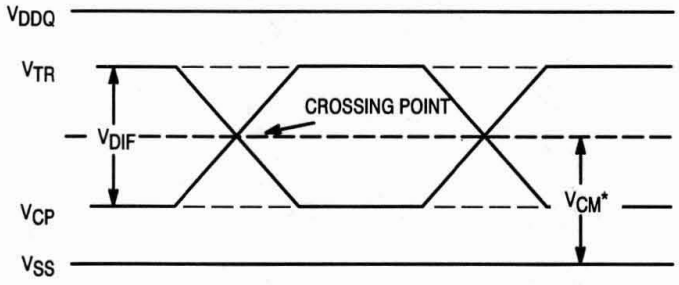


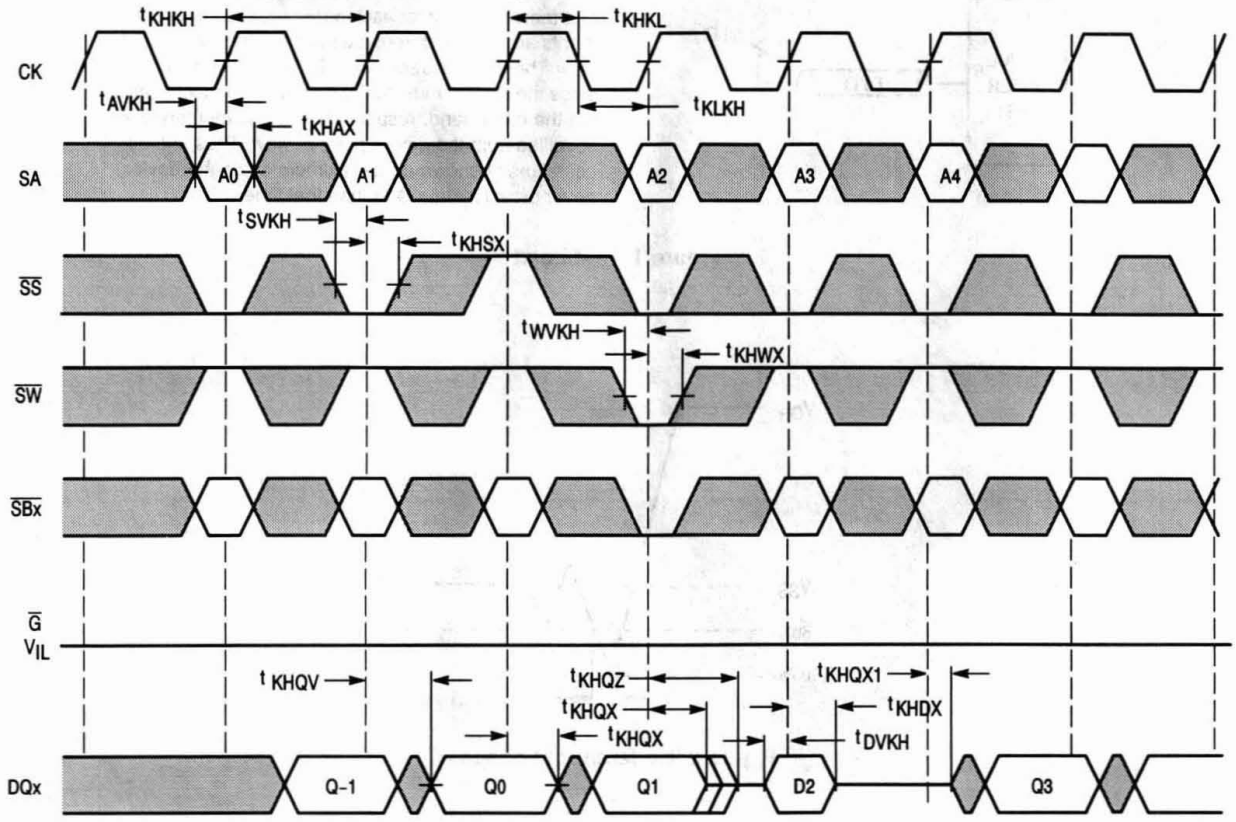
Figure 2. Undershoot Voltage



*V_{CM}, the Common Mode Input Voltage, equals $V_{TR} - ((V_{TR} - V_{CP})/2)$.

Figure 3. Differential Inputs/Common Mode Input Voltage

REGISTER/REGISTER READ–WRITE–READ CYCLES



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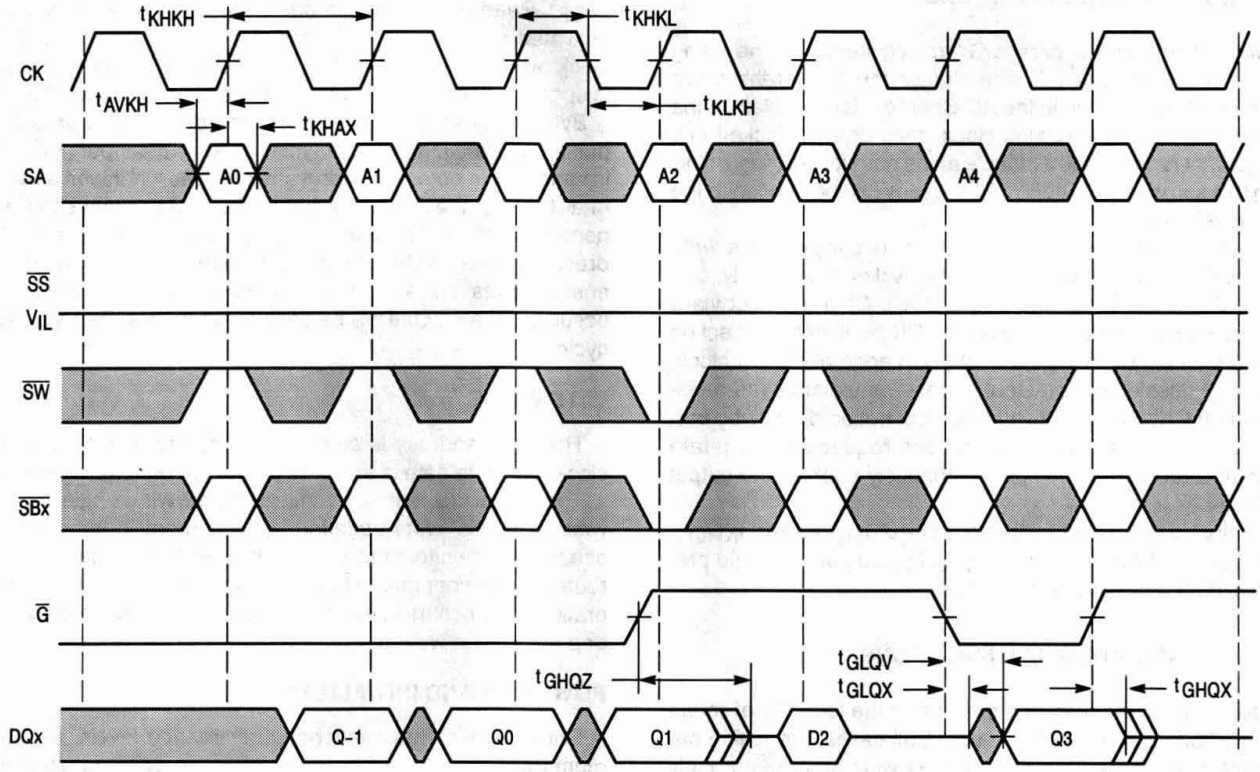
REGISTER/REGISTER READ–WRITE–READ
($\overline{G}$ Controlled)



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FUNCTIONAL OPERATION

READ AND WRITE OPERATIONS

All control signals except $\overline{G}$ are registered on the rising edge of the CK clock. These signals must meet the setup and hold times shown in the AC Characteristics table. On the rising edge of the following clock, read data is clocked into the output register and available at the outputs at t_{KHQV}. During this same cycle a new read address can be applied to the address pins.

A deselect cycle (dead cycle) must occur prior to a write cycle. Read cycles may follow write cycles immediately.

$\overline{G}$, $\overline{SS}$, and $\overline{SW}$ control output drive. Chip deselect via a high on $\overline{SS}$ at the rising edge of the CK clock has its effect on the output drivers after the next rising edge of the CK clock. $\overline{SW}$ low deselects the output drivers immediately (as registered by CK). Output drive is also controlled directly by output enable, $\overline{G}$. No clock edges are required to generate output disable with $\overline{G}$. $\overline{G}$ asynchronously enables the output drivers.

Output data will be valid the latter of t_{GLQV} and t_{KHQV}. Outputs will begin driving at t_{KHQX1}. Outputs will hold previous data until t_{KHQX} or t_{GHQX}.

WRITE AND BYTE WRITE FUNCTIONS

Note that in the following discussion the term "byte" refers to nine bits of the RAM I/O bus. In all cases, the timing parameters described for synchronous write input ($\overline{SW}$) apply to each of the byte write enable inputs ($\overline{SBa}$, $\overline{SBb}$, etc.).

Byte write enable inputs have no effect on read cycles. This allows the system designer not interested in performing byte writes to connect the byte enable inputs to active low (V_{SS}). Reads of all bytes proceed normally and write cycles, activated via a low on $\overline{SW}$, and the rising edge of the CK clock, write the entire RAM I/O width. This way the designer is spared having to drive multiple write input buffer loads.

Byte writes are performed using the byte write enable inputs in conjunction with the synchronous write input ($\overline{SW}$). It is important to note that writing any one byte will inhibit a read of all bytes at the current address. The RAM cannot simultaneously read one byte and write another at the same address. A write cycle initiated with none of the byte write enable inputs active is neither a read or a write. No write will occur, but the outputs will be deselected as in a normal write cycle.

LATE WRITE

The write address is sampled on the first rising edge of clock and write data is sampled on the following rising edge.

The late write feature is implemented with single stage write buffering. Write buffering is transparent to the user. A comparator monitors the address bus and, when necessary, routes buffer contents to the outputs to assure coherent operation. This occurs in all cases whether there is a byte write or a full word is written.

POWER UP AND INITIALIZATION

Once supplies have reached specification levels, a minimum dwell of 1.0 ms with CK clock inputs cycling is required before beginning normal operations.

SERIAL BOUNDARY SCAN TEST ACCESS PORT OPERATION

OVERVIEW

The serial boundary scan test access port (TAP) on this RAM is designed to operate in a manner consistent with IEEE Standard 1149.1–1990 (commonly referred to as JTAG), but does not implement all of the functions required for 1149.1 compliance. Certain functions have been modified or eliminated because their implementation places extra delays in the RAMs critical speed path. Nevertheless, the RAM supports the standard TAP controller architecture. (The TAP controller is the state machine that controls the TAPs operation) and can be expected to function in a manner that does not conflict with the operation of devices with Standard 1149.1 compliant TAPs. The TAP operates using conventional JEDEC Standard 8–1B Low Voltage (3.3 V) TTL / CMOS logic level signaling.

DISABLING THE TEST ACCESS PORT

It is possible to use this device without utilizing the TAP. To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid level inputs. TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a 1 k resistor. TDO should be left unconnected.

3

TAP DC OPERATING CHARACTERISTICS

(0°C ≤ T_A ≤ 70 °C, Unless Otherwise Noted)

Parameter	Symbol	Min	Max	Unit	Note
Logic Input Logic High	$V_{IH}1$	2.0	V_{DD} + 0.3	V	
Logic Input Logic Low	$V_{IL}1$	– 0.3	0.8	V	
Logic Input Leakage Current	I_{lkg}	—	± 5	µA	1
Output Logic Low	$V_{OL}1$	—	0.2	V	2
Output Logic High	$V_{OH}1$	V_{DD} – 0.2	—	V	3
Output Logic Low	$V_{OL}2$	—	0.4	V	4
Output Logic High	$V_{OH}2$	2.4	—	V	5

NOTES:

1. 0 V ≤ V_{in} ≤ V_{DD} for all logic input pins.
2. $I_{OL}1$ ≤ 100 µA @ V_{OL} = 0.2 V. Sampled, not 100% tested.
3. $|I_{OH}1|$ ≤ 100 µA @ V_{DDQ} – 0.2 V. Sampled, not 100% tested.
4. $I_{OL}2$ ≤ 8 mA @ V_{OL} = 0.4 V.
5. $|I_{OH}2|$ ≤ 8 mA @ V_{OH} = 2.4 V.

TAP AC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V

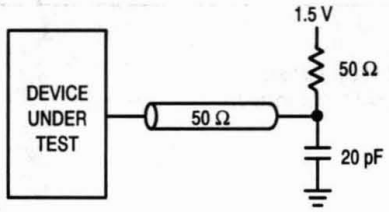
Output Test Load ..... 50 Ω Parallel Terminated T–line with 20 pF Receiver Input Capacitance
Test Load Termination Supply Voltage (V_T) ..... 1.5 V

TAP CONTROLLER TIMING

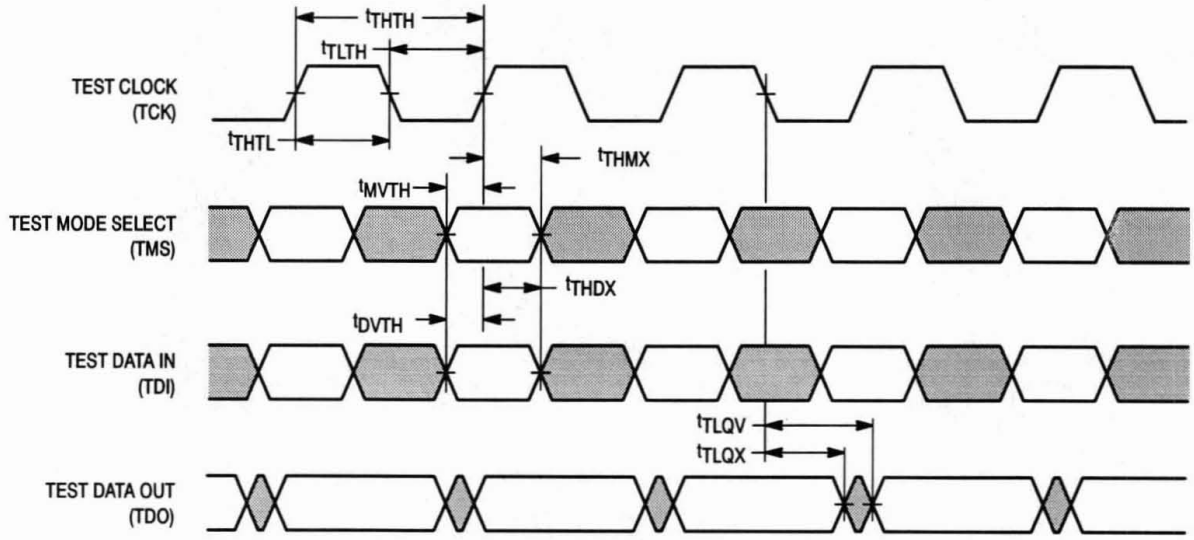
Parameter	Symbol	Min	Max	Unit	Notes
Cycle Time	t_{THTH}	100	—	ns	
Clock High Time	t_{THTL}	40	—	ns	
Clock Low Time	t_{TLTH}	40	—	ns	
TMS Setup	t_{MVTH}	10	—	ns	
TMS Hold	t_{THMX}	10	—	ns	
TDI Valid to TCK High	t_{DVTH}	10	—	ns	
TCK High to TDI Don't Care	t_{THDX}	10	—	ns	
Capture Setup	t_{CS}	10	—	ns	1
Capture Hold	t_{CH}	10	—	ns	1
TCK Low to TDO Unknown	t_{TLQX}	0	—	ns	
TCK Low to TDO Valid	t_{TLOV}	—	20	ns	

NOTES:
1. t_{CS} + t_{CH} defines the minimum pause in RAM I/O pad transitions to assure accurate pad data capture.

AC TEST LOAD



TAP CONTROLLER TIMING DIAGRAM



TEST ACCESS PORT PINS

TCK – TEST CLOCK (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

TMS – TEST MODE SELECT (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.

TDI – TEST DATA IN (INPUT)

The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (refer to Figure 6 TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.

TDO – TEST DATA OUT (OUTPUT)

Output that is active depending on the state of the TAP state machine (refer to Figure 5 TAP Controller State Diagram). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

TRST – TAP RESET

This device does not have a TRST pin. TRST is optional in **IEEE 1149.1.** The test–logic reset state is entered while TMS is held high for five rising edges of TCK. Power on reset circuitry is included internally. This type of reset does not affect the operation of the system logic. The reset affects test logic only.

TEST ACCESS PORT REGISTERS

OVERVIEW

The various TAP registers are selected (one at a time) via the sequences of ones and zeros input to the TMS pin as the TCK is strobed. Each of the TAPs registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on subsequent falling edge of TCK. When a register is selected it is "placed" between the TDI and TDO pins.

INSTRUCTION REGISTER

The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run test/idle or the various data register states. The instructions are three bits long. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power–up or whenever the controller is placed in test–logic–reset state.

BYPASS REGISTER

The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.

BOUNDARY SCAN REGISTER

The boundary scan register is identical in length to the number of active input and I/O connections on the RAM (not counting the TAP pins). This also includes a number of place holder locations (always set to a logic 1) reserved for density upgrade address pins. There are a total of 70 bits in the case of the x36 device and 51 bits in the case of the x18 device. The boundary scan register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture–DR state and then is placed between the TDI and TDO pins when the controller is moved to shift–DR state. Several TAP instructions can be used to activate the boundary scan register.

The Bump/Bit Scan Order tables describe which device bump connects to each boundary scan register location. The first column defines the bit's position in the boundary scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the input or I/O at the bump and the third column is the bump number.

IDENTIFICATION (ID) REGISTER

The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture–DR state with the IDCODE command loaded in the instruction register. The code is loaded from a 32 bit on–chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into shift–DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Presence Indicator

Bit #	0
Value	1

Motorola JEDEC ID Code (Compressed Format, per IEEE Standard 1149.1 – 1990

Bit #	11	10	9	8	7	6	5	4	3	2	1
Value	0	0	0	0	0	0	0	1	1	1	0

Reserved For Future Use

Bit #	17	16	15	14	13	12
Value	x	x	x	x	x	x

Device Width

Configuration	Bit #	22	21	20	19	18
32Kx36	Value	0	0	1	0	0
64Kx18	Value	0	0	0	1	1

Device Depth

Configuration	Bit #	27	26	25	24	23
32Kx36	Value	0	0	0	1	1
64Kx18	Value	0	0	1	0	0

Revision Number

Bit #	31	30	29	28
Value	x	x	x	x

Figure 4. ID Register Bit Meanings

MCM69R537 Bump/Bit Scan Order

BIT #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	NC	3B
2	SA	4P		37	NC	2B
3	SA	4T		38	SA	3A
4	SA	6R		39	SA	3C
5	SA	5T		40	SA	2C
6	ZZ	7T		41	SA	2A
7	DQa	6P		42	DQc	2D
8	DQa	7P		43	DQc	1D
9	DQa	6N		44	DQc	2E
10	DQa	7N		45	DQc	1E
11	DQa	6M		46	DQc	2F
12	DQa	6L		47	DQc	2G
13	DQa	7L		48	DQc	1G
14	DQa	6K		49	DQc	2H
15	DQa	7K		50	DQc	1H
16	$\overline{SBa}$	5L		51	$\overline{SBc}$	3G
17	$\overline{CK}$	4L		52	ZQ	4D
18	CK	4K		53	$\overline{SS}$	4E
19	$\overline{G}$	4F		54	NF	4G
20	$\overline{SBb}$	5G		55	NF	4H
21	DQb	7H		56	$\overline{SW}$	4M
22	DQb	6H		57	$\overline{SBd}$	3L
23	DQb	7G		58	DQd	1K
24	DQb	6G		59	DQd	2K
25	DQb	6F		60	DQd	1L
26	DQb	7E		61	DQd	2L
27	DQb	6E		62	DQd	2M
28	DQb	7D		63	DQd	1N
29	DQb	6D		64	DQd	2N
30	SA	6A		65	DQd	1P
31	SA	6C		66	DQd	2P
32	SA	5C		67	SA	3T
33	SA	5A		68	SA	2R
34	NC	6B		69	SA	4N
35	NC	5B		70	M1	3R

MCM69R619 Bump/Bit Scan Order

Bit #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	$\overline{SBb}$	3G
2	SA	6T		37	ZQ	4D
3	SA	4P		38	$\overline{SS}$	4E
4	SA	6R		39	NF	4G
5	SA	5T		40	NF	4H
6	ZZ	7T		41	$\overline{SW}$	4M
7	DQa	7P		42	DQb	2K
8	DQa	6N		43	DQb	1L
9	DQa	6L		44	DQb	2M
10	DQa	7K		45	DQb	1N
11	$\overline{SBa}$	5L		46	DQb	2P
12	$\overline{CK}$	4L		47	SA	3T
13	CK	4K		48	SA	2R
14	$\overline{G}$	4F		49	SA	4N
15	DQa	6H		50	SA	2T
16	DQa	7G		51	M1	3R
17	DQa	6F				
18	DQa	7E				
19	DQa	6D				
20	SA	6A				
21	SA	6C				
22	SA	5C				
23	SA	5A				
24	NC	6B				
25	NC	5B				
26	NC	3B				
27	NC	2B				
28	SA	3A				
29	SA	3C				
30	SA	2C				
31	SA	2A				
32	DQb	1D				
33	DQb	2E				
34	DQb	2G				
35	DQb	1H				

NOTES:

1. The NC pads listed in this table are indeed no connects, but are represented in the boundary scan register by a "place holder" bit that is forced to logic 1. These pads are reserved for use as address inputs on higher density RAMs that follow this pad out and scan order standard.
2. CK, $\overline{CK}$, are sampled individually. $\overline{CK}$ is not simply a forced complement of the CK input. In scan mode these differential inputs are referenced to V_{ref}, not each other.
3. M1 and M2 are not ordinary inputs and may not respond to standard I/O logic levels. M1 and M2 must be driven to within 100 mV of a V_{DD} or V_{SS} supply rail to ensure consistent results.
4. ZZ must remain at V_{IL} during boundary scan to ensure consistent results.

TAP Controller Instruction Set

OVERVIEW

There are two classes of instructions defined in the Standard 1149.1–1990; the standard (public) instructions, and device specific (private) instructions. Some public instructions, are mandatory for 1149.1 compliance. Optional public instructions must be implemented in prescribed ways.

Although the TAP controller in this device follows the 1149.1 conventions, it is not 1194.1 compliant because some of the mandatory instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads, but cannot be used to load address, data or control signals into the RAM or to preload the I/O buffers. In other words, the device will not perform Standard 1149.1 EXTEST, INTEST or the preload portion of the SAMPLE / PRELOAD command.

When the TAP controller is placed in capture–IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the shift–IR state the instruction register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to update–IR state. The TAP instruction sets for this device are listed in the following tables.

STANDARD (PUBLIC) INSTRUCTIONS

BYPASS

The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift–DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

Sample/preload is a Standard 1149.1 mandatory public instruction. When the sample / preload instruction is loaded in the Instruction register, moving the TAP controller into the capture–DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set–up plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register.

Moving the controller to shift–DR state then places the boundary scan register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the update–DR state with the SAMPLE / PRELOAD instruction loaded in the instruction register has the same effect as the pause–DR command. This functionality is not Standard 1149.1 compliant.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic 0s. EXTEST is not implemented in this device. Therefore this device is not 1149.1 compliant. Nevertheless, this RAMs TAP does respond to an all zeros instruction, as follows. With the EXTEST (000) instruction loaded in the instruction register the RAM responds just as it does in response to the SAMPLE / PRELOAD instruction described above, except the RAM outputs are forced to high–Z any time the instruction is loaded.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture–DR mode and places the ID register between the TDI and TDO pins in shift–DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test–logic–reset state.

THE DEVICE SPECIFIC (PUBLIC) INSTRUCTION

SAMPLE–Z

If the SAMPLE–Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high–Z) and the boundary scan register is connected between TDI and TDO when the TAP controller is moved to the shift–DR state.

THE DEVICE SPECIFIC (PRIVATE) INSTRUCTION

NOOP

Do not use these instructions; they are reserved for future use.

STANDARD (PUBLIC) INSTRUCTION CODES

Instruction	Code*	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM outputs to High–Z state. *NOT 1149.1 COMPLIANT*
IDCODE	001**	Preloads ID register and places it between TDI and TDO. Does not affect RAM operation.
SAMPLE / PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect RAM operation. Does not implement 1149.1 Preload function. * NOT 1149.1 COMPLIANT *
BYPASS	111	Places bypass register between TDI and TDO. Does not affect RAM operation.
SAMPLE–Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM output drivers to High–Z.

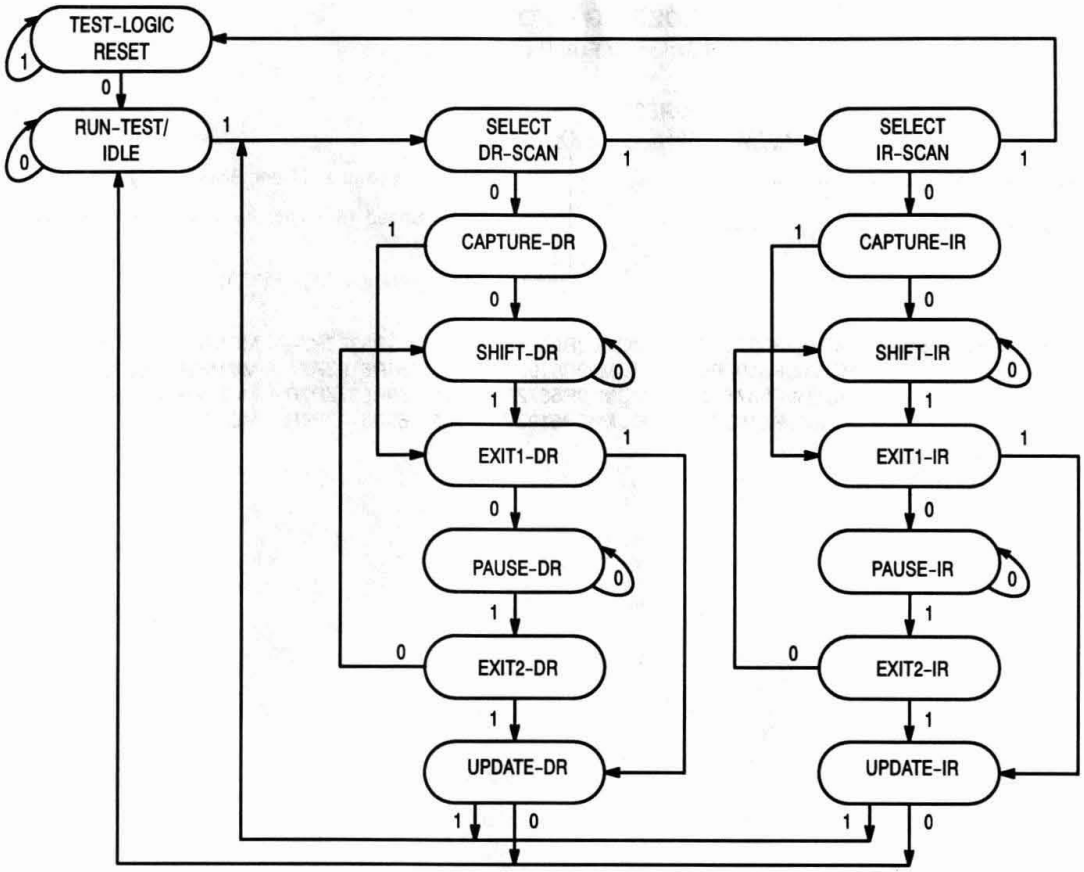
3

* Instruction codes expressed in binary, MSB on left, LSB on right.
** Default instruction automatically loaded at power–up and in test–logic–reset state.

STANDARD (PRIVATE) INSTRUCTION CODES

Instruction	Code*	Description
NO OP	011	Do not use these instructions; they are reserved for future use.
NO OP	101	Do not use these instructions; they are reserved for future use.
NO OP	110	Do not use these instructions; they are reserved for future use.

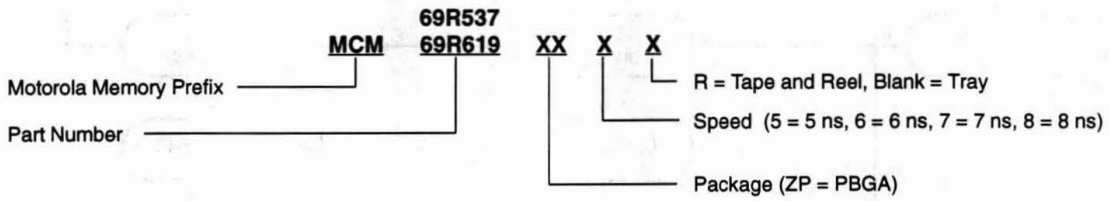
* Instruction codes expressed in binary, MSB on left, LSB on right.



NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 5. TAP Controller State Diagram

ORDERING INFORMATION
(Order by Full Part Number)


69R537
MCM 69R619 XX X X
Motorola Memory Prefix
Part Number
R = Tape and Reel, Blank = Tray
Speed (5 = 5 ns, 6 = 6 ns, 7 = 7 ns, 8 = 8 ns)
Package (ZP = PBGA)

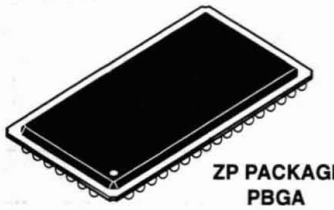
Full Part Numbers				
	MCM69R537ZP5	MCM69R537ZP6	MCM69R537ZP7—	MCM69R537ZP8
	MCM69R619ZP5	MCM69R619ZP6	MCM69R619ZP7	MCM69R619ZP8
	MCM69R537ZP5R	MCM69R537ZP6R	MCM69R537ZP7R	MCM69R537ZP8R
	MCM69R619ZP5R	MCM69R619ZP6R	MCM69R619ZP7R	MCM69R619ZP8R

3

MCM69R538
MCM69R620

Advance Information

1M Late Write 2.5 V I/O



ZP PACKAGE
PBGA
CASE 999–01

3

The MCM69R538/620 is a 1 megabit synchronous late write fast static RAM designed to provide high performance in secondary cache, ATM switch, Telecom, and other high speed memory applications. The MCM69R620 organized as 64K words by 18 bits, and the MCM69R538 organized as 32K words by 36 bits wide are fabricated in Motorola's high performance silicon gate BiCMOS technology.

The differential CK clock inputs control the timing of read/write operations of the RAM. At the rising edge of the CK clock all addresses, write enables, and synchronous selects are registered. An internal buffer and special logic enable the memory to accept write data on the rising edge of the CK clock a cycle after address and control signals. Read data is driven on the rising edge of the CK clock also.

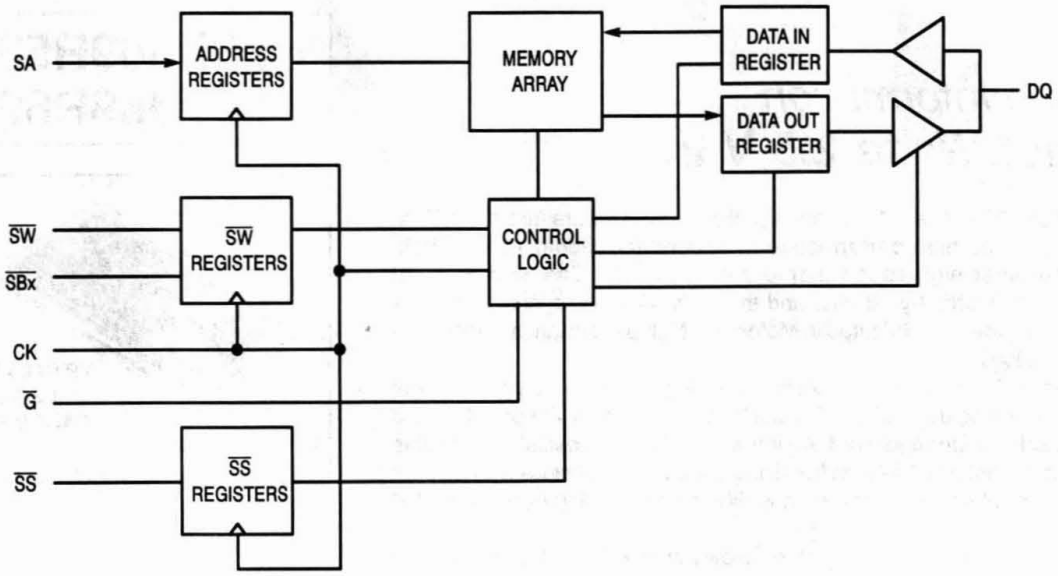
The synchronous write and byte enables allow writing to individual bytes or the entire word.

- Byte Write Control
- Single 3.3 V + 10%, – 5% Operation
- 2.5 V I/O
- Register to Register Synchronous Operation
- Asynchronous Output Enable
- Boundary Scan (JTAG) IEEE 1149.1 Compatible
- Differential Clock Inputs
- Optional x 18 or x 36 organization
- MCM69R538/618 – 5 = 5 ns
  MCM69R538/618 – 6 = 6 ns
  MCM69R538/618 – 7 = 7 ns
  MCM69R538/618 – 8 = 8 ns
- 119 Bump, 50 mil (1.27 mm) Pitch, 14 mm x 22 mm Plastic Ball Grid Array (PBGA) Package

This document contains information on a new product. Specifications and information herein are subject to change without notice.

4/2/97

FUNCTIONAL BLOCK DIAGRAM



3

PIN ASSIGNMENTS

TOP VIEW

MCM69R538

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	NC	NC	NC	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
E	DQc	DQc	V_{SS}	$\overline{SS}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{G}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{SBc}$	NF	$\overline{SBb}$	DQb	DQb
H	DQc	DQc	V_{SS}	NF	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CK	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{SBd}$	$\overline{CK}$	$\overline{SBa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{SW}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
P	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
R	NC	SA	V_{SS}	V_{DD}	V_{DD}	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69R620

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	NC	NC	NC	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQb	NC	V_{SS}	NC	V_{SS}	DQa	NC
E	NC	DQb	V_{SS}	$\overline{SS}$	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	$\overline{SBb}$	NF	V_{SS}	NC	DQa
H	DQb	NC	V_{SS}	NF	V_{SS}	DQa	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	CK	V_{SS}	NC	DQa
L	DQb	NC	V_{SS}	$\overline{CK}$	$\overline{SBa}$	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{SW}$	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	SA	V_{SS}	DQa	NC
P	NC	DQb	V_{SS}	SA	V_{SS}	NC	DQa
R	NC	SA	V_{SS}	V_{DD}	V_{DD}	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69R538 PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6K, 7K, 6L, 7L, 6M, 6N, 7N, 6P, 7P (b) 6D, 7D, 6E, 7E, 6F, 6G, 7G, 6H, 7H (c) 1D, 2D, 1E, 2E, 2F, 1G, 2G, 1H, 2H (d) 1K, 2K, 1L, 2L, 2M, 1N, 2N, 1P, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 3T, 4T, 5T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 5G, 3G, 3L (a), (b), (c), (d)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
7T	ZZ	Input	Sleep mode, active high.
4C, 2J, 4J, 6J, 4R, 5R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 3H, 5H, 3K, 5K, 3M, 5M, 3N, 5N, 3P, 5P, 3R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 3B, 4B, 5B, 6B, 7B, 1C, 7C, 4D, 3J, 5J, 1R, 7R, 1T, 2T, 6T, 6U	NC	—	No Connection: There is no connection to the chip. Note: 3J and 5J are tied common.
4G, 4H	NF	—	No Function: There is an internal connection to the chip, but the pin has no function on this device.

MCM69R620 PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6D, 7E, 6F, 7G, 6H, 7K, 6L, 6N, 7P (b) 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 2T, 3T, 5T, 6T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 3G (a), (b)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
7T	ZZ	Input	Sleep mode, active high.
4C, 2J, 4J, 6J, 4R, 5R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P, 3R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 3B, 4B, 5B, 6B, 7B, 1C, 7C, 2D, 4D, 7D, 1E, 6E, 2F, 1G, 6G, 2H, 7H, 3J, 5J, 1K, 6K, 2L, 7L, 6M, 2N, 7N, 1P, 6P, 1R, 7R, 1T, 4T, 6U	NC	—	No Connection: There is no connection to the chip. Note: 3J and 5J are tied common.
4G, 4H	NF	—	No Function: There is an internal connection to the chip, but the pin has no function on this device.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS}, See Note 1)

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Output Supply Voltage	V_{DDQ}	– 0.5 to V_{DD} + 0.5	V
Voltage On Any Pin	V_{in}	– 0.5 to V_{DD} + 0.5	V
Input Current (per I/O)	I_{in}	± 50	mA
Output Current (per I/O)	I_{out}	± 70	mA
Power Dissipation (See Note 2)	P_D	—	W
Operating Temperature	T_A	0 to + 70	°C
Temperature Under Bias	T_{bias}	–10 to + 85	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability will be dependent upon package characteristics and use environment. See enclosed thermal impedance data.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

3

PBGA PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (Still Air)		$R_{\theta JA}$	59	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Single Layer Board	$R_{\theta JA}$	44	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Four Layer Board	$R_{\theta JA}$	28	°C/W	
Junction to Board (Bottom)		$R_{\theta JB}$	18	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, pwer dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

($0°C \le T_A \le 70°C$, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (See Notes 1 through 4)

Parameter		Symbol	Min	Typical –5	Typical –6	Typical –7	Typical –8	Max	Unit	Notes
Core Power Supply Voltage		V_{DD}	3.15	—	—	—	—	3.6	V	
Output Driver Supply Voltage		V_{DDQ}	2.3	—	—	—	—	1.6	V	
Active Power Supply Current	(x18) (x36)	I_{DD1}	— —	TBD TBD	TBD TBD	TBD TBD	TBD TBD	TBD TBD	mA	5
Quiescent Active Power Supply Current	(x18) (x36)	I_{DD2}	— —	TBD TBD	TBD TBD	TBD TBD	TBD TBD	TBD TBD	mA	6, 9
Active Standby Power Supply Current	(x18) (x36)	I_{SB1}	— —	TBD TBD	TBD TBD	TBD TBD	TBD TBD	TBD TBD	mA	7
Quiescent Standby Power Supply Current	(x18) (x36)	I_{SB2}	— —	TBD TBD	TBD TBD	TBD TBD	TBD TBD	TBD TBD	mA	8, 9
Sleep Mode Power Supply Current		I_{SB3}	—	TBD	TBD	TBD	TBD	TBD	mA	8, 9

NOTES:
1. All data sheet parameters specified to full range of V_{DD} unless otherwise noted. All voltages are referenced to voltage applied to V_{SS} bumps.
2. Supply voltage applied to V_{DD} connections.
3. Supply voltage applied to V_{DDQ} connections.
4. All power supply currents measured with outputs open or deselected.
5. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered active, 50% read cycles.
6. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered active.
7. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered inactive.
8. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered inactive.
9. $200 \text{ mV} \ge V_{in} \ge V_{DDQ} - 200 \text{ mV}$.
10. Although considerable latitude in the selection of the nominal dc value (i.e., rms value) of V_{ref} is supported, the peak to peak ac component superimposed on V_{ref} may not exceed 5% of the dc component of V_{ref}.

DC INPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
DC Input Logic High	V_{IH} (dc)	1.7	$V_{DD} + 0.3$	V	
DC Input Logic Low	V_{IL} (dc)	– 0.3	0.7	V	1
Input Leakage Current	I_{lkg}	—	± 5	µA	2
Clock Input Leakage Current	I_{clkg}	—	± 8	µA	2
Clock Input Signal Voltage	V_{in}	– 0.3	$V_{DD} + 0.3$	V	
Clock Input Differential Voltage	V_{DIF}(dc)	0.2	$V_{DD} + 0.6$	V	3
Clock Input Common Mode Voltage Range (See Figure 3)	V_{CM}(dc)	1.1	2.1	V	4

NOTES:
1. Inputs may undershoot to – 0.5 V (peak) for up to 20% t_{KHKH} (e.g., 2 ns at a clock cycle time of 10 ns).
2. $0 \text{ V} \le V_{in} \le V_{DD}$ for all pins.
3. Minimum instantaneous differential input voltage required for differential input clock operation.
4. Maximum rejectable common mode input voltage variation.

DC OUTPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
Output Leakage Current	I_{lkg}	–1.0	1.0	µA	
Output Low Voltage	V_{OL}	—	0.7	V	1
Output High Voltage	V_{OH}	1.7	—	V	2

NOTES:
1. $I_{OL} = 8.0$ mA.
2. $I_{OH} = -8.0$ mA.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, 0°C ≤ T_A ≤ 70°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	5	pF
Input/Output Capacitance	$C_{I/O}$	7	8	pF
CK, $\overline{CK}$ Capacitance	C_{CK}	4	5	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

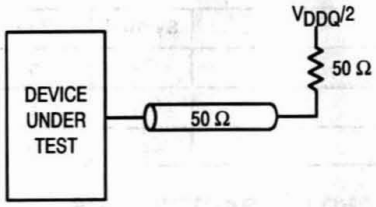
(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 2.5 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.25 V
Output Timing Reference Level ..... 1.25 V
Clock Input Timing Reference Level ..... Differential Cross–Point
Clock Input Pulse Level ..... 1.8 V to 2.1 V

READ/WRITE CYCLE TIMING (See Note 3)

Parameter	Symbol	MCM69R538–5 MCM69R620–5		MCM69R538–6 MCM69R620–6		MCM69R538–7 MCM69R620–7		MCM69R538–8 MCM69R620–8		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	5	—	6	—	7	—	8	—	ns	
Clock High Pulse Width	t_{KHKL}	2.4	—	2.4	—	2.8	—	3.2	—	ns	
Clock Low Pulse Width	t_{KLKH}	2.4	—	2.4	—	2.8	—	3.2	—	ns	
Clock High to Output Low–Z	t_{KHQX1}	1	—	1	—	1	—	1	—	ns	2
Clock High to Output Valid	t_{KHQV}	—	2.5	—	3	—	3.5	—	4	ns	1
Clock High to Output Hold	t_{KHQX}	1	—	1	—	1	—	0.5	—	ns	2
Clock High to Output High–Z	t_{KHQZ}	—	2.5	—	3	—	3.5	—	4	ns	2
Output Enable Low to Output Low–Z	t_{GLQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	2
Output Enable Low to Output Valid	t_{GLQV}	—	2.5	—	3	—	3.5	—	4	ns	2
Output Enable to Output Hold	t_{GHQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	2
Output Enable High to Output High–Z	t_{GHQZ}	—	2.5	—	3	—	3.5	—	4	ns	2
Setup Times: Address Data In Chip Select Write Enable	t_{AVKH} t_{DVKH} t_{SVKH} t_{WVKH}	0.5	—	0.5	—	0.5	—	0.5	—	ns	
Hold Times: Address Data In Chip Select Write Enable	t_{KHAX} t_{KHDX} t_{KHSX} t_{KHWX}	1	—	1	—	1	—	1	—	ns	

NOTES:
1. Tested per AC Test Load diagram. See Figure 1.
2. Measured at ± 200 mV from steady state.
3. In no case may control input signals (e.g., $\overline{SS}$) be operated with pulse widths less than the minimum clock input pulse width specifications (e.g., t_{KHKL}) or at frequencies that exceed the applied K clock frequency.



TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Figure 1. Test Loads

3

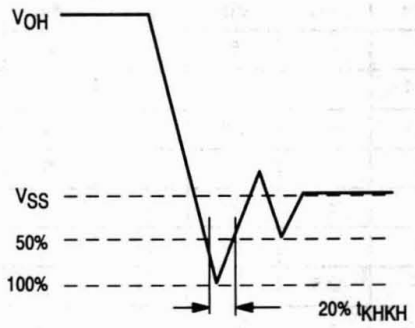
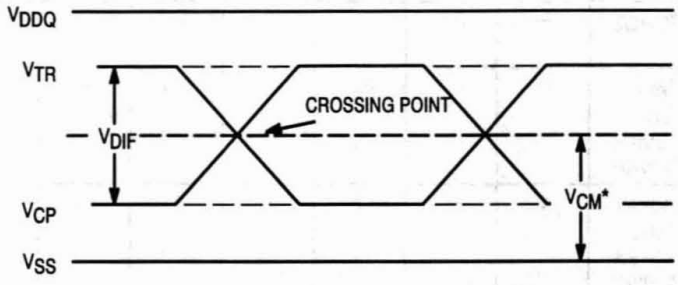


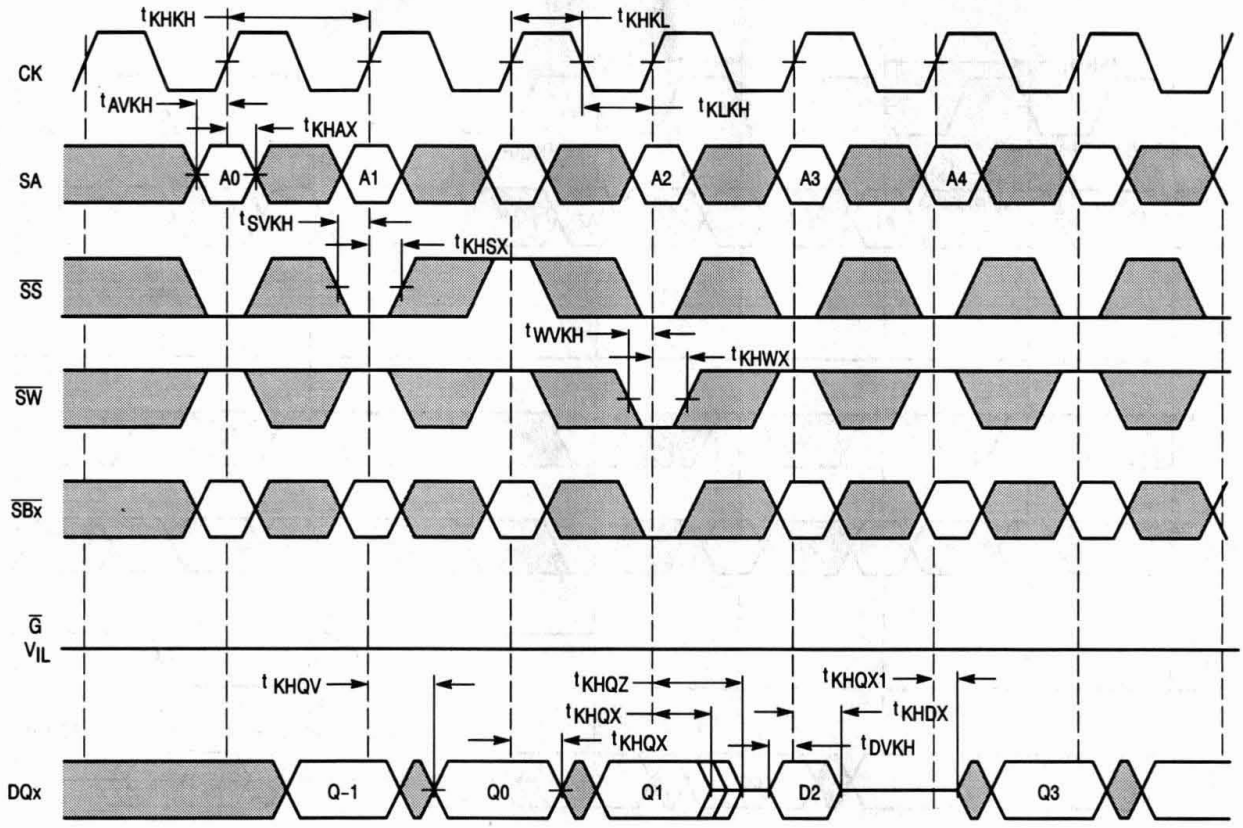
Figure 2. Undershoot Voltage



*V_{CM}, the Common Mode Input Voltage, equals $V_{TR} - ((V_{TR} - V_{CP})/2)$.

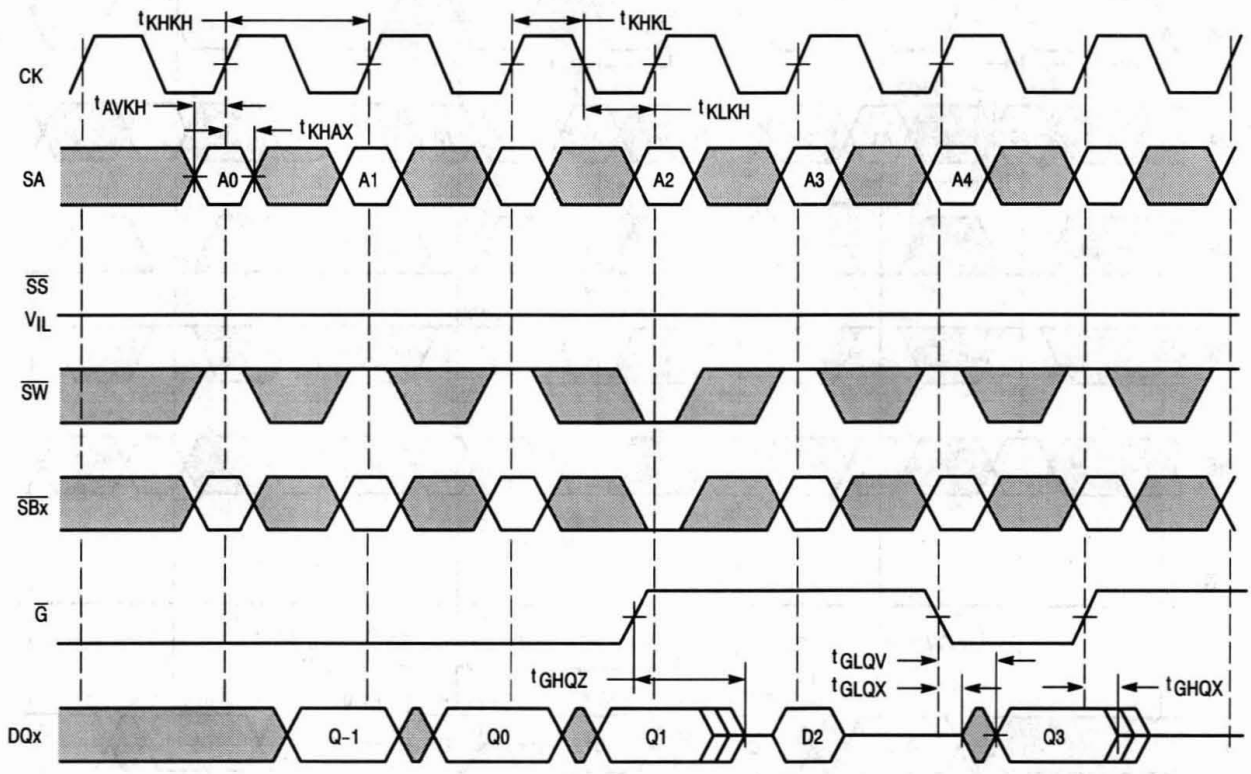
Figure 3. Differential Inputs/Common Mode Input Voltage

REGISTER/REGISTER READ–WRITE–READ CYCLES



3

REGISTER/REGISTER READ–WRITE–READ
($\overline{G}$ Controlled)



FUNCTIONAL OPERATION

READ AND WRITE OPERATIONS

All control signals except $\overline{G}$ are registered on the rising edge of the CK clock. These signals must meet the setup and hold times shown in the AC Characteristics table. On the rising edge of the following clock, read data is clocked into the output register and available at the outputs at t_{KHQV}. During this same cycle a new read address can be applied to the address pins.

A deselect cycle (dead cycle) must occur prior to a write cycle. Read cycles may follow write cycles immediately.

$\overline{G}$, $\overline{SS}$, and $\overline{SW}$ control output drive. Chip deselect via a high on $\overline{SS}$ at the rising edge of the CK clock has its effect on the output drivers after the next rising edge of the CK clock. $\overline{SW}$ low deselects the output drivers immediately (as registered by CK). Output drive is also controlled directly by output enable, $\overline{G}$. No clock edges are required to generate output disable with $\overline{G}$. $\overline{G}$ asynchronously enables the output drivers.

Output data will be valid the latter of t_{GLQV} and t_{KHQV}. Outputs will begin driving at t_{KHQX1}. Outputs will hold previous data until t_{KHQX} or t_{GHQX}.

WRITE AND BYTE WRITE FUNCTIONS

Note that in the following discussion the term "byte" refers to nine bits of the RAM I/O bus. In all cases, the timing parameters described for synchronous write input ($\overline{SW}$) apply to each of the byte write enable inputs ($\overline{SBa}$, $\overline{SBb}$, etc.).

Byte write enable inputs have no effect on read cycles. This allows the system designer not interested in performing byte writes to connect the byte enable inputs to active low (V_{SS}). Reads of all bytes proceed normally and write cycles, activated via a low on $\overline{SW}$, and the rising edge of the CK clock, write the entire RAM I/O width. This way the designer is spared having to drive multiple write input buffer loads.

Byte writes are performed using the byte write enable inputs in conjunction with the synchronous write input ($\overline{SW}$). It is important to note that writing any one byte will inhibit a read of all bytes at the current address. The RAM cannot simultaneously read one byte and write another at the same address. A write cycle initiated with none of the byte write enable inputs active is neither a read or a write. No write will occur, but the outputs will be deselected as in a normal write cycle.

LATE WRITE

The write address is sampled on the first rising edge of clock and write data is sampled on the following rising edge.

The late write feature is implemented with single stage write buffering. Write buffering is transparent to the user. A comparator monitors the address bus and, when necessary, routes buffer contents to the outputs to assure coherent operation. This occurs in all cases whether there is a byte write or a full word is written.

POWER UP AND INITIALIZATION

Once supplies have reached specification levels, a minimum dwell of 1.0 ms with CK clock inputs cycling is required before beginning normal operations.

SERIAL BOUNDARY SCAN TEST ACCESS PORT OPERATION

OVERVIEW

The serial boundary scan test access port (TAP) on this RAM is designed to operate in a manner consistent with IEEE Standard 1149.1–1990 (commonly referred to as JTAG), but does not implement all of the functions required for 1149.1 compliance. Certain functions have been modified or eliminated because their implementation places extra delays in the RAMs critical speed path. Nevertheless, the RAM supports the standard TAP controller architecture. (The TAP controller is the state machine that controls the TAPs operation) and can be expected to function in a manner that does not conflict with the operation of devices with Standard 1149.1 compliant TAPs. The TAP operates using conventional JEDEC Standard 8–1B Low Voltage (3.3 V) TTL / CMOS logic level signaling.

DISABLING THE TEST ACCESS PORT

It is possible to use this device without utilizing the TAP. To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid level inputs. TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a 1 k resistor. TDO should be left unconnected.

3

TAP DC OPERATING CHARACTERISTICS

($0°C \le T_A \le 70°C$, Unless Otherwise Noted)

Parameter	Symbol	Min	Max	Unit	Note
Logic Input Logic High	$V_{IH}1$	2.0	V_{DD} + 0.3	V	
Logic Input Logic Low	$V_{IL}1$	– 0.3	0.8	V	
Logic Input Leakage Current	I_{lkg}	—	± 5	µA	1
Output Logic Low	$V_{OL}1$	—	0.2	V	2
Output Logic High	$V_{OH}1$	V_{DD} – 0.2	—	V	3
Output Logic Low	$V_{OL}2$	—	0.4	V	4
Output Logic High	$V_{OH}2$	2.4	—	V	5

NOTES:

1. $0 V \le V_{in} \le V_{DD}$ for all logic input pins.
2. $I_{OL}1 \le 100$ µA @ $V_{OL} = 0.2$ V. Sampled, not 100% tested.
3. $|I_{OH}1| \le 100$ µA @ $V_{DDQ} - 0.2$ V. Sampled, not 100% tested.
4. $I_{OL}2 \le 8$ mA @ $V_{OL} = 0.4$ V.
5. $|I_{OH}2| \le 8$ mA @ $V_{OH} = 2.4$ V.

TAP AC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V

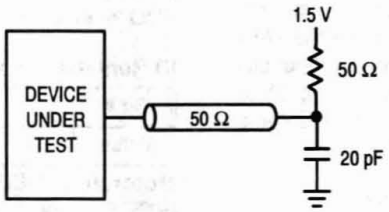
Output Test Load ..... 50 Ω Parallel Terminated T–line with 20 pF Receiver Input Capacitance
Test Load Termination Supply Voltage (V_T) ..... 1.5 V

TAP CONTROLLER TIMING

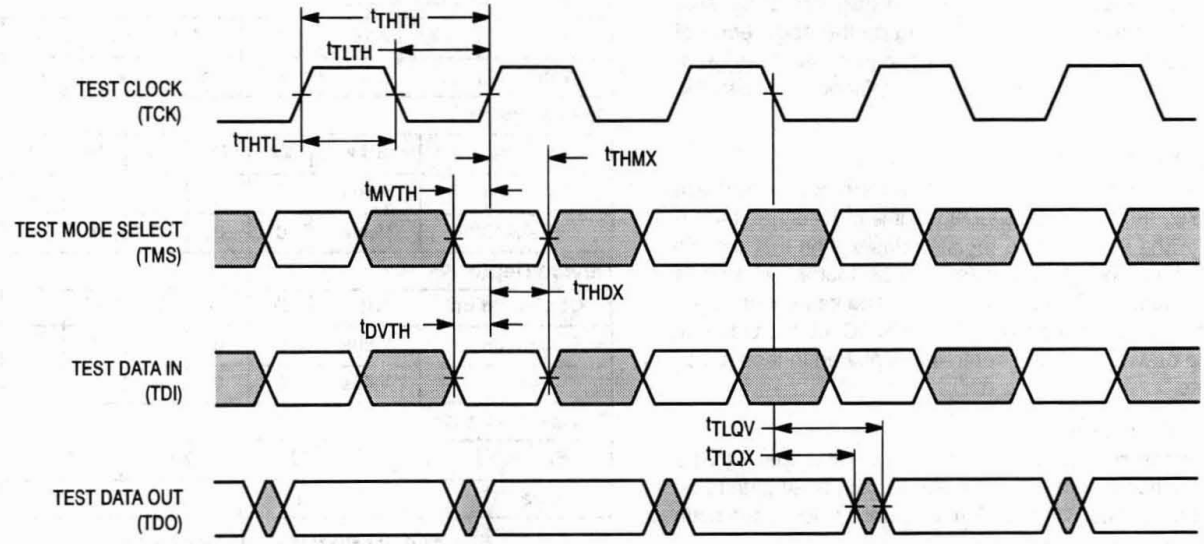
Parameter	Symbol	Min	Max	Unit	Notes
Cycle Time	t_{THTH}	100	—	ns	
Clock High Time	t_{THTL}	40	—	ns	
Clock Low Time	t_{TLTH}	40	—	ns	
TMS Setup	t_{MVTH}	10	—	ns	
TMS Hold	t_{THMX}	10	—	ns	
TDI Valid to TCK High	t_{DVTH}	10	—	ns	
TCK High to TDI Don't Care	t_{THDX}	10	—	ns	
Capture Setup	t_{CS}	10	—	ns	1
Capture Hold	t_{CH}	10	—	ns	1
TCK Low to TDO Unknown	t_{TLQX}	0	—	ns	
TCK Low to TDO Valid	t_{TLOV}	—	20	ns	

NOTES:
1. t_{CS} + t_{CH} defines the minimum pause in RAM I/O pad transitions to assure accurate pad data capture.

AC TEST LOAD



TAP CONTROLLER TIMING DIAGRAM



TEST ACCESS PORT PINS

TCK – TEST CLOCK (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

TMS – TEST MODE SELECT (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.

TDI – TEST DATA IN (INPUT)

The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (refer to Figure 5 TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.

TDO – TEST DATA OUT (OUTPUT)

Output that is active depending on the state of the TAP state machine (refer to Figure 5 TAP Controller State Diagram). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

TRST – TAP RESET

This device does not have a TRST pin. TRST is optional in **IEEE 1149.1.** The test–logic reset state is entered while TMS is held high for five rising edges of TCK. Power on reset circuitry is included internally. This type of reset does not affect the operation of the system logic. The reset affects test logic only.

TEST ACCESS PORT REGISTERS

OVERVIEW

The various TAP registers are selected (one at a time) via the sequences of ones and zeros input to the TMS pin as the TCK is strobed. Each of the TAPs registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on subsequent falling edge of TCK. When a register is selected it is "placed" between the TDI and TDO pins.

INSTRUCTION REGISTER

The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run test/idle or the various data register states. The instructions are three bits long. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power–up or whenever the controller is placed in test–logic–reset state.

BYPASS REGISTER

The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.

BOUNDARY SCAN REGISTER

The boundary scan register is identical in length to the number of active input and I/O connections on the RAM (not counting the TAP pins). This also includes a number of place holder locations (always set to a logic 1) reserved for density upgrade address pins. There are a total of 70 bits in the case of the x36 device and 51 bits in the case of the x18 device. The boundary scan register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture–DR state and then is placed between the TDI and TDO pins when the controller is moved to shift–DR state. Several TAP instructions can be used to activate the boundary scan register.

The Bump/Bit Scan Order tables describe which device bump connects to each boundary scan register location. The first column defines the bit's position in the boundary scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the input or I/O at the bump and the third column is the bump number.

IDENTIFICATION (ID) REGISTER

The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture–DR state with the IDCODE command loaded in the instruction register. The code is loaded from a 32 bit on–chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into shift–DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Presence Indicator

Bit #	0
Value	1

Motorola JEDEC ID Code (Compressed Format, per IEEE Standard 1149.1 – 1990

Bit #	11	10	9	8	7	6	5	4	3	2	1
Value	0	0	0	0	0	0	0	1	1	1	0

Reserved For Future Use

Bit #	17	16	15	14	13	12
Value	x	x	x	x	x	x

Device Width

Configuration	Bit #	22	21	20	19	18
32Kx36	Value	0	0	1	0	0
64Kx18	Value	0	0	0	1	1

Device Depth

Configuration	Bit #	27	26	25	24	23
32Kx36	Value	0	0	0	1	1
64Kx18	Value	0	0	1	0	0

Revision Number

Bit #	31	30	29	28
Value	x	x	x	x

Figure 4. ID Register Bit Meanings

MCM69R538 Bump/Bit Scan Order

BIT #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	NC	3B
2	SA	4P		37	NC	2B
3	SA	4T		38	SA	3A
4	SA	6R		39	SA	3C
5	SA	5T		40	SA	2C
6	ZZ	7T		41	SA	2A
7	DQa	6P		42	DQc	2D
8	DQa	7P		43	DQc	1D
9	DQa	6N		44	DQc	2E
10	DQa	7N		45	DQc	1E
11	DQa	6M		46	DQc	2F
12	DQa	6L		47	DQc	2G
13	DQa	7L		48	DQc	1G
14	DQa	6K		49	DQc	2H
15	DQa	7K		50	DQc	1H
16	$\overline{SBa}$	5L		51	$\overline{SBc}$	3G
17	$\overline{CK}$	4L		52	ZQ	4D
18	CK	4K		53	$\overline{SS}$	4E
19	$\overline{G}$	4F		54	NF	4G
20	$\overline{SBb}$	5G		55	NF	4H
21	DQb	7H		56	$\overline{SW}$	4M
22	DQb	6H		57	$\overline{SBd}$	3L
23	DQb	7G		58	DQd	1K
24	DQb	6G		59	DQd	2K
25	DQb	6F		60	DQd	1L
26	DQb	7E		61	DQd	2L
27	DQb	6E		62	DQd	2M
28	DQb	7D		63	DQd	1N
29	DQb	6D		64	DQd	2N
30	SA	6A		65	DQd	1P
31	SA	6C		66	DQd	2P
32	SA	5C		67	SA	3T
33	SA	5A		68	SA	2R
34	NC	6B		69	SA	4N
35	NC	5B		70	M1	3R

MCM69R620 Bump/Bit Scan Order

Bit #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	$\overline{SBb}$	3G
2	SA	6T		37	ZQ	4D
3	SA	4P		38	$\overline{SS}$	4E
4	SA	6R		39	NF	4G
5	SA	5T		40	NF	4H
6	ZZ	7T		41	$\overline{SW}$	4M
7	DQa	7P		42	DQb	2K
8	DQa	6N		43	DQb	1L
9	DQa	6L		44	DQb	2M
10	DQa	7K		45	DQb	1N
11	$\overline{SBa}$	5L		46	DQb	2P
12	$\overline{CK}$	4L		47	SA	3T
13	CK	4K		48	SA	2R
14	$\overline{G}$	4F		49	SA	4N
15	DQa	6H		50	SA	2T
16	DQa	7G		51	M1	3R
17	DQa	6F				
18	DQa	7E				
19	DQa	6D				
20	SA	6A				
21	SA	6C				
22	SA	5C				
23	SA	5A				
24	NC	6B				
25	NC	5B				
26	NC	3B				
27	NC	2B				
28	SA	3A				
29	SA	3C				
30	SA	2C				
31	SA	2A				
32	DQb	1D				
33	DQb	2E				
34	DQb	2G				
35	DQb	1H				

NOTES:

1. The NC pads listed in this table are indeed no connects, but are represented in the boundary scan register by a "place holder" bit that is forced to logic 1. These pads are reserved for use as address inputs on higher density RAMs that follow this pad out and scan order standard.
2. CK, $\overline{CK}$, are sampled individually. $\overline{CK}$ is not simply a forced complement of the CK input. In scan mode these differential inputs are referenced to each other.
3. M1 and M2 are not ordinary inputs and may not respond to standard I/O logic levels. M1 and M2 must be driven to within 100 mV of a V_{DD} or V_{SS} supply rail to ensure consistent results.
4. ZZ must remain at V_{IL} during boundary scan to ensure consistent results.

TAP Controller Instruction Set

OVERVIEW

There are two classes of instructions defined in the Standard 1149.1–1990; the standard (public) instructions, and device specific (private) instructions. Some public instructions, are mandatory for 1149.1 compliance. Optional public instructions must be implemented in prescribed ways.

Although the TAP controller in this device follows the 1149.1 conventions, it is not 1194.1 compliant because some of the mandatory instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads, but cannot be used to load address, data or control signals into the RAM or to preload the I/O buffers. In other words, the device will not perform Standard 1149.1 EXTEST, INTEST or the preload portion of the SAMPLE / PRELOAD command.

When the TAP controller is placed in capture–IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the shift–IR state the instruction register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to update–IR state. The TAP instruction sets for this device are listed in the following tables.

STANDARD (PUBLIC) INSTRUCTIONS

BYPASS

The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift–DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

Sample/preload is a Standard 1149.1 mandatory public instruction. When the sample / preload instruction is loaded in the Instruction register, moving the TAP controller into the capture–DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set–up plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register.

Moving the controller to shift–DR state then places the boundary scan register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the update–DR state with the SAMPLE / PRELOAD instruction loaded in the instruction register has the same effect as the pause–DR command. This functionality is not Standard 1149.1 compliant.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic 0s. EXTEST is not implemented in this device. Therefore this device is not 1149.1 compliant. Nevertheless, this RAMs TAP does respond to an all zeros instruction, as follows. With the EXTEST (000) instruction loaded in the instruction register the RAM responds just as it does in response to the SAMPLE / PRELOAD instruction described above, except the RAM outputs are forced to high–Z any time the instruction is loaded.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture–DR mode and places the ID register between the TDI and TDO pins in shift–DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test–logic–reset state.

THE DEVICE SPECIFIC (PUBLIC) INSTRUCTION

SAMPLE–Z

If the SAMPLE–Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high–Z) and the boundary scan register is connected between TDI and TDO when the TAP controller is moved to the shift–DR state.

THE DEVICE SPECIFIC (PRIVATE) INSTRUCTION

NOOP

Do not use these instructions; they are reserved for future use.

STANDARD (PUBLIC) INSTRUCTION CODES

Instruction	Code*	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM outputs to High–Z state. *NOT 1149.1 COMPLIANT*
IDCODE	001**	Preloads ID register and places it between TDI and TDO. Does not affect RAM operation.
SAMPLE / PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect RAM operation. Does not implement 1149.1 Preload function. * NOT 1149.1 COMPLIANT *
BYPASS	111	Places bypass register between TDI and TDO. Does not affect RAM operation.
SAMPLE–Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM output drivers to High–Z.

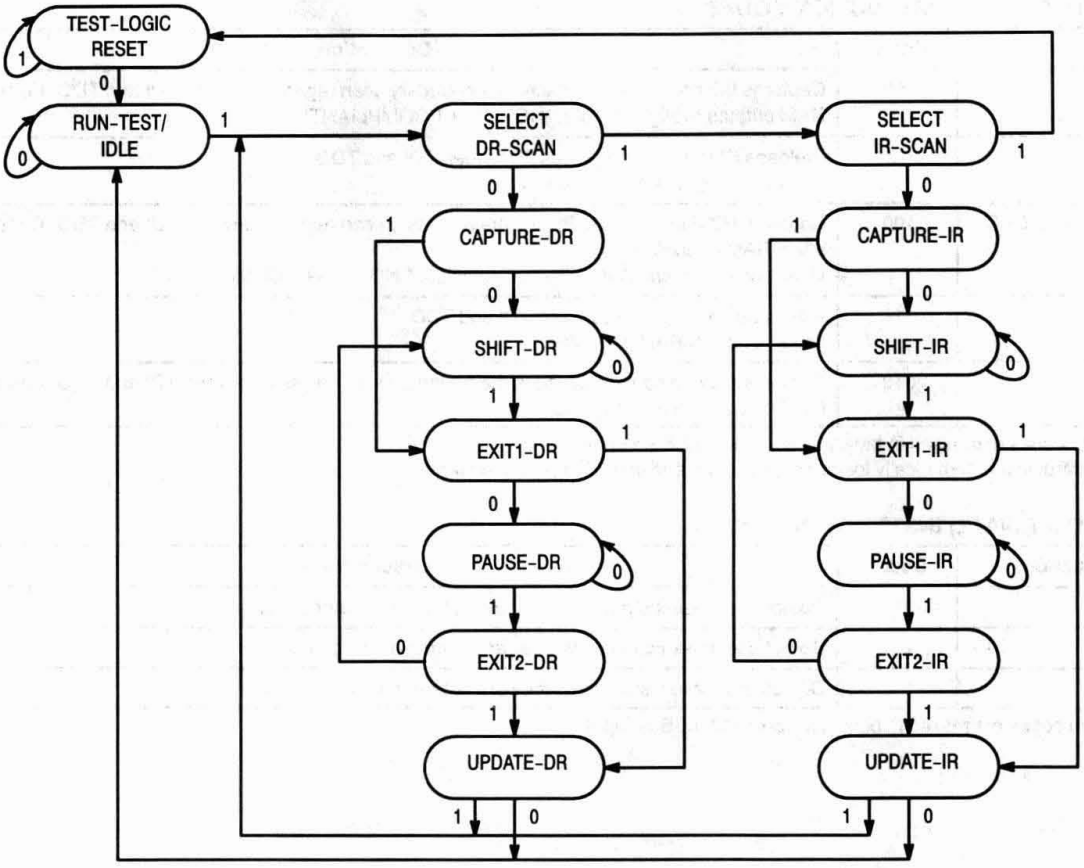
* Instruction codes expressed in binary, MSB on left, LSB on right.
** Default instruction automatically loaded at power–up and in test–logic–reset state.

3

STANDARD (PRIVATE) INSTRUCTION CODES

Instruction	Code*	Description
NO OP	011	Do not use these instructions; they are reserved for future use.
NO OP	101	Do not use these instructions; they are reserved for future use.
NO OP	110	Do not use these instructions; they are reserved for future use.

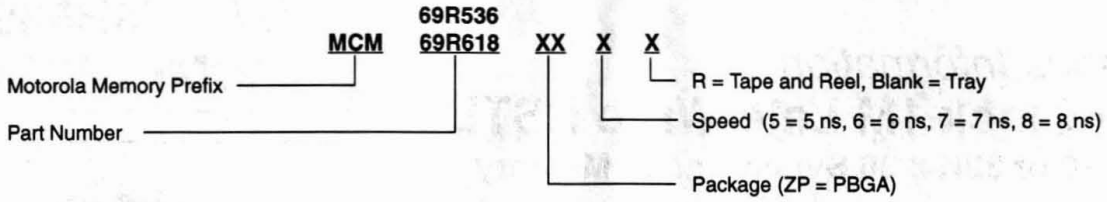
* Instruction codes expressed in binary, MSB on left, LSB on right.



NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 5. TAP Controller State Diagram

ORDERING INFORMATION
(Order by Full Part Number)


69R536
MCM 69R618 XX X X
Motorola Memory Prefix
Part Number
R = Tape and Reel, Blank = Tray
Speed (5 = 5 ns, 6 = 6 ns, 7 = 7 ns, 8 = 8 ns)
Package (ZP = PBGA)

Full Part Numbers —	MCM69R538ZP5	MCM69R538ZP6	MCM69R538ZP7	MCM69R538ZP8
	MCM69R620ZP5	MCM69R620ZP6	MCM69R620ZP7	MCM69R620ZP8
	MCM69R538ZP5R	MCM69R538ZP6R	MCM69R538ZP7R	MCM69R538ZP8R
	MCM69R620ZP5R	MCM69R620ZP6R	MCM69R620ZP7R	MCM69R620ZP8R

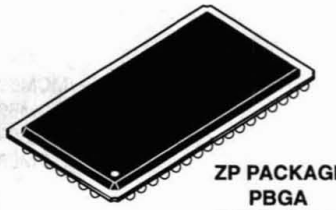
3

MCM69R539
MCM69R621

Advance Information

Dual Clock 1M Late Write HSTL

64K x 18 or 32K x 36 Synchronous Memory



ZP PACKAGE
PBGA
CASE 999–01

3

The MCM69R539/621 is a 1 megabit synchronous late write fast static RAM designed to provide high performance in secondary cache, ATM switch, Telecom, and other high speed memory applications. The MCM69R621 organized as 64K words by 18 bits, and the MCM69R539 organized as 32K words by 36 bits wide.

The differential K and C clock inputs control the timing of read/write operations of the RAM. At the rising edge of the K clock all addresses, write enables, and synchronous selects are registered. An internal buffer and special logic enable the memory to accept write data on the rising edge of the K clock a cycle after address and control signals. The outputs are enabled on the rising edge of the C clock which operates at the same frequency as the K clock; but shifted in time.

The RAM uses HSTL inputs and outputs. The adjustable input trip – point (V_{ref}) and output voltage (V_{DDQ}) gives the system designer greater flexibility in optimizing system performance.

The synchronous write and byte enables allow writing to individual bytes or the entire word.

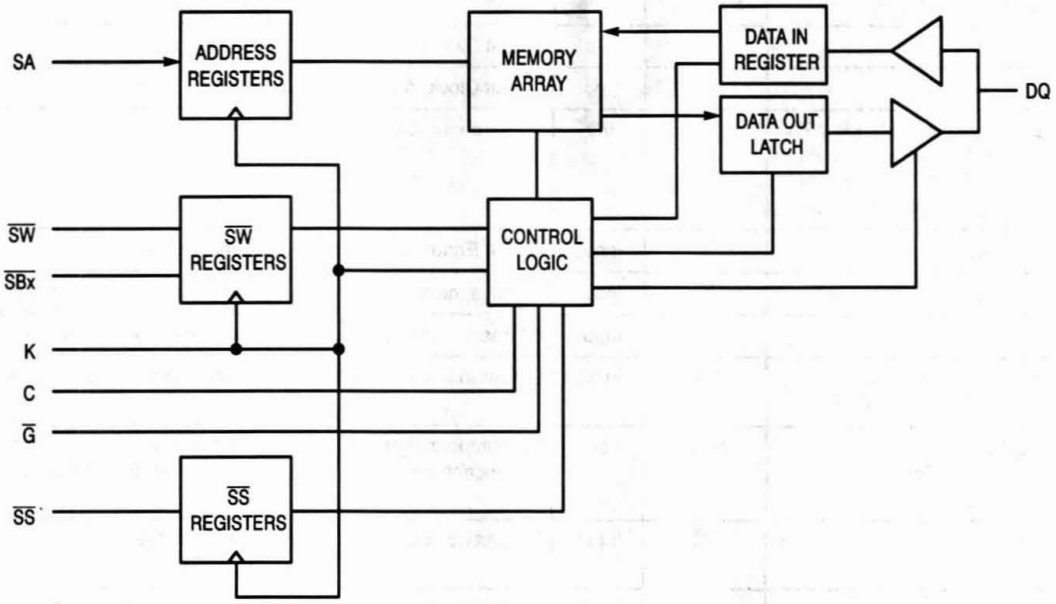
The impedance of the output buffers is programmable allowing the outputs to match the impedance of the circuit traces which reduces signal reflections.

- Byte Write Control
- 3.3 V Power Supply
- HSTL – I/O (JEDEC Standard JESD8–6 Class I Compatible)
- HSTL – User Selectable Input Trip–Point
- HSTL – Compatible Programmable Impedance Output Drivers
- Synchronous Operation
- Asynchronous Impedance Update
- Boundary Scan (JTAG) IEEE 1149.1 Compatible
- Differential Clock Inputs C and K provide separate Input and Output Clocks
- Optional x 18 or x 36 organization
- MCM69R539/621–4.5 = 4.5 ns
  MCM69R539/621–5 = 5 ns
- 119 Bump, 50 mil (1.27 mm) Pitch, 14 mm x 22 mm Plastic Ball Grid Array (PBGA) Package

This document contains information on a new product. Specifications and information herein are subject to change without notice.

4/2/97

FUNCTIONAL BLOCK DIAGRAM



3

PIN ASSIGNMENTS

TOP VIEW

MCM69R539

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	NC	NC	NC	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQc	DQc	V_{SS}	ZQ	V_{SS}	DQb	DQb
E	DQc	DQc	V_{SS}	$\overline{SS}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{G}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{SBc}$	$\overline{C}$	$\overline{SBb}$	DQb	DQb
H	DQc	DQc	V_{SS}	C	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	V_{ref}	V_{DD}	V_{ref}	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	K	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{SBd}$	$\overline{K}$	$\overline{SBa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{SW}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
P	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
R	NC	SA	V_{DD}	V_{DD}	V_{DD}	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69R621

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	NC	NC	NC	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQb	NC	V_{SS}	ZQ	V_{SS}	DQa	NC
E	NC	DQb	V_{SS}	$\overline{SS}$	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	$\overline{SBb}$	$\overline{C}$	V_{SS}	NC	DQa
H	DQb	NC	V_{SS}	C	V_{SS}	DQa	NC
J	V_{DDQ}	V_{DD}	V_{ref}	V_{DD}	V_{ref}	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	K	V_{SS}	NC	DQa
L	DQb	NC	V_{SS}	$\overline{K}$	$\overline{SBa}$	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{SW}$	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	SA	V_{SS}	DQa	NC
P	NC	DQb	V_{SS}	SA	V_{SS}	NC	DQa
R	NC	SA	V_{DD}	V_{DD}	V_{DD}	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69R539 PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4H	C	Input	Output Clock. Active high.
4G	$\overline{C}$	Input	Output Clock. Active low.
(a) 6K, 7K, 6L, 7L, 6M, 6N, 7N, 6P, 7P (b) 6D, 7D, 6E, 7E, 6F, 6G, 7G, 6H, 7H (c) 1D, 2D, 1E, 2E, 2F, 1G, 2G, 1H, 2H (d) 1K, 2K, 1L, 2L, 2M, 1N, 2N, 1P, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
4K	K	Input	Address, data in and control input register clock. Active high.
4L	$\overline{K}$	Input	Address, data in and control input register clock. Active low.
2A, 3A, 5A, 6A, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 3T, 4T, 5T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 5G, 3G, 3L (a), (b), (c), (d)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
3J, 5J	V_{ref}	Supply	Input Reference: provides reference voltage for input buffers.
4D	ZQ	Input	Programmable Output Impedance: Programming pin.
7T	ZZ	Input	Reserved for future use. Must be grounded.
4C, 2J, 4J, 6J, 4R, 5R, 3R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 3H, 5H, 3K, 5K, 3M, 5M, 3N, 5N, 3P, 5P	V_{SS}	Supply	Ground.
4A, 1B, 2B, 3B, 4B, 5B, 6B, 7B, 1C, 7C, 1R, 7R, 1T, 2T, 6T, 6U	NC	—	No Connection: There is no connection to the chip.

MCM69R621 PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4H	C	Input	Output Clock. Active high.
4G	$\overline{C}$	Input	Output Clock. Active low.
(a) 6D, 7E, 6F, 7G, 6H, 7K, 6L, 6N, 7P (b) 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
4K	K	Input	Address, data in and control input register clock. Active high.
4L	$\overline{K}$	Input	Address, data in and control input register clock. Active low.
2A, 3A, 5A, 6A, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 2T, 3T, 5T, 6T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 3G (a), (b)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
3J, 5J	V_{ref}	Supply	Input Reference: provides reference voltage for input buffers.
4D	ZQ	Input	Programmable Output Impedance: Programming pin.
7T	ZZ	Input	Reserved for future use. Must be grounded.
4C, 2J, 4J, 6J, 4R, 5R, 3R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P	V_{SS}	Supply	Ground.
4A, 1B, 2B, 3B, 4B, 5B, 6B, 7B, 1C, 7C, 2D, 7D, 1E, 6E, 2F, 1G, 6G, 2H, 7H, 1K, 6K, 2L, 7L, 6M, 2N, 7N, 1P, 6P, 1R, 7R, 1T, 4T, 6U	NC	—	No Connection: There is no connection to the chip.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS}, See Note 1)

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Output Supply Voltage	V_{DDQ}	– 0.5 to V_{DD} + 0.5	V
Voltage On Any Pin	V_{in}	– 0.5 to V_{DD} + 0.5	V
Input Current (per I/O)	I_{in}	± 50	mA
Output Current (per I/O)	I_{out}	± 70	mA
Power Dissipation (See Note 2)	P_D	—	W
Operating Temperature	T_A	0 to + 70	°C
Temperature Under Bias	T_{bias}	–10 to + 85	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability will be dependent upon package characteristics and use environment. See enclosed thermal impedance data.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

PBGA PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (Still Air)		$R_{\theta JA}$	59	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Single Layer Board	$R_{\theta JA}$	44	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Four Layer Board	$R_{\theta JA}$	28	°C/W	
Junction to Board (Bottom)		$R_{\theta JB}$	18	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, pwer dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ TA ≤ 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (See Notes 1 through 4)

Parameter		Symbol	Min	Typical –4.5	Typical –5	Max	Unit	Notes
Input Reference DC Voltage		V_{ref} (dc)	0.6	—	—	1.1	V	11
Core Power Supply Voltage		V_{DD}	3.15	—	—	3.6	V	
Output Driver Supply Voltage		V_{DDQ}	1.4	—	—	1.6	V	
Active Power Supply Current	(x18) (x36)	I_{DD1}	— —	TBD TBD	TBD TBD	TBD TBD	mA	5
Quiescent Active Power Supply Current	(x18) (x36)	I_{DD2}	— —	TBD TBD	TBD TBD	TBD	mA	6, 10
Active Standby Power Supply Current	(x18) (x36)	I_{SB1}	— —	TBD TBD	TBD TBD	TBD	mA	7
Quiescent Standby Power Supply Current	(x18) (x36)	I_{SB2}	— —	TBD TBD	TBD TBD	TBD	mA	8, 10
Sleep Mode Power Supply Current		I_{SB3}	—	TBD	TBD	TBD	mA	9, 10

NOTES:

1. All data sheet parameters specified to full range of V_{DD} unless otherwise noted. All voltages are referenced to voltage applied to V_{SS} bumps.
2. Supply voltage applied to V_{DD} connections.
3. Supply voltage applied to V_{DDQ} connections.
4. All power supply currents measured with outputs open or deselected.
5. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered active, 50% read cycles.
6. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered active.
7. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered inactive.
8. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered inactive, ZZ low.
9. $V_{DD} = V_{DD}$ (Max), t_{KHKH} = dc, registered inactive, ZZ high.
10. 200 mV ≥ V_{in} ≥ V_{DDQ} – 200 mV.
11. Although considerable latitude in the selection of the nominal dc value (i.e., rms value) of V_{ref} is supported, the peak to peak ac component superimposed on V_{ref} may not exceed 5% of the dc component of V_{ref}.

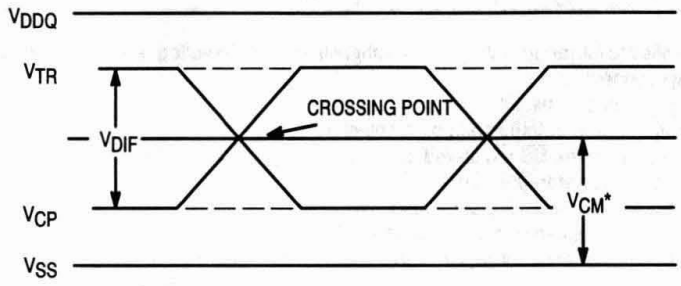
3

DC INPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
DC Input Logic High	$V_{IH(dc)}$	V_{ref} + 0.1	V_{DD} + 0.3	V	
DC Input Logic Low	$V_{IL(dc)}$	– 0.3	V_{ref} – 0.1	V	1
Input Reference DC Voltage	$V_{ref\ (dc)}$	0.6	1.1	V	2
Input Leakage Current	$I_{lkg(1)}$	—	± 5	µA	3
Clock Input Signal Voltage	$V_{in(dc)}$	– 0.3	V_{DD} + 0.3	V	
Clock Input Differential Voltage	$V_{DIF(dc)}$	0.2	V_{DD} + 0.6	V	4
Clock Input Common Mode Voltage Range (See Figure 1)	$V_{CM\ (dc)}$	0.68	1.1	V	
Clock Input Crossing Point Voltage Range (See Figure 1)	V_X	0.68	1.1	V	

NOTES:

1. Inputs may undershoot to – 0.5 V (peak) for up to 20% t_{KHKH} (e.g., 2 ns at a clock cycle time of 10 ns).
2. Although considerable latitude in the selection of the nominal dc value (i.e., rms value) of V_{ref} is supported, the peak to peak ac component superimposed on V_{ref} may not exceed 5% of the dc component of V_{ref}.
3. $0\ V \le V_{in} \le V_{DD}$ for all pins.
4. Minimum differential input voltage required for differential input clock operation.



*V_{CM}, the Common Mode Input Voltage, equals $V_{TR} - ((V_{TR} - V_{CP})/2)$.

Figure 1. Differential Inputs/Common Mode Input Voltage

DC OUTPUT BUFFER CHARACTERISTICS – PROGRAMMABLE IMPEDANCE PUSH–PULL OUTPUT BUFFER MODE

($0°C \le T_A \le 70°C$, Unless Otherwise Noted, See Notes 5 and 6)

Parameter	Symbol	Min	Max	Unit	Notes
Output Logic Low	V_{OL}	$V_{DDQ}/2 - 0.025$	$V_{DDQ}/2 + 0.025$	V	1
Output Logic High	V_{OH}	$V_{DDQ}/2 - 0.025$	$V_{DDQ}/2 + 0.025$	V	2
Light Load Output Logic Low	$V_{OL}1$	V_{SS}	0.2	V	3
Light Load Output Logic High	$V_{OH}1$	$V_{DDQ} - 0.2$	V_{DDQ}	V	4

NOTES:
1. $I_{OL} = (V_{DDQ}/2) / (RQ/5)$ for values of $RQ = 175\ \Omega \le RQ \le 350\ \Omega$.
2. $|I_{OH}| = (V_{DDQ}/2) / (RQ/5)$ for values of $RQ = 175\ \Omega \le RQ \le 350\ \Omega$.
3. $I_{OL} \le 100\ \mu A$.
4. $|I_{OH}| \le 100\ \mu A$.
5. The impedance controlled mode is expected to be used in point–to–point applications, driving high impedance inputs.
6. The ZQ pin is connected through RQ to V_{SS} for the controlled impedance mode.

3

DC OUTPUT BUFFER CHARACTERISTICS – MINIMUM IMPEDANCE PUSH–PULL OUTPUT BUFFER MODE

($0°C \le T_A \le 70°C$, $ZQ = V_{DD}$, See Notes 5 and 6)

Parameter	Symbol	Min	Max	Unit	Notes
Output Logic Low	$V_{OL}2$	V_{SS}	0.4	V	1
Output Logic High	$V_{OH}2$	$V_{DDQ} - 0.4$	V_{DDQ}	V	2
Light Load Output Logic Low	VOL_3	V_{SS}	0.2	V	3
Light Load Output Logic High	$V_{OH}3$	$V_{DDQ} - 0.2$	V_{DDQ}	V	4

NOTES:
1. $I_{OL} \le 16$ mA.
2. $|I_{OH}| \le 16$ mA.
3. $I_{OL} \le 100\ \mu A$.
4. $|I_{OH}| \le 100\ \mu A$.
5. The push–pull output mode is expected to be used in bussed applications and may be series or parallel terminated. Conforms to the JEDEC Standard JESD8–6 Class II.
6. The ZQ pin is connected to V_{DD} to enable the minimum impedance mode.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, $0°C \le T_A \le 70°C$, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	5	pF
Input/Output Capacitance	$C_{I/O}$	7	8	pF
K, $\overline{K}$, Capacitance C, $\overline{C}$ Capacitance	C_K C_C	4	5	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

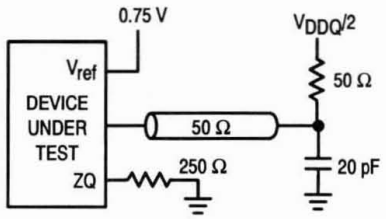
(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0.25 to 1.25 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 0.75 V
Output Timing Reference Level ..... 0.75 V
Clock Input Timing Reference Level ..... Differential Cross–Point
RQ for 50 Ω Impedance ..... 250 Ω

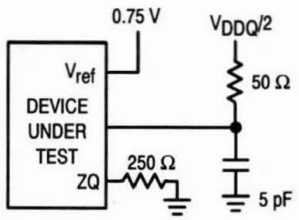
READ/WRITE CYCLE TIMING (See Note 3)

Parameter	Symbol	MCM69R539–4.5 MCM69R621–4.5		MCM69R539–5 MCM69R621–5		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{KHKH}	4.5	—	5	—	ns	
K Clock High Pulse Width	t_{KHKL}	1.8	—	2	—	ns	
K Clock Low Pulse Width	t_{KLKH}	1.8	—	2	—	ns	
C Clock High Pulse Width	t_{CHCL}	1.8		2		ns	
C Clock Low Pulse Width	t_{CLCH}	1.8		2		ns	
C Clock High to K Clock High Delay	t_{CHKH}	0.8		1		ns	
K Clock High to C Clock High Delay	t_{KHCH}	1.5		2.5		ns	
Clock High to Output Valid	t_{KHQV}	—	6.7	—	7.5	ns	1
C Clock High to Output Valid	t_{CHQV}		2.2		2.5	ns	1
C Clock High to Output Hold	t_{CHQX}	0.7		1		ns	2
Output Enable Low to Output Low–Z	t_{GLQX}	0.5	—	0.5	—	ns	2
Output Enable Low to Output Valid	t_{GLQV}	—	2.2	—	2.5	ns	1
Output Enable to Output Hold	t_{GHQX}	0.5	—	0.5	—	ns	2
Output Enable High to Output High–Z	t_{GHQZ}	—	2.2	—	2.5	ns	2
Setup Times: Address Data In Chip Select Write Enable	t_{AVKH} t_{DVKH} t_{SVKH} t_{WVKH}	0.5	—	0.5	—	ns	
Hold Times: Address Data In Chip Select Write Enable	t_{KHAX} t_{KHDX} t_{KHSX} t_{KHWX}	1	—	1	—	ns	

NOTES:
1. Tested per AC Test Load diagram. See Figure 2a.
2. Measured at ± 200 mV from steady state. See Figure 2b.
3. In no case may control input signals (e.g., $\overline{SS}$) be operated with pulse widths less than the minimum clock input pulse width specifications (e.g., t_{KHKL}) or at frequencies that exceed the applied K clock frequency.



(a)



(b)

Figure 2. AC Test Loads

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

AC INPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Note
AC Input Logic High (See Figure 4)	V_{IH} (ac)	V_{ref} + 200 mV		
AC Input Logic Low (See Figure 3 and 4)	V_{IL} (ac)		V_{ref} – 200 mV	1
Input Reference Peak to Peak ac Voltage	V_{ref}(ac)		5% V_{ref} (dc)	2
Clock Input Differential Voltage	V_{DIF} (ac)	400 mV	V_{DD} + 600 mV	3

NOTES:
1. Inputs may undershoot to – 0.5 V (peak) for up to 20% t_{KHKH} (e.g., 2 ns at a clock cycle time of 10 ns).
2. Although considerable latitude in the selection of the nominal dc value (i.e., rms value) of V_{ref} is supported, the peak to peak ac component superimposed on V_{ref} may not exceed 5% of the dc component of V_{ref}.
3. Minimum differential input voltage required for differential input clock operation.

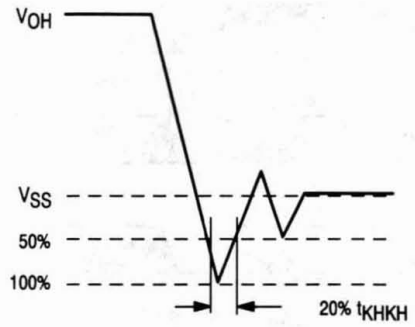


Figure 3. Undershoot Voltage

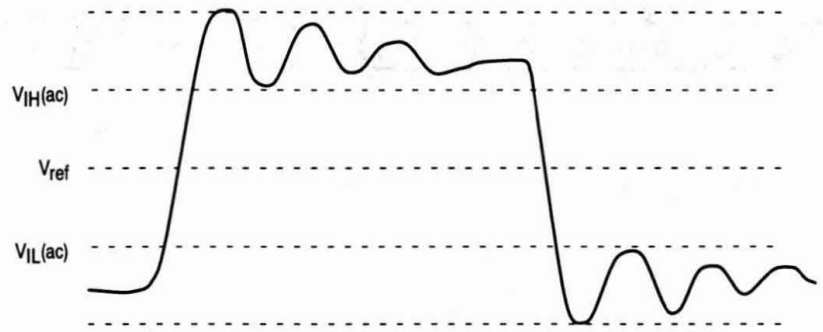
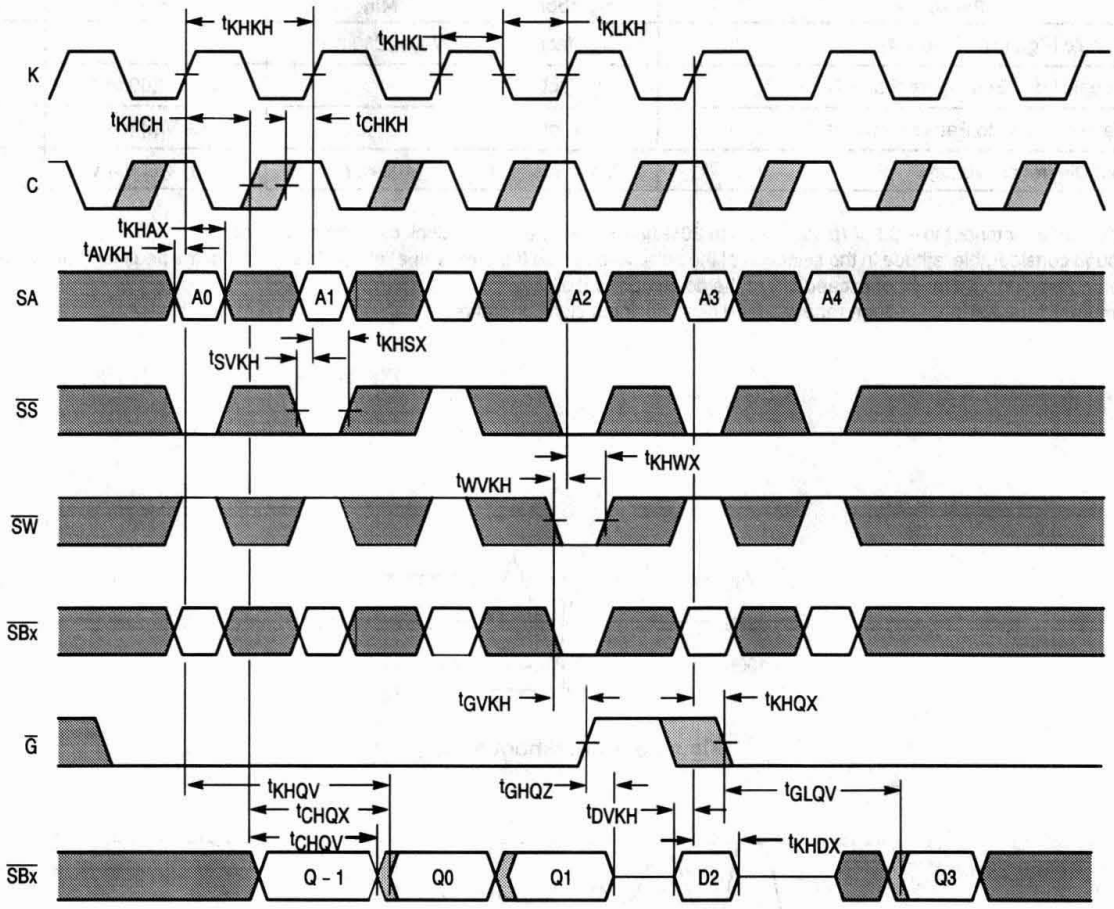
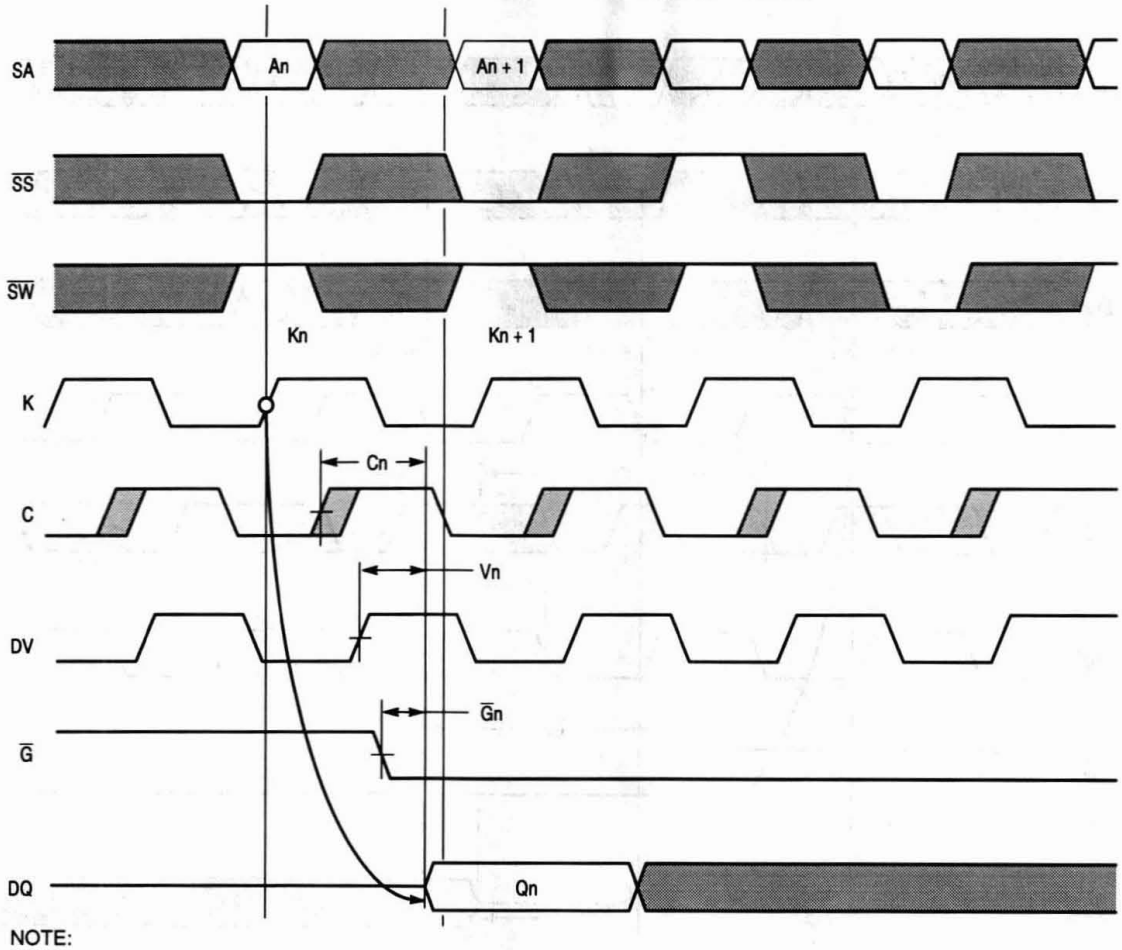


Figure 4. Differential Inputs/Common Mode Input Voltage

BASIC TIMING



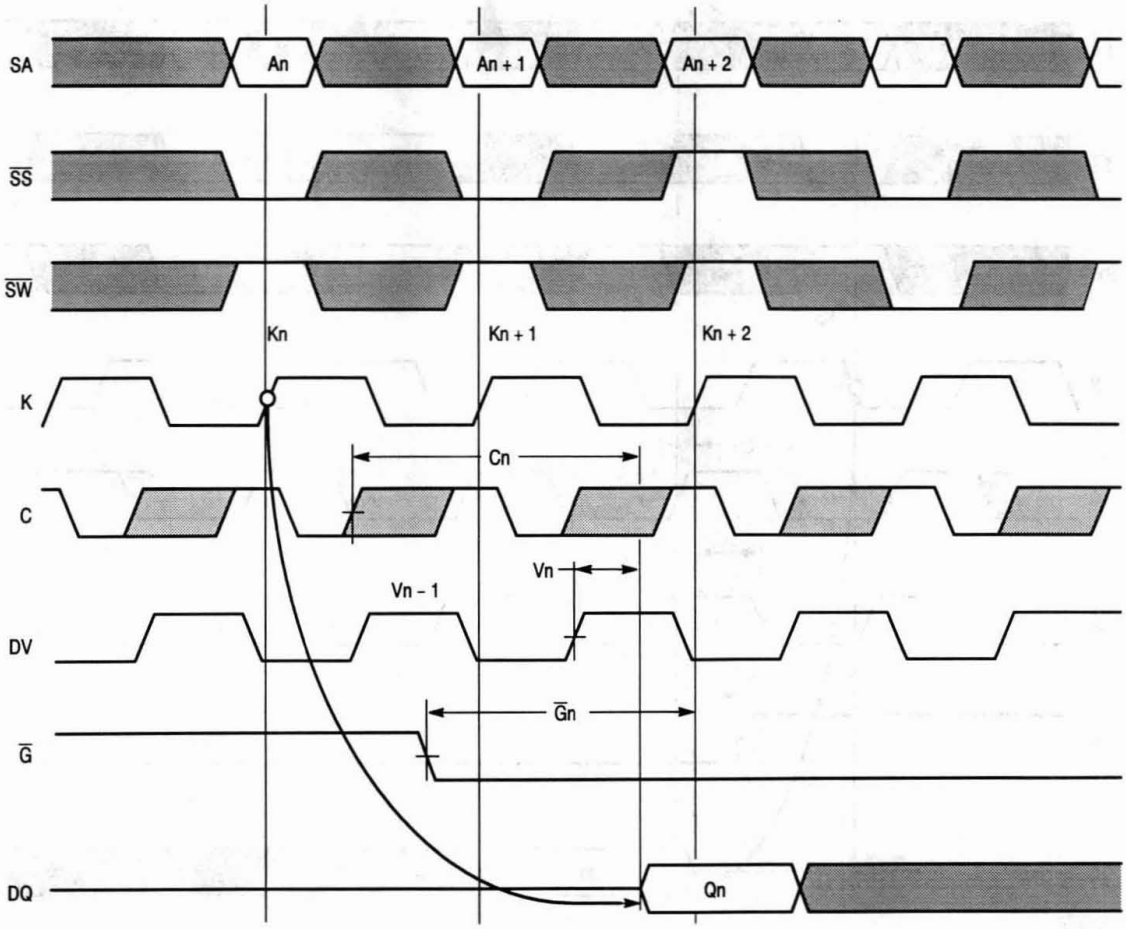
READ TIMING OUTPUT ENABLE ($t_{KHQV} < t_{KHKH}$)



NOTE:

1. The outputs are enabled by a combination of events, both internal and external.
2. DV is an internal signal and is not visible externally. It indicates when new valid data is available. Actual output enable occurs only after all three events; C clock, DV, $\overline{G}$ have occurred for cycle Kn. They do not have to occur in the order shown.

READ TIMING OUTPUT ENABLE ($t_{KHQV} > t_{KHKH}$)



NOTE:
1. The outputs are enabled by a combination of events, both internal and external.
2. DV is an internal signal and is not visible externally. It indicates when new valid data is available. Actual output enable occurs only after all three events; C clock, DV, $\overline{G}$ have occurred for cycle Kn. They do not have to occur in the order shown.

FUNCTIONAL OPERATION

GENERAL

All control signals except $\overline{G}$ are registered on the rising edge of the K clock. All signals must meet the setup and hold times shown in the AC Characteristics table.

OUTPUT ENABLE and $\overline{G}$

$\overline{G}$ asynchronously three–states the output buffers. However when going from three–state to a low–Z condition, the state and timing of K, C, $\overline{SW}$, $\overline{SS}$, and $\overline{G}$ determine when the data bus comes out of three–state. The Read Timing Output Enable Timing diagrams ($t_{KHQV} < t_{KHKH}$) and ($t_{KHQV} > t_{KHKH}$) show the conditions that must occur before the output is enabled.

If $\overline{SS}$ is high at the rising edge of K the device will be deselected at the next rising edge of the C clock, if it is not already deselected from a previous event.

READ OPERATION

The read operation is controlled by $\overline{G}$, K, C , $\overline{SW}$, and $\overline{SS}$. The K and C clock operate at the same frequency but are shifted in phase with each other. There is a minimum separation of the K and C clock as specified by t_{KHCH} and t_{CHKH}. The rising edge of the C clock allows valid data to be output and disables further changes in the output until the next rising edge of C clock.

WRITE OPERATION

$\overline{G}$ must be used to three–state the data bus for a write cycle. $\overline{SW}$ does not three–state the bus.

The write address is sampled on the first rising edge of K clock and write data is sampled on the following rising edge.

The late write feature is implemented with single stage write buffering. Write buffering is transparent to the user. A comparator monitors the address bus and, when necessary, routes buffer contents to the outputs to assure coherent operation. This occurs in all cases whether there is a byte write or a full word is written.

Data is transferred to the array at the next write cycle.

WRITE AND BYTE WRITE FUNCTIONS

Note that in the following discussion the term "byte" refers to nine bits of the RAM I/O bus. In all cases, the timing parameters described for synchronous write input ($\overline{SW}$) apply to each of the byte write enable inputs ($\overline{SBa}$, $\overline{SBb}$, etc.).

Byte write enable inputs have no effect on read cycles. This allows the system designer not interested in performing byte writes to connect the byte enable inputs to active low (V_{SS}). Reads of all bytes proceed normally and write cycles, activated via a low on $\overline{SW}$, and the rising edge of the K clock, write the entire RAM I/O width. This way the designer is spared having to drive multiple write input buffer loads.

Byte writes are performed using the byte write enable inputs in conjunction with the synchronous write input ($\overline{SW}$). It is important to note that writing any one byte will inhibit a read of all bytes at the current address. The RAM cannot simultaneously read one byte and write another at the same address. A write cycle initiated with none of the byte write enable inputs active is neither a read or a write. No write will occur.

PROGRAMMABLE IMPEDANCE OPERATION

The designer can program the RAMs output buffer impedance by terminating the ZQ pin to V_{SS} through a precision resistor (RQ). The value of RQ is five times the output impedance desired. For example, 250 Ω resistor will give an output impedance of 50 Ω.

Impedance updates occur continuously and the frequency of the update is based on the subdivided K clock. Note that if the K clock stops so does the impedance update.

The actual change in the impedance occurs in small increments and is monotonic. There are no significant disturbances that occur on the output because of this smooth update method.

The impedance update is not related to any particular type of cycle because the impedance is updated continuously and is based on the K clock. Updates occur regardless of whether the the device is performing a read, write or a deselect cycle and does not depend on the state of $\overline{G}$.

At power up, the output impedance defaults to approximately 50 ohms. It will take 4,000 to 16,000 cycles for the impedance to be completely updated if the programmed impedance is much higher or lower than 50 Ω.

The output buffers can also be programmed in a minimum impedance configuration by connecting ZQ to V_{DD}.

POWER UP AND INITIALIZATION

The following supply voltage application sequence is recommended: V_{SS}, V_{DD}, then V_{DDQ}. Please note, per the Absolute Maximum Ratings table, V_{DDQ} is not to exceed V_{DD} + 0.5 V, whatever the instantaneous value of V_{DD}. Once supplies have reached specification levels, a minimum dwell of 1.0 ms with C/K clock inputs cycling is required before beginning normal operations. At power up the output impedance will be set at approximately 50 Ω as stated above.

3

SERIAL BOUNDARY SCAN TEST ACCESS PORT OPERATION

OVERVIEW

The serial boundary scan test access port (TAP) on this RAM is designed to operate in a manner consistent with IEEE Standard 1149.1–1990 (commonly referred to as JTAG), but does not implement all of the functions required for 1149.1 compliance. Certain functions have been modified or eliminated because their implementation places extra delays in the RAMs critical speed path. Nevertheless, the RAM supports the standard TAP controller architecture. (The TAP controller is the state machine that controls the TAPs operation) and can be expected to function in a manner that does not conflict with the operation of devices with Standard 1149.1 compliant TAPs. The TAP operates using conventional JEDEC Standard 8–1B Low Voltage (3.3 V) TTL / CMOS logic level signaling.

DISABLING THE TEST ACCESS PORT

It is possible to use this device without utilizing the TAP. To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid level inputs. TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a 1 k resistor. TDO should be left unconnected.

3

TAP DC OPERATING CHARACTERISTICS

($0°C \le T_A \le 70°C$, Unless Otherwise Noted)

Parameter	Symbol	Min	Max	Unit	Note
Logic Input Logic High	$V_{IH}1$	2.0	V_{DD} + 0.3	V	
Logic Input Logic Low	$V_{IL}1$	– 0.3	0.8	V	
Logic Input Leakage Current	I_{lkg}	—	± 5	µA	1
Output Logic Low	$V_{OL}1$	—	0.2	V	2
Output Logic High	$V_{OH}1$	V_{DD} – 0.2	—	V	3
Output Logic Low	$V_{OL}2$	—	0.4	V	4
Output Logic High	$V_{OH}2$	2.4	—	V	5

NOTES:
1. $0 V \le V_{in} \le V_{DDQ}$ for all logic input pins.
2. $I_{OL}1 \le 100$ µA @ $V_{OL} = 0.2$ V. Sampled, not 100% tested.
3. $|I_{OH}1| \le 100$ µA @ $V_{DDQ} - 0.2$ V. Sampled, not 100% tested.
4. $I_{OL}2 \le 8$ mA @ $V_{OL} = 0.4$ V.
5. $|I_{OH}2| \le 8$ mA @ $V_{OH} = 2.4$ V.

TAP AC OPERATING CONDITIONS AND CHARACTERISTICS

($0°C \le T_A \le 70°C$, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V

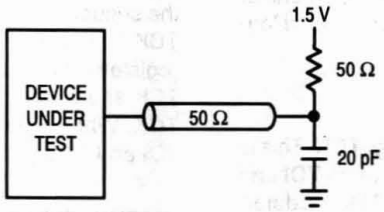
Output Test Load ..... 50 Ω Parallel Terminated T–line with 20 pF
..... Receiver Input Capacitance
Test Load Termination Supply Voltage (VT) ..... 1.5 V

TAP CONTROLLER TIMING

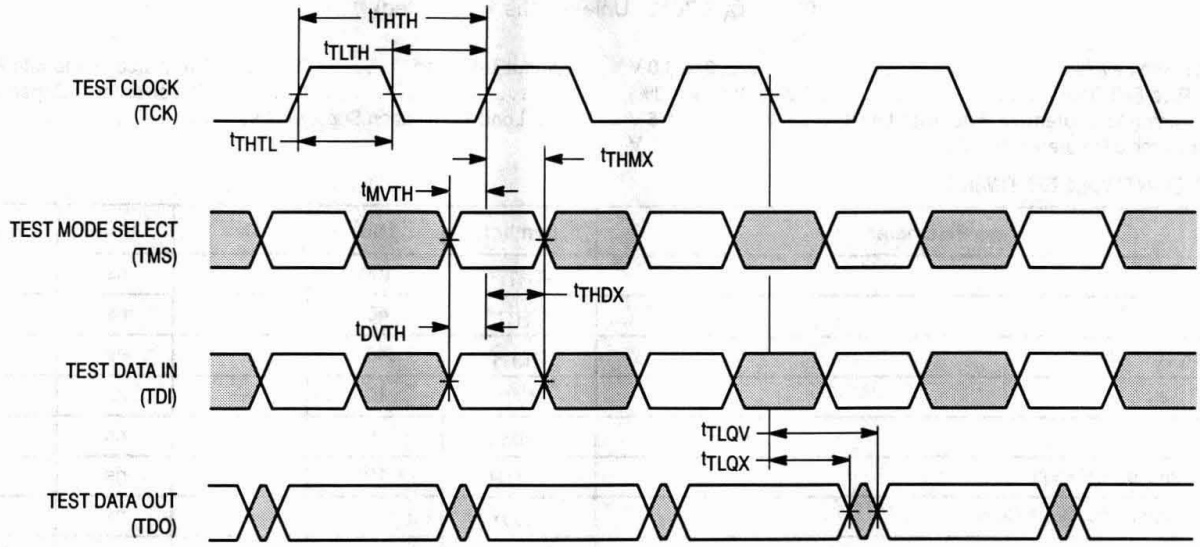
Parameter	Symbol	Min	Max	Unit	Notes
Cycle Time	t_{THTH}	100	—	ns	
Clock High Time	t_{THTL}	40	—	ns	
Clock Low Time	t_{TLTH}	40	—	ns	
TMS Setup	t_{MVTH}	10	—	ns	
TMS Hold	t_{THMX}	10	—	ns	
TDI Valid to TCK High	t_{DVTH}	10	—	ns	
TCK High to TDI Don't Care	t_{THDX}	10	—	ns	
Capture Setup	t_{CS}	10	—	ns	1
Capture Hold	t_{CH}	10	—	ns	1
TCK Low to TDO Unknown	t_{TLQX}	0	—	ns	
TCK Low to TDO Valid	t_{TLOV}	—	20	ns	

NOTES:
1. $t_{CS} + t_{CH}$ defines the minimum pause in RAM I/O pad transitions to assure accurate pad data capture.

AC TEST LOAD



TAP CONTROLLER TIMING DIAGRAM



TEST ACCESS PORT PINS

TCK – TEST CLOCK (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

TMS – TEST MODE SELECT (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.

TDI – TEST DATA IN (INPUT)

The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (refer to Figure 6 TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.

TDO – TEST DATA OUT (OUTPUT)

Output that is active depending on the state of the TAP state machine (refer to Figure 6 TAP Controller State Diagram). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

TRST – TAP RESET

This device does not have a TRST pin. TRST is optional in IEEE 1149.1. The test–logic reset state is entered while TMS is held high for five rising edges of TCK. Power on reset circuitry is included internally. This type of reset does not affect the operation of the system logic. The reset affects test logic only.

TEST ACCESS PORT REGISTERS

OVERVIEW

The various TAP registers are selected (one at a time) via the sequences of ones and zeros input to the TMS pin as the TCK is strobed. Each of the TAPs registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on subsequent falling edge of TCK. When a register is selected it is "placed" between the TDI and TDO pins.

INSTRUCTION REGISTER

The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run test/idle or the various data register states. The instructions are three bits long. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power–up or whenever the controller is placed in test–logic–reset state.

BYPASS REGISTER

The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.

BOUNDARY SCAN REGISTER

The boundary scan register is identical in length to the number of active input and I/O connections on the RAM (not counting the TAP pins). This also includes a number of place holder locations (always set to a logic 1) reserved for density upgrade address pins. There are a total of 70 bits in the case of the x36 device and 51 bits in the case of the x18 device. The boundary scan register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture–DR state and then is placed between the TDI and TDO pins when the controller is moved to shift–DR state. Several TAP instructions can be used to activate the boundary scan register.

The Bump/Bit Scan Order tables describe which device bump connects to each boundary scan register location. The first column defines the bit's position in the boundary scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the input or I/O at the bump and the third column is the bump number.

IDENTIFICATION (ID) REGISTER

The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture–DR state with the IDCODE command loaded in the instruction register. The code is loaded from a 32 bit on–chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into shift–DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Presence Indicator

Bit #	0
Value	1

Motorola JEDEC ID Code (Compressed Format, per IEEE Standard 1149.1 – 1990

Bit #	11	10	9	8	7	6	5	4	3	2	1
Value	0	0	0	0	0	0	0	1	1	1	0

Reserved For Future Use

Bit #	17	16	15	14	13	12
Value	x	x	x	x	x	x

Device Width

Configuration	Bit #	22	21	20	19	18
32Kx36	Value	0	0	1	0	0
64Kx18	Value	0	0	0	1	1

Device Depth

Configuration	Bit #	27	26	25	24	23
32Kx36	Value	0	0	0	1	1
64Kx18	Value	0	0	1	0	0

Revision Number

Bit #	31	30	29	28
Value	x	x	x	x

Figure 5. ID Register Bit Meanings

3

MCM69R539 Bump/Bit Scan Order

BIT #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	NC	3B
2	SA	4P		37	NC	2B
3	SA	4T		38	SA	3A
4	SA	6R		39	SA	3C
5	SA	5T		40	SA	2C
6	ZZ	7T		41	SA	2A
7	DQa	6P		42	DQc	2D
8	DQa	7P		43	DQc	1D
9	DQa	6N		44	DQc	2E
10	DQa	7N		45	DQc	1E
11	DQa	6M		46	DQc	2F
12	DQa	6L		47	DQc	2G
13	DQa	7L		48	DQc	1G
14	DQa	6K		49	DQc	2H
15	DQa	7K		50	DQc	1H
16	$\overline{SBa}$	5L		51	$\overline{SBc}$	3G
17	$\overline{K}$	4L		52	ZQ	4D
18	K	4K		53	$\overline{SS}$	4E
19	$\overline{G}$	4F		54	$\overline{C}$	4G
20	$\overline{SBb}$	5G		55	C	4H
21	DQb	7H		56	$\overline{SW}$	4M
22	DQb	6H		57	$\overline{SBd}$	3L
23	DQb	7G		58	DQd	1K
24	DQb	6G		59	DQd	2K
25	DQb	6F		60	DQd	1L
26	DQb	7E		61	DQd	2L
27	DQb	6E		62	DQd	2M
28	DQb	7D		63	DQd	1N
29	DQb	6D		64	DQd	2N
30	SA	6A		65	DQd	1P
31	SA	6C		66	DQd	2P
32	SA	5C		67	SA	3T
33	SA	5A		68	SA	2R
34	NC	6B		69	SA	4N
35	NC	5B		70	M1	3R

MCM69R621 Bump/Bit Scan Order

Bit #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	$\overline{SBb}$	3G
2	SA	6T		37	ZQ	4D
3	SA	4P		38	$\overline{SS}$	4E
4	SA	6R		39	$\overline{C}$	4G
5	SA	5T		40	C	4H
6	ZZ	7T		41	$\overline{SW}$	4M
7	DQa	7P		42	DQb	2K
8	DQa	6N		43	DQb	1L
9	DQa	6L		44	DQb	2M
10	DQa	7K		45	DQb	1N
11	$\overline{SBa}$	5L		46	DQb	2P
12	$\overline{K}$	4L		47	SA	3T
13	K	4K		48	SA	2R
14	$\overline{G}$	4F		49	SA	4N
15	DQa	6H		50	SA	2T
16	DQa	7G		51	M1	3R
17	DQa	6F				
18	DQa	7E				
19	DQa	6D				
20	SA	6A				
21	SA	6C				
22	SA	5C				
23	SA	5A				
24	NC	6B				
25	NC	5B				
26	NC	3B				
27	NC	2B				
28	SA	3A				
29	SA	3C				
30	SA	2C				
31	SA	2A				
32	DQb	1D				
33	DQb	2E				
34	DQb	2G				
35	DQb	1H				

NOTES:

1. The NC pads listed in this table are indeed no connects, but are represented in the boundary scan register by a "place holder" bit that is forced to logic 1. These pads are reserved for use as address inputs on higher density RAMs that follow this pad out and scan order standard.
2. K, $\overline{K}$, C, $\overline{C}$ are sampled individually. $\overline{K}$, $\overline{C}$ is not simply a forced complement of the K, C input. In scan mode these differential inputs are referenced to V_{ref}, not each other.
3. ZQ, M1, and M2 are not ordinary inputs and may not respond to standard I/O logic levels. ZQ, M1, and M2 must be driven to within 100 mV of a V_{DD} or V_{SS} supply rail to ensure consistent results.
4. ZZ must remain at V_{IL} during boundary scan to ensure consistent results.

TAP CONTROLLER INSTRUCTION SET

OVERVIEW

There are two classes of instructions defined in the Standard 1149.1–1990; the standard (public) instructions, and device specific (private) instructions. Some public instructions, are mandatory for 1149.1 compliance. Optional public instructions must be implemented in prescribed ways.

Although the TAP controller in this device follows the 1149.1 conventions, it is not 1194.1 compliant because some of the mandatory instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads, but cannot be used to load address, data or control signals into the RAM or to preload the I/O buffers. In other words, the device will not perform Standard 1149.1 EXTEST, INTEST or the preload portion of the SAMPLE / PRELOAD command.

When the TAP controller is placed in capture–IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the shift–IR state the instruction register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to update–IR state. The TAP instruction sets for this device are listed in the following tables.

STANDARD (PUBLIC) INSTRUCTIONS

BYPASS

The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift–DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

Sample/preload is a Standard 1149.1 mandatory public instruction. When the sample / preload instruction is loaded in the Instruction register, moving the TAP controller into the capture–DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set–up plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register.

Moving the controller to shift–DR state then places the boundary scan register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the update–DR state with the SAMPLE / PRELOAD instruction loaded in the instruction register has the same effect as the pause–DR command. This functionality is not Standard 1149.1 compliant.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic 0s. EXTEST is not implemented in this device. Therefore this device is not 1149.1 compliant. Nevertheless, this RAMs TAP does respond to an all zeros instruction, as follows. With the EXTEST (000) instruction loaded in the instruction register the RAM responds just as it does in response to the SAMPLE / PRELOAD instruction described above, except the RAM outputs are forced to high–Z any time the instruction is loaded.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture–DR mode and places the ID register between the TDI and TDO pins in shift–DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test–logic–reset state.

THE DEVICE SPECIFIC (PUBLIC) INSTRUCTION

SAMPLE–Z

If the SAMPLE–Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high–Z) and the boundary scan register is connected between TDI and TDO when the TAP controller is moved to the shift–DR state.

THE DEVICE SPECIFIC (PRIVATE) INSTRUCTION

NOOP

Do not use these instructions; they are reserved for future use.

STANDARD (PUBLIC) INSTRUCTION CODES

Instruction	Code*	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM outputs to High–Z state. *NOT 1149.1 COMPLIANT*
IDCODE	001**	Preloads ID register and places it between TDI and TDO. Does not affect RAM operation.
SAMPLE / PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect RAM operation. Does not implement 1149.1 Preload function. * NOT 1149.1 COMPLIANT *
BYPASS	111	Places bypass register between TDI and TDO. Does not affect RAM operation.
SAMPLE–Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM output drivers to High–Z.

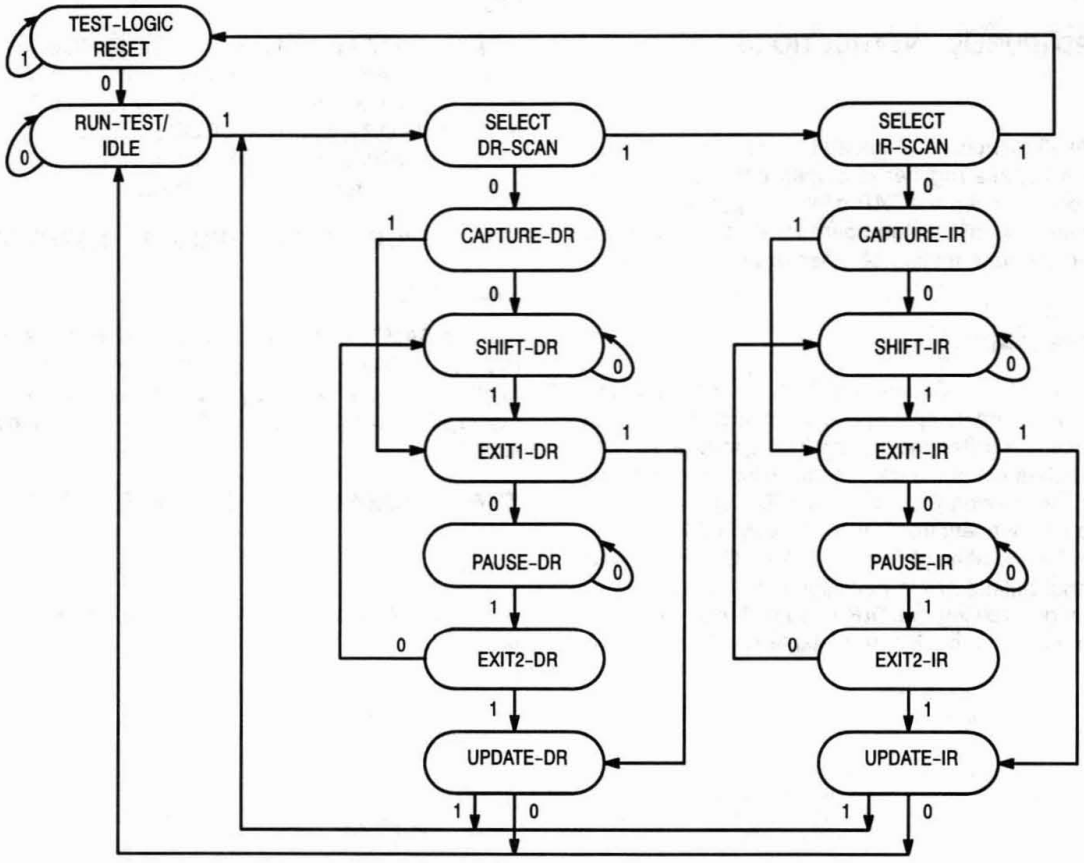
3

* Instruction codes expressed in binary, MSB on left, LSB on right.
** Default instruction automatically loaded at power–up and in test–logic–reset state.

STANDARD (PRIVATE) INSTRUCTION CODES

Instruction	Code*	Description
NO OP	011	Do not use these instructions; they are reserved for future use.
NO OP	101	Do not use these instructions; they are reserved for future use.
NO OP	110	Do not use these instructions; they are reserved for future use.

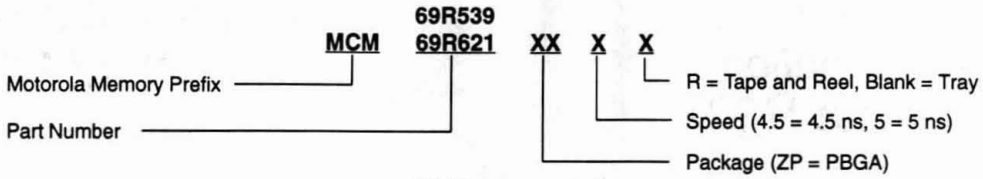
* Instruction codes expressed in binary, MSB on left, LSB on right.



NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 6. TAP Controller State Diagram

ORDERING INFORMATION
(Order by Full Part Number)



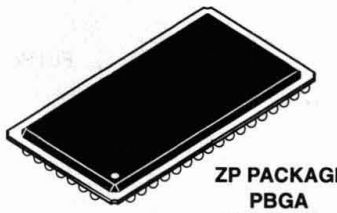
Full Part Numbers — MCM69R539ZP4.5 MCM69R539ZP5
MCM69R621ZP4.5 MCM69R621ZP5
MCM69R539ZP4.5R MCM69R539ZP5R
MCM69R621ZP4.5R MCM69R621ZP5R

3

MCM69L536
MCM69L618

Advance Information

1M Late Write HSTL



ZP PACKAGE
PBGA
CASE 999–01

The MCM69L536/618 is a 1 megabit synchronous late write fast static RAM designed to provide high performance in secondary cache, ATM switch, Telecom, and other high speed memory applications. The MCM69L618 organized as 64K words by 18 bits, and the MCM69L536 organized as 32K words by 36 bits wide are fabricated in Motorola's high performance silicon gate BiCMOS technology.

The differential CK clock inputs control the timing of read/write operations of the RAM. At the rising edge of the CK clock all addresses, write enables, and synchronous selects are registered. An internal buffer and special logic enable the memory to accept write data on the rising edge of the CK clock a cycle after address and control signals. Read data is driven on the falling edge of the CK clock also.

The RAM uses HSTL inputs and outputs. The adjustable input trip – point (V_{ref}) and output voltage (V_{DDQ}) gives the system designer greater flexibility in optimizing system performance.

The synchronous write and byte enables allow writing to individual bytes or the entire word.

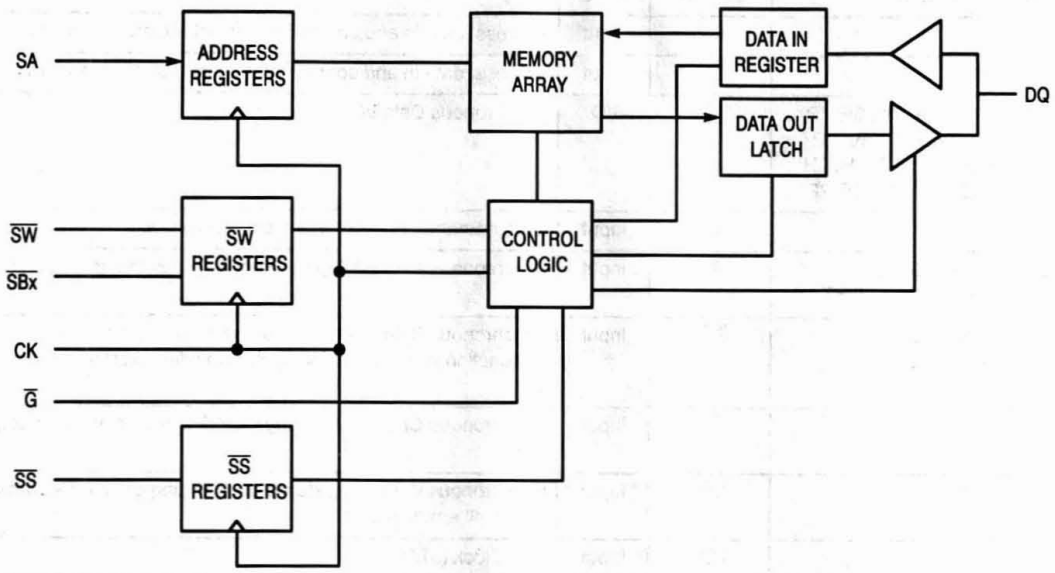
The impedance of the output buffers is programmable allowing the outputs to match the impedance of the circuit traces which reduces signal reflections.

- Byte Write Control
- Single 3.3 V + 10%, – 5% Operation
- HSTL – I/O (JEDEC Standard JESD8–6 Class II Compatible)
- HSTL – User Selectable Input Trip–Point
- HSTL – Compatible Programmable Impedance Output Drivers
- Register to Latch Synchronous Operation
- Asynchronous Output Enable
- Boundary Scan (JTAG) IEEE 1149.1 Compatible
- Differential Clock Inputs
- Optional x 18 or x 36 organization
- MCM69L536/618 – 7.5 = 7.5 ns
  MCM69L536/618 – 8.5 = 8.5 ns
  MCM69L536/618 – 9.5 = 9.5 ns
  MCM69L536/618 – 10.5 = 10.5 ns
- 119 Bump, 50 mil (1.27 mm) Pitch, 14 mm x 22 mm Plastic Ball Grid Array (PBGA) Package

This document contains information on a new product. Specifications and information herein are subject to change without notice.

4/2/97

FUNCTIONAL BLOCK DIAGRAM



3

PIN ASSIGNMENTS

TOP VIEW

MCM69L536

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	NC	NC	NC	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQc	DQc	V_{SS}	ZQ	V_{SS}	DQb	DQb
E	DQc	DQc	V_{SS}	$\overline{SS}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{G}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{SBc}$	NF	$\overline{SBb}$	DQb	DQb
H	DQc	DQc	V_{SS}	NF	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	V_{ref}	V_{DD}	V_{ref}	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CK	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{SBd}$	$\overline{CK}$	$\overline{SBa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{SW}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
P	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
R	NC	SA	V_{SS}	V_{DD}	V_{DD}	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69L618

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	NC	NC	NC	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQb	NC	V_{SS}	ZQ	V_{SS}	DQa	NC
E	NC	DQb	V_{SS}	$\overline{SS}$	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	$\overline{SBb}$	NF	V_{SS}	NC	DQa
H	DQb	NC	V_{SS}	NF	V_{SS}	DQa	NC
J	V_{DDQ}	V_{DD}	V_{ref}	V_{DD}	V_{ref}	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	CK	V_{SS}	NC	DQa
L	DQb	NC	V_{SS}	$\overline{CK}$	$\overline{SBa}$	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{SW}$	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	SA	V_{SS}	DQa	NC
P	NC	DQb	V_{SS}	SA	V_{SS}	NC	DQa
R	NC	SA	V_{SS}	V_{DD}	V_{DD}	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69L536 PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6K, 7K, 6L, 7L, 6M, 6N, 7N, 6P, 7P (b) 6D, 7D, 6E, 7E, 6F, 6G, 7G, 6H, 7H (c) 1D, 2D, 1E, 2E, 2F, 1G, 2G, 1H, 2H (d) 1K, 2K, 1L, 2L, 2M, 1N, 2N, 1P, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 3T, 4T, 5T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 5G, 3G, 3L (a), (b), (c), (d)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
3J, 5J	V_{ref}	Supply	Input Reference: provides reference voltage for input buffers.
4D	ZQ	Input	Programmable Output Impedance: Programming pin.
7T	ZZ	Input	Reserved for future use. Must be grounded.
4C, 2J, 4J, 6J, 4R, 5R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 3H, 5H, 3K, 5K, 3M, 5M, 3N, 5N, 3P, 5P, 3R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 3B, 4B, 5B, 6B, 7B, 1C, 7C, 1R, 7R, 1T, 2T, 6T, 6U	NC	—	No Connection: There is no connection to the chip.
4G, 4H	NF	—	No Function: There is an internal connection to the chip, but the pin has no function on this device.

MCM69L618 PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6D, 7E, 6F, 7G, 6H, 7K, 6L, 6N, 7P (b) 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 2T, 3T, 5T, 6T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 3G (a), (b)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
3J, 5J	V_{ref}	Supply	Input Reference: provides reference voltage for input buffers.
4D	ZQ	Input	Programmable Output Impedance: Programming pin.
7T	ZZ	Input	Reserved for future use. Must be grounded.
4C, 2J, 4J, 6J, 4R, 5R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P, 3R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 3B, 4B, 5B, 6B, 7B, 1C, 7C, 2D, 7D, 1E, 6E, 2F, 1G, 6G, 2H, 7H, 1K, 6K, 2L, 7L, 6M, 2N, 7N, 1P, 6P, 1R, 7R, 1T, 4T, 6U	NC	—	No Connection: There is no connection to the chip.
4G, 4H	NF	—	No Function: There is an internal connection to the chip, but the pin has no function on this device.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS}, See Note 1)

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Output Supply Voltage	V_{DDQ}	– 0.5 to V_{DD} + 0.5	V
Voltage On Any Pin	V_{in}	– 0.5 to V_{DD} + 0.5	V
Input Current (per I/O)	I_{in}	± 50	mA
Output Current (per I/O)	I_{out}	± 70	mA
Power Dissipation (See Note 2)	P_D	—	W
Operating Temperature	T_A	0 to + 70	°C
Temperature Under Bias	T_{bias}	–10 to + 85	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability will be dependent upon package characteristics and use environment. See enclosed thermal impedance data.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

PBGA PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (Still Air)		$R_{\theta JA}$	59	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Single Layer Board	$R_{\theta JA}$	44	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Four Layer Board	$R_{\theta JA}$	28	°C/W	
Junction to Board (Bottom)		$R_{\theta JB}$	18	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, pwer dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

($0°C \le T_A \le 70°C$, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (See Notes 1 through 4)

Parameter		Symbol	Min	Typical –7.5	Typical –8.5	Typical –9.5	Typical –10.5	Max	Unit	Notes
Input Reference DC Voltage		V_{ref} (dc)	0.6	—	—	—	—	1.1	V	11
Core Power Supply Voltage		V_{DD}	3.15	—	—	—	—	3.6	V	
Output Driver Supply Voltage		V_{DDQ}	1.4	—	—	—	—	1.6	V	
Active Power Supply Current	(x18)	I_{DD1}	—	TBD	TBD	TBD	TBD	TBD	mA	5
	(x36)		—	TBD	TBD	TBD	TBD	TBD		
Quiescent Active Power Supply Current	(x18)	I_{DD2}	—	TBD	TBD	TBD	TBD	TBD	mA	6, 10
	(x36)		—	TBD	TBD	TBD	TBD			
Active Standby Power Supply Current	(x18)	I_{SB1}	—	TBD	TBD	TBD	TBD	TBD	mA	7
	(x36)		—	TBD	TBD	TBD	TBD			
Quiescent Standby Power Supply Current	(x18)	I_{SB2}	—	TBD	TBD	TBD	TBD	TBD	mA	8, 10
	(x36)		—	TBD	TBD	TBD	TBD			
Sleep Mode Power Supply Current		I_{SB3}	—	TBD	TBD	TBD	TBD	TBD	mA	9, 10

NOTES:
1. All data sheet parameters specified to full range of V_{DD} unless otherwise noted. All voltages are referenced to voltage applied to V_{SS} bumps.
2. Supply voltage applied to V_{DD} connections.
3. Supply voltage applied to V_{DDQ} connections.
4. All power supply currents measured with outputs open or deselected.
5. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered active, 50% read cycles.
6. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered active.
7. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered inactive.
8. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered inactive, ZZ low.
9. $V_{DD} = V_{DD}$ (Max), t_{KHKH} = dc, registered inactive, ZZ high.
10. 200 mV $\ge V_{in} \ge V_{DDQ} - 200$ mV.
11. Although considerable latitude in the selection of the nominal dc value (i.e., rms value) of V_{ref} is supported, the peak to peak ac component superimposed on V_{ref} may not exceed 5% of the dc component of V_{ref}.

DC INPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
DC Input Logic High	V_{IH} (dc)	$V_{ref} + 0.1$	$V_{DD} + 0.3$	V	
DC Input Logic Low (See Figure 2)	V_{IL} (dc)	– 0.3	$V_{ref} - 0.1$	V	1
Input Leakage Current	I_{lkg}	—	± 5	µA	2
Clock Input Signal Voltage	V_{in}	– 0.3	$V_{DD} + 0.3$	V	
Clock Input Differential Voltage	V_{DIF} (dc)	0.2	$V_{DD} + 0.6$	V	3
Clock Input Common Mode Voltage Range (See Figure 3)	V_{CM} (dc)	0.68	1.1	V	4
Clock Input Crossing Point Voltage Range (See Figure 3)	V_X	0.68	1.1	V	

NOTES:
1. Inputs may undershoot to –0.5 V (peak) for up to 20% t_{KHKH} (e.g., 2 ns at a clock cycle time of 10 ns).
2. $0 V \le V_{in} \le V_{DDQ}$ for all pins.
3. Minimum differential input voltage required for differential input clock operation.
4. Maximum rejectable common mode input voltage variation.

DC OUTPUT BUFFER CHARACTERISTICS – PROGRAMMABLE IMPEDANCE PUSH–PULL OUTPUT BUFFER MODE

($0°C \le T_A \le 70°C$, Unless Otherwise Noted, See Notes 5 and 6)

Parameter	Symbol	Min	Max	Unit	Notes
Output Logic Low	V_{OL}	$V_{DDQ}/2 - 0.025$	$V_{DDQ}/2 + 0.025$	V	1
Output Logic High	V_{OH}	$V_{DDQ}/2 - 0.025$	$V_{DDQ}/2 + 0.025$	V	2
Light Load Output Logic Low	$V_{OL}1$	V_{SS}	0.2	V	3
Light Load Output Logic High	$V_{OH}1$	$V_{DDQ} - 0.2$	V_{DDQ}	V	4

NOTES:
1. $I_{OL} = (V_{DDQ}/2)/(RQ/5)$ for values of $RQ = 175\ \Omega \le RQ \le 350\ \Omega$.
2. $|I_{OH}| = (V_{DDQ}/2)/(RQ/5)$ for values of $RQ = 175\ \Omega \le RQ \le 350\ \Omega$.
3. $I_{OL} \le 100\ \mu A$.
4. $|I_{OH}| \le 100\ \mu A$.
5. The impedance controlled mode is expected to be used in point–to–point applications, driving high impedance inputs.
6. The ZQ pin is connected through RQ to V_{SS} for the controlled impedance mode.

3

DC OUTPUT BUFFER CHARACTERISTICS — MINIMUM IMPEDANCE PUSH–PULL OUTPUT BUFFER MODE

($0°C \le T_A \le 70°C$, ZQ = V_{DD}, See Notes 5 and 6)

Parameter	Symbol	Min	Max	Unit	Notes
Output Logic Low	$V_{OL}2$	V_{SS}	0.4	V	1
Output Logic High	$V_{OH}2$	$V_{DDQ} - 0.4$	V_{DDQ}	V	2
Light Load Output Logic Low	$V_{OL}3$	V_{SS}	0.2	V	3
Light Load Output Logic High	$V_{OH}3$	$V_{DDQ} - 0.2$	V_{DDQ}	V	4

NOTES:
1. $I_{OL} \le 16$ mA.
2. $|I_{OH}| \le 16$ mA.
3. $I_{OL} \le 100\ \mu A$.
4. $|I_{OH}| \le 100\ \mu A$.
5. The push–pull output mode is expected to be used in bussed applications and may be series or parallel terminated. Conforms to the JEDEC Standard JESD8–6 Class II.
6. The ZQ pin is connected to V_{DD} to enable the minimum impedance mode.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, $0°C \le T_A \le 70°C$, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	5	pF
Input/Output Capacitance	$C_{I/O}$	7	8	pF
CK, $\overline{CK}$ Capacitance	C_{CK}	4	5	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0.25 to 1.25 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 0.75 V
Output Timing Reference Level ..... 0.75 V
Clock Input Timing Reference Level ..... Differential Cross–Point
ZQ for 50 Ω Impedance ..... 250 Ω

READ/WRITE CYCLE TIMING (See Note 3)

Parameter	Symbol	MCM69L536–7.5 MCM69L618–7.5		MCM69L536–8.5 MCM69L618–8.5		MCM69L536–9.5 MCM69L618–9.5		MCM69L536–10.5 MCM69L618–10.5		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	7	—	8	—	9	—	10	—	ns	
Clock High Pulse Width	t_{KHKL}	2.8	—	3.2	—	3.6	—	4	—	ns	
Clock Low Pulse Width	t_{KLKH}	2.8	—	3.2	—	3.6	—	4	—	ns	
Clock High to Output Valid	t_{KHQV}	—	7.5	—	8.5	—	9.5	—	10.5	ns	1
Clock Low to Output Valid	t_{KLQV}	—	3.5	—	4	—	4	—	4	ns	2
Clock Low to Output Hold	t_{KLQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	2
Clock Low to Output Low–Z	t_{KLQX1}	1	—	1	—	1	—	1	—	ns	2
Clock High to Output High–Z	t_{KHQZ}	—	3.5	—	4	—	4	—	4	ns	2
Output Enable Low to Output Low–Z	t_{GLQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	2
Output Enable Low to Output Valid	t_{GLQV}	—	3.5	—	4	—	4	—	4	ns	2
Output Enable to Output Hold	t_{GHQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	2
Output Enable High to Output High–Z	t_{GHQZ}	—	3.5	—	4	—	4	—	4	ns	2
Setup Times: Address Data In Chip Select Write Enable	t_{AVKH} t_{DVKH} t_{SVKH} t_{WVKH}	0.5	—	0.5	—	0.5	—	0.5	—	ns	
Hold Times: Address Data In Chip Select Write Enable	t_{KHAX} t_{KHDX} t_{KHSX} t_{KHWX}	1	—	1	—	1	—	1	—	ns	

NOTES:
1. Tested per AC Test Load diagram. See Figure 1.
2. Measured at ± 200 mV from steady state.
3. In no case may control input signals (e.g., $\overline{SS}$) be operated with pulse widths less than the minimum clock input pulse width specifications (e.g., t_{KHKL}) or at frequencies that exceed the applied K clock frequency.

AC INPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Note
AC Input Logic High (See Figure 4)	V_{IH} (ac)	V_{ref} + 200 mV		
AC Input Logic Low (See Figure 2 and 4)	V_{IL} (ac)		V_{ref} – 200 mV	1
Input Reference Peak to Peak ac Voltage	V_{ref} (ac)		5% V_{ref} (dc)	2
Clock Input Differential Voltage	V_{dif} (ac)	400 mV	V_{DDQ} + 600 mV	3

NOTES:
1. Inputs may undershoot to –0.5 V (peak) for up to 20% t_{KHKH} (e.g., 2 ns at a clock cycle time of 10 ns).
2. Although considerable latitude in the selection of the nominal dc value (i.e., rms value) of V_{ref} is supported, the peak to peak ac component superimposed on V_{ref} may not exceed 5% of the dc component of V_{ref}.
3. Minimum differential input voltage required for differential input clock operation.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

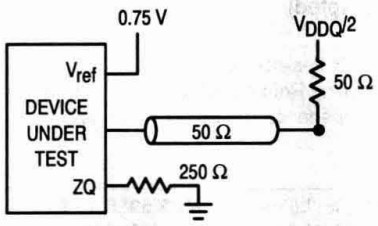


Figure 1. AC Test Load

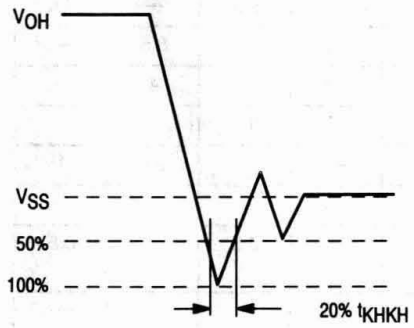
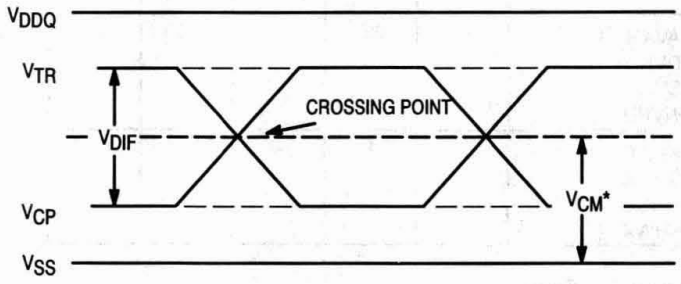


Figure 2. Undershoot Voltage



*V_{CM}, the Common Mode Input Voltage, equals $V_{TR} - ((V_{TR} - V_{CP})/2)$.

Figure 3. Differential Inputs/Common Mode Input Voltage

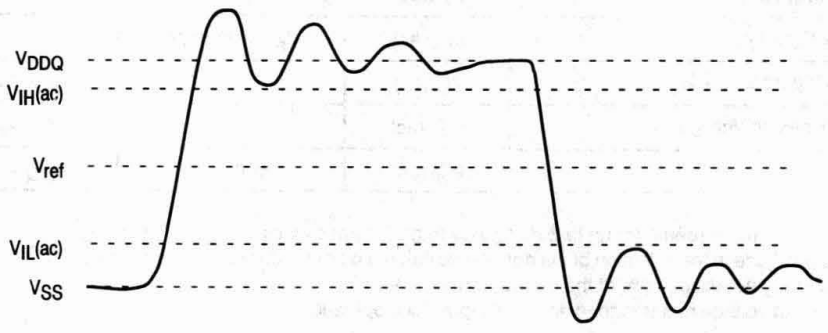
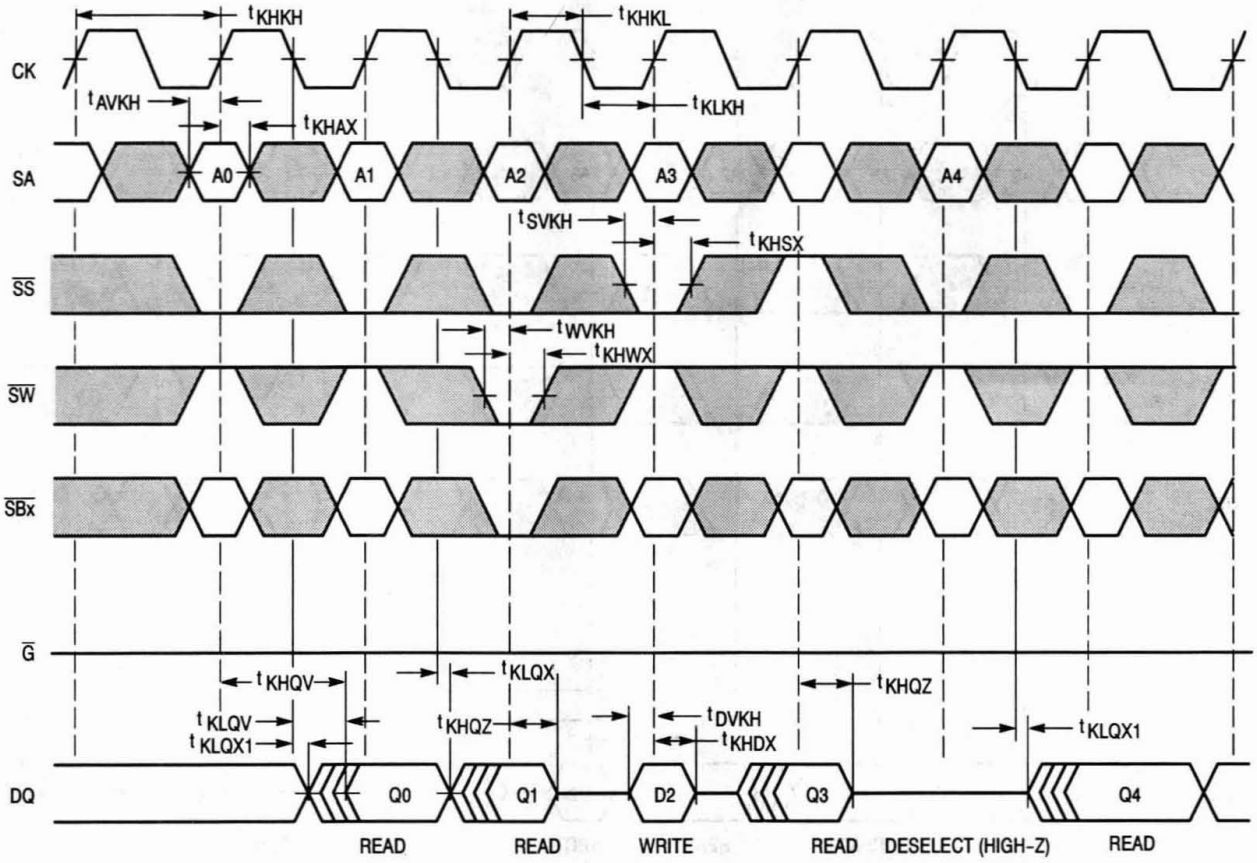
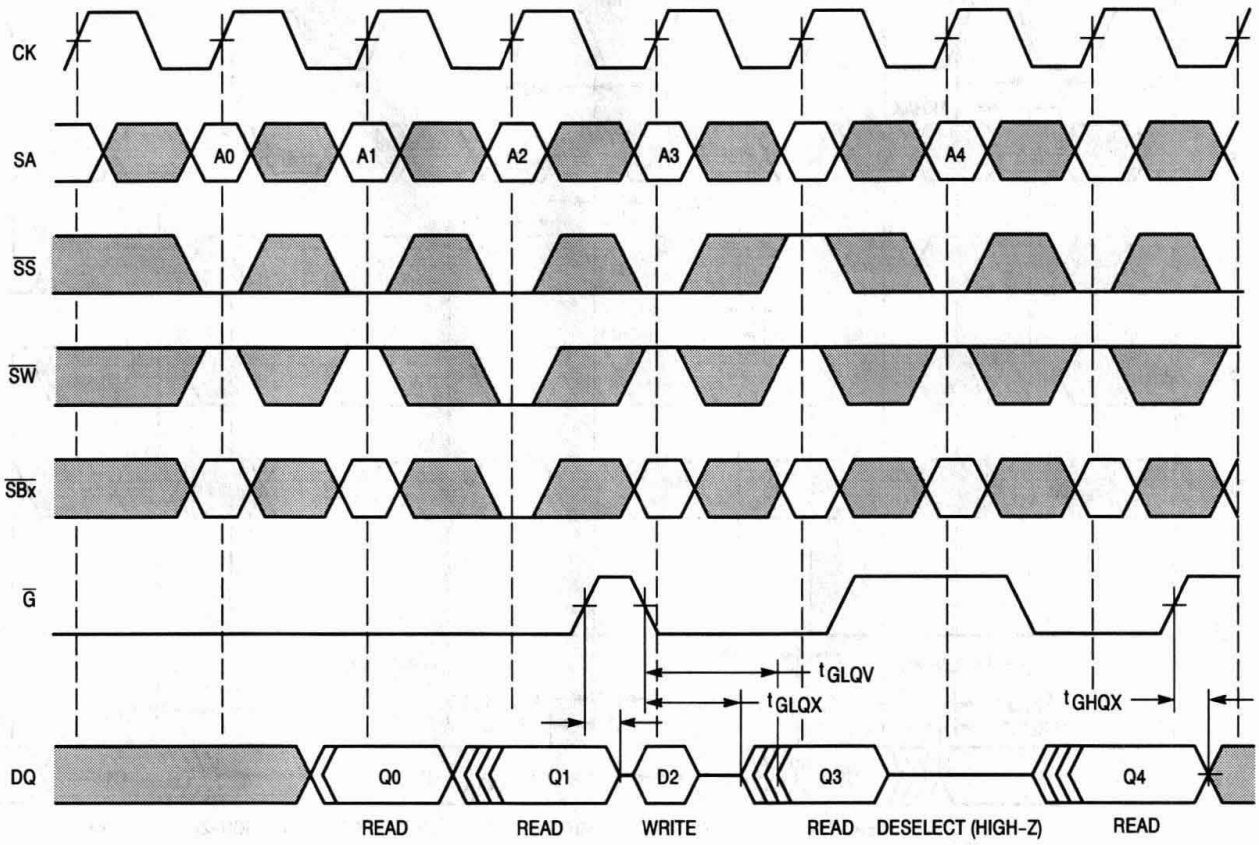


Figure 4. AC Input Conditions

REGISTER LATCH READ–WRITE–READ CYCLES



REGISTER LATCH READ–WRITE–READ CYCLES
($\overline{G}$ Controlled)



FUNCTIONAL OPERATION

READ AND WRITE OPERATIONS

All control signals except $\overline{G}$ are registered on the rising edge of the CK clock. These signals must meet the setup and hold times shown in the AC Characteristics table. On the falling edge of the current cycle, the output latch becomes transparent and data is available. The output data is latched on the rising edge of the next clock. The output data is available at the output at t_{KLQV} or t_{KHQV} whichever is later. t_{KHQV} is the internal latency of the device. During this same cycle a new read address can be applied to the address pins.

A write cycle can occur on the next cycle as long as t_{KLQX} and t_{DVKH} are met. Read cycles may follow write cycles immediately.

$\overline{G}$, $\overline{SS}$, and $\overline{SW}$ control output drive. Chip deselect via a high on $\overline{SS}$ at the rising edge of the CK clock has its effect on the output drivers immediately. $\overline{SW}$ low deselects the output drivers immediately (on the same cycle). Output selecting via a low on $\overline{SS}$ and high on $\overline{SW}$ at a rising CK clock has its effect on the output drivers at t_{KLQX}. Output drive is also controlled directly by output enable, $\overline{G}$. $\overline{G}$ is an asynchronous input. No clock edges are required to enable or disable the output with $\overline{G}$.

Output data will be valid the latter of t_{GLQV}, t_{KHQV}, or t_{KLQV}. Outputs will begin driving at t_{KLQX1}. Outputs will hold previous data until t_{KLQX} or t_{GHQX}.

WRITE AND BYTE WRITE FUNCTIONS

Note that in the following discussion the term "byte" refers to nine bits of the RAM I/O bus. In all cases, the timing parameters described for synchronous write input ($\overline{SW}$) apply to each of the byte write enable inputs ($\overline{SBa}$, $\overline{SBb}$, etc.).

Byte write enable inputs have no effect on read cycles. This allows the system designer not interested in performing byte writes to connect the byte enable inputs to active low (V_{SS}). Reads of all bytes proceed normally and write cycles, activated via a low on $\overline{SW}$, and the rising edge of the CK clock, write the entire RAM I/O width. This way the designer is spared having to drive multiple write input buffer loads.

Byte writes are performed using the byte write enable inputs in conjunction with the synchronous write input ($\overline{SW}$). It is important to note that writing any one byte will inhibit a read of all bytes at the current address. The RAM cannot simultaneously read one byte and write another at the same address. A write cycle initiated with none of the byte write enable inputs active is neither a read or a write. No write will occur, but the outputs will be deselected as in a normal write cycle.

LATE WRITE

The write address is sampled on the first rising edge of clock and write data is sampled on the following rising edge.

The late write feature is implemented with single stage write buffering. Write buffering is transparent to the user. A comparator monitors the address bus and, when necessary, routes buffer contents to the outputs to assure coherent operation. This occurs in all cases whether there is a byte write or a full word is written.

POWER UP AND INITIALIZATION

Please note, per the Absolute Maximum Ratings table, V_{DDQ} is not to exceed V_{DD} + 0.5 V, whatever the instantaneous value of V_{DD}. Once supplies have reached specification levels, a minimum dwell of 1.0 µs with CK clock inputs cycling is required before beginning normal operations.

SERIAL BOUNDARY SCAN TEST ACCESS PORT OPERATION

OVERVIEW

The serial boundary scan test access port (TAP) on this RAM is designed to operate in a manner consistent with IEEE Standard 1149.1–1990 (commonly referred to as JTAG), but does not implement all of the functions required for 1149.1 compliance. Certain functions have been modified or eliminated because their implementation places extra delays in the RAMs critical speed path. Nevertheless, the RAM supports the standard TAP controller architecture. (The TAP controller is the state machine that controls the TAPs operation) and can be expected to function in a manner that does not conflict with the operation of devices with Standard 1149.1 compliant TAPs. The TAP operates using conventional JEDEC Standard 8–1B Low Voltage (3.3 V) TTL / CMOS logic level signaling.

DISABLING THE TEST ACCESS PORT

It is possible to use this device without utilizing the TAP. To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid level inputs. TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a 1 k resistor. TDO should be left unconnected.

3

TAP DC OPERATING CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Parameter	Symbol	Min	Max	Unit	Note
Logic Input Logic High	$V_{IH}1$	2.0	V_{DD} + 0.3	V	
Logic Input Logic Low	$V_{IL}1$	– 0.3	0.8	V	
Logic Input Leakage Current	I_{lkg}	—	± 5	µA	1
Output Logic Low	$V_{OL}1$	—	0.2	V	2
Output Logic High	$V_{OH}1$	V_{DD} – 0.2	—	V	3
Output Logic Low	$V_{OL}2$	—	0.4	V	4
Output Logic High	$V_{OH}2$	2.4	—	V	5

NOTES:
1. 0 V ≤ V_{in} ≤ V_{DD} for all logic input pins.
2. $I_{OL}1$ ≤ 100 µA @ V_{OL} = 0.2 V. Sampled, not 100% tested.
3. $|I_{OH}1|$ ≤ 100 µA @ V_{DDQ} – 0.2 V. Sampled, not 100% tested.
4. $I_{OL}2$ ≤ 8 mA @ V_{OL} = 0.4 V.
5. $|I_{OH}2|$ ≤ 8 mA @ V_{OH} = 2.4 V.

TAP AC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V

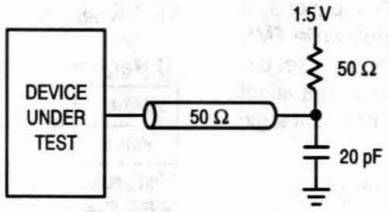
Output Test Load ..... 50 Ω Parallel Terminated T–line with 20 pF Receiver Input Capacitance
Test Load Termination Supply Voltage (V_T) ..... 1.5 V

TAP CONTROLLER TIMING

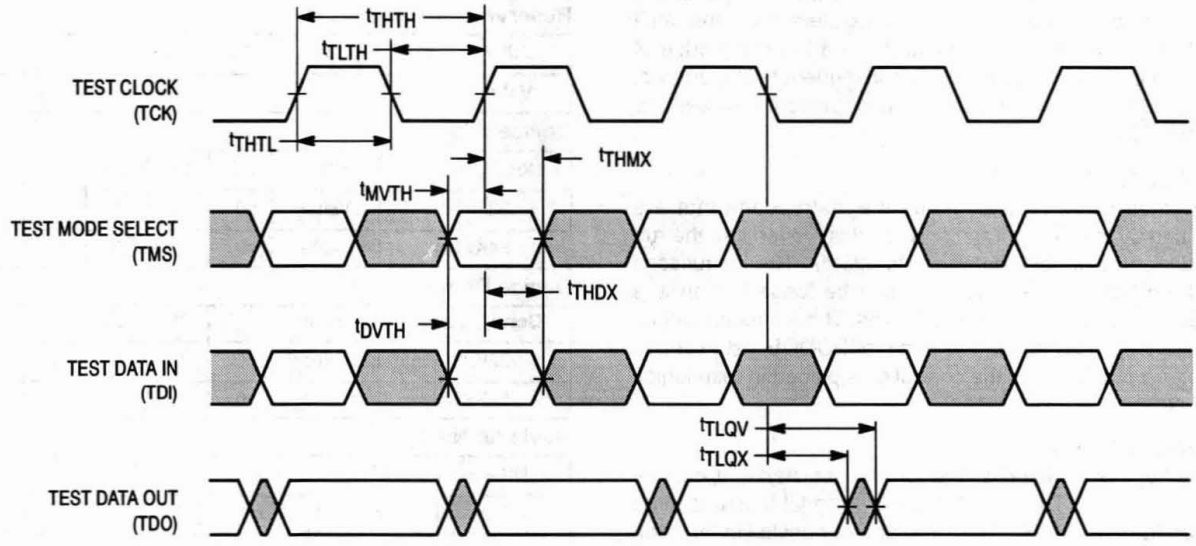
Parameter	Symbol	Min	Max	Unit	Notes
Cycle Time	t_{THTH}	100	—	ns	
Clock High Time	t_{THTL}	40	—	ns	
Clock Low Time	t_{TLTH}	40	—	ns	
TMS Setup	t_{MVTH}	10	—	ns	
TMS Hold	t_{THMX}	10	—	ns	
TDI Valid to TCK High	t_{DVTH}	10	—	ns	
TCK High to TDI Don't Care	t_{THDX}	10	—	ns	
Capture Setup	t_{CS}	10	—	ns	1
Capture Hold	t_{CH}	10	—	ns	1
TCK Low to TDO Unknown	t_{TLQX}	0	—	ns	
TCK Low to TDO Valid	t_{TLOV}	—	20	ns	

NOTES:
1. t_{CS} + t_{CH} defines the minimum pause in RAM I/O pad transitions to assure accurate pad data capture.

AC TEST LOAD



TAP CONTROLLER TIMING DIAGRAM



TEST ACCESS PORT PINS

TCK – TEST CLOCK (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

TMS – TEST MODE SELECT (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.

TDI – TEST DATA IN (INPUT)

The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (refer to Figure 6 TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.

TDO – TEST DATA OUT (OUTPUT)

Output that is active depending on the state of the TAP state machine (refer to Figure 6 TAP Controller State Diagram). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

TRST – TAP RESET

This device does not have a TRST pin. TRST is optional in **IEEE 1149.1.** The test–logic reset state is entered while TMS is held high for five rising edges of TCK. Power on reset circuitry is included internally. This type of reset does not affect the operation of the system logic. The reset affects test logic only.

TEST ACCESS PORT REGISTERS

OVERVIEW

The various TAP registers are selected (one at a time) via the sequences of ones and zeros input to the TMS pin as the TCK is strobed. Each of the TAPs registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on subsequent falling edge of TCK. When a register is selected it is "placed" between the TDI and TDO pins.

INSTRUCTION REGISTER

The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run test/idle or the various data register states. The instructions are three bits long. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power–up or whenever the controller is placed in test–logic–reset state.

BYPASS REGISTER

The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.

BOUNDARY SCAN REGISTER

The boundary scan register is identical in length to the number of active input and I/O connections on the RAM (not counting the TAP pins). This also includes a number of place holder locations (always set to a logic 1) reserved for density upgrade address pins. There are a total of 70 bits in the case of the x36 device and 51 bits in the case of the x18 device. The boundary scan register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture–DR state and then is placed between the TDI and TDO pins when the controller is moved to shift–DR state. Several TAP instructions can be used to activate the boundary scan register.

The Bump/Bit Scan Order tables describe which device bump connects to each boundary scan register location. The first column defines the bit's position in the boundary scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the input or I/O at the bump and the third column is the bump number.

IDENTIFICATION (ID) REGISTER

The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture–DR state with the IDCODE command loaded in the instruction register. The code is loaded from a 32 bit on–chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into shift–DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Presence Indicator

Bit #	0
Value	1

Motorola JEDEC ID Code (Compressed Format, per IEEE Standard 1149.1 – 1990

Bit #	11	10	9	8	7	6	5	4	3	2	1
Value	0	0	0	0	0	0	0	1	1	1	0

Reserved For Future Use

Bit #	17	16	15	14	13	12
Value	x	x	x	x	x	x

Device Width

Configuration	Bit #	22	21	20	19	18
32Kx36	Value	0	0	1	0	0
64Kx18	Value	0	0	0	1	1

Device Depth

Configuration	Bit #	27	26	25	24	23
32Kx36	Value	0	0	0	1	1
64Kx18	Value	0	0	1	0	0

Revision Number

Bit #	31	30	29	28
Value	x	x	x	x

Figure 5. ID Register Bit Meanings

MCM69L536 Bump/Bit Scan Order

BIT #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID
1	M2	5R	36	NC	3B
2	SA	4P	37	NC	2B
3	SA	4T	38	SA	3A
4	SA	6R	39	SA	3C
5	SA	5T	40	SA	2C
6	ZZ	7T	41	SA	2A
7	DQa	6P	42	DQc	2D
8	DQa	7P	43	DQc	1D
9	DQa	6N	44	DQc	2E
10	DQa	7N	45	DQc	1E
11	DQa	6M	46	DQc	2F
12	DQa	6L	47	DQc	2G
13	DQa	7L	48	DQc	1G
14	DQa	6K	49	DQc	2H
15	DQa	7K	50	DQc	1H
16	$\overline{SBa}$	5L	51	$\overline{SBc}$	3G
17	$\overline{CK}$	4L	52	ZQ	4D
18	CK	4K	53	$\overline{SS}$	4E
19	$\overline{G}$	4F	54	NF	4G
20	$\overline{SBb}$	5G	55	NF	4H
21	DQb	7H	56	$\overline{SW}$	4M
22	DQb	6H	57	$\overline{SBd}$	3L
23	DQb	7G	58	DQd	1K
24	DQb	6G	59	DQd	2K
25	DQb	6F	60	DQd	1L
26	DQb	7E	61	DQd	2L
27	DQb	6E	62	DQd	2M
28	DQb	7D	63	DQd	1N
29	DQb	6D	64	DQd	2N
30	SA	6A	65	DQd	1P
31	SA	6C	66	DQd	2P
32	SA	5C	67	SA	3T
33	SA	5A	68	SA	2R
34	NC	6B	69	SA	4N
35	NC	5B	70	M1	3R

MCM69L618 Bump/Bit Scan Order

Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID
1	M2	5R	36	$\overline{SBb}$	3G
2	SA	6T	37	ZQ	4D
3	SA	4P	38	$\overline{SS}$	4E
4	SA	6R	39	NF	4G
5	SA	5T	40	NF	4H
6	ZZ	7T	41	$\overline{SW}$	4M
7	DQa	7P	42	DQb	2K
8	DQa	6N	43	DQb	1L
9	DQa	6L	44	DQb	2M
10	DQa	7K	45	DQb	1N
11	$\overline{SBa}$	5L	46	DQb	2P
12	$\overline{CK}$	4L	47	SA	3T
13	CK	4K	48	SA	2R
14	$\overline{G}$	4F	49	SA	4N
15	DQa	6H	50	SA	2T
16	DQa	7G	51	M1	3R
17	DQa	6F			
18	DQa	7E			
19	DQa	6D			
20	SA	6A			
21	SA	6C			
22	SA	5C			
23	SA	5A			
24	NC	6B			
25	NC	5B			
26	NC	3B			
27	NC	2B			
28	SA	3A			
29	SA	3C			
30	SA	2C			
31	SA	2A			
32	DQb	1D			
33	DQb	2E			
34	DQb	2G			
35	DQb	1H			

NOTES:

1. The NC pads listed in this table are indeed no connects, but are represented in the boundary scan register by a "place holder" bit that is forced to logic 1. These pads are reserved for use as address inputs on higher density RAMs that follow this pad out and scan order standard.
2. CK, $\overline{CK}$, are sampled individually. $\overline{CK}$ is not simply a forced complement of the CK input. In scan mode these differential inputs are referenced to V_{ref}, not each other.
3. ZQ, M1, and M2 are not ordinary inputs and may not respond to standard I/O logic levels. ZQ, M1, and M2 must be driven to within 100 mV of a V_{DD} or V_{SS} supply rail to ensure consistent results.
4. ZZ must remain at V_{IL} during boundary scan to ensure consistent results.

TAP Controller Instruction Set

OVERVIEW

There are two classes of instructions defined in the Standard 1149.1–1990; the standard (public) instructions, and device specific (private) instructions. Some public instructions, are mandatory for 1149.1 compliance. Optional public instructions must be implemented in prescribed ways.

Although the TAP controller in this device follows the 1149.1 conventions, it is not 1194.1 compliant because some of the mandatory instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads, but cannot be used to load address, data or control signals into the RAM or to preload the I/O buffers. In other words, the device will not perform Standard 1149.1 EXTEST, INTEST or the preload portion of the SAMPLE / PRELOAD command.

When the TAP controller is placed in capture–IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the shift–IR state the instruction register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to update–IR state. The TAP instruction sets for this device are listed in the following tables.

STANDARD (PUBLIC) INSTRUCTIONS

BYPASS

The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift–DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

Sample/preload is a Standard 1149.1 mandatory public instruction. When the sample / preload instruction is loaded in the Instruction register, moving the TAP controller into the capture–DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set–up plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register.

Moving the controller to shift–DR state then places the boundary scan register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the update–DR state with the SAMPLE / PRELOAD instruction loaded in the instruction register has the same effect as the pause–DR command. This functionality is not Standard 1149.1 compliant.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic 0s. EXTEST is not implemented in this device. Therefore this device is not 1149.1 compliant. Nevertheless, this RAMs TAP does respond to an all zeros instruction, as follows. With the EXTEST (000) instruction loaded in the instruction register the RAM responds just as it does in response to the SAMPLE / PRELOAD instruction described above, except the RAM outputs are forced to high–Z any time the instruction is loaded.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture–DR mode and places the ID register between the TDI and TDO pins in shift–DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test–logic–reset state.

THE DEVICE SPECIFIC (PUBLIC) INSTRUCTION

SAMPLE–Z

If the SAMPLE–Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high–Z) and the boundary scan register is connected between TDI and TDO when the TAP controller is moved to the shift–DR state.

THE DEVICE SPECIFIC (PRIVATE) INSTRUCTION

NOOP

Do not use these instructions; they are reserved for future use.

STANDARD (PUBLIC) INSTRUCTION CODES

Instruction	Code*	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM outputs to High–Z state. *NOT 1149.1 COMPLIANT*
IDCODE	001**	Preloads ID register and places it between TDI and TDO. Does not affect RAM operation.
SAMPLE / PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect RAM operation. Does not implement 1149.1 Preload function. * NOT 1149.1 COMPLIANT *
BYPASS	111	Places bypass register between TDI and TDO. Does not affect RAM operation.
SAMPLE–Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM output drivers to High–Z.

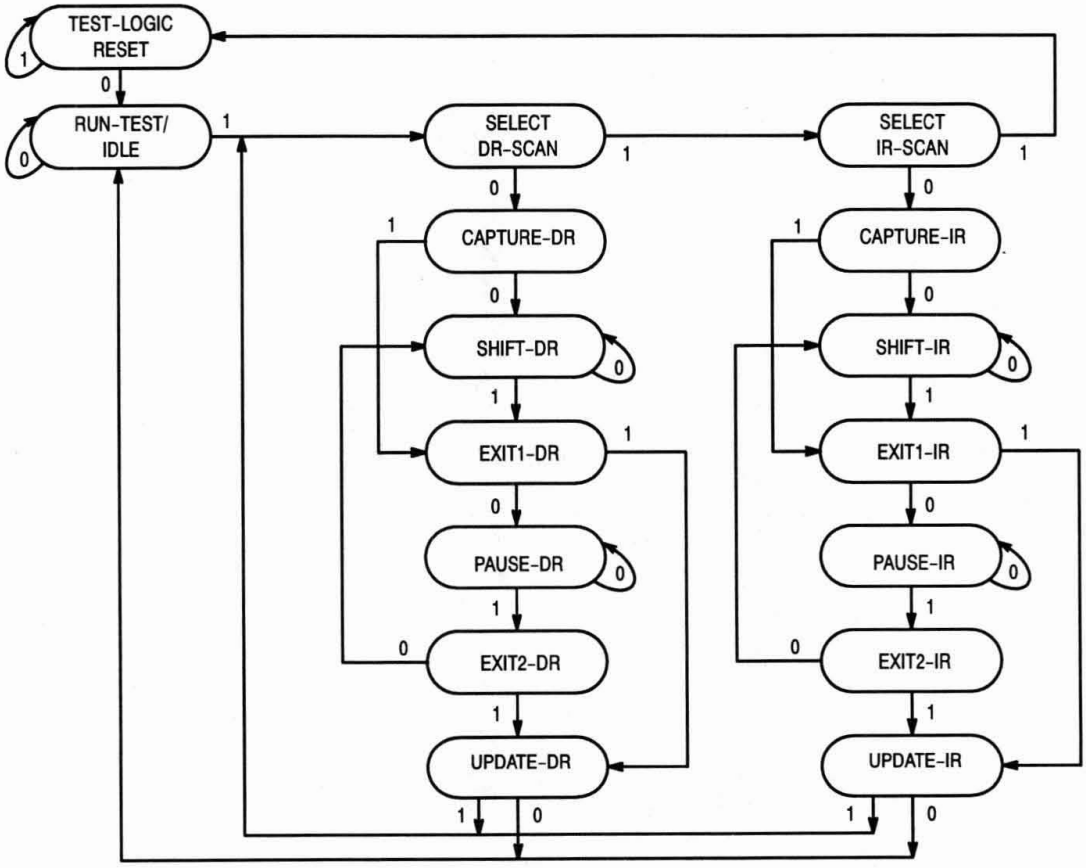
* Instruction codes expressed in binary, MSB on left, LSB on right.
** Default instruction automatically loaded at power–up and in test–logic–reset state.

3

STANDARD (PRIVATE) INSTRUCTION CODES

Instruction	Code*	Description
NO OP	011	Do not use these instructions; they are reserved for future use.
NO OP	101	Do not use these instructions; they are reserved for future use.
NO OP	110	Do not use these instructions; they are reserved for future use.

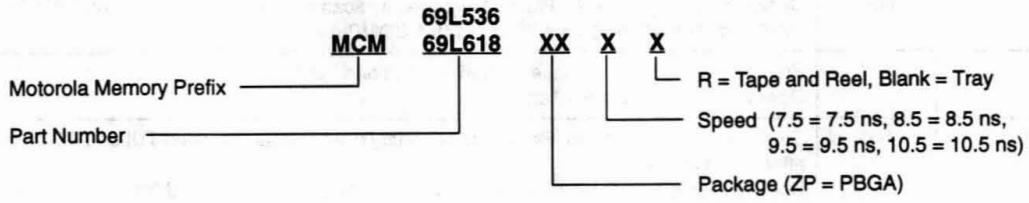
* Instruction codes expressed in binary, MSB on left, LSB on right.



NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 6. TAP Controller State Diagram

ORDERING INFORMATION
(Order by Full Part Number)


69L536
MCM 69L618 XX X X
Motorola Memory Prefix
Part Number
R = Tape and Reel, Blank = Tray
Speed (7.5 = 7.5 ns, 8.5 = 8.5 ns, 9.5 = 9.5 ns, 10.5 = 10.5 ns)
Package (ZP = PBGA)

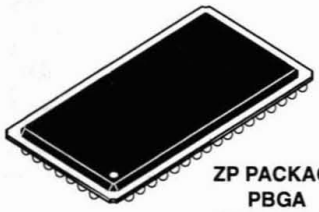
Full Part Numbers —	MCM69L536ZP7.5	MCM69L536ZP8.5	MCM69L536ZP9.5	MCM69L536ZP10.5
	MCM69L618ZP7.5	MCM69L618ZP8.5	MCM69L618ZP9.5	MCM69L618ZP10.5
	MCM69L536ZP7.5R	MCM69L536ZP8.5R	MCM69L536ZP9.5R	MCM69L536ZP10.5R
	MCM69L618ZP7.5R	MCM69L618ZP8.5R	MCM69L618ZP9.5R	MCM69L618ZP10.5R

3

MCM69L537
MCM69L619

Advance Information

1M Late Write LVTTL



ZP PACKAGE
PBGA
CASE 999–01

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The MCM69L537/619 is a 1 megabit synchronous late write fast static RAM designed to provide high performance in secondary cache, ATM switch, Telecom, and other high speed memory applications. The MCM69L619 organized as 64K words by 18 bits, and the MCM69L537 organized as 32K words by 36 bits wide are fabricated in Motorola's high performance silicon gate BiCMOS technology.

The differential CK clock inputs control the timing of read/write operations of the RAM. At the rising edge of the CK clock all addresses, write enables, and synchronous selects are registered. An internal buffer and special logic enable the memory to accept write data on the rising edge of the CK clock a cycle after address and control signals. Read data is driven on the falling edge of the CK clock also.

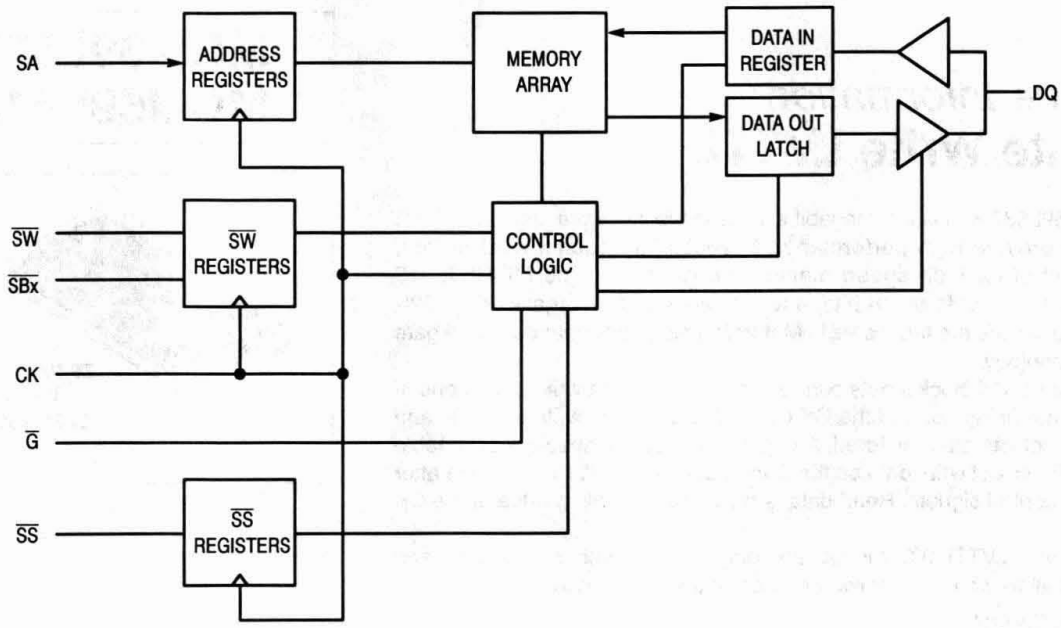
The RAM uses LVTTL 3.3 V inputs and outputs. The synchronous write and byte enables allow writing to individual bytes or the entire word.

- Byte Write Control
- Single 3.3 V + 10%, – 5% Operation
- LVTTL 3.3 V I/O (V_{DDQ})
- Register to Latch Synchronous Operation
- Asynchronous Output Enable
- Boundary Scan (JTAG) IEEE 1149.1 Compatible
- Differential Clock Inputs
- Optional x 18 or x 36 organization
- MCM69L537/619 – 7.5 = 7.5 ns
  MCM69L537/619 – 8.5 = 8.5 ns
  MCM69L537/619 – 9.5 = 9.5 ns
  MCM69L537/619 – 10.5 = 10.5 ns
- 119 Bump, 50 mil (1.27 mm) Pitch, 14 mm x 22 mm Plastic Ball Grid Array (PBGA) Package

This document contains information on a new product. Specifications and information herein are subject to change without notice.

4/2/97

FUNCTIONAL BLOCK DIAGRAM



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PIN ASSIGNMENTS

TOP VIEW

MCM69L537

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	NC	NC	NC	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
E	DQc	DQc	V_{SS}	$\overline{SS}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{G}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{SBc}$	NF	$\overline{SBb}$	DQb	DQb
H	DQc	DQc	V_{SS}	NF	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CK	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{SBd}$	$\overline{CK}$	$\overline{SBa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{SW}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
P	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
R	NC	SA	V_{DD}	V_{DD}	V_{SS}	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69L619

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	NC	NC	NC	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQb	NC	V_{SS}	NC	V_{SS}	DQa	NC
E	NC	DQb	V_{SS}	$\overline{SS}$	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	$\overline{SBb}$	NF	V_{SS}	NC	DQa
H	DQb	NC	V_{SS}	NF	V_{SS}	DQa	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	CK	V_{SS}	NC	DQa
L	DQb	NC	V_{SS}	$\overline{CK}$	$\overline{SBa}$	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{SW}$	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	SA	V_{SS}	DQa	NC
P	NC	DQb	V_{SS}	SA	V_{SS}	NC	DQa
R	NC	SA	V_{DD}	V_{DD}	V_{SS}	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69L537 PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6K, 7K, 6L, 7L, 6M, 6N, 7N, 6P, 7P (b) 6D, 7D, 6E, 7E, 6F, 6G, 7G, 6H, 7H (c) 1D, 2D, 1E, 2E, 2F, 1G, 2G, 1H, 2H (d) 1K, 2K, 1L, 2L, 2M, 1N, 2N, 1P, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 3T, 4T, 5T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 5G, 3G, 3L (a), (b), (c), (d)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
7T	ZZ	Input	Sleep mode, active high.
4C, 2J, 4J, 6J, 3R, 4R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 3H, 5H, 3K, 5K, 3M, 5M, 3N, 5N, 3P, 5P, 5R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 3B, 4B, 5B, 6B, 7B, 1C, 7C, 4D, 3J, 5J, 1R, 7R, 1T, 2T, 6T, 6U	NC	—	No Connection: There is no connection to the chip.
4G, 4H	NF	—	No Function: There is an internal connection to the chip, but the pin has no function on this device.

MCM69L619 PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6D, 7E, 6F, 7G, 6H, 7K, 6L, 6N, 7P (b) 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 2T, 3T, 5T, 6T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 3G (a), (b)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
7T	ZZ	Input	Sleep mode, active high.
4C, 2J, 4J, 6J, 3R, 4R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P, 5R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 3B, 4B, 5B, 6B, 7B, 1C, 7C, 2D, 4D, 7D, 1E, 6E, 2F, 1G, 6G, 2H, 7H, 3J, 5J, 1K, 6K, 2L, 7L, 6M, 2N, 7N, 1P, 6P, 1R, 7R, 1T, 4T, 6U	NC	—	No Connection: There is no connection to the chip.
4G, 4H	NF	—	No Function: There is an internal connection to the chip, but the pin has no function on this device.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS}, See Note 1)

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Output Supply Voltage	V_{DDQ}	– 0.5 to V_{DD} + 0.5	V
Voltage On Any Pin	V_{in}	– 0.5 to V_{DD} + 0.5	V
Input Current (per I/O)	I_{in}	± 50	mA
Output Current (per I/O)	I_{out}	± 70	mA
Power Dissipation (See Note 2)	P_D	—	W
Operating Temperature	T_A	0 to + 70	°C
Temperature Under Bias	T_{bias}	–10 to + 85	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability will be dependent upon package characteristics and use environment. See enclosed thermal impedance data.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

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PBGA PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (Still Air)		$R_{\theta JA}$	59	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Single Layer Board	$R_{\theta JA}$	44	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Four Layer Board	$R_{\theta JA}$	28	°C/W	
Junction to Board (Bottom)		$R_{\theta JB}$	18	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, pwer dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

($0°C \le T_A \le 70°C$, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (See Notes 1 through 4)

Parameter		Symbol	Min	Typical –7.5	Typical –8.5	Typical –9.5	Typical –10.5	Max	Unit	Notes
Core Power Supply Voltage		V_{DD}	3.15	—	—	—	—	3.6	V	
Output Driver Supply Voltage		V_{DDQ}	1.4	—	—	—	—	1.6	V	
Active Power Supply Current	(x18) (x36)	I_{DD1}	— —	TBD TBD	TBD TBD	TBD TBD	TBD TBD	TBD	mA	5
Quiescent Active Power Supply Current	(x18) (x36)	I_{DD2}	— —	TBD TBD	TBD TBD	TBD TBD	TBD TBD	TBD	mA	6, 10
Active Standby Power Supply Current	(x18) (x36)	I_{SB1}	— —	TBD TBD	TBD TBD	TBD TBD	TBD TBD	TBD	mA	7
Quiescent Standby Power Supply Current	(x18) (x36)	I_{SB2}	— —	TBD TBD	TBD TBD	TBD TBD	TBD TBD	TBD	mA	8, 10
Sleep Mode Power Supply Current		I_{SB3}	—	TBD	TBD	TBD	TBD	TBD	mA	9, 10

NOTES:
1. All data sheet parameters specified to full range of V_{DD} unless otherwise noted. All voltages are referenced to voltage applied to V_{SS} bumps.
2. Supply voltage applied to V_{DD} connections.
3. Supply voltage applied to V_{DDQ} connections.
4. All power supply currents measured with outputs open or deselected.
5. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered active, 50% read cycles.
6. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered active.
7. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered inactive.
8. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered inactive. ZZ low.
9. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered inactive, ZZ high.
10. 200 mV ≥ V_{in} ≥ V_{DDQ} – 200 mV.

DC INPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
DC Input Logic High	V_{IH} (dc)	2.0	V_{DD} + 0.3	V	
DC Input Logic Low	V_{IL} (dc)	– 0.3	0.8	V	1
Input Leakage Current	I_{lkg}	—	± 5	µA	2
Clock Input Leakage Current	I_{clkg}	—	± 8	µA	2
Clock Input Signal Voltage	V_{in}	– 0.3	V_{DD} + 0.3	V	
Clock Input Differential Voltage	V_{DIF} (dc)	0.2	V_{DD} + 0.6	V	3
Clock Input Common Mode Voltage Range (See Figure 3)	V_{CM} (dc)	1.1	2.1	V	4

NOTES:
1. Inputs may undershoot to – 0.5 V (peak) for up to 20% t_{KHKH} (e.g., 2 ns at a clock cycle time of 10 ns).
2. $0 V \le V_{in} \le V_{DD}$.
3. Minimum instantaneous differential input voltage required for differential input clock operation.
4. Maximum rejectable common mode input voltage variation.

DC OUTPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
Output Leakage Current	I_{lkg}	–1.0	1.0	µA	
Output Low Voltage	V_{OL}	—	0.4	V	1
Output High Voltage	V_{OH}	2.4	—	V	2

NOTES:
1. I_{OL} = 8.0 mA.
2. I_{OH} = – 8.0 mA.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, 0°C ≤ T_A ≤ 70°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	5	pF
Input/Output Capacitance	$C_{I/O}$	7	8	pF
CK, $\overline{CK}$ Capacitance	C_{CK}	4	5	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V
Clock Input Timing Reference Level ..... Differential Cross–Point

READ/WRITE CYCLE TIMING (See Note 3)

Parameter	Symbol	MCM69L536–7.5 MCM69L618–7.5		MCM69L536–8.5 MCM69L618–8.5		MCM69L536–9.5 MCM69L618–9.5		MCM69L536–10.5 MCM69L618–10.5		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	7	—	8	—	9	—	10	—	ns	
Clock High Pulse Width	t_{KHKL}	2.8	—	3.2	—	3.6	—	4	—	ns	
Clock Low Pulse Width	t_{KLKH}	2.8	—	3.2	—	3.6	—	4	—	ns	
Clock High to Output Valid	t_{KHQV}	—	7.5	—	8.5	—	9.5	—	10.5	ns	1
Clock Low to Output Valid	t_{KLQV}	—	3.5	—	4	—	4	—	4	ns	1
Clock Low to Output Hold	t_{KLQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	
Clock Low to Output Low–Z	t_{KLQX1}	1	—	1	—	1	—	1	—	ns	2
Clock High to Output High–Z	t_{KHQZ}	—	3.5	—	4	—	4	—	4	ns	2
Output Enable Low to Output Low–Z	t_{GLQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	2
Output Enable Low to Output Valid	t_{GLQV}	—	3.5	—	4	—	4	—	4	ns	2
Output Enable to Output Hold	t_{GHQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	2
Output Enable High to Output High–Z	t_{GHQZ}	—	3.5	—	4	—	4	—	4	ns	2
Setup Times: Address Data In Chip Select Write Enable	t_{AVKH} t_{DVKH} t_{SVKH} t_{WVKH}	0.5	—	0.5	—	0.5	—	0.5	—	ns	
Hold Times: Address Data In Chip Select Write Enable	t_{KHAX} t_{KHDX} t_{KHSX} t_{KHWX}	1	—	1	—	1	—	1	—	ns	

NOTES:
1. Tested per AC Test Load diagram. See Figure 1.
2. Measured at ± 200 mV from steady state.
3. In no case may control input signals (e.g., $\overline{SS}$) be operated with pulse widths less than the minimum clock input pulse width specifications (e.g., t_{KHKL}) or at frequencies that exceed the applied K clock frequency.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

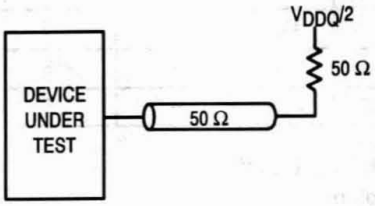


Figure 1. Test Loads

3

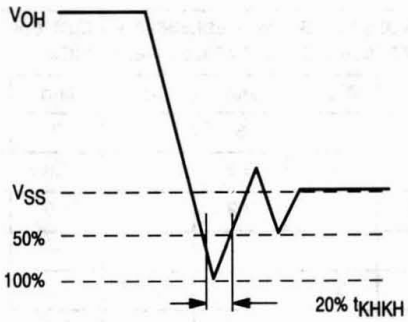
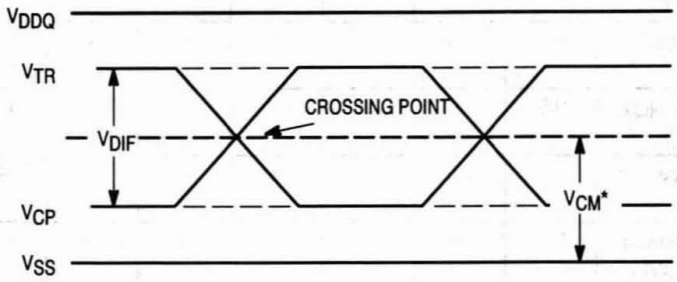


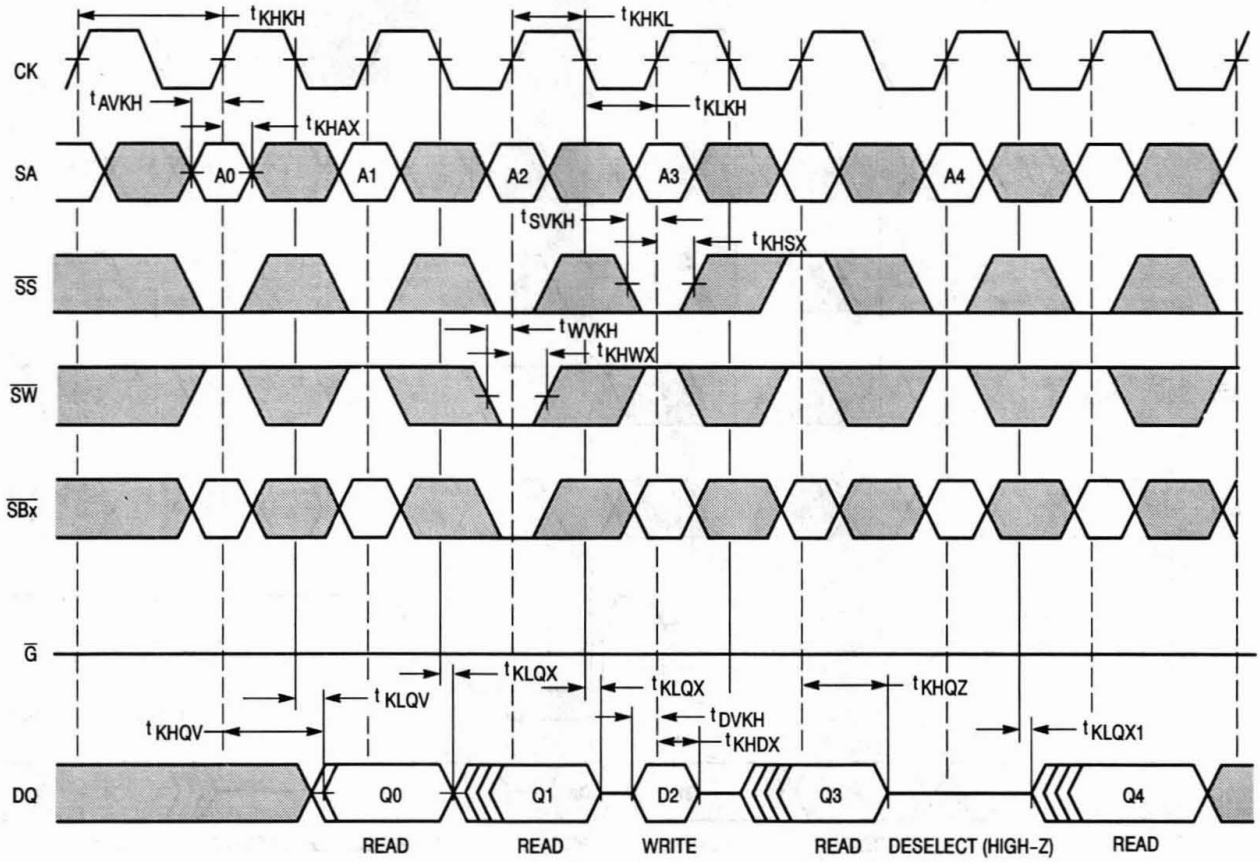
Figure 2. Undershoot Voltage



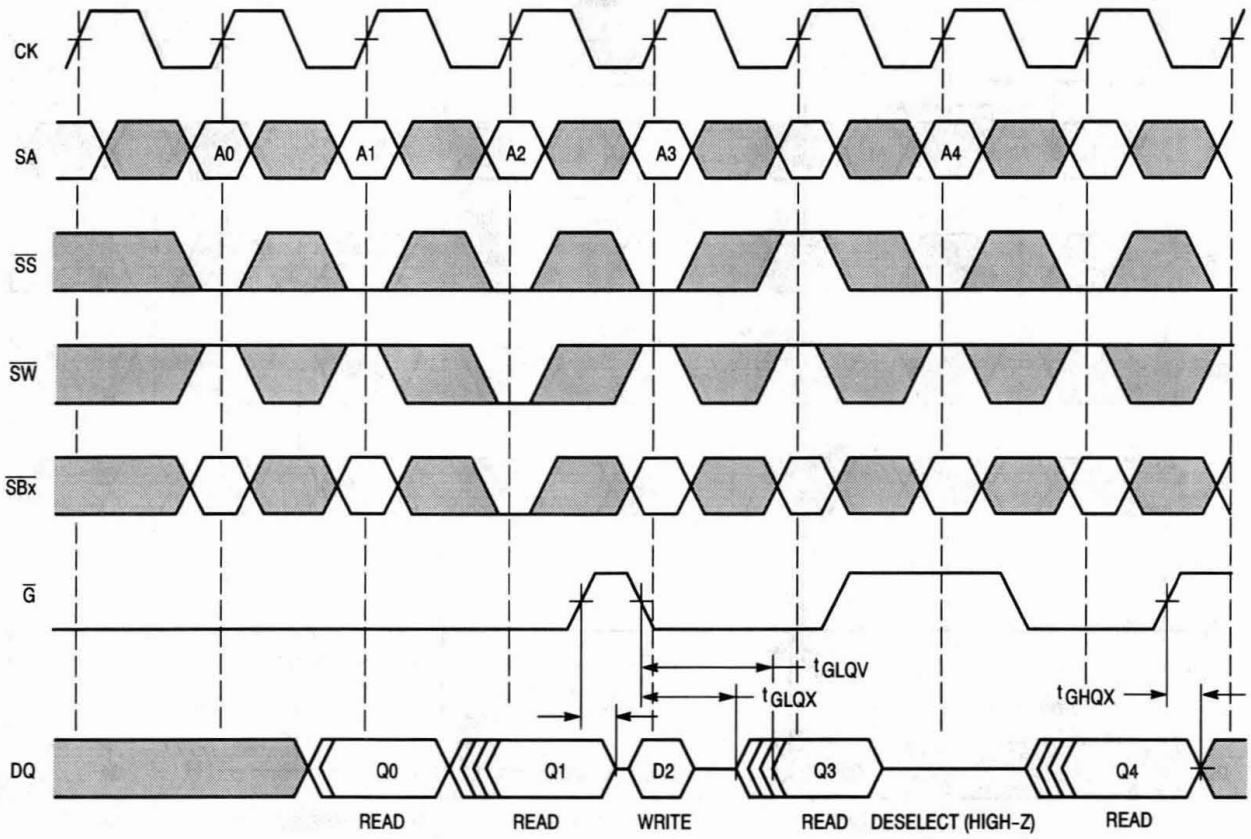
*V_{CM}, the Common Mode Input Voltage, equals $V_{TR} - ((V_{TR} - V_{CP})/2)$.

Figure 3. Differential Inputs/Common Mode Input Voltage

REGISTER LATCH READ–WRITE–READ CYCLES



REGISTER LATCH READ–WRITE–READ CYCLES
($\overline{G}$ Controlled)



FUNCTIONAL OPERATION

READ AND WRITE OPERATIONS

All control signals except $\overline{G}$ are registered on the rising edge of the CK clock. These signals must meet the setup and hold times shown in the AC Characteristics table.On the falling edge of the current cycle, the output latch becomes transparent and data is available. The output data is latched on the rising edge of the next clock. The output data is available at the output at t_{KLQV} or t_{KHQV} whichever is later. t_{KHQV} is the internal latency of the device. During this same cycle a new read address can be applied to the address pins.

A write cycle can occur on the next cycle as long as t_{KLQX} and t_{DVKH} are met. Read cycles may follow write cycles immediately.

$\overline{G}$, $\overline{SS}$, and $\overline{SW}$ control output drive. Chip deselect via a high on $\overline{SS}$ at the rising edge of the CK clock has its effect on the output drivers immediately. $\overline{SW}$ low deselects the output drivers immediately (on the same cycle). Output selecting via a low on $\overline{SS}$ and high on $\overline{SW}$ at a rising CK clock has its effect on the output drivers at t_{KLQX}. Output drive is also controlled directly by output enable, $\overline{G}$. $\overline{G}$ is an asynchronous input. No clock edges are required to enable or disable the output with $\overline{G}$.

Output data will be valid the latter of t_{GLQV}, t_{KHQV}, or t_{KLQV}. Outputs will begin driving at t_{KLQX1}. Outputs will hold previous data until t_{KLQX} or t_{GHQX}.

WRITE AND BYTE WRITE FUNCTIONS

Note that in the following discussion the term "byte" refers to nine bits of the RAM I/O bus. In all cases, the timing parameters described for synchronous write input ($\overline{SW}$) apply to each of the byte write enable inputs ($\overline{SBa}$, $\overline{SBb}$, etc.).

Byte write enable inputs have no effect on read cycles. This allows the system designer not interested in performing byte writes to connect the byte enable inputs to active low (V_{SS}). Reads of all bytes proceed normally and write cycles, activated via a low on $\overline{SW}$, and the rising edge of the CK clock, write the entire RAM I/O width. This way the designer is spared having to drive multiple write input buffer loads.

Byte writes are performed using the byte write enable inputs in conjunction with the synchronous write input ($\overline{SW}$). It is important to note that writing any one byte will inhibit a read of all bytes at the current address. The RAM cannot simultaneously read one byte and write another at the same address. A write cycle initiated with none of the byte write enable inputs active is neither a read or a write. No write will occur, but the outputs will be deselected as in a normal write cycle.

LATE WRITE

The write address is sampled on the first rising edge of clock and write data is sampled on the following rising edge.

The late write feature is implemented with single stage write buffering. Write buffering is transparent to the user. A comparator monitors the address bus and, when necessary, routes buffer contents to the outputs to assure coherent operation. This occurs in all cases whether there is a byte write or a full word is written.

POWER UP AND INITIALIZATION

Please note, per the Absolute Maximum Ratings table, V_{DDQ} is not to exceed V_{DD} + 0.5 V, whatever the instantaneous value of V_{DD}. Once supplies have reached specification levels, a minimum dwell of 1.0 µs with CK clock inputs cycling is required before beginning normal operations.

SERIAL BOUNDARY SCAN TEST ACCESS PORT OPERATION

OVERVIEW

The serial boundary scan test access port (TAP) on this RAM is designed to operate in a manner consistent with IEEE Standard 1149.1–1990 (commonly referred to as JTAG), but does not implement all of the functions required for 1149.1 compliance. Certain functions have been modified or eliminated because their implementation places extra delays in the RAMs critical speed path. Nevertheless, the RAM supports the standard TAP controller architecture. (The TAP controller is the state machine that controls the TAPs operation) and can be expected to function in a manner that does not conflict with the operation of devices with Standard 1149.1 compliant TAPs. The TAP operates using conventional JEDEC Standard 8–1B Low Voltage (3.3 V) TTL / CMOS logic level signaling.

DISABLING THE TEST ACCESS PORT

It is possible to use this device without utilizing the TAP. To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid level inputs. TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a 1 k resistor. TDO should be left unconnected.

3

TAP DC OPERATING CHARACTERISTICS

($0°C \le T_A \le 70°C$, Unless Otherwise Noted)

Parameter	Symbol	Min	Max	Unit	Note
Logic Input Logic High	$V_{IH}1$	2.0	V_{DD} + 0.3	V	
Logic Input Logic Low	$V_{IL}1$	– 0.3	0.8	V	
Logic Input Leakage Current	I_{lkg}	—	± 5	µA	1
Output Logic Low	$V_{OL}1$	—	0.2	V	2
Output Logic High	$V_{OH}1$	V_{DD} – 0.2	—	V	3
Output Logic Low	$V_{OL}2$	—	0.4	V	4
Output Logic High	$V_{OH}2$	2.4	—	V	5

NOTES:
1. $0 V \le V_{in} \le V_{DD}$ for all logic input pins.
2. $I_{OL}1 \le 100$ µA @ $V_{OL} = 0.2$ V. Sampled, not 100% tested.
3. $|I_{OH}1| \le 100$ µA @ $V_{DDQ} - 0.2$ V. Sampled, not 100% tested.
4. $I_{OL}2 \le 8$ mA @ $V_{OL} = 0.4$ V.
5. $|I_{OH}2| \le 8$ mA @ $V_{OH} = 2.4$ V.

TAP AC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V

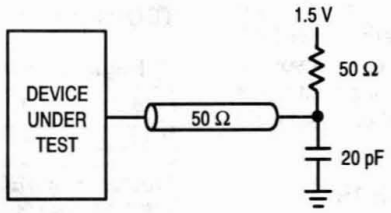
Output Test Load ..... 50 Ω Parallel Terminated T–line with 20 pF Receiver Input Capacitance
Test Load Termination Supply Voltage (V_T) ..... 1.5 V

TAP CONTROLLER TIMING

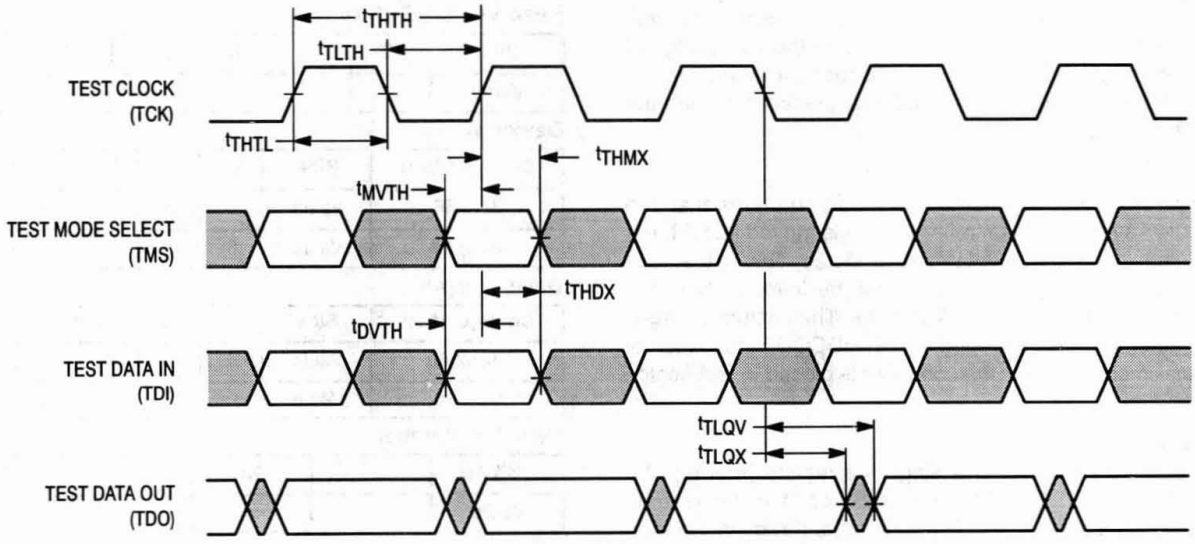
Parameter	Symbol	Min	Max	Unit	Notes
Cycle Time	t_{THTH}	100	—	ns	
Clock High Time	t_{THTL}	40	—	ns	
Clock Low Time	t_{TLTH}	40	—	ns	
TMS Setup	t_{MVTH}	10	—	ns	
TMS Hold	t_{THMX}	10	—	ns	
TDI Valid to TCK High	t_{DVTH}	10	—	ns	
TCK High to TDI Don't Care	t_{THDX}	10	—	ns	
Capture Setup	t_{CS}	10	—	ns	1
Capture Hold	t_{CH}	10	—	ns	1
TCK Low to TDO Unknown	t_{TLQX}	0	—	ns	
TCK Low to TDO Valid	t_{TLOV}	—	20	ns	

NOTES:
1. t_{CS} + t_{CH} defines the minimum pause in RAM I/O pad transitions to assure accurate pad data capture.

AC TEST LOAD



TAP CONTROLLER TIMING DIAGRAM



TEST ACCESS PORT PINS

TCK – TEST CLOCK (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

TMS – TEST MODE SELECT (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.

TDI – TEST DATA IN (INPUT)

The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (refer to Figure 5 TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.

TDO – TEST DATA OUT (OUTPUT)

Output that is active depending on the state of the TAP state machine (refer to Figure 5 TAP Controller State Diagram). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

TRST – TAP RESET

This device does not have a TRST pin. TRST is optional in **IEEE 1149.1.** The test–logic reset state is entered while TMS is held high for five rising edges of TCK. Power on reset circuitry is included internally. This type of reset does not affect the operation of the system logic. The reset affects test logic only.

TEST ACCESS PORT REGISTERS

OVERVIEW

The various TAP registers are selected (one at a time) via the sequences of ones and zeros input to the TMS pin as the TCK is strobed. Each of the TAPs registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on subsequent falling edge of TCK. When a register is selected it is "placed" between the TDI and TDO pins.

INSTRUCTION REGISTER

The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run test/idle or the various data register states. The instructions are three bits long. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power–up or whenever the controller is placed in test–logic–reset state.

BYPASS REGISTER

The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.

BOUNDARY SCAN REGISTER

The boundary scan register is identical in length to the number of active input and I/O connections on the RAM (not counting the TAP pins). This also includes a number of place holder locations (always set to a logic 1) reserved for density upgrade address pins. There are a total of 70 bits in the case of the x36 device and 51 bits in the case of the x18 device. The boundary scan register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture–DR state and then is placed between the TDI and TDO pins when the controller is moved to shift–DR state. Several TAP instructions can be used to activate the boundary scan register.

The Bump/Bit Scan Order tables describe which device bump connects to each boundary scan register location. The first column defines the bit's position in the boundary scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the input or I/O at the bump and the third column is the bump number.

IDENTIFICATION (ID) REGISTER

The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture–DR state with the IDCODE command loaded in the instruction register. The code is loaded from a 32 bit on–chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into shift–DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Presence Indicator

Bit #	0
Value	1

Motorola JEDEC ID Code (Compressed Format, per IEEE Standard 1149.1 – 1990)

Bit #	11	10	9	8	7	6	5	4	3	2	1
Value	0	0	0	0	0	0	0	1	1	1	0

Reserved For Future Use

Bit #	17	16	15	14	13	12
Value	x	x	x	x	x	x

Device Width

Configuration	Bit #	22	21	20	19	18
32Kx36	Value	0	0	1	0	0
64Kx18	Value	0	0	0	1	1

Device Depth

Configuration	Bit #	27	26	25	24	23
32Kx36	Value	0	0	0	1	1
64Kx18	Value	0	0	1	0	0

Revision Number

Bit #	31	30	29	28
Value	x	x	x	x

Figure 4. ID Register Bit Meanings

MCM69L537 Bump/Bit Scan Order

BIT #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	NC	3B
2	SA	4P		37	NC	2B
3	SA	4T		38	SA	3A
4	SA	6R		39	SA	3C
5	SA	5T		40	SA	2C
6	ZZ	7T		41	SA	2A
7	DQa	6P		42	DQc	2D
8	DQa	7P		43	DQc	1D
9	DQa	6N		44	DQc	2E
10	DQa	7N		45	DQc	1E
11	DQa	6M		46	DQc	2F
12	DQa	6L		47	DQc	2G
13	DQa	7L		48	DQc	1G
14	DQa	6K		49	DQc	2H
15	DQa	7K		50	DQc	1H
16	$\overline{SBa}$	5L		51	$\overline{SBc}$	3G
17	$\overline{CK}$	4L		52	ZQ	4D
18	CK	4K		53	$\overline{SS}$	4E
19	$\overline{G}$	4F		54	NF	4G
20	$\overline{SBb}$	5G		55	NF	4H
21	DQb	7H		56	$\overline{SW}$	4M
22	DQb	6H		57	$\overline{SBd}$	3L
23	DQb	7G		58	DQd	1K
24	DQb	6G		59	DQd	2K
25	DQb	6F		60	DQd	1L
26	DQb	7E		61	DQd	2L
27	DQb	6E		62	DQd	2M
28	DQb	7D		63	DQd	1N
29	DQb	6D		64	DQd	2N
30	SA	6A		65	DQd	1P
31	SA	6C		66	DQd	2P
32	SA	5C		67	SA	3T
33	SA	5A		68	SA	2R
34	NC	6B		69	SA	4N
35	NC	5B		70	M1	3R

MCM69L619 Bump/Bit Scan Order

Bit #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	$\overline{SBb}$	3G
2	SA	6T		37	ZQ	4D
3	SA	4P		38	$\overline{SS}$	4E
4	SA	6R		39	NF	4G
5	SA	5T		40	NF	4H
6	ZZ	7T		41	$\overline{SW}$	4M
7	DQa	7P		42	DQb	2K
8	DQa	6N		43	DQb	1L
9	DQa	6L		44	DQb	2M
10	DQa	7K		45	DQb	1N
11	$\overline{SBa}$	5L		46	DQb	2P
12	$\overline{CK}$	4L		47	SA	3T
13	CK	4K		48	SA	2R
14	$\overline{G}$	4F		49	SA	4N
15	DQa	6H		50	SA	2T
16	DQa	7G		51	M1	3R
17	DQa	6F				
18	DQa	7E				
19	DQa	6D				
20	SA	6A				
21	SA	6C				
22	SA	5C				
23	SA	5A				
24	NC	6B				
25	NC	5B				
26	NC	3B				
27	NC	2B				
28	SA	3A				
29	SA	3C				
30	SA	2C				
31	SA	2A				
32	DQb	1D				
33	DQb	2E				
34	DQb	2G				
35	DQb	1H				

NOTES:

1. The NC pads listed in this table are indeed no connects, but are represented in the boundary scan register by a "place holder" bit that is forced to logic 1. These pads are reserved for use as address inputs on higher density RAMs that follow this pad out and scan order standard.
2. CK, $\overline{CK}$, are sampled individually. $\overline{CK}$ is not simply a forced complement of the CK input.
3. M1 and M2 are not ordinary inputs and may not respond to standard I/O logic levels. M1 and M2 must be driven to within 100 mV of a V_{DD} or V_{SS} supply rail to ensure consistent results.
4. ZZ must remain at V_{IL} during boundary scan to ensure consistent results.

TAP Controller Instruction Set

OVERVIEW

There are two classes of instructions defined in the Standard 1149.1–1990; the standard (public) instructions, and device specific (private) instructions. Some public instructions, are mandatory for 1149.1 compliance. Optional public instructions must be implemented in prescribed ways.

Although the TAP controller in this device follows the 1149.1 conventions, it is not 1194.1 compliant because some of the mandatory instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads, but cannot be used to load address, data or control signals into the RAM or to preload the I/O buffers. In other words, the device will not perform Standard 1149.1 EXTEST, INTEST or the preload portion of the SAMPLE / PRELOAD command.

When the TAP controller is placed in capture–IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the shift–IR state the instruction register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to update–IR state. The TAP instruction sets for this device are listed in the following tables.

STANDARD (PUBLIC) INSTRUCTIONS

BYPASS

The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift–DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

Sample/preload is a Standard 1149.1 mandatory public instruction. When the sample / preload instruction is loaded in the Instruction register, moving the TAP controller into the capture–DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set–up plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register.

Moving the controller to shift–DR state then places the boundary scan register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the update–DR state with the SAMPLE / PRELOAD instruction loaded in the instruction register has the same effect as the pause–DR command. This functionality is not Standard 1149.1 compliant.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic 0s. EXTEST is not implemented in this device. Therefore this device is not 1149.1 compliant. Nevertheless, this RAMs TAP does respond to an all zeros instruction, as follows. With the EXTEST (000) instruction loaded in the instruction register the RAM responds just as it does in response to the SAMPLE / PRELOAD instruction described above, except the RAM outputs are forced to high–Z any time the instruction is loaded.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture–DR mode and places the ID register between the TDI and TDO pins in shift–DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test–logic–reset state.

THE DEVICE SPECIFIC (PUBLIC) INSTRUCTION

SAMPLE–Z

If the SAMPLE–Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high–Z) and the boundary scan register is connected between TDI and TDO when the TAP controller is moved to the shift–DR state.

THE DEVICE SPECIFIC (PRIVATE) INSTRUCTION

NOOP

Do not use these instructions; they are reserved for future use.

STANDARD (PUBLIC) INSTRUCTION CODES

Instruction	Code*	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM outputs to High–Z state. *NOT 1149.1 COMPLIANT*
IDCODE	001**	Preloads ID register and places it between TDI and TDO. Does not affect RAM operation.
SAMPLE / PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect RAM operation. Does not implement 1149.1 Preload function. * NOT 1149.1 COMPLIANT *
BYPASS	111	Places bypass register between TDI and TDO. Does not affect RAM operation.
SAMPLE–Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM output drivers to High–Z.

* Instruction codes expressed in binary, MSB on left, LSB on right.
** Default instruction automatically loaded at power–up and in test–logic–reset state.

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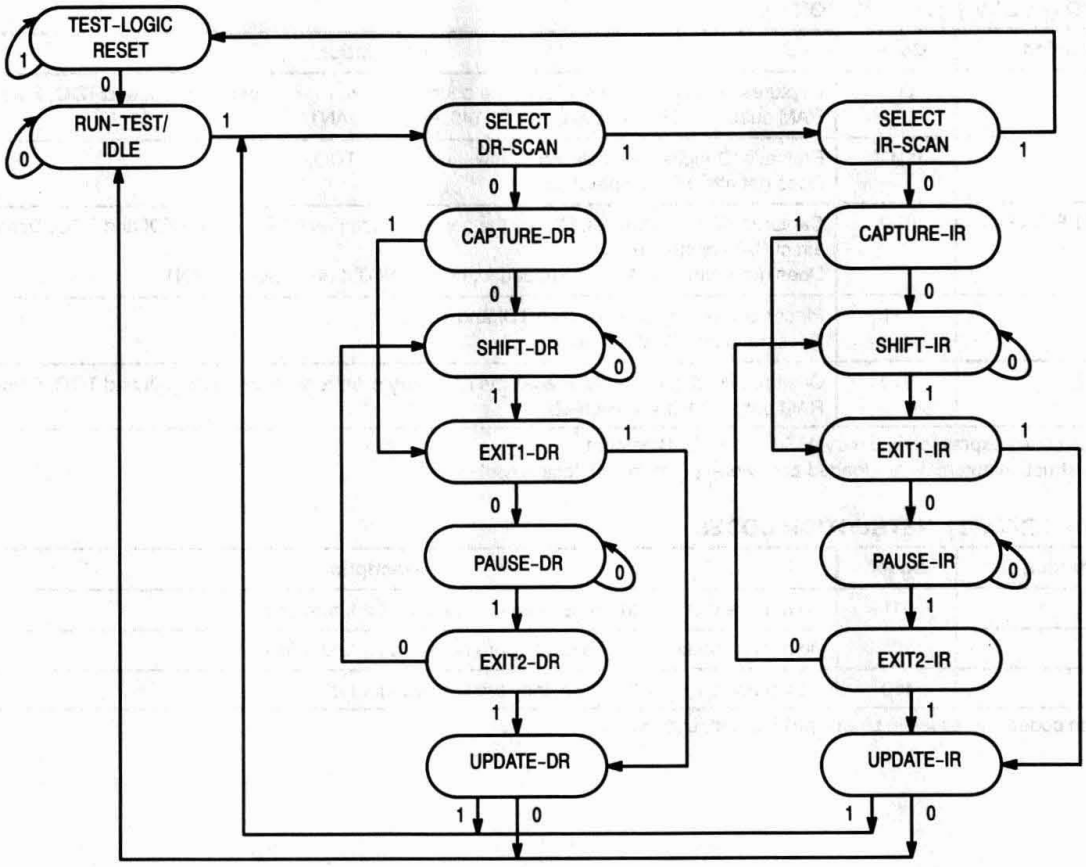
STANDARD (PRIVATE) INSTRUCTION CODES

Instruction	Code*	Description
NO OP	011	Do not use these instructions; they are reserved for future use.
NO OP	101	Do not use these instructions; they are reserved for future use.
NO OP	110	Do not use these instructions; they are reserved for future use.

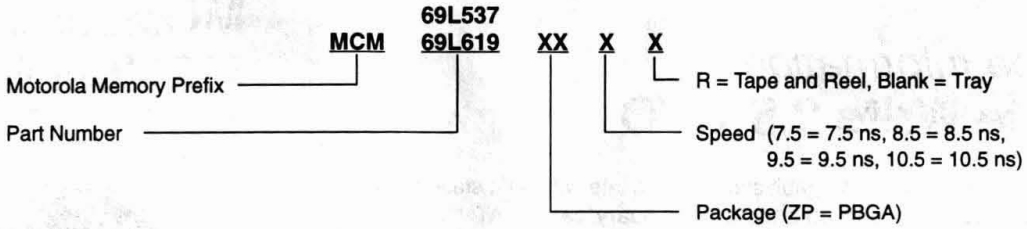
* Instruction codes expressed in binary, MSB on left, LSB on right.



NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 5. TAP Controller State Diagram

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers —	MCM69L537ZP7.5	MCM69L537ZP8.5	MCM69L537ZP9.5	MCM69L537ZP10.5
	MCM69L619ZP7.5	MCM69L619ZP8.5	MCM69L619ZP9.5	MCM69L619ZP10.5
	MCM69L537ZP7.5R	MCM69L537ZP8.5R	MCM69L537ZP9.5R	MCM69L537ZP10.5R
	MCM69L619ZP7.5R	MCM69L619ZP8.5R	MCM69L619ZP9.5R	MCM69L619ZP10.5R

3

MCM69L538
MCM69L620

Advance Information

1M Late Write 2.5 V I/O

ZP PACKAGE
PBGA
CASE 999–01

The MCM69L538/618 is a 1 megabit synchronous late write fast static RAM designed to provide high performance in secondary cache, ATM switch, Telecom, and other high speed memory applications. The MCM69L620 organized as 64K words by 18 bits, and the MCM69L538 organized as 32K words by 36 bits wide are fabricated in Motorola's high performance silicon gate BiCMOS technology.

The differential CK clock inputs control the timing of read/write operations of the RAM. At the rising edge of the CK clock all addresses, write enables, and synchronous selects are registered. An internal buffer and special logic enable the memory to accept write data on the rising edge of the CK clock a cycle after address and control signals. Read data is driven on the falling edge of the CK clock also.

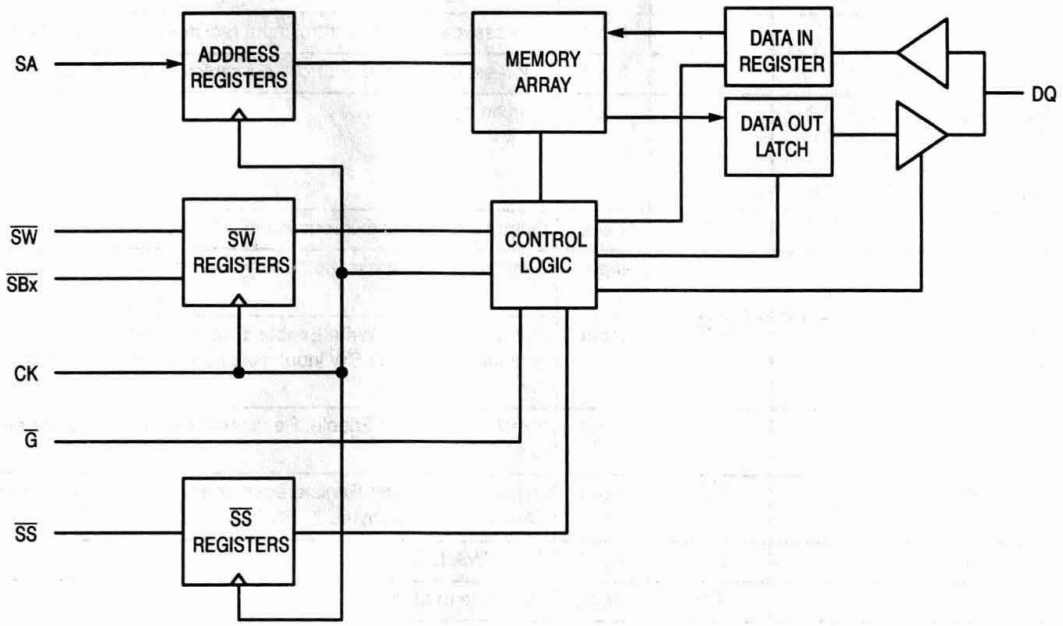
The synchronous write and byte enables allow writing to individual bytes or the entire word.

- Byte Write Control
- Single 3.3 V + 10%, – 5% Operation
- 2.5 V I/O
- Register to Latch Synchronous Operation
- Asynchronous Output Enable
- Boundary Scan (JTAG) IEEE 1149.1 Compatible
- Differential Clock Inputs
- Optional x 18 or x 36 organization
- MCM69L538/618 – 7.5 = 7.5 ns
  MCM69L538/618 – 8.5 = 8.5 ns
  MCM69L538/618 – 9.5 = 9.5 ns
  MCM69L538/618 – 10.5 = 10.5 ns
- 119 Bump, 50 mil (1.27 mm) Pitch, 14 mm x 22 mm Plastic Ball Grid Array (PBGA) Package

This document contains information on a new product. Specifications and information herein are subject to change without notice.

4/2/97

FUNCTIONAL BLOCK DIAGRAM



3

PIN ASSIGNMENTS

TOP VIEW

MCM69L538

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	NC	NC	NC	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
E	DQc	DQc	V_{SS}	$\overline{SS}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{G}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{SBc}$	NF	$\overline{SBb}$	DQb	DQb
H	DQc	DQc	V_{SS}	NF	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CK	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{SBd}$	$\overline{CK}$	$\overline{SBa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{SW}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
P	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
R	NC	SA	V_{DD}	V_{DD}	V_{SS}	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

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	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	NC	NC	NC	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQb	NC	V_{SS}	NC	V_{SS}	DQa	NC
E	NC	DQb	V_{SS}	$\overline{SS}$	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	$\overline{SBb}$	NF	V_{SS}	NC	DQa
H	DQb	NC	V_{SS}	NF	V_{SS}	DQa	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	CK	V_{SS}	NC	DQa
L	DQb	NC	V_{SS}	$\overline{CK}$	$\overline{SBa}$	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{SW}$	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	SA	V_{SS}	DQa	NC
P	NC	DQb	V_{SS}	SA	V_{SS}	NC	DQa
R	NC	SA	V_{DD}	V_{DD}	V_{SS}	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

MCM69L538 PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6K, 7K, 6L, 7L, 6M, 6N, 7N, 6P, 7P (b) 6D, 7D, 6E, 7E, 6F, 6G, 7G, 6H, 7H (c) 1D, 2D, 1E, 2E, 2F, 1G, 2G, 1H, 2H (d) 1K, 2K, 1L, 2L, 2M, 1N, 2N, 1P, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 3T, 4T, 5T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 5G, 3G, 3L (a), (b), (c), (d)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
7T	ZZ	Input	Sleep mode, active high.
4C, 2J, 4J, 6J, 4R, 3R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 3H, 5H, 3K, 5K, 3M, 5M, 3N, 5N, 3P, 5P, 5R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 3B, 4B, 5B, 6B, 7B, 1C, 7C, 4D, 3J, 5J, 1R, 7R, 1T, 2T, 6T, 6U	NC	—	No Connection: There is no connection to the chip. Note: 3J and 5J are tied common.
4G, 4H	NF	—	No Function: There is an internal connection to the chip, but the pin has no function on this device.

MCM69L620 PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
4K	CK	Input	Address, data in and control input register clock. Active high.
4L	$\overline{CK}$	Input	Address, data in and control input register clock. Active low.
(a) 6D, 7E, 6F, 7G, 6H, 7K, 6L, 6N, 7P (b) 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 2P	DQx	I/O	Synchronous Data I/O.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low.
2A, 3A, 5A, 6A, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 2T, 3T, 5T, 6T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5L, 3G (a), (b)	$\overline{SBx}$	Input	Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the $\overline{SW}$ input. Has no effect on read cycles, active low.
4E	$\overline{SS}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4M	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.
4U	TCK	Input	Test Clock (JTAG).
3U	TDI	Input	Test Data In (JTAG).
5U	TDO	Output	Test Data Out (JTAG).
2U	TMS	Input	Test Mode Select (JTAG).
7T	ZZ	Input	Sleep mode, active high.
4C, 2J, 4J, 6J, 4R, 3R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	Output Power Supply: provides operating power for output buffers.
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P, 5R	V_{SS}	Supply	Ground.
4A, 1B, 2B, 3B, 4B, 5B, 6B, 7B, 1C, 7C, 2D, 4D, 7D, 1E, 6E, 2F, 1G, 6G, 2H, 7H, 3J, 5J, 1K, 6K, 2L, 7L, 6M, 2N, 7N, 1P, 6P, 1R, 7R, 1T, 4T, 6U	NC	—	No Connection: There is no connection to the chip. Note: 3J and 5J are tied common.
4G, 4H	NF	—	No Function: There is an internal connection to the chip, but the pin has no function on this device.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS}, See Note 1)

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Output Supply Voltage	V_{DDQ}	– 0.5 to V_{DD} + 0.5	V
Voltage On Any Pin	V_{in}	– 0.5 to V_{DD} + 0.5	V
Input Current (per I/O)	I_{in}	± 50	mA
Output Current (per I/O)	I_{out}	± 70	mA
Power Dissipation (See Note 2)	P_D	—	W
Operating Temperature	T_A	0 to + 70	°C
Temperature Under Bias	T_{bias}	–10 to + 85	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability will be dependent upon package characteristics and use environment. See enclosed thermal impedance data.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

PBGA PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (Still Air)		$R_{\theta JA}$	59	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Single Layer Board	$R_{\theta JA}$	44	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Four Layer Board	$R_{\theta JA}$	28	°C/W	
Junction to Board (Bottom)		$R_{\theta JB}$	18	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, pwer dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

($0°C \le T_A \le 70°C$, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (See Notes 1 through 4)

Parameter		Symbol	Min	Typical –7.5	Typical –8.5	Typical –9.5	Typical –10.5	Max	Unit	Notes
Core Power Supply Voltage		V_{DD}	3.15	—	—	—	—	3.6	V	
Output Driver Supply Voltage		V_{DDQ}	2.3	—	—	—	—	2.7	V	
Active Power Supply Current	(x18) (x36)	I_{DD1}	— —	TBD TBD	TBD TBD	TBD TBD	TBD TBD	TBD	mA	5
Quiescent Active Power Supply Current	(x18) (x36)	I_{DD2}	— —	TBD TBD	TBD TBD	TBD TBD	TBD TBD	TBD	mA	6, 10
Active Standby Power Supply Current	(x18) (x36)	I_{SB1}	— —	TBD TBD	TBD TBD	TBD TBD	TBD TBD	TBD	mA	7
Quiescent Standby Power Supply Current	(x18) (x36)	I_{SB2}	— —	TBD TBD	TBD TBD	TBD TBD	TBD TBD	TBD	mA	8, 10
Sleep Mode Power Supply Current		I_{SB3}	—	TBD	TBD	TBD	TBD	TBD	mA	9, 10

NOTES:
1. All data sheet parameters specified to full range of V_{DD} unless otherwise noted. All voltages are referenced to voltage applied to V_{SS} bumps.
2. Supply voltage applied to V_{DD} connections.
3. Supply voltage applied to V_{DDQ} connections.
4. All power supply currents measured with outputs open or deselected.
5. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered active, 50% read cycles.
6. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered active.
7. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), $\overline{SS}$ registered inactive.
8. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered inactive. ZZ low.
9. $V_{DD} = V_{DD}$ (max), t_{KHKH} = dc, $\overline{SS}$ registered inactive, ZZ high.
10. $200 \text{ mV} \ge V_{in} \ge V_{DDQ} - 200 \text{ mV}$.

DC INPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
DC Input Logic High	V_{IH} (dc)	1.7	$V_{DD} + 0.3$	V	
DC Input Logic Low	V_{IL} (dc)	– 0.3	0.7	V	1
Input Leakage Current	I_{lkg}	—	± 5	µA	2
Clock Input Leakage Current	I_{clkg}	—	± 8	µA	2
Clock Input Signal Voltage	V_{in}	– 0.3	$V_{DD} + 0.3$	V	
Clock Input Differential Voltage	V_{DIF}(dc)	0.2	$V_{DD} + 0.6$	V	3
Clock Input Common Mode Voltage Range (See Figure 3)	V_{CM}(dc)	1.1	2.1	V	4

NOTES:
1. Inputs may undershoot to – 0.5 V (peak) for up to 20% t_{KHKH} (e.g., 2 ns at a clock cycle time of 10 ns).
2. $0 \text{ V} \le V_{in} \le V_{DD}$ for all pins.
3. Minimum instantaneous differential input voltage required for differential input clock operation.
4. Maximum rejectable common mode input voltage variation.

DC OUTPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
Output Leakage Current	I_{lkg}	–1.0	1.0	µA	
Output Low Voltage	V_{OL}	—	0.7	V	1
Output High Voltage	V_{OH}	1.7	—	V	2

NOTES:
1. $I_{OL} = 8.0$ mA.
2. $I_{OH} = – 8.0$ mA.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, 0°C ≤ T_A ≤ 70°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	5	pF
Input/Output Capacitance	$C_{I/O}$	7	8	pF
CK, $\overline{CK}$ Capacitance	C_{CK}	4	5	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

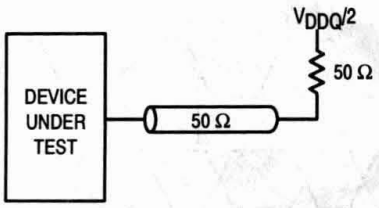
Input Pulse Levels ..... 0 to 2.5 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.25 V
Output Timing Reference Level ..... 1.25 V
Clock Input Timing Reference Level ..... Differential Cross–Point
Clock Input Pulse Level ..... 1.8 V to 2.1 V

3

READ/WRITE CYCLE TIMING (See Note 3)

Parameter	Symbol	MCM69L536–7.5 MCM69L618–7.5		MCM69L536–8.5 MCM69L618–8.5		MCM69L536–9.5 MCM69L618–9.5		MCM69L536–10.5 MCM69L618–10.5		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	7	—	8	—	9	—	10	—	ns	
Clock High Pulse Width	t_{KHKL}	2.8	—	3.2	—	3.6	—	4	—	ns	
Clock Low Pulse Width	t_{KLKH}	2.8	—	3.2	—	3.6	—	4	—	ns	
Clock High to Output Valid	t_{KHQV}	—	7.5	—	8.5	—	9.5	—	10.5	ns	1
Clock Low to Output Valid	t_{KLQV}	—	3.5	—	4	—	4	—	4	ns	2
Clock Low to Output Hold	t_{KLQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	2
Clock Low to Output Low–Z	t_{KLQX1}	1	—	1	—	1	—	1	—	ns	2
Clock High to Output High–Z	t_{KHQZ}	—	3.5	—	4	—	4	—	4	ns	2
Output Enable Low to Output Low–Z	t_{GLQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	2
Output Enable Low to Output Valid	t_{GLQV}	—	3.5	—	4	—	4	—	4	ns	2
Output Enable to Output Hold	t_{GHQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	2
Output Enable High to Output High–Z	t_{GHQZ}	—	3.5	—	4	—	4	—	4	ns	2
Setup Times: Address Data In Chip Select Write Enable	t_{AVKH} t_{DVKH} t_{SVKH} t_{WVKH}	0.5	—	0.5	—	0.5	—	0.5	—	ns	
Hold Times: Address Data In Chip Select Write Enable	t_{KHAX} t_{KHDX} t_{KHSX} t_{KHWX}	1	—	1	—	1	—	1	—	ns	

NOTES:
1. Tested per AC Test Load diagram. See Figure 1.
2. Measured at ± 200 mV from steady state.
3. In no case may control input signals (e.g., $\overline{SS}$) be operated with pulse widths less than the minimum clock input pulse width specifications (e.g., t_{KHKL}) or at frequencies that exceed the applied K clock frequency.



TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Figure 1. Test Loads

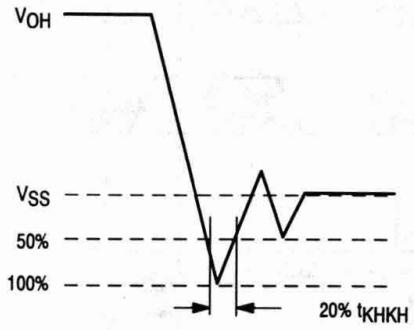
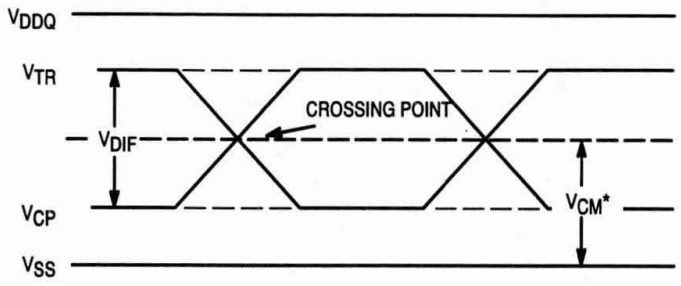


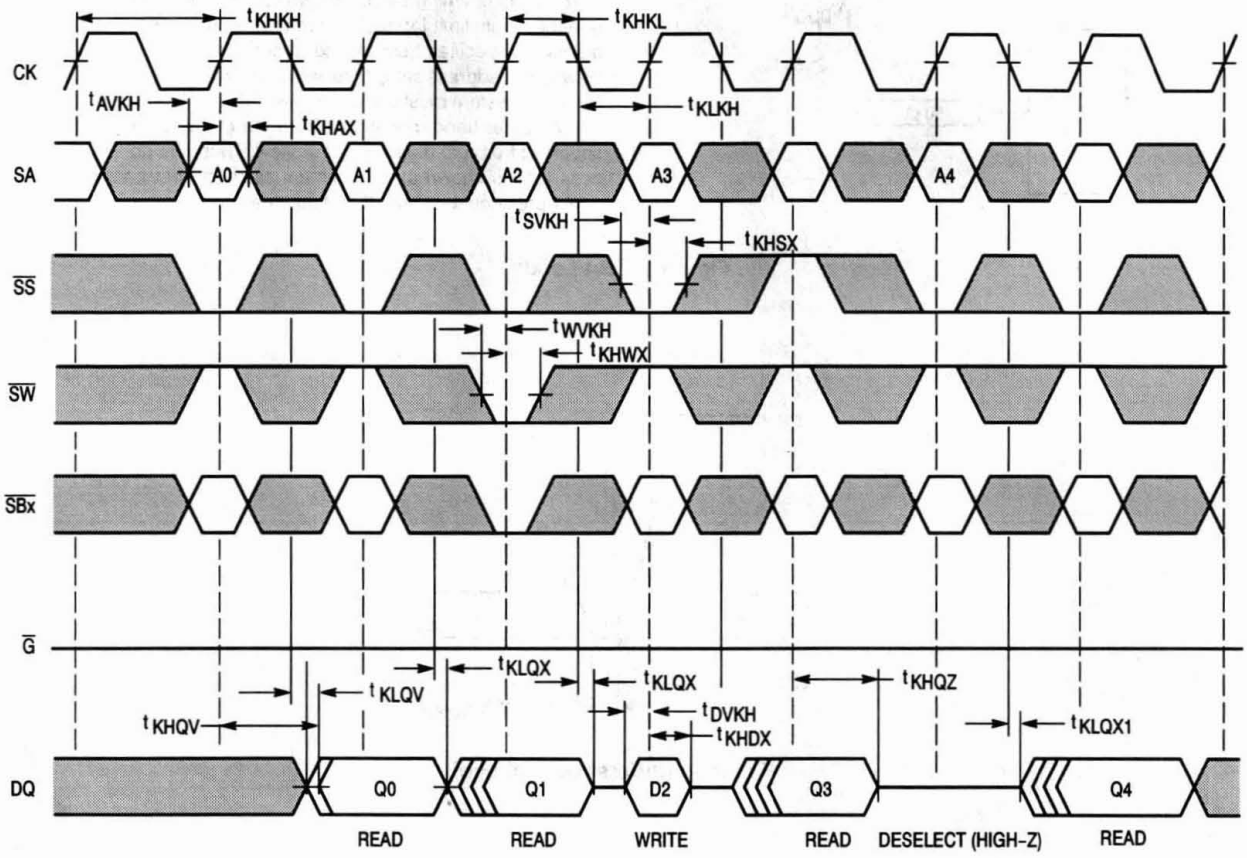
Figure 2. Undershoot Voltage



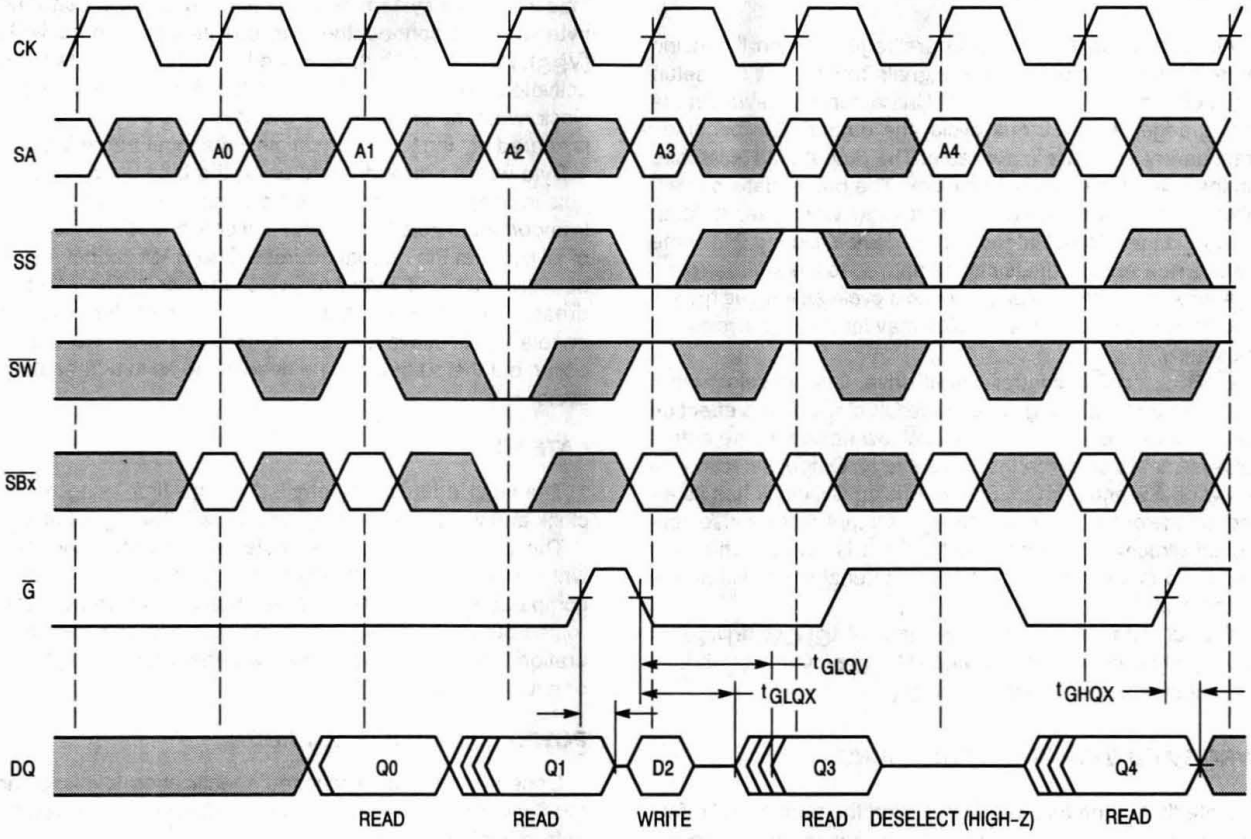
*V_{CM}, the Common Mode Input Voltage, equals $V_{TR} - ((V_{TR} - V_{CP})/2)$.

Figure 3. Differential Inputs/Common Mode Input Voltage

REGISTER LATCH READ–WRITE–READ CYCLES



REGISTER LATCH READ–WRITE–READ CYCLES
($\overline{G}$ Controlled)



FUNCTIONAL OPERATION

READ AND WRITE OPERATIONS

All control signals except $\overline{G}$ are registered on the rising edge of the CK clock. These signals must meet the setup and hold times shown in the AC Characteristics table.On the falling edge of the current cycle, the output latch becomes transparent and data is available. The output data is latched on the rising edge of the next clock. The output data is available at the output at t_{KLQV} or t_{KHQV} whichever is later. t_{KHQV} is the internal latency of the device. During this same cycle a new read address can be applied to the address pins.

A write cycle can occur on the next cycle as long as t_{KLQX} and t_{DVKH} are met. Read cycles may follow write cycles immediately.

$\overline{G}$, $\overline{SS}$, and $\overline{SW}$ control output drive. Chip deselect via a high on $\overline{SS}$ at the rising edge of the CK clock has its effect on the output drivers immediately. $\overline{SW}$ low deselects the output drivers immediately (on the same cycle). Output selecting via a low on $\overline{SS}$ and high on $\overline{SW}$ at a rising CK clock has its effect on the output drivers at t_{KLQX}. Output drive is also controlled directly by output enable, $\overline{G}$. $\overline{G}$ is an asynchronous input. No clock edges are required to enable or disable the output with $\overline{G}$.

Output data will be valid the latter of t_{GLQV}, t_{KHQV}, or t_{KLQV}. Outputs will begin driving at t_{KLQX1}. Outputs will hold previous data until t_{KLQX} or t_{GHQX}.

WRITE AND BYTE WRITE FUNCTIONS

Note that in the following discussion the term "byte" refers to nine bits of the RAM I/O bus. In all cases, the timing parameters described for synchronous write input ($\overline{SW}$) apply to each of the byte write enable inputs ($\overline{SBa}$, $\overline{SBb}$, etc.).

Byte write enable inputs have no effect on read cycles. This allows the system designer not interested in performing byte writes to connect the byte enable inputs to active low (V_{SS}). Reads of all bytes proceed normally and write cycles, activated via a low on $\overline{SW}$, and the rising edge of the CK clock, write the entire RAM I/O width. This way the designer is spared having to drive multiple write input buffer loads.

Byte writes are performed using the byte write enable inputs in conjunction with the synchronous write input ($\overline{SW}$). It is important to note that writing any one byte will inhibit a read of all bytes at the current address. The RAM cannot simultaneously read one byte and write another at the same address. A write cycle initiated with none of the byte write enable inputs active is neither a read or a write. No write will occur, but the outputs will be deselected as in a normal write cycle.

LATE WRITE

The write address is sampled on the first rising edge of clock and write data is sampled on the following rising edge.

The late write feature is implemented with single stage write buffering. Write buffering is transparent to the user. A comparator monitors the address bus and, when necessary, routes buffer contents to the outputs to assure coherent operation. This occurs in all cases whether there is a byte write or a full word is written.

POWER UP AND INITIALIZATION

Once supplies have reached specification levels, a minimum dwell of 1.0 ms with CK clock inputs cycling is required before beginning normal operations.

SERIAL BOUNDARY SCAN TEST ACCESS PORT OPERATION

OVERVIEW

The serial boundary scan test access port (TAP) on this RAM is designed to operate in a manner consistent with IEEE Standard 1149.1–1990 (commonly referred to as JTAG), but does not implement all of the functions required for 1149.1 compliance. Certain functions have been modified or eliminated because their implementation places extra delays in the RAMs critical speed path. Nevertheless, the RAM supports the standard TAP controller architecture. (The TAP controller is the state machine that controls the TAPs operation) and can be expected to function in a manner that does not conflict with the operation of devices with Standard 1149.1 compliant TAPs. The TAP operates using conventional JEDEC Standard 8–1B Low Voltage (3.3 V) TTL / CMOS logic level signaling.

DISABLING THE TEST ACCESS PORT

It is possible to use this device without utilizing the TAP. To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid level inputs. TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a 1 k resistor. TDO should be left unconnected.

TAP DC OPERATING CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Parameter	Symbol	Min	Max	Unit	Note
Logic Input Logic High	$V_{IH}1$	2.0	V_{DD} + 0.3	V	
Logic Input Logic Low	$V_{IL}1$	– 0.3	0.8	V	
Logic Input Leakage Current	I_{lkg}	—	± 5	µA	1
Output Logic Low	$V_{OL}1$	—	0.2	V	2
Output Logic High	$V_{OH}1$	V_{DD} – 0.2	—	V	3
Output Logic Low	$V_{OL}2$	—	0.4	V	4
Output Logic High	$V_{OH}2$	2.4	—	V	5

NOTES:

1. 0 V ≤ V_{in} ≤ V_{DD} for all logic input pins.
2. $I_{OL}1$ ≤ 100 µA @ V_{OL} = 0.2 V. Sampled, not 100% tested.
3. $I_{OH}1I$ ≤ 100 µA @ V_{DDQ} – 0.2 V. Sampled, not 100% tested.
4. $I_{OL}2$ ≤ 8 mA @ V_{OL} = 0.4 V.
5. $I_{OH}2I$ ≤ 8 mA @ V_{OH} = 2.4 V.

TAP AC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V

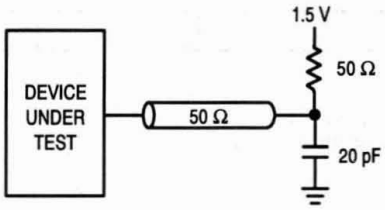
Output Test Load ..... 50 Ω Parallel Terminated T–line with 20 pF Receiver Input Capacitance
Test Load Termination Supply Voltage (V_T) ..... 1.5 V

TAP CONTROLLER TIMING

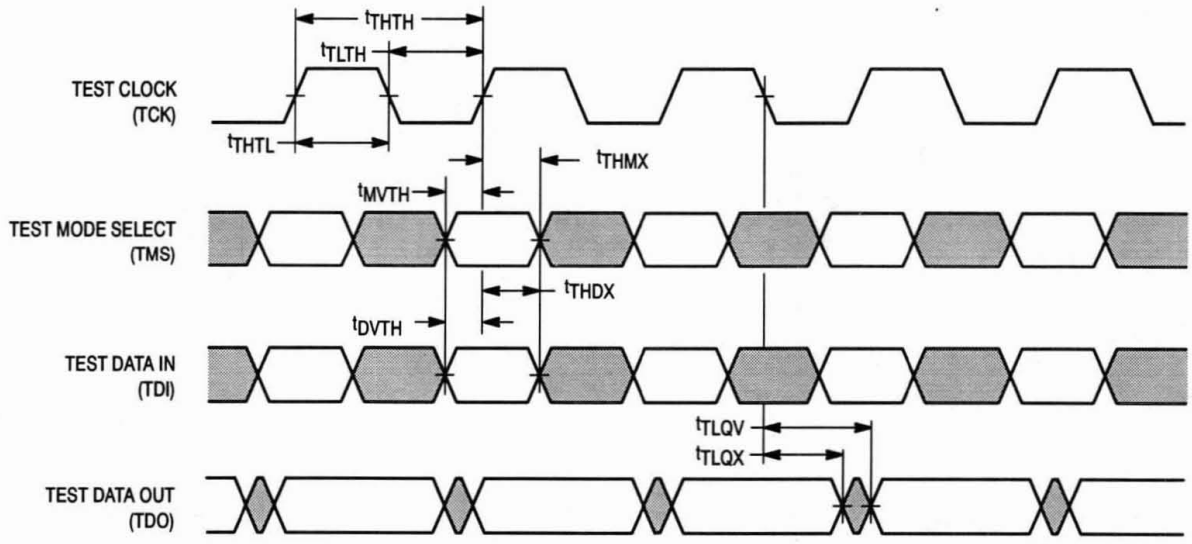
Parameter	Symbol	Min	Max	Unit	Notes
Cycle Time	t_{THTH}	100	—	ns	
Clock High Time	t_{THTL}	40	—	ns	
Clock Low Time	t_{TLTH}	40	—	ns	
TMS Setup	t_{MVTH}	10	—	ns	
TMS Hold	t_{THMX}	10	—	ns	
TDI Valid to TCK High	t_{DVTH}	10	—	ns	
TCK High to TDI Don't Care	t_{THDX}	10	—	ns	
Capture Setup	t_{CS}	10	—	ns	1
Capture Hold	t_{CH}	10	—	ns	1
TCK Low to TDO Unknown	t_{TLQX}	0	—	ns	
TCK Low to TDO Valid	t_{TLOV}	—	20	ns	

NOTES:
1. t_{CS} + t_{CH} defines the minimum pause in RAM I/O pad transitions to assure accurate pad data capture.

AC TEST LOAD



TAP CONTROLLER TIMING DIAGRAM



TEST ACCESS PORT PINS

TCK – TEST CLOCK (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

TMS – TEST MODE SELECT (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.

TDI – TEST DATA IN (INPUT)

The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (refer to Figure 5 TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.

TDO – TEST DATA OUT (OUTPUT)

Output that is active depending on the state of the TAP state machine (refer to Figure 5 TAP Controller State Diagram). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

TRST – TAP RESET

This device does not have a TRST pin. TRST is optional in **IEEE 1149.1.** The test–logic reset state is entered while TMS is held high for five rising edges of TCK. Power on reset circuitry is included internally. This type of reset does not affect the operation of the system logic. The reset affects test logic only.

TEST ACCESS PORT REGISTERS

OVERVIEW

The various TAP registers are selected (one at a time) via the sequences of ones and zeros input to the TMS pin as the TCK is strobed. Each of the TAPs registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on subsequent falling edge of TCK. When a register is selected it is "placed" between the TDI and TDO pins.

INSTRUCTION REGISTER

The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run test/idle or the various data register states. The instructions are three bits long. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power–up or whenever the controller is placed in test–logic–reset state.

BYPASS REGISTER

The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.

BOUNDARY SCAN REGISTER

The boundary scan register is identical in length to the number of active input and I/O connections on the RAM (not counting the TAP pins). This also includes a number of place holder locations (always set to a logic 1) reserved for density upgrade address pins. There are a total of 70 bits in the case of the x36 device and 51 bits in the case of the x18 device. The boundary scan register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture–DR state and then is placed between the TDI and TDO pins when the controller is moved to shift–DR state. Several TAP instructions can be used to activate the boundary scan register.

The Bump/Bit Scan Order tables describe which device bump connects to each boundary scan register location. The first column defines the bit's position in the boundary scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the input or I/O at the bump and the third column is the bump number.

IDENTIFICATION (ID) REGISTER

The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture–DR state with the IDCODE command loaded in the instruction register. The code is loaded from a 32 bit on–chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into shift–DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Presence Indicator

Bit #	0
Value	1

Motorola JEDEC ID Code (Compressed Format, per IEEE Standard 1149.1 – 1990

Bit #	11	10	9	8	7	6	5	4	3	2	1
Value	0	0	0	0	0	0	0	1	1	1	0

Reserved For Future Use

Bit #	17	16	15	14	13	12
Value	x	x	x	x	x	x

Device Width

Configuration	Bit #	22	21	20	19	18
32Kx36	Value	0	0	1	0	0
64Kx18	Value	0	0	0	1	1

Device Depth

Configuration	Bit #	27	26	25	24	23
32Kx36	Value	0	0	0	1	1
64Kx18	Value	0	0	1	0	0

Revision Number

Bit #	31	30	29	28
Value	x	x	x	x

Figure 4. ID Register Bit Meanings

MCM69L538 Bump/Bit Scan Order

BIT #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	NC	3B
2	SA	4P		37	NC	2B
3	SA	4T		38	SA	3A
4	SA	6R		39	SA	3C
5	SA	5T		40	SA	2C
6	ZZ	7T		41	SA	2A
7	DQa	6P		42	DQc	2D
8	DQa	7P		43	DQc	1D
9	DQa	6N		44	DQc	2E
10	DQa	7N		45	DQc	1E
11	DQa	6M		46	DQc	2F
12	DQa	6L		47	DQc	2G
13	DQa	7L		48	DQc	1G
14	DQa	6K		49	DQc	2H
15	DQa	7K		50	DQc	1H
16	$\overline{SBa}$	5L		51	$\overline{SBc}$	3G
17	$\overline{CK}$	4L		52	ZQ	4D
18	CK	4K		53	$\overline{SS}$	4E
19	$\overline{G}$	4F		54	NF	4G
20	$\overline{SBb}$	5G		55	NF	4H
21	DQb	7H		56	$\overline{SW}$	4M
22	DQb	6H		57	$\overline{SBd}$	3L
23	DQb	7G		58	DQd	1K
24	DQb	6G		59	DQd	2K
25	DQb	6F		60	DQd	1L
26	DQb	7E		61	DQd	2L
27	DQb	6E		62	DQd	2M
28	DQb	7D		63	DQd	1N
29	DQb	6D		64	DQd	2N
30	SA	6A		65	DQd	1P
31	SA	6C		66	DQd	2P
32	SA	5C		67	SA	3T
33	SA	5A		68	SA	2R
34	NC	6B		69	SA	4N
35	NC	5B		70	M1	3R

MCM69L620 Bump/Bit Scan Order

Bit #	Signal Name	Bump ID		Bit #	Signal Name	Bump ID
1	M2	5R		36	$\overline{SBb}$	3G
2	SA	6T		37	ZQ	4D
3	SA	4P		38	$\overline{SS}$	4E
4	SA	6R		39	NF	4G
5	SA	5T		40	NF	4H
6	ZZ	7T		41	$\overline{SW}$	4M
7	DQa	7P		42	DQb	2K
8	DQa	6N		43	DQb	1L
9	DQa	6L		44	DQb	2M
10	DQa	7K		45	DQb	1N
11	$\overline{SBa}$	5L		46	DQb	2P
12	$\overline{CK}$	4L		47	SA	3T
13	CK	4K		48	SA	2R
14	$\overline{G}$	4F		49	SA	4N
15	DQa	6H		50	SA	2T
16	DQa	7G		51	M1	3R
17	DQa	6F				
18	DQa	7E				
19	DQa	6D				
20	SA	6A				
21	SA	6C				
22	SA	5C				
23	SA	5A				
24	NC	6B				
25	NC	5B				
26	NC	3B				
27	NC	2B				
28	SA	3A				
29	SA	3C				
30	SA	2C				
31	SA	2A				
32	DQb	1D				
33	DQb	2E				
34	DQb	2G				
35	DQb	1H				

NOTES:

1. The NC pads listed in this table are indeed no connects, but are represented in the boundary scan register by a "place holder" bit that is forced to logic 1. These pads are reserved for use as address inputs on higher density RAMs that follow this pad out and scan order standard.
2. CK, $\overline{CK}$, are sampled individually. $\overline{CK}$ is not simply a forced complement of the CK input. In scan mode these differential inputs are referenced to each other.
3. M1 and M2 are not ordinary inputs and may not respond to standard I/O logic levels. M1 and M2 must be driven to within 100 mV of a V_{DD} or V_{SS} supply rail to ensure consistent results.
4. ZZ must remain at V_{IL} during boundary scan to ensure consistent results.

TAP Controller Instruction Set

OVERVIEW

There are two classes of instructions defined in the Standard 1149.1–1990; the standard (public) instructions, and device specific (private) instructions. Some public instructions, are mandatory for 1149.1 compliance. Optional public instructions must be implemented in prescribed ways.

Although the TAP controller in this device follows the 1149.1 conventions, it is not 1194.1 compliant because some of the mandatory instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads, but cannot be used to load address, data or control signals into the RAM or to preload the I/O buffers. In other words, the device will not perform Standard 1149.1 EXTEST, INTEST or the preload portion of the SAMPLE / PRELOAD command.

When the TAP controller is placed in capture–IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the shift–IR state the instruction register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to update–IR state. The TAP instruction sets for this device are listed in the following tables.

STANDARD (PUBLIC) INSTRUCTIONS

BYPASS

The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift–DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

Sample/preload is a Standard 1149.1 mandatory public instruction. When the sample / preload instruction is loaded in the Instruction register, moving the TAP controller into the capture–DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set–up plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register.

Moving the controller to shift–DR state then places the boundary scan register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the update–DR state with the SAMPLE / PRELOAD instruction loaded in the instruction register has the same effect as the pause–DR command. This functionality is not Standard 1149.1 compliant.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic 0s. EXTEST is not implemented in this device. Therefore this device is not 1149.1 compliant. Nevertheless, this RAMs TAP does respond to an all zeros instruction, as follows. With the EXTEST (000) instruction loaded in the instruction register the RAM responds just as it does in response to the SAMPLE / PRELOAD instruction described above, except the RAM outputs are forced to high–Z any time the instruction is loaded.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture–DR mode and places the ID register between the TDI and TDO pins in shift–DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test–logic–reset state.

THE DEVICE SPECIFIC (PUBLIC) INSTRUCTION

SAMPLE–Z

If the SAMPLE–Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high–Z) and the boundary scan register is connected between TDI and TDO when the TAP controller is moved to the shift–DR state.

THE DEVICE SPECIFIC (PRIVATE) INSTRUCTION

NOOP

Do not use these instructions; they are reserved for future use.

STANDARD (PUBLIC) INSTRUCTION CODES

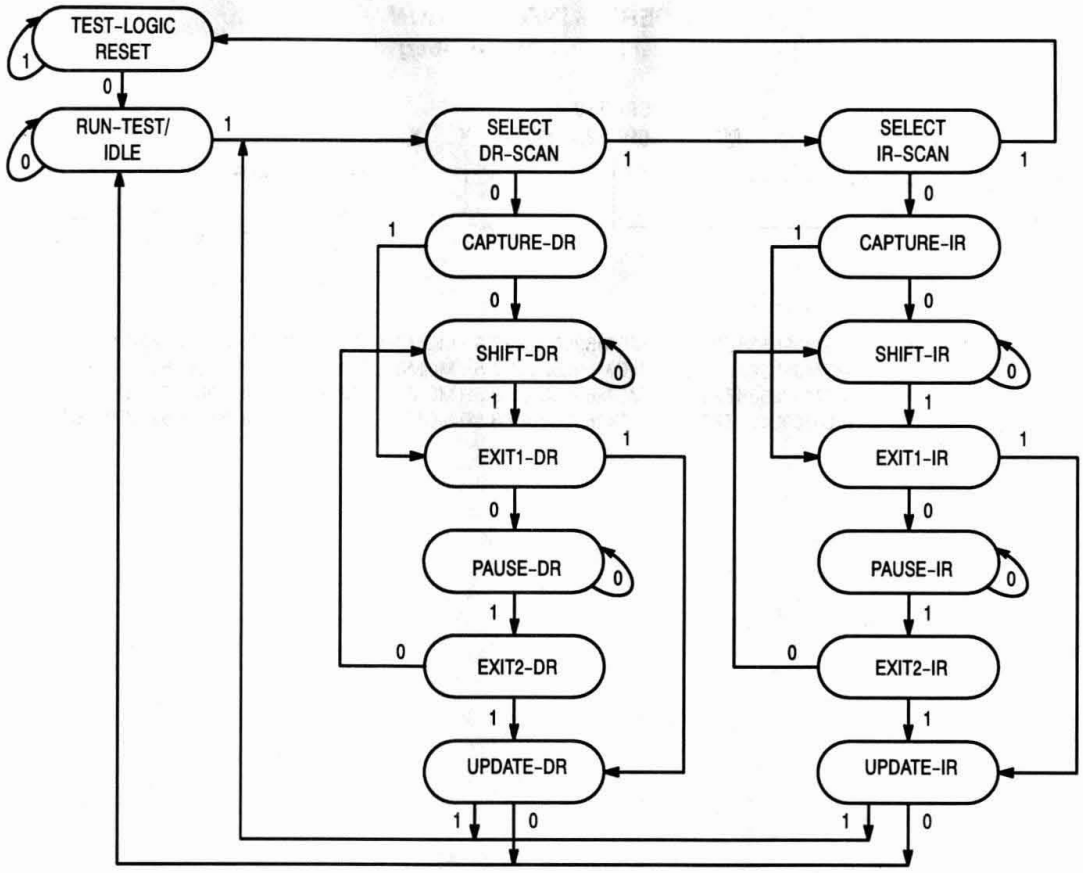
Instruction	Code*	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM outputs to High–Z state. *NOT 1149.1 COMPLIANT*
IDCODE	001**	Preloads ID register and places it between TDI and TDO. Does not affect RAM operation.
SAMPLE / PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect RAM operation. Does not implement 1149.1 Preload function. * NOT 1149.1 COMPLIANT *
BYPASS	111	Places bypass register between TDI and TDO. Does not affect RAM operation.
SAMPLE–Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM output drivers to High–Z.

* Instruction codes expressed in binary, MSB on left, LSB on right.
** Default instruction automatically loaded at power–up and in test–logic–reset state.

STANDARD (PRIVATE) INSTRUCTION CODES

Instruction	Code*	Description
NO OP	011	Do not use these instructions; they are reserved for future use.
NO OP	101	Do not use these instructions; they are reserved for future use.
NO OP	110	Do not use these instructions; they are reserved for future use.

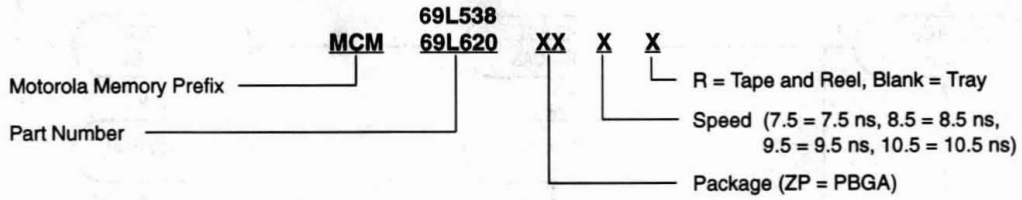
* Instruction codes expressed in binary, MSB on left, LSB on right.



NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 5. TAP Controller State Diagram

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM69L538ZP7.5 MCM69L538ZP8.5 MCM69L538ZP9.5 MCM69L538ZP10.5
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MCM69L620ZP7.5R MCM69L620ZP8.5R MCM69L620ZP9.5R MCM69L620ZP10.5R

3

BurstRAMs

256K X 18

3.3 V MCM69F819 4–3
3.3 V MCM69P819 4–19

128K X 36

3.3 V MCM69F737 4–35
3.3 V MCM69P737 4–51

64K X 32

3.3 V MCM63P631 4–67

64K X 18

3.3 V MCM69F618A 4–80
3.3 V MCM69F618C 4–91
3.3 V ..... MCM69P618A ... 4–102
3.3 V MCM69P618C 4–113
5 V ..... MCM67B618A ... 4–124
5 V ..... MCM67C618A ... 4–133

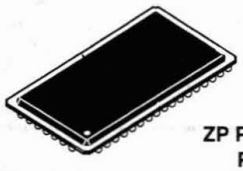
32K X 36

3.3 V ..... MCM69F536A ... 4–142
3.3 V ..... MCM69F536B ... 4–153
3.3 V ..... MCM69F536C ... 4–164
3.3 V ..... MCM69P536A ... 4–175
3.3 V ..... MCM69P536B ... 4–186
3.3 V ..... MCM69P536C ... 4–197

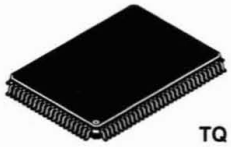
MCM69F819

Product Preview

256K x 18 Bit Flow–Through BurstRAM™ Synchronous Fast Static RAM



ZP PACKAGE
PBGA
CASE 999–01



TQ PACKAGE
TQFP
CASE 983A–01

The MCM69F819 is a 4M bit synchronous fast static RAM designed to provide a burstable, high performance, secondary cache for the PowerPC™ and other high performance microprocessors. It is organized as 256K words of 18 bits each. This device integrates input registers, a 2–bit address counter, and high speed SRAM onto a single monolithic circuit for reduced parts count in cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K).

Addresses (SA), data inputs (DQx), and all control signals except output enable ($\overline{G}$) and linear burst order ($\overline{LBO}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ input pins. Subsequent burst addresses can be generated internally by the MCM69F819 (burst sequence operates in linear or interleaved mode dependent upon the state of $\overline{LBO}$) and controlled by the burst address advance ($\overline{ADV}$) input pin.

Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased timing flexibility for incoming signals.

Synchronous byte write ($\overline{SBx}$), synchronous global write ($\overline{SGW}$), and synchronous write enable ($\overline{SW}$) are provided to allow writes to either individual bytes or to all bytes. The two bytes are designated as "a" and "b". $\overline{SBa}$ controls DQa and $\overline{SBb}$ controls DQb. Individual bytes are written if the selected byte writes $\overline{SBx}$ are asserted with $\overline{SW}$. All bytes are written if either $\overline{SGW}$ is asserted or if all $\overline{SBx}$ and $\overline{SW}$ are asserted.

For read cycles, a flow–through SRAM allows output data to simply flow freely from the memory array.

The MCM69F819 operates from a 3.3 V core power supply and all outputs operate on a 2.5 V power supply. All inputs and outputs are JEDEC standard JESD8–5 compatible.

- MCM69F819 Speed Options

Speed	t_{KHKH}	Flow–Through t_{KHQV}	Setup	Hold	I_{DD}
117 MHz	8.5 ns	7.5 ns	2 ns	0.5 ns	350 mA
100 MHz	10 ns	8 ns	2 ns	0.5 ns	325 mA
90 MHz	11 ns	8.5 ns	2 ns	0.5 ns	300 mA

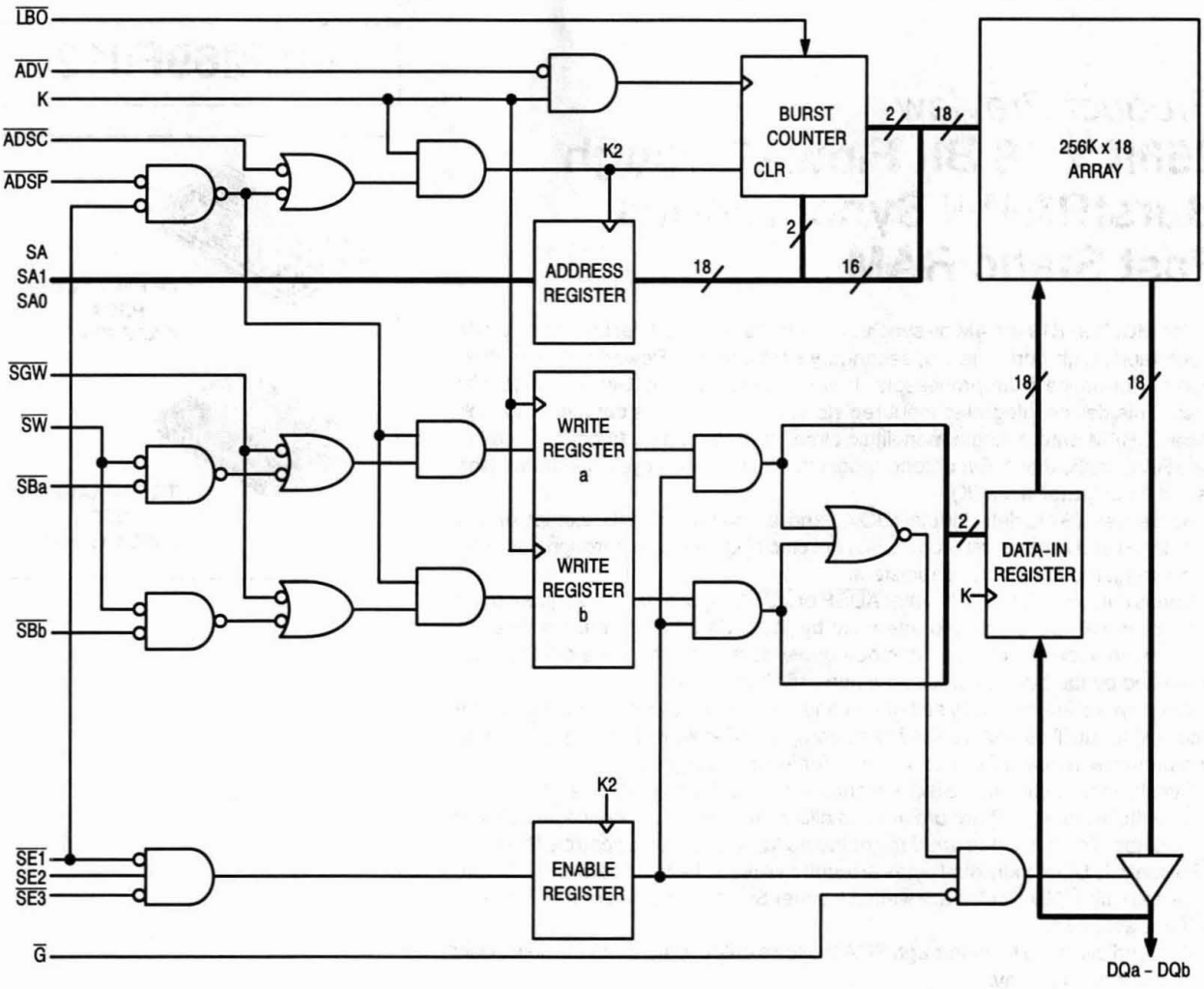
- 3.3 V + 10%, – 5% Core Power Supply, 2.5 V I/O Supply
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Selectable Burst Sequencing Order (Linear/Interleaved)
- Single–Cycle Deselect Timing
- Internally Self–Timed Write Cycle
- Byte Write and Global Write Control
- JEDEC Standard 119 Pin PBGA and 100 Pin TQFP Packages

BurstRAM is a trademark of Motorola, Inc.
The PowerPC name is a trademark of IBM Corp., used under license therefrom.

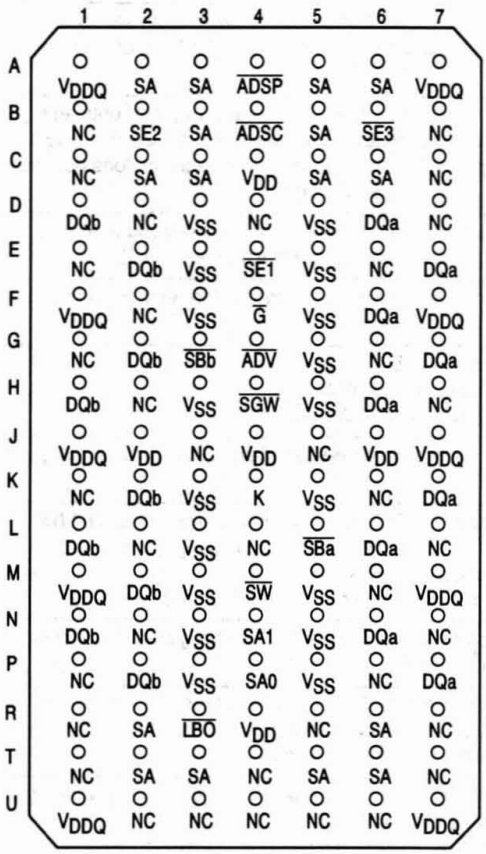
This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

REV 2
4/9/97

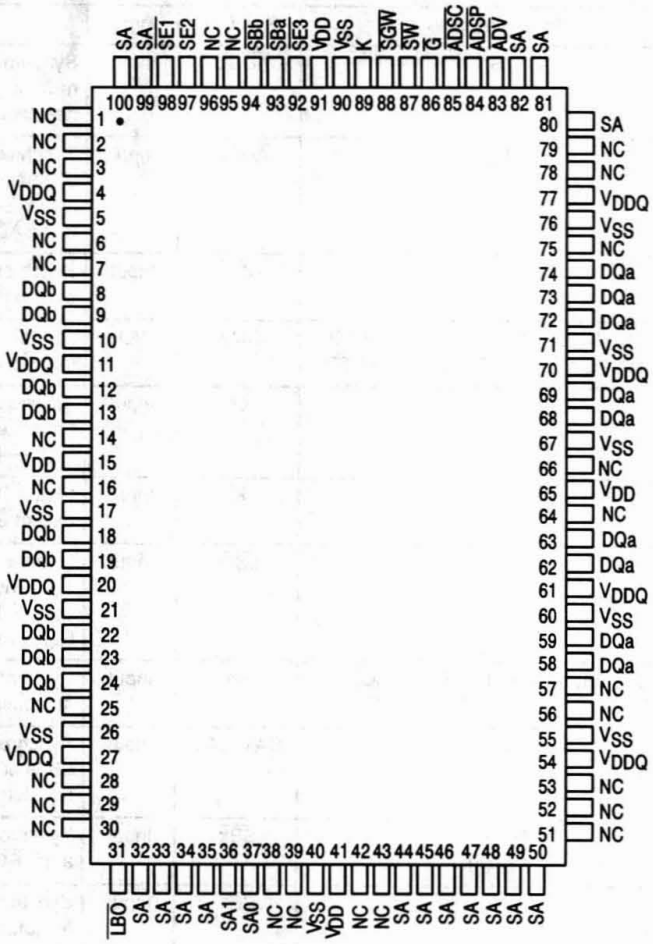
FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENTS


1 2 3 4 5 6 7
A VDDQ SA SA ADSP SA SA VDDQ
B NC SE2 SA ADSC SA SE3 NC
C NC SA SA VDD SA SA NC
D DQb NC VSS NC VSS DQa NC
E NC DQb VSS SE1 VSS NC DQa
F VDDQ NC VSS G VSS DQa VDDQ
G NC DQb SBb ADV VSS NC DQa
H DQb NC VSS SGW VSS DQa NC
J VDDQ VDD NC VDD NC VDD VDDQ
K NC DQb VSS K VSS NC DQa
L DQb NC VSS NC SBa DQa NC
M VDDQ DQb VSS SW VSS NC VDDQ
N DQb NC VSS SA1 VSS DQa NC
P NC DQb VSS SA0 VSS NC DQa
R NC SA LBO VDD NC SA NC
T NC SA SA NC SA SA NC
U VDDQ NC NC NC NC NC VDDQ

TOP VIEW 119 BUMP PBGA



TOP VIEW 100 PIN TQFP

Not to Scale

PBGA PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
4B	$\overline{ADSC}$	Input	Synchronous Address Status Controller: Active low, is used to latch a new external address. Used to initiate a READ, WRITE, or chip deselect.
4A	$\overline{ADSP}$	Input	Synchronous Address Status Processor: Active low, interrupts any ongoing burst and latches a new external address. Used to initiate a new READ or chip deselect (exception — chip deselect does not occur when $\overline{ADSP}$ is asserted and $\overline{SE1}$ is high).
4G	$\overline{ADV}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
(a) 6D, 7E, 6F, 7G, 6H, 7K, 6L, 6N, 7P (b) 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 2P	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b).
4F	$\overline{G}$	Input	Asynchronous Output Enable Input: Low — enables output buffers (DQx pins). High — DQx pins are high impedance.
4K	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$ and $\overline{LBO}$.
3R	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst counter (68K/PowerPC). High — interleaved burst counter (486/i960/Pentium).
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 2R, 6R, 2T, 3T, 5T, 6T	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
4N, 4P	SA1, SA0	Input	Synchronous Address Inputs: These pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
5L, 3G (a) (b)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: "x" refers to the byte being written (byte a, b). $\overline{SGW}$ overrides $\overline{SBx}$.
4E	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high — blocks $\overline{ADSP}$ or deselects chip when $\overline{ADSC}$ is asserted.
2B	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
6B	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
4H	$\overline{SGW}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the $\overline{SBx}$ and $\overline{SW}$ signals. If only byte write signals $\overline{SBx}$ are being used, tie this pin high.
4M	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{SBx}$ pins. If only byte write signals $\overline{SBx}$ are being used, tie this pin low.
4C, 2J, 4J, 6J, 4R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	I/O Power Supply.
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P	V_{SS}	Supply	Ground.
1B, 7B, 1C, 7C, 2D, 4D, 7D, 1E, 6E, 2F, 1G, 6G, 2H, 7H, 3J, 5J, 1K, 6K, 2L, 4L, 7L, 6M, 2N, 7N, 1P, 6P, 1R, 5R, 7R, 1T, 4T, 7T, 2U, 3U, 4U, 5U, 6U	NC	—	No Connection: There is no connection to the chip.

TQFP PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: Active low, is used to latch a new external address. Used to initiate a READ, WRITE, or chip deselect.
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: Active low, interrupts any ongoing burst and latches a new external address. Used to initiate a new READ or chip deselect (exception — chip deselect does not occur when $\overline{ADSP}$ is asserted and $\overline{SE1}$ is high).
83	$\overline{ADV}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
(a) 58, 59, 62, 63, 68, 69, 72, 73, 74 (b) 8, 9, 12, 13, 18, 19, 22, 23, 24	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b).
86	$\overline{G}$	Input	Asynchronous Output Enable Input: Low — enables output buffers (DQx pins). High — DQx pins are high impedance.
89	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$ and $\overline{LBO}$.
31	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst counter (68K/PowerPC). High — interleaved burst counter (486/i960/Pentium).
32, 33, 34, 35, 44, 45, 46, 47, 48, 49, 50, 80, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
36, 37	SA1, SA0	Input	Synchronous Address Inputs: These pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
93, 94 (a) (b)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: "x" refers to the byte being written (byte a, b). $\overline{SGW}$ overrides $\overline{SBx}$.
88	$\overline{SGW}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the $\overline{SBx}$ and $\overline{SW}$ signals. If only byte write signals $\overline{SBx}$ are being used, tie this pin high.
98	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high — blocks $\overline{ADSP}$ or deselects chip when $\overline{ADSC}$ is asserted.
97	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
92	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
87	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{SBx}$ pins. If only byte write signals $\overline{SBx}$ are being used, tie this pin low.
15, 41, 65, 91	V_{DD}	Supply	Core Power Supply.
4, 11, 20, 27, 54, 61, 70, 77	V_{DDQ}	Supply	I/O Power Supply.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground.
1, 2, 3, 6, 7, 14, 16, 25, 28, 29, 30, 38, 39, 42, 43, 51, 52, 53, 56, 57, 64, 66, 75, 78, 79, 95, 96	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE (See Notes 1 Through 5)

Next Cycle	Address Used	$\overline{SE1}$	SE2	$\overline{SE3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{G}$ [3]	DQx	Write [2, 4]
Deselect	None	1	X	X	X	0	X	X	High–Z	X
Deselect	None	0	X	1	0	X	X	X	High–Z	X
Deselect	None	0	0	X	0	X	X	X	High–Z	X
Deselect	None	X	X	1	1	0	X	X	High–Z	X
Deselect	None	X	0	X	1	0	X	X	High–Z	X
Begin Read	External	0	1	0	0	X	X	0	High–Z	X[5]
Begin Read	External	0	1	0	1	0	X	0	High–Z	READ[5]
Continue Read	Next	X	X	X	1	1	0	1	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	0	DQ	READ
Continue Read	Next	1	X	X	X	1	0	1	High–Z	READ
Continue Read	Next	1	X	X	X	1	0	0	DQ	READ
Suspend Read	Current	X	X	X	1	1	1	1	High–Z	READ
Suspend Read	Current	X	X	X	1	1	1	0	DQ	READ
Suspend Read	Current	1	X	X	X	1	1	1	High–Z	READ
Suspend Read	Current	1	X	X	X	1	1	0	DQ	READ
Begin Write	External	0	1	0	1	0	X	X	High–Z	WRITE
Continue Write	Next	X	X	X	1	1	0	X	High–Z	WRITE
Continue Write	Next	1	X	X	X	1	0	X	High–Z	WRITE
Suspend Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Suspend Write	Current	1	X	X	X	1	1	X	High–Z	WRITE

NOTES:
1. X = Don't Care. 1 = logic high. 0 = logic low.
2. Write is defined as either 1) any $\overline{SBx}$ and $\overline{SW}$ low or 2) $\overline{SGW}$ is low.
3. $\overline{G}$ is an asynchronous signal and is not sampled by the clock K. $\overline{G}$ drives the bus immediately (t_{GLQX}) following $\overline{G}$ going low.
4. On write cycles that follow read cycles, $\overline{G}$ must be negated prior to the start of the write cycle to ensure proper write data setup times. $\overline{G}$ must also remain negated at the completion of the write cycle to ensure proper write data hold times.
5. This read assumes the RAM was previously deselected.

LINEAR BURST ADDRESS TABLE ($\overline{LBO} = V_{SS}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

INTERLEAVED BURST ADDRESS TABLE ($\overline{LBO} = V_{DD}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

WRITE TRUTH TABLE

Cycle Type	$\overline{SGW}$	$\overline{SW}$	$\overline{SBa}$	$\overline{SBb}$
Read	H	H	X	X
Read	H	L	H	H
Write Byte a	H	L	L	H
Write Byte b	H	L	H	L
Write All Bytes	H	L	L	L
Write All Bytes	L	X	X	X

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	V_{SS} – 0.5 to + 4.6	V
I/O Supply Voltage (See Note 2)	V_{DDQ}	V_{SS} – 0.5 to V_{DD}	V
Input Voltage Relative to V_{SS} for Any Pin Except V_{DD} (See Note 2)	V_{in}, V_{out}	V_{SS} – 0.5 to V_{DD} + 0.5	V
Input Voltage (Three–State I/O) (See Note 2)	V_{IT}	V_{SS} – 0.5 to V_{DDQ} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Package Power Dissipation (See Note 3)	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to 85	°C
Storage Temperature	T_{stg}	– 55 to 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. This is a steady–state DC parameter that is in effect after the power supply has achieved its nominal operating level. Power sequencing is not necessary.
3. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

4

PACKAGE THERMAL CHARACTERISTICS — PBGA

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	38 22	°C/W	1, 2
Junction to Board (Bottom)		$R_{\theta JB}$	14	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	5	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

PACKAGE THERMAL CHARACTERISTICS — TQFP (See Note 1)

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	40 25	°C/W	2
Junction to Board (Bottom)		$R_{\theta JB}$	17	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(3.6 V ≥ V_{DD} ≥ 3.1 V, 110°C ≥ T_J ≥ 20°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.1	3.3	3.6	V
Operating Temperature	T_J	20	—	110	°C
Input Low Voltage	V_{IL}	– 0.3	—	0.8	V
Input High Voltage	V_{IH}	1.7	—	V_{DD} + 0.3	V
Input High Voltage I/O Pins	V_{IH2}	1.7	—	V_{DDQ} + 0.3	V
I/O Supply Voltage	V_{DDQ}	2.375	2.5	V_{DD}	V

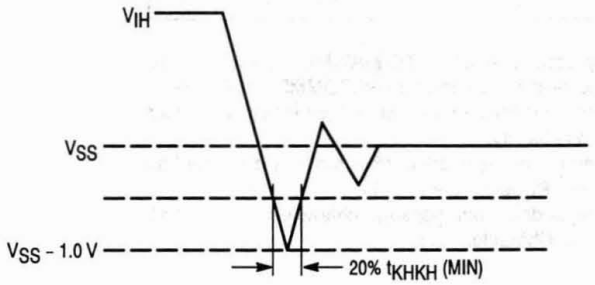


Figure 1. Undershoot Voltage

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input Leakage Current (0 V ≤ V_{in} ≤ V_{DD})	$I_{lkg(I)}$	—	—	± 1	µA	
Output Leakage Current (0 V ≤ V_{in} ≤ V_{DDQ})	$I_{lkg(O)}$	—	—	± 1	µA	
AC Supply Current (Device Selected, All Outputs Open, Cycle Time = t_{KHKH} Min) Includes V_{DD} and V_{DDQ} — MCM69F819–7.5	I_{DDA}	—	—	350	mA	1, 2, 3
MCM69F819–8				325		
MCM69F819–8.5				300		
CMOS Standby Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH})	I_{SB1}	—	—	190	mA	1, 2, 3, 4
Clock Running Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}, All Other Inputs Held to Static CMOS Levels V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{DD} – 0.2 V)	I_{SB2}	—	—	85	mA	4
Output Low Voltage (I_{OL} = 2 mA) (See Figure 4)	V_{OL}	—	—	0.7	V	
Output High Voltage (I_{OL} = –2 mA) (See Figure 4)	V_{OH}	1.7	—	—	V	
Output Low Voltage (I_{OL} = 2 mA) V_{DDQ} = 3.3 V	V_{OL2}	—	—	0.4	V	
Output High Voltage (I_{OH} = –2 mA) V_{DDQ} = 3.3 V	V_{OH2}	2.4	—	—	V	
Desk Top Suspend Current (Selected, All Inputs ≤ 0.2 V, Freq. = Max, V_{DD} = Max, $\overline{ADSP}$ and $\overline{ADSC}$ = Logic High, Outputs Disabled)	I_{DS1}	—	—	TBD	mA	
Desk Top Idle Current (Selected, All Inputs ≤ 0.2 V, Freq. = 0, V_{DD} = Max, $\overline{ADSP}$ and $\overline{ADSC}$ = Logic High, Outputs Disabled)	I_{DS1A}	—	—	TBD	mA	
Desk Top Standby Current (Deselected, All Inputs ≤ 0.2 V, Freq. = 0, V_{DDQ} = Max, Outputs Disabled)	I_{DS2}	—	—	TBD	mA	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing.
2. All addresses transition simultaneously low (LSB) then high (MSB).
3. Data states are all zero.
4. Device is deselected as defined by the Truth Table.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, 110°C ≥ T_J ≥ 20°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	4	5	pF
Input/Output Capacitance	$C_{I/O}$	—	7	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(3.6 V ≥ V_{DD} ≥ 3.1 V, 110°C ≥ T_J ≥ 20°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.25 V
Input Pulse Levels ..... 0 to 2.5 V
Input Slew Rate (See Note 1) ..... 1.0 V/ns

Output Timing Reference Level ..... 1.25 V
Output Load ..... See Figure 2 Unless Otherwise Noted
Output Rise/Fall Times (max) ..... 1.8 ns

READ/WRITE CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM69F819–7.5 117 MHz		MCM69F819–8 100 MHz		MCM69F819–8.5 90 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	8.5	—	10	—	11	—	ns	
Clock High Pulse Width	t_{KHKL}	3	—	4	—	4.5	—	ns	
Clock Low Pulse Width	t_{KLKH}	3	—	4	—	4.5	—	ns	
Clock Access Time	t_{KHQV}	—	7.5	—	8	—	8.5	ns	3
Output Enable to Output Valid	t_{GLQV}	—	3.5	—	3.5	—	3.5	ns	3
Clock High to Output Active	t_{KHQX1}	0	—	0	—	0	—	ns	3, 4, 5, 6
Clock High to Output Change	t_{KHQX2}	2	—	2	—	2	—	ns	3, 5
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	3, 4, 5
Output Disable to Q High–Z	t_{GHQZ}	—	3.5	—	3.5	—	3.5	ns	3, 4, 5
Clock High to Q High–Z	t_{KHQZ}	2	3.5	2	3.5	2	3.5	ns	3, 4, 5, 6
Setup Times: Address	t_{ADKH}	2.0	—	2.0	—	2.0	—	ns	
$\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$	t_{ADSKH}								
Data In	t_{DVKH}								
Write	t_{WVKH}								
Chip Enable	t_{EVKH}								
Hold Times: Address	t_{KHAX}	0.5	—	0.5	—	0.5	—	ns	
$\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$	t_{KHADSX}								
Data In	t_{KHDX}								
Write	t_{KHWX}								
Chip Enable	t_{KHEX}								

NOTES:
1. Write is defined as either any $\overline{SBx}$ and $\overline{SW}$ low or $\overline{SGW}$ is low. Chip Enable is defined as $\overline{SE1}$ low, SE2 high, and $\overline{SE3}$ low whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. Tested per AC Test Load, Figure 2.
4. Measured at ± 200 mV from steady state.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX1} min for a given device and from device to device.

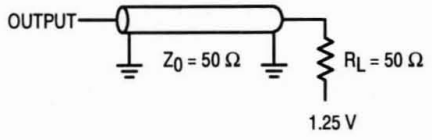
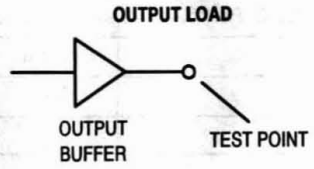
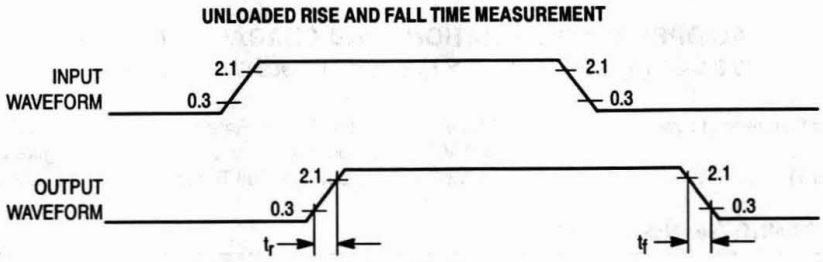


Figure 2. AC Test Load



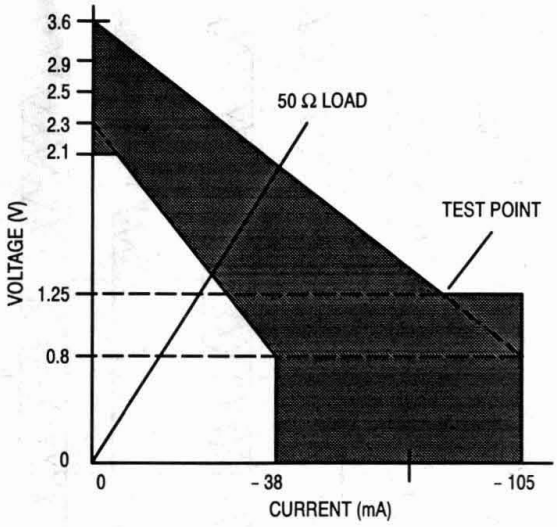


NOTES:
1. Input waveform has a slew rate of 1 V/ns.
2. Rise time is measured from 0.3 to 2.1 V unloaded.
3. Fall time is measured from 2.1 to 0.3 V unloaded.

Figure 3. Unloaded Rise and Fall Time Characterization

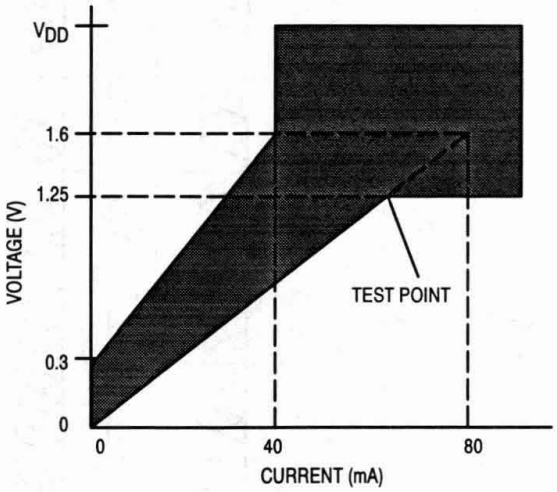
4

PULL-UP		
VOLTAGE (V)	I (mA) MIN	I (mA) MAX
- 0.5	- 38	- 105
0	- 38	- 105
0.8	- 38	- 105
1.25	- 26	- 83
1.5	- 20	- 70
2.3	0	- 30
2.7	0	- 10
2.9	0	0
3.4	0	0
3.6	0	0



(a) Pull–Up

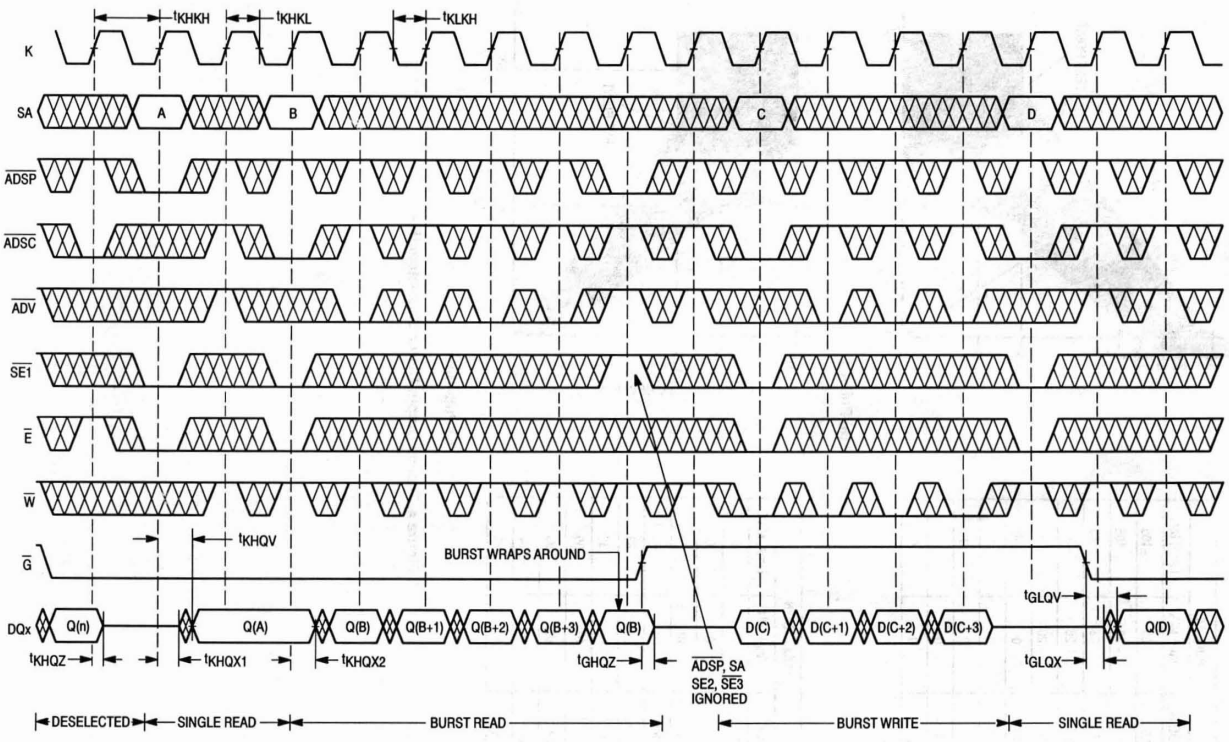
PULL-DOWN		
VOLTAGE (V)	I (mA) MIN	I (mA) MAX
- 0.5	0	0
0	0	0
0.4	10	20
0.8	20	40
1.25	31	63
1.6	40	80
2.8	40	80
3.2	40	80
3.4	40	80
3.6	46	80



(b) Pull–Down

Figure 4. Typical Output Buffer Characteristics

READ/WRITE CYCLES



NOTE: $\overline{E}$ low = SE2 high and $\overline{SE3}$ low.
$\overline{W}$ low = $\overline{SGW}$ low and/or $\overline{SW}$ and $\overline{SBx}$ low.

APPLICATION INFORMATION

STOP CLOCK OPERATION

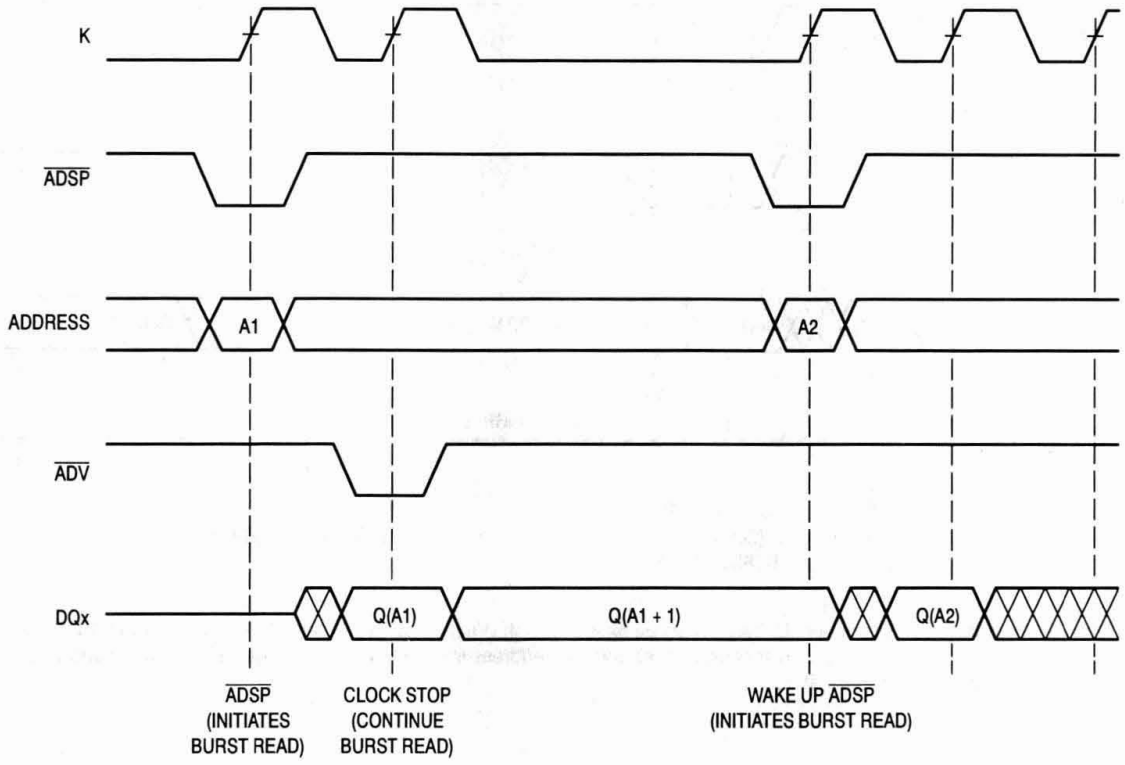
In the stop clock mode of operation, the SRAM will hold all state and data values even though the clock is not running (full static operation). The SRAM design allows the clock to start with $\overline{ADSP}$ and $\overline{ADSC}$, and stops the clock after the last write data is latched, or the last read data is driven out.

When starting and stopping the clock, the AC clock timing and parametrics must be strictly maintained. For example, clock pulse width and edge rates must be guaranteed when starting and stopping the clocks.To achieve the lowest power operation for all three stop clock modes, stop read, stop write, and stop deselect:

To achieve the lowest power operation for all three stop clock modes, stop read, stop write, and stop deselect:

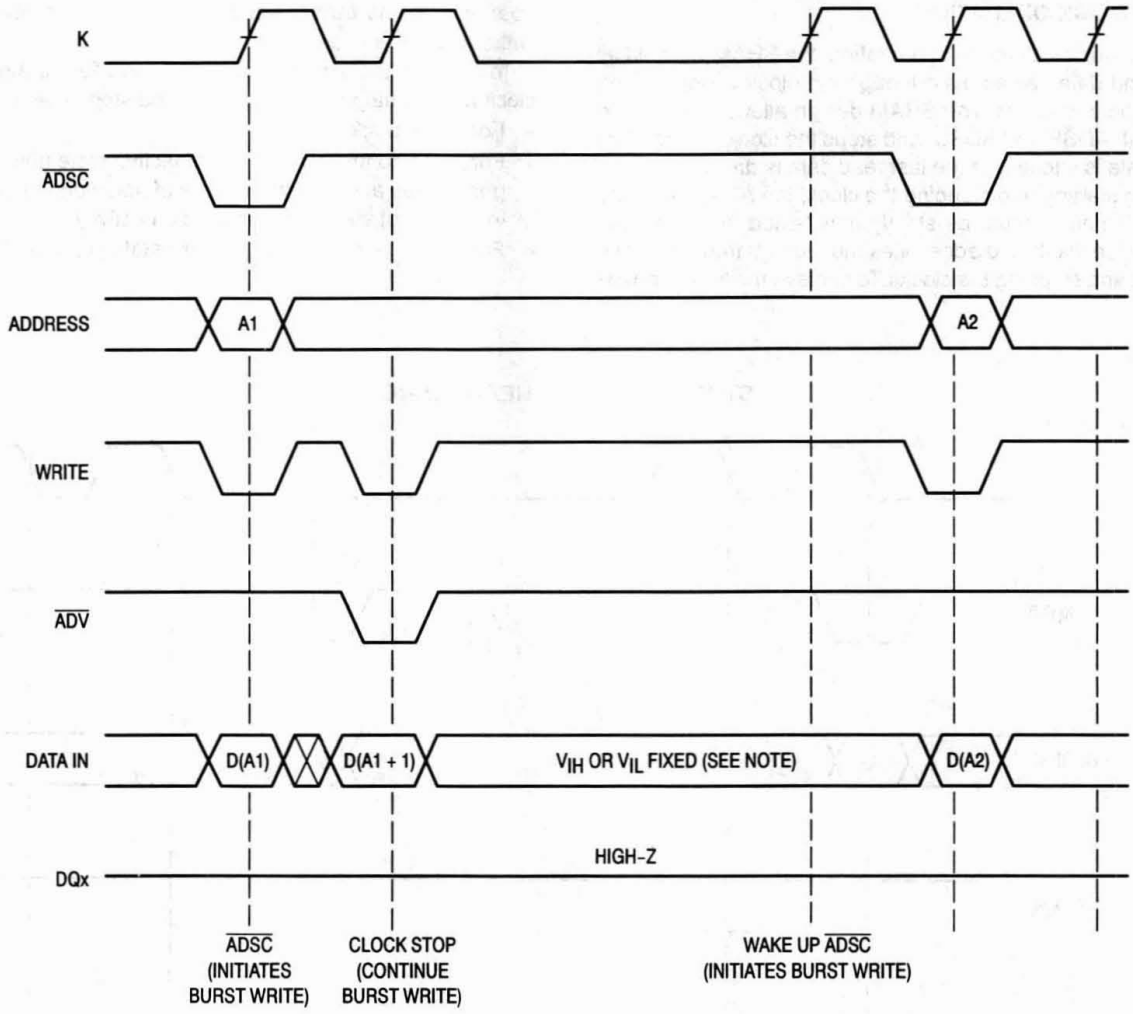
- Force the clock to a low state.
- Force the control signals to an inactive state (this guarantees any potential source of noise on the clock input will not start an unplanned on activity).
- Force the address inputs to a low state (V_{IL}), preferably < 0.2 V.

STOP CLOCK WITH READ TIMING



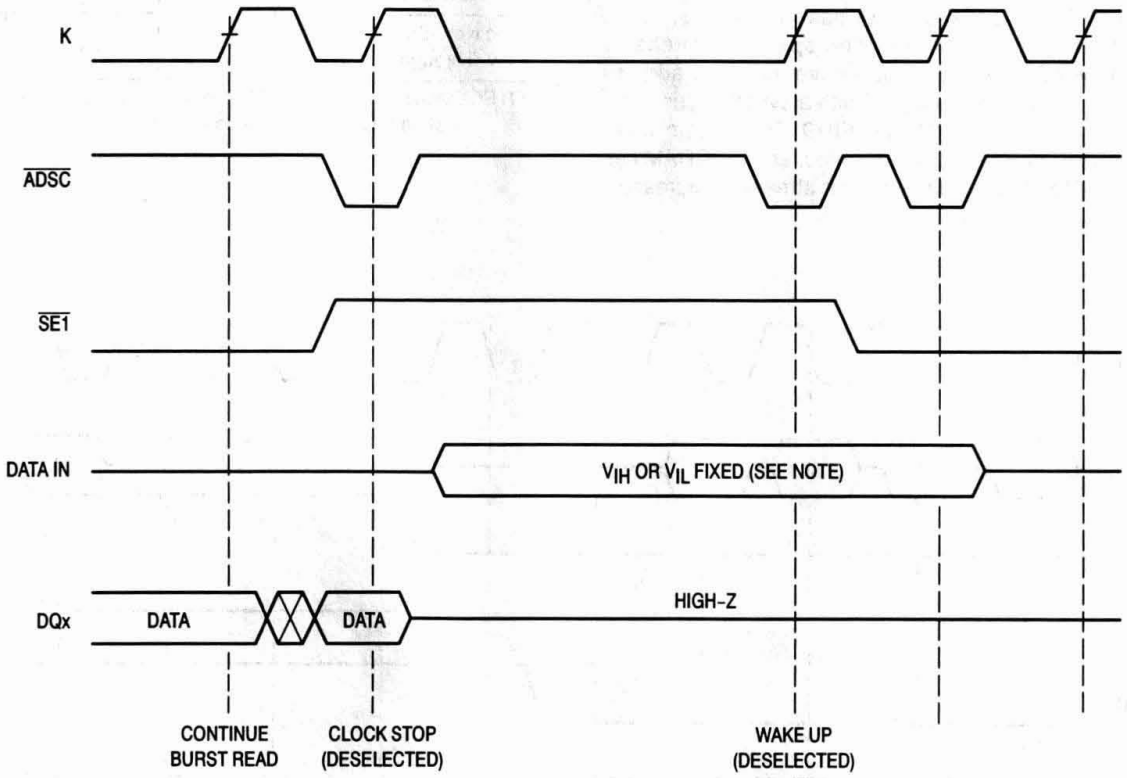
NOTE: For lowest possible power consumption during stop clock, the addresses should be driven to a low state (V_{IL}). Best results are obtained if V_{IL} < 0.2 V.

STOP CLOCK WITH WRITE TIMING



NOTE: While the clock is stopped, DATA IN must be fixed in a high (V_{IH}) or low (V_{IL}) state to reduce the DC current of the input buffers. For lowest power operation, all data and address lines should be held in a low (V_{IL}) state and control lines held in an inactive state.

STOP CLOCK WITH DESELECT OPERATION TIMING



NOTE: While the clock is stopped, DATA IN must be fixed in a high (V_{IH}) or low (V_{IL}) state to reduce the DC current of the input buffers. For lowest power operation, all data and address lines should be held in a low (V_{IL}) state and control lines held in an inactive state.

NON–BURST SYNCHRONOUS OPERATION

Although this BurstRAM has been designed for PowerPC–based and other high end MPU–based systems, these SRAMs can be used in other high speed L2 cache or memory applications that do not require the burst address feature. Most L2 caches designed with a synchronous interface can make use of the MCM69F819. The burst counter feature of the BurstRAM can be disabled, and the SRAM can be configured to act upon a continuous stream of addresses. See Figure 5.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

Non–Burst	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
Sync Non–Burst, Flow–Through SRAM	H	L	H	L	X

NOTE: Although X is specified in the table as a don't care, the pin must be tied either high or low.

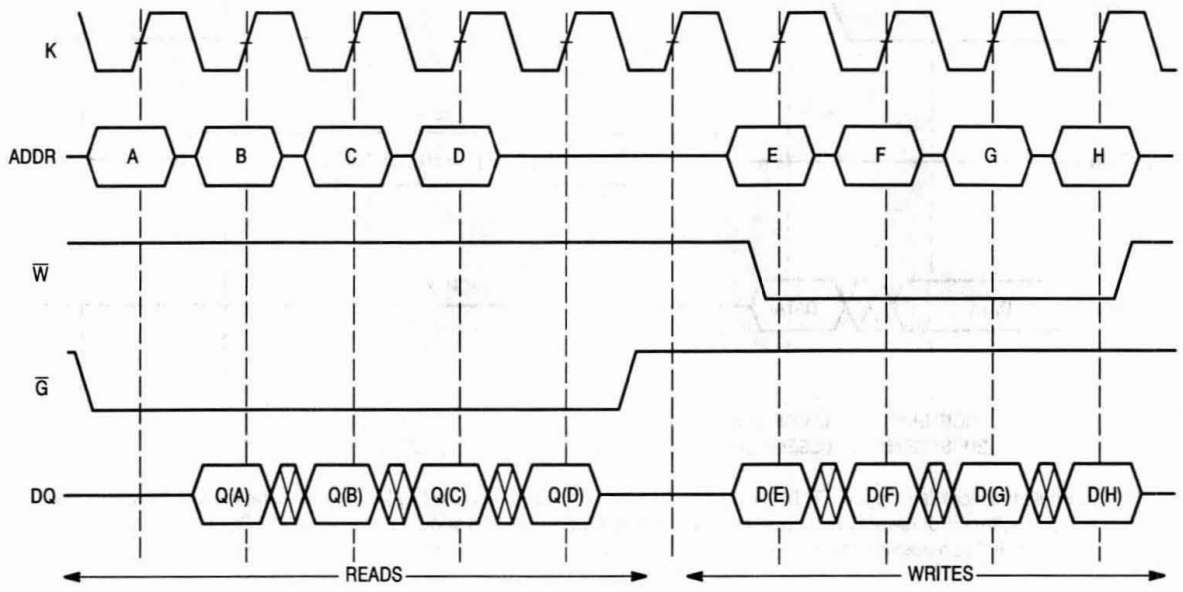


Figure 5. Configured as Non–Burst Synchronous SRAM

ORDERING INFORMATION
(Order by Full Part Number)

MCM 69F819 XX X X

- MCM: Motorola Memory Prefix
- 69F819: Part Number
- XX: Package (ZP = PBGA, TQ = TQFP)
- X: Speed (7.5 = 7.5 ns, 8 = 8 ns, 8.5 = 8.5 ns)
- X: Blank = Trays, R = Tape and Reel

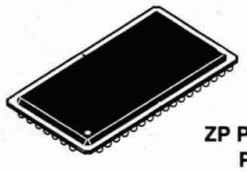
Full Part Numbers —

MCM69F819ZP7.5	MCM69F819ZP8	MCM69F819ZP8.5
MCM69F819ZP7.5R	MCM69F819ZP8R	MCM69F819ZP8.5R
MCM69F819TQ7.5	MCM69F819TQ8	MCM69F819TQ8.5
MCM69F819TQ7.5R	MCM69F819TQ8R	MCM69F819TQ8.5R

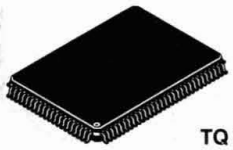
MCM69P819

Product Preview

256K x 18 Bit Pipelined BurstRAM™ Synchronous Fast Static RAM



ZP PACKAGE
PBGA
CASE 999–01



TQ PACKAGE
TQFP
CASE 983A–01

The MCM69P819 is a 4M bit synchronous fast static RAM designed to provide a burstable, high performance, secondary cache for the PowerPC™ and other high performance microprocessors. It is organized as 256K words of 18 bits each. This device integrates input registers, an output register, a 2–bit address counter, and high speed SRAM onto a single monolithic circuit for reduced parts count in cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K).

Addresses (SA), data inputs (DQx), and all control signals except output enable ($\overline{G}$) and linear burst order ($\overline{LBO}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ input pins. Subsequent burst addresses can be generated internally by the MCM69P819 (burst sequence operates in linear or interleaved mode dependent upon the state of $\overline{LBO}$) and controlled by the burst address advance ($\overline{ADV}$) input pin.

Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased timing flexibility for incoming signals.

Synchronous byte write ($\overline{SBx}$), synchronous global write ($\overline{SGW}$), and synchronous write enable ($\overline{SW}$) are provided to allow writes to either individual bytes or to all bytes. The two bytes are designated as "a" and "b". $\overline{SBa}$ controls DQa and $\overline{SBb}$ controls DQb. Individual bytes are written if the selected byte writes $\overline{SBx}$ are asserted with $\overline{SW}$. All bytes are written if either $\overline{SGW}$ is asserted or if all $\overline{SBx}$ and $\overline{SW}$ are asserted.

For read cycles, pipelined SRAMs output data is temporarily stored by an edge–triggered output register and then released to the output buffers at the next rising edge of clock (K).

The MCM69P819 operates from a 3.3 V core power supply and all outputs operate on a 2.5 V power supply. All inputs and outputs are JEDEC standard JESD8–5 compatible.

- MCM69P819 Speed Options

Speed	t_{KHKH}	Pipelined t_{KHQV}	Setup	Hold	I_{DD}	Pkg
166 MHz	6 ns	3.5 ns	1.5 ns	0.5 ns	425 mA	PBGA
150 MHz	6.7 ns	3.8 ns	1.5 ns	0.5 ns	400 mA	PBGA
133 MHz	7.5 ns	4 ns	1.5 ns	0.5 ns	375 mA	PBGA/TQFP

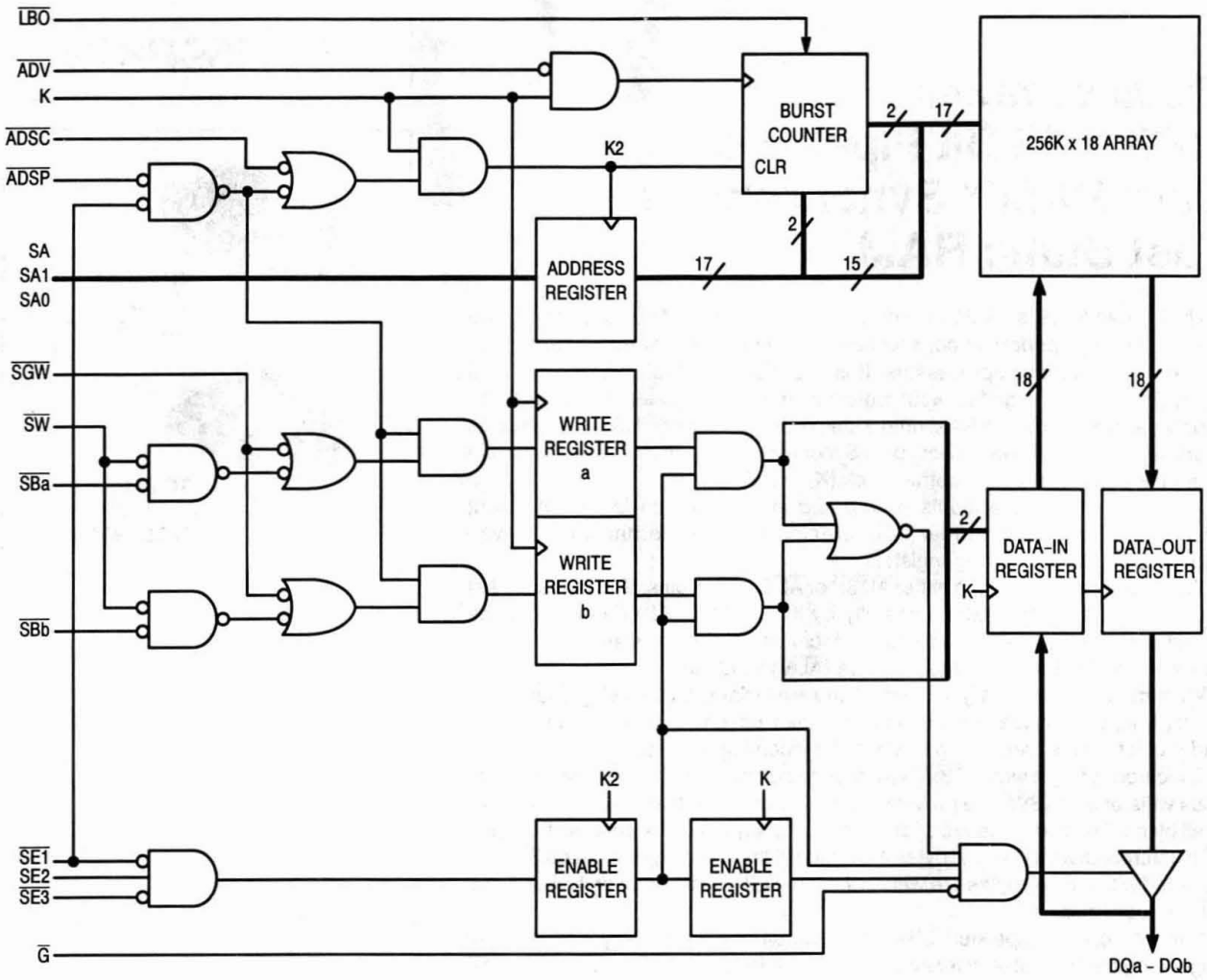
- 3.3 V + 10%, – 5% Core Power Supply, 2.5 V I/O Supply
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Selectable Burst Sequencing Order (Linear/Interleaved)
- Single–Cycle Deselect Timing
- Internally Self–Timed Write Cycle
- Byte Write and Global Write Control
- JEDEC Standard 119 Pin PBGA and 100 Pin TQFP Packages

BurstRAM is a trademark of Motorola, Inc.
The PowerPC name is a trademark of IBM Corp., used under license therefrom.

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

REV 2
4/9/97

FUNCTIONAL BLOCK DIAGRAM



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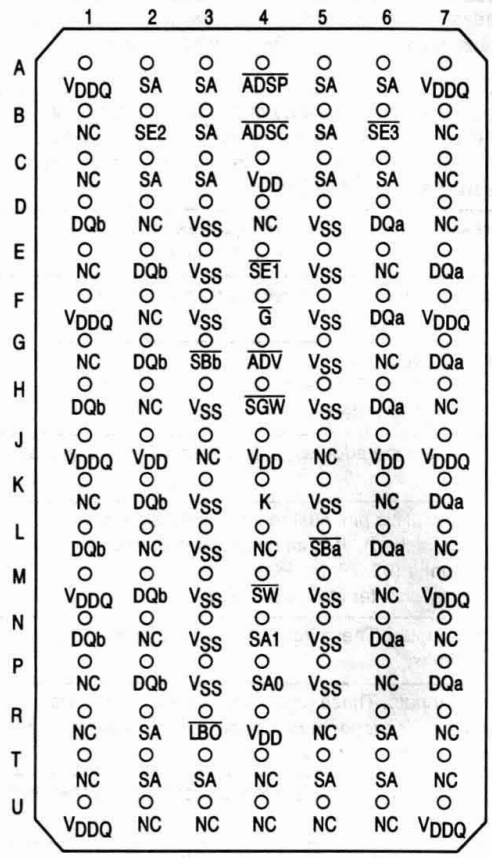
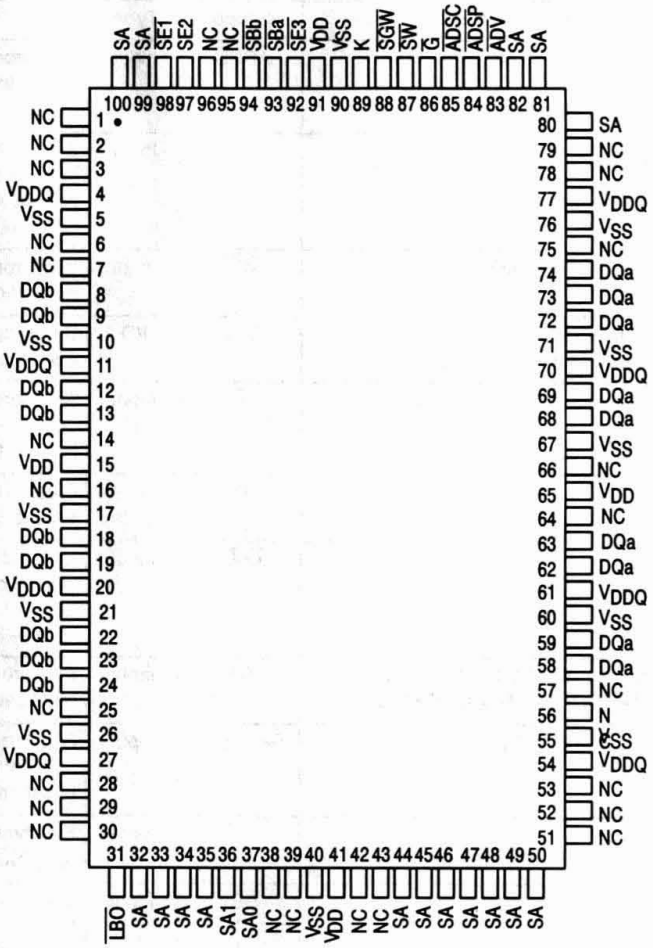
PIN ASSIGNMENTS


1 2 3 4 5 6 7
A VDDQ SA SA ADSP SA SA VDDQ
B NC SE2 SA ADSC SA SE3 NC
C NC SA SA VDD SA SA NC
D DQb NC VSS NC VSS DQa NC
E NC DQb VSS SE1 VSS NC DQa
F VDDQ NC VSS G VSS DQa VDDQ
G NC DQb SBb ADV VSS NC DQa
H DQb NC VSS SGW VSS DQa NC
J VDDQ VDD NC VDD NC VDD VDDQ
K NC DQb VSS K VSS NC DQa
L DQb NC VSS NC SBa DQa NC
M VDDQ DQb VSS SW VSS NC VDDQ
N DQb NC VSS SA1 VSS DQa NC
P NC DQb VSS SA0 VSS NC DQa
R NC SA LBO VDD NC SA NC
T NC SA SA NC SA SA NC
U VDDQ NC NC NC NC NC VDDQ

TOP VIEW 119 BUMP PBGA



TOP VIEW 100 PIN TQFP

Not to Scale

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PBGA PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
4B	$\overline{ADSC}$	Input	Synchronous Address Status Controller: Active low, is used to latch a new external address. Used to initiate a READ, WRITE, or chip deselect.
4A	$\overline{ADSP}$	Input	Synchronous Address Status Processor: Active low, interrupts any ongoing burst and latches a new external address. Used to initiate a new READ or chip deselect (exception — chip deselect does not occur when $\overline{ADSP}$ is asserted and $\overline{SE1}$ is high).
4G	$\overline{ADV}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
(a) 6D, 7E, 6F, 7G, 6H, 7K, 6L, 6N, 7P (b) 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 2P	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b).
4F	$\overline{G}$	Input	Asynchronous Output Enable Input: Low — enables output buffers (DQx pins). High — DQx pins are high impedance.
4K	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$ and $\overline{LBO}$.
3R	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst counter (68K/PowerPC). High — interleaved burst counter (486/i960/Pentium).
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 2R, 6R, 2T, 3T, 5T, 6T	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
4N, 4P	SA1, SA0	Input	Synchronous Address Inputs: These pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
5L, 3G (a) (b)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: "x" refers to the byte being written (byte a, b). $\overline{SGW}$ overrides $\overline{SBx}$.
4E	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high — blocks $\overline{ADSP}$ or deselects chip when $\overline{ADSC}$ is asserted.
2B	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
6B	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
4H	$\overline{SGW}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the $\overline{SBx}$ and $\overline{SW}$ signals. If only byte write signals $\overline{SBx}$ are being used, tie this pin high.
4M	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{SBx}$ pins. If only byte write signals $\overline{SBx}$ are being used, tie this pin low.
4C, 2J, 4J, 6J, 4R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	I/O Power Supply.
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P	V_{SS}	Supply	Ground.
1B, 7B, 1C, 7C, 2D, 4D, 7D, 1E, 6E, 2F, 1G, 6G, 2H, 7H, 3J, 5J, 1K, 6K, 2L, 4L, 7L, 6M, 2N, 7N, 1P, 6P, 1R, 5R, 7R, 1T, 4T, 7T, 2U, 3U, 4U, 5U, 6U	NC	—	No Connection: There is no connection to the chip.

TQFP PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: Active low, is used to latch a new external address. Used to initiate a READ, WRITE, or chip deselect.
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: Active low, interrupts any ongoing burst and latches a new external address. Used to initiate a new READ or chip deselect (exception — chip deselect does not occur when $\overline{ADSP}$ is asserted and $\overline{SE1}$ is high).
83	$\overline{ADV}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
(a) 58, 59, 62, 63, 68, 69, 72, 73, 74 (b) 8, 9, 12, 13, 18, 19, 22, 23, 24	$\overline{DQx}$	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b).
86	$\overline{G}$	Input	Asynchronous Output Enable Input: Low — enables output buffers (DQx pins). High — DQx pins are high impedance.
89	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$ and $\overline{LBO}$.
31	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst counter (68K/PowerPC). High — interleaved burst counter (486/i960/Pentium).
32, 33, 34, 35, 44, 45, 46, 47, 48, 49, 50, 80, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
36, 37	SA1, SA0	Input	Synchronous Address Inputs: These pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
93, 94 (a) (b)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: "x" refers to the byte being written (byte a, b). $\overline{SGW}$ overrides $\overline{SBx}$.
98	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high — blocks $\overline{ADSP}$ or deselects chip when $\overline{ADSC}$ is asserted.
97	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
92	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
88	$\overline{SGW}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the $\overline{SBx}$ and $\overline{SW}$ signals. If only byte write signals $\overline{SBx}$ are being used, tie this pin high.
87	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{SBx}$ pins. If only byte write signals $\overline{SBx}$ are being used, tie this pin low.
15, 41, 65, 91	V_{DD}	Supply	Core Power Supply.
4, 11, 20, 27, 54, 61, 70, 77	V_{DDQ}	Supply	I/O Power Supply.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground.
1, 2, 3, 6, 7, 14, 16, 25, 28, 29, 30, 38, 39, 42, 43, 51, 52, 53, 56, 57, 64, 66, 75, 78, 79, 95, 96	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE (See Notes 1 Through 5)

Next Cycle	Address Used	$\overline{SE1}$	SE2	$\overline{SE3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{G}$ [3]	DQx	Write [2, 4]
Deselect	None	1	X	X	X	0	X	X	High–Z	X
Deselect	None	0	X	1	0	X	X	X	High–Z	X
Deselect	None	0	0	X	0	X	X	X	High–Z	X
Deselect	None	X	X	1	1	0	X	X	High–Z	X
Deselect	None	X	0	X	1	0	X	X	High–Z	X
Begin Read	External	0	1	0	0	X	X	X	High–Z	X[5]
Begin Read	External	0	1	0	1	0	X	X	High–Z	READ[5]
Continue Read	Next	X	X	X	1	1	0	1	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	0	DQ	READ
Continue Read	Next	1	X	X	X	1	0	1	High–Z	READ
Continue Read	Next	1	X	X	X	1	0	0	DQ	READ
Suspend Read	Current	X	X	X	1	1	1	1	High–Z	READ
Suspend Read	Current	X	X	X	1	1	1	0	DQ	READ
Suspend Read	Current	1	X	X	X	1	1	1	High–Z	READ
Suspend Read	Current	1	X	X	X	1	1	0	DQ	READ
Begin Write	External	0	1	0	1	0	X	X	High–Z	WRITE
Continue Write	Next	X	X	X	1	1	0	X	High–Z	WRITE
Continue Write	Next	1	X	X	X	1	0	X	High–Z	WRITE
Suspend Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Suspend Write	Current	1	X	X	X	1	1	X	High–Z	WRITE

NOTES:
1. X = Don't Care. 1 = logic high. 0 = logic low.
2. Write is defined as either 1) any $\overline{SBx}$ and $\overline{SW}$ low or 2) $\overline{SGW}$ is low.
3. $\overline{G}$ is an asynchronous signal and is not sampled by the clock K. $\overline{G}$ drives the bus immediately (t_{GLQX}) following $\overline{G}$ going low.
4. On write cycles that follow read cycles, $\overline{G}$ must be negated prior to the start of the write cycle to ensure proper write data setup times. $\overline{G}$ must also remain negated at the completion of the write cycle to ensure proper write data hold times.
5. This read assumes the RAM was previously deselected.

LINEAR BURST ADDRESS TABLE ($\overline{LBO} = V_{SS}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X10	X . . . X11	X . . . X00
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X00	X . . . X01	X . . . X10

INTERLEAVED BURST ADDRESS TABLE ($\overline{LBO} = V_{DD}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00

WRITE TRUTH TABLE

Cycle Type	$\overline{SGW}$	$\overline{SW}$	$\overline{SBa}$	$\overline{SBb}$
Read	H	H	X	X
Read	H	L	H	H
Write Byte a	H	L	L	H
Write Byte b	H	L	H	L
Write All Bytes	H	L	L	L
Write All Bytes	L	X	X	X

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	V_{SS} – 0.5 to + 4.6	V
I/O Supply Voltage (See Note 2)	V_{DDQ}	V_{SS} – 0.5 to V_{DD}	V
Input Voltage Relative to V_{SS} for Any Pin Except V_{DD} (See Note 2)	V_{in}, V_{out}	V_{SS} – 0.5 to V_{DD} + 0.5	V
Input Voltage (Three–State I/O) (See Note 2)	V_{IT}	V_{SS} – 0.5 to V_{DDQ} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Package Power Dissipation (See Note 3)	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to 85	°C
Storage Temperature	T_{stg}	– 55 to 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. This is a steady–state DC parameter that is in effect after the power supply has achieved its nominal operating level. Power sequencing is not necessary.
3. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

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PACKAGE THERMAL CHARACTERISTICS — PBGA

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	38 22	°C/W	1, 2
Junction to Board (Bottom)		$R_{\theta JB}$	14	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	5	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

PACKAGE THERMAL CHARACTERISTICS — TQFP (See Note 1)

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	40 25	°C/W	2
Junction to Board (Bottom)		$R_{\theta JB}$	17	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(3.6 V ≥ V_{DD} ≥ 3.1 V, 110°C ≥ T_J ≥ 20°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.1	3.3	3.6	V
Operating Temperature	T_J	20	—	110	°C
Input Low Voltage	V_{IL}	– 0.3	—	0.8	V
Input High Voltage	V_{IH}	1.7	—	V_{DD} + 0.3	V
Input High Voltage I/O Pins	V_{IH2}	1.7	—	V_{DDQ} + 0.3	V
I/O Supply Voltage	V_{DDQ}	2.375	2.5	V_{DD}	V

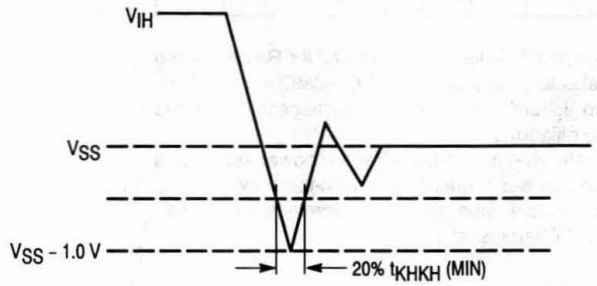


Figure 1. Undershoot Voltage

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input Leakage Current (0 V ≤ V_{in} ≤ V_{DD})	$I_{lkg(I)}$	—	—	± 1	µA	
Output Leakage Current (0 V ≤ V_{in} ≤ V_{DDQ})	$I_{lkg(O)}$	—	—	± 1	µA	
AC Supply Current (Device Selected, All Outputs Open, Cycle Time = t_{KHKH} Min) Includes V_{DD} and V_{DDQ} — MCM69P819–3.5	I_{DDA}	—	—	425	mA	1, 2, 3
MCM69P819–3.8				400		
MCM69P819–4				375		
CMOS Standby Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH})	I_{SB1}	—	—	190	mA	1, 2, 3, 4
Clock Running Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}, All Other Inputs Held to Static CMOS Levels V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{DD} – 0.2 V)	I_{SB2}	—	—	85	mA	4
Output Low Voltage (I_{OL} = 2 mA) (See Figure 5) V_{DDQ} = 2.5 V	V_{OL}	—	—	0.7	V	
Output High Voltage (I_{OL} = –2 mA) (See Figure 5) V_{DDQ} = 2.5 V	V_{OH}	1.7	—	—	V	
Output Low Voltage (I_{OL} = 2 mA) V_{DDQ} = 3.3 V	V_{OL2}	—	—	0.4	V	
Output High Voltage (I_{OL} = –2 mA) V_{DDQ} = 3.3 V	V_{OH2}	2.4	—	—	V	
Desk Top Suspend Current (Selected, All Inputs ≤ 0.2 V, Freq. = Max, V_{DD} = Max, $\overline{ADSP}$ and $\overline{ADSC}$ = Logic High, Outputs Disabled)	I_{DS1}	—	—	TBD	mA	
Desk Top Idle Current (Selected, All Inputs ≤ 0.2 V, Freq. = 0, V_{DD} = Max, $\overline{ADSP}$ and $\overline{ADSC}$ = Logic High, Outputs Disabled)	I_{DS1A}	—	—	TBD	mA	
Desk Top Standby Current (Deselected, All Inputs ≤ 0.2 V, Freq. = 0, V_{DDQ} = Max, Outputs Disabled)	I_{DS2}	—	—	TBD	mA	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing.
2. All addresses transition simultaneously low (LSB) then high (MSB).
3. Data states are all zero.
4. Device is deselected as defined by the Truth Table.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, 110°C ≥ T_J ≥ 20°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	4	5	pF
Input/Output Capacitance	$C_{I/O}$	—	7	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(3.6 V ≥ V_{DD} ≥ 3.135 V, 110°C ≥ T_J ≥ 20°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.25 V
Input Pulse Levels ..... 0 to 2.5 V
Input Slew Rate (See Figure 4) ..... 1.0 V/ns

Output Timing Reference Level ..... 1.25 V
Output Load ..... See Figure 2 Unless Otherwise Noted
Output Rise/Fall Times (max) ..... 1.8 ns

READ/WRITE CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM69P819–3.5 166 MHz		MCM69P819–3.8 150 MHz		MCM69P819–4 133 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	6	—	6.7	—	7.5	—	ns	
Clock High Pulse Width	t_{KHKL}	2.4	—	2.6	—	2.8	—	ns	3, 6
Clock Low Pulse Width	t_{KLKH}	2.4	—	2.6	—	2.8	—	ns	3, 6
Clock Low	t_{KL}	1.5	—	1.7	—	1.9	—	ns	3, 6
Clock High	t_{KH}	1.3	—	1.5	—	1.7	—	ns	3, 6
Clock Access Time	t_{KHQV}	—	3.5	—	3.8	—	4	ns	3
Output Enable to Output Valid	t_{GLQV}	—	3.5	—	3.5	—	3.8	ns	3
Clock High to Output Active	t_{KHQX1}	0	—	0	—	0	—	ns	3, 4, 5
Clock High to Output Change	t_{KHQX2}	1.5	—	1.5	—	1.5	—	ns	3, 5
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	3. 4.5
Output Disable to Q High–Z	t_{GHQZ}	—	3.5	—	3.5	—	3.8	ns	3, 4, 5
Clock High to Q High–Z	t_{KHQZ}	1.5	6	1.5	6.7	1.5	7.5	ns	3, 4, 5
Setup Times: Address	t_{ADKH}	1.5	—	1.5	—	1.5	—	ns	3
$\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$	t_{ADSKH}								
Data In	t_{DVKH}								
Write	t_{WVKH}								
Chip Enable	t_{EVKH}								
Hold Times: Address	t_{KHAX}	0.5	—	0.5	—	0.5	—	ns	3
$\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$	t_{KHADSX}								
Data In	t_{KHDX}								
Write	t_{KHWX}								
Chip Enable	t_{KHEX}								

NOTES:
1. Write is defined as either any $\overline{SBx}$ and $\overline{SW}$ low or $\overline{SGW}$ is low. Chip Enable is defined as $\overline{SE1}$ low, SE2 high, and $\overline{SE3}$ low whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. Tested per AC Test Load, Figure 2.
4. Measured at ± 200 mV from steady state.
5. This parameter is sampled and not 100% tested.
6. In order to reduce test correlation issues and to reduce the effects of application specific input edge rate variations on correlation between data sheet parameters and actual system performance, FSRAM AC parametric specifications are always specified at $V_{DDQ}/2$. In some design exercises, it is desirable to evaluate timing using other reference levels. Since the maximum test input edge rate is known and is given in the AC Test Conditions section of the data sheet as 1 V/ns, one can easily interpolate timing values to other reference levels. Figure 3 shows interpolation to DC V_{IH} and DC V_{IL} levels.

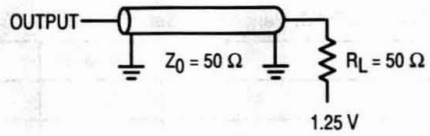


Figure 2. AC Test Load

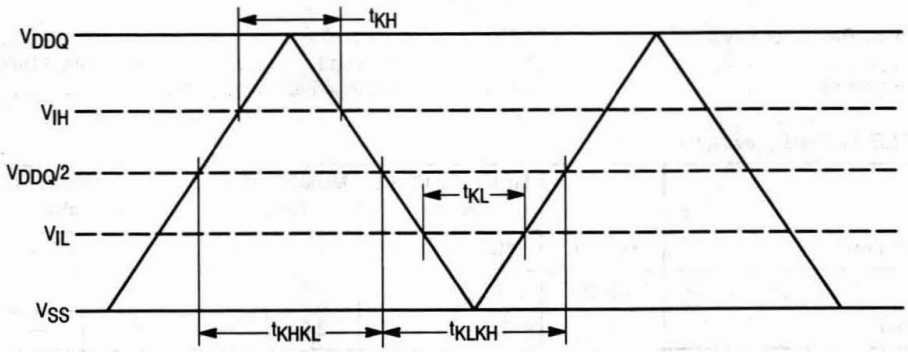
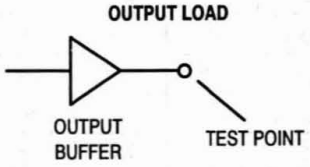
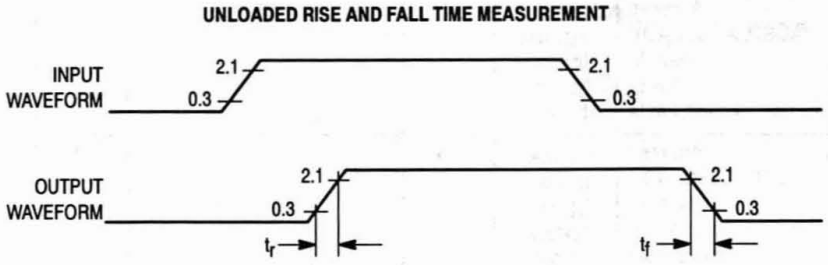


Figure 3. Interpolation to DC V_{IH} and DC V_{IL} Levels

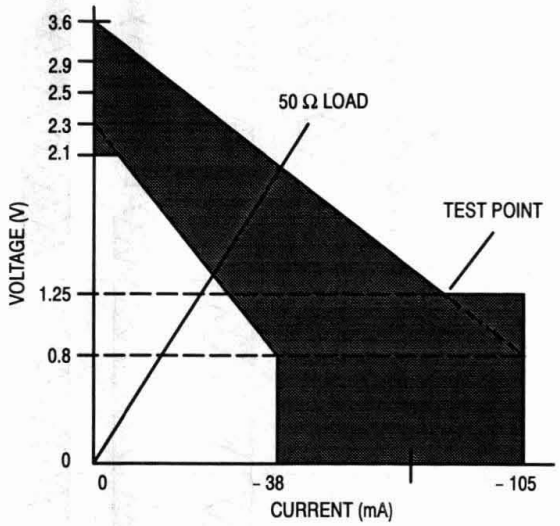




NOTES:
1. Input waveform has a slew rate of 1 V/ns.
2. Rise time is measured from 0.3 to 2.1 V unloaded.
3. Fall time is measured from 2.1 to 0.3 V unloaded.

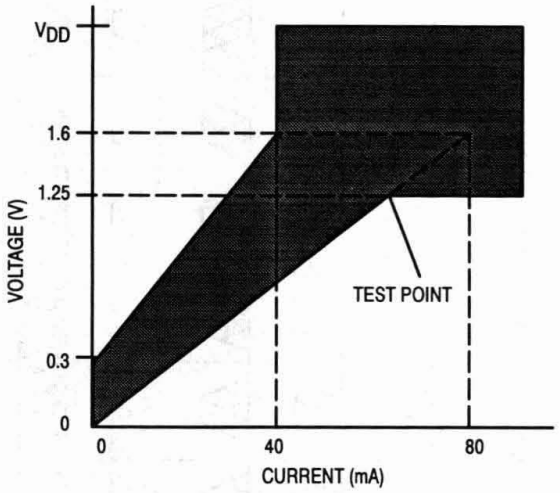
Figure 4. Unloaded Rise and Fall Time Characterization

PULL-UP		
VOLTAGE (V)	I (mA) MIN	I (mA) MAX
- 0.5	- 38	- 105
0	- 38	- 105
0.8	- 38	- 105
1.25	- 26	- 83
1.5	- 20	- 70
2.3	0	- 30
2.7	0	- 10
2.9	0	0
3.4	0	0
3.6	0	0



(a) Pull–Up

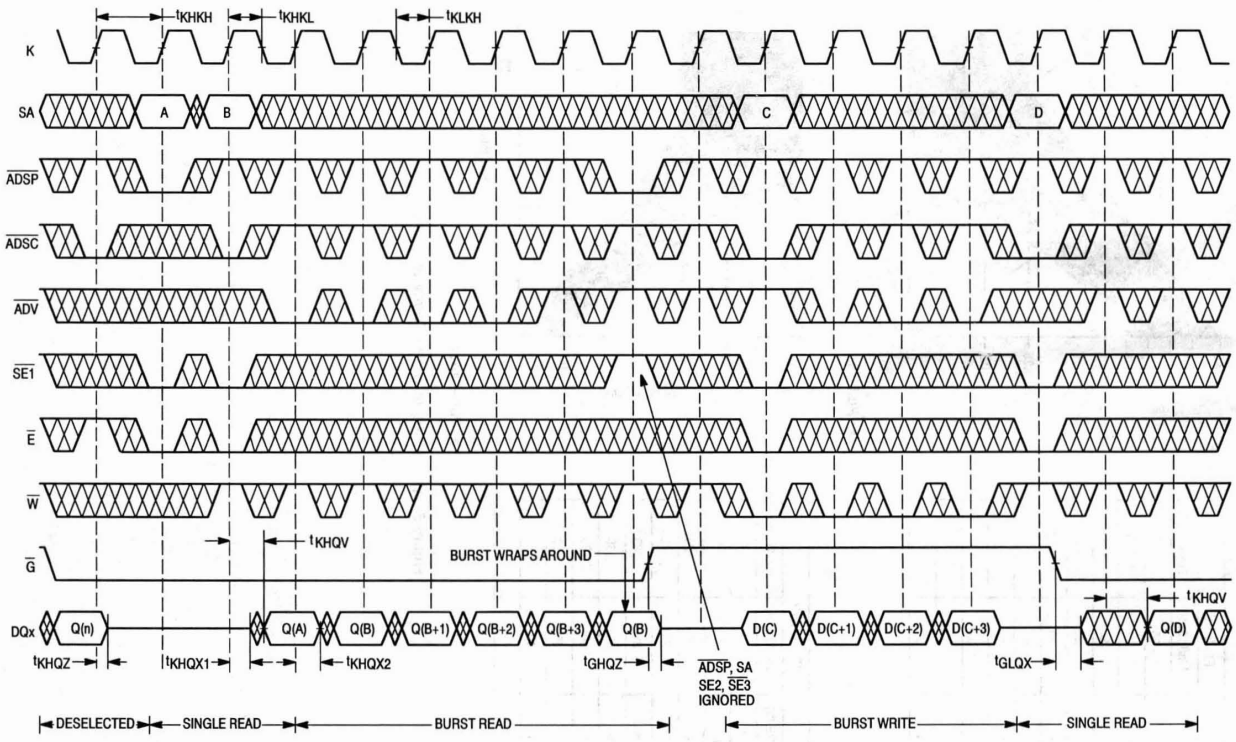
PULL-DOWN		
VOLTAGE (V)	I (mA) MIN	I (mA) MAX
- 0.5	0	0
0	0	0
0.4	10	20
0.8	20	40
1.25	31	63
1.6	40	80
2.8	40	80
3.2	40	80
3.4	40	80
3.6	46	80



(b) Pull–Down

Figure 5. Typical Output Buffer Characteristics

READ/WRITE CYCLES



NOTE: $\overline{E}$ low = SE2 high and $\overline{SE3}$ low.
$\overline{W}$ low = $\overline{SGW}$ low and/or $\overline{SW}$ and $\overline{SBx}$ low.

STOP CLOCK OPERATION

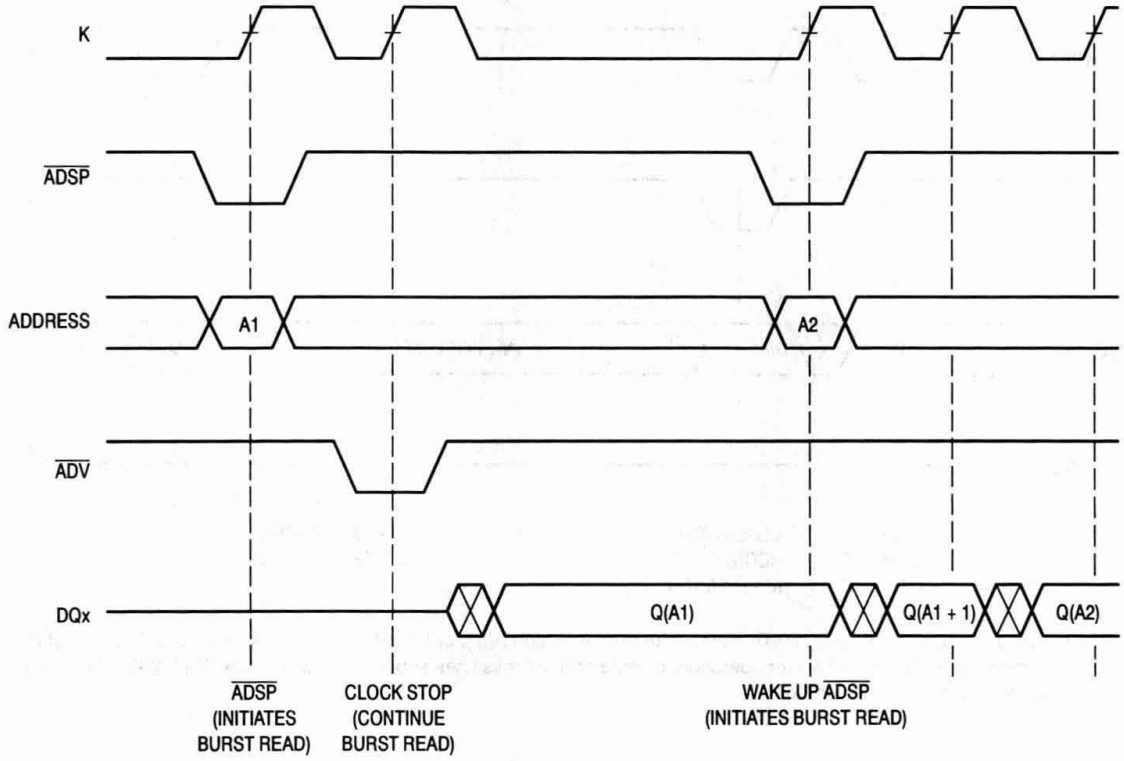
In the stop clock mode of operation, the SRAM will hold all state and data values even though the clock is not running (full static operation). The SRAM design allows the clock to start with $\overline{ADSP}$ and $\overline{ADSC}$, and stops the clock after the last write data is latched, or the last read data is driven out.

When starting and stopping the clock, the AC clock timing and parametrics must be strictly maintained. For example, clock pulse width and edge rates must be guaranteed when starting and stopping the clocks.

To achieve the lowest power operation for all three stop clock modes, stop read, stop write, and stop deselect:

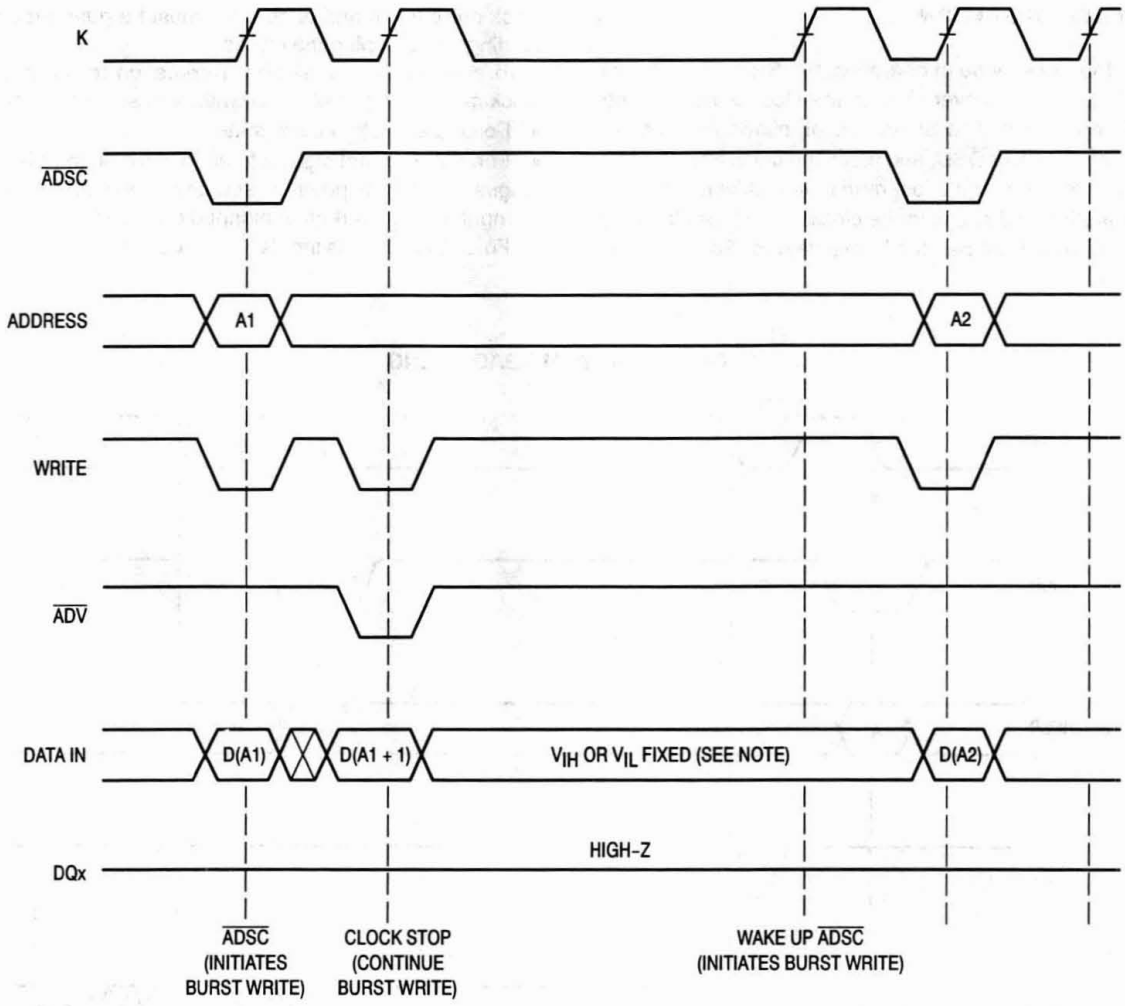
- Force the clock to a low state.
- Force the control signals to an inactive state (this guarantees any potential source of noise on the clock input will not start an unplanned on activity).
- Force the address inputs to a low state.

STOP CLOCK WITH READ TIMING



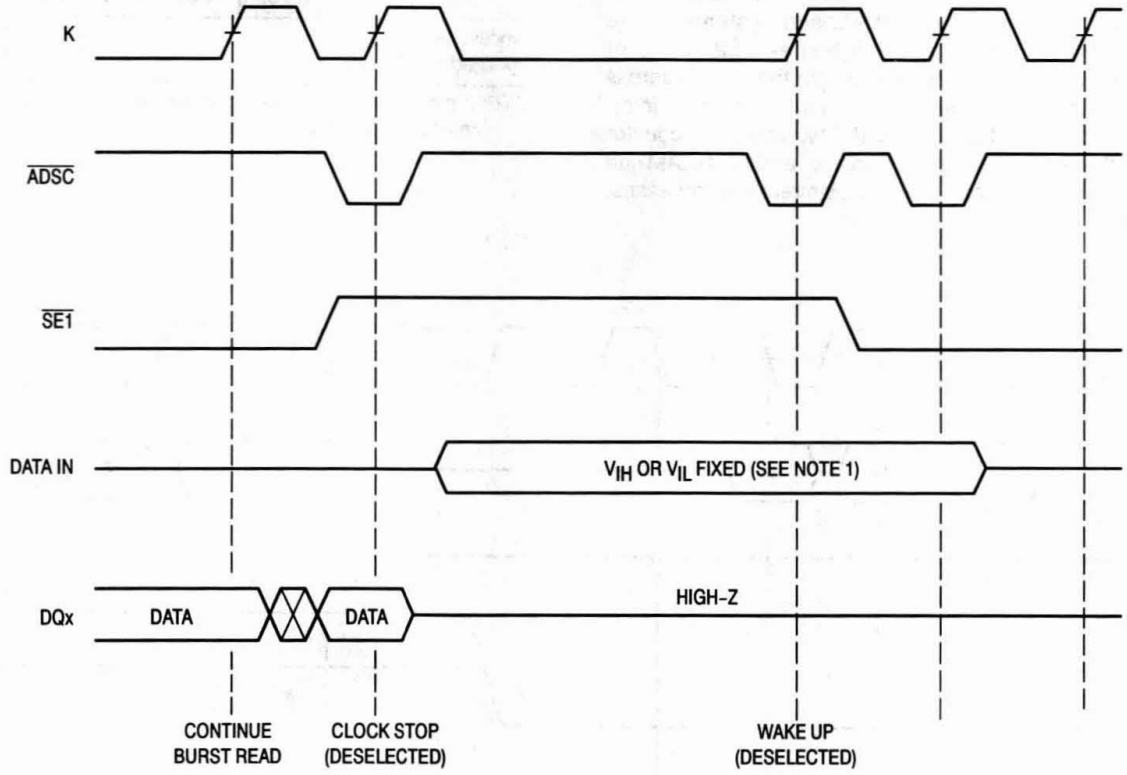
NOTE: For lowest possible power consumption during stop clock, the addresses should be driven to a low state (V_{IL}). Best results are obtained if $V_{IL} < 0.2$ V.

STOP CLOCK WITH WRITE TIMING



NOTE: While the clock is stopped, DATA IN must be fixed in a high (V_{IH}) or low (V_{IL}) state to reduce the DC current of the input buffers. For lowest power operation, all data and address lines should be held in a low (V_{IL}) state and control lines held in an inactive state.

STOP CLOCK WITH DESELECT OPERATION TIMING



NOTES:
1. While the clock is stopped, DATA IN must be fixed in a high (V_{IH}) or low (V_{IL}) state to reduce the DC current of the input buffers. For lowest power operation, all data and address lines should be held in a low (V_{IL}) state and control lines held in an inactive state.
2. For best possible power savings, the data–in should be driven low.

NON–BURST SYNCHRONOUS OPERATION

Although this BurstRAM has been designed for PowerPC–based and other high end MPU–based systems, these SRAMs can be used in other high speed L2 cache or memory applications that do not require the burst address feature. Most L2 caches designed with a synchronous interface can make use of the MCM69P819. The burst counter feature of the BurstRAM can be disabled, and the SRAM can be configured to act upon a continuous stream of addresses. See Figure 6.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

Non–Burst	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
Sync Non–Burst, Pipelined SRAM	H	L	H	L	X

NOTE: Although X is specified in the table as a don't care, the pin must be tied either high or low.

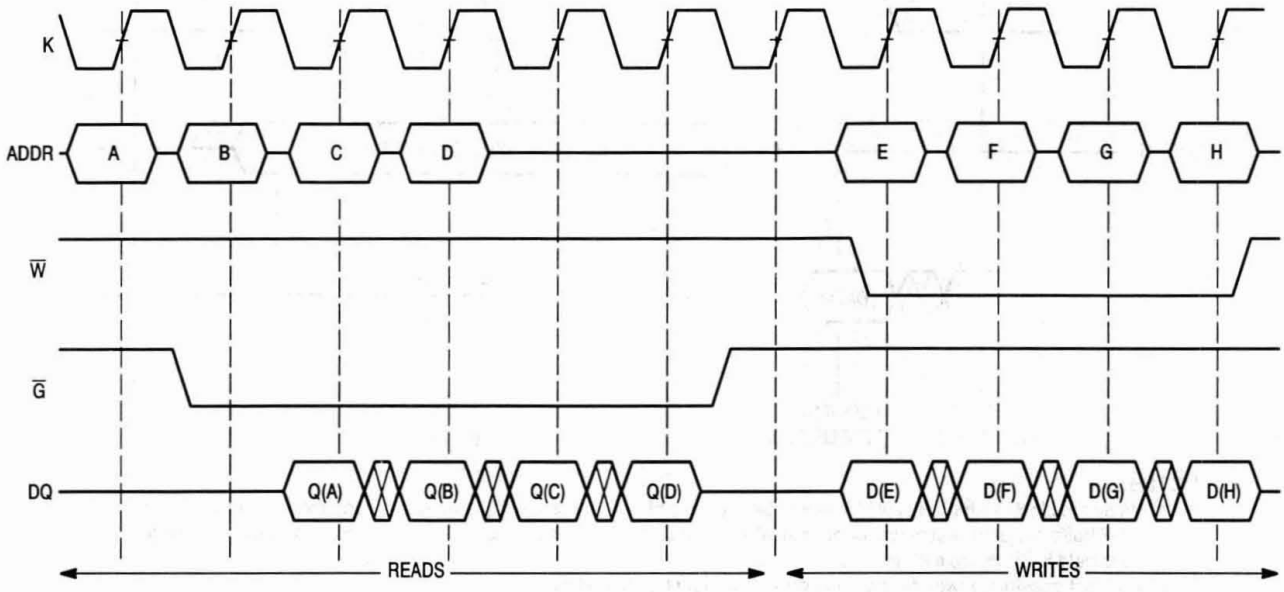


Figure 6. Configured as Non–Burst Synchronous SRAM

ORDERING INFORMATION

(Order by Full Part Number)

MCM 69P819 XX X X

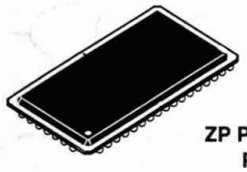
- Motorola Memory Prefix
- Part Number
- Blank = Trays, R = Tape and Reel
- Speed (3.5 = 3.5 ns, 3.8 = 3.8 ns, 4 = 4 ns)
- Package (ZP = PBGA, TQ = TQFP)

Full Part Numbers — MCM69P819ZP3.5, MCM69P819ZP3.5R, MCM69P819ZP3.8, MCM69P819ZP3.8R, MCM69P819ZP4, MCM69P819ZP4R, MCM69P819TQ4, MCM69P819TQ4R

MCM69F737

Product Preview

128K x 36 Bit Flow–Through BurstRAM™ Synchronous Fast Static RAM



ZP PACKAGE
PBGA
CASE 999–01

TQ PACKAGE
TQFP
CASE 983A–01

The MCM69F737 is a 4M bit synchronous fast static RAM designed to provide a burstable, high performance, secondary cache for the PowerPC™ and other high performance microprocessors. It is organized as 128K words of 36 bits each. This device integrates input registers, a 2–bit address counter, and high speed SRAM onto a single monolithic circuit for reduced parts count in cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K).

Addresses (SA), data inputs (DQx), and all control signals except output enable ($\overline{G}$) and linear burst order ($\overline{LBO}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ input pins. Subsequent burst addresses can be generated internally by the MCM69F737 (burst sequence operates in linear or interleaved mode dependent upon the state of $\overline{LBO}$) and controlled by the burst address advance ($\overline{ADV}$) input pin.

Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased timing flexibility for incoming signals.

Synchronous byte write ($\overline{SBx}$), synchronous global write ($\overline{SGW}$), and synchronous write enable ($\overline{SW}$) are provided to allow writes to either individual bytes or to all bytes. The four bytes are designated as "a", "b", "c", and "d". $\overline{SBa}$ controls DQa, $\overline{SBb}$ controls DQb, etc. Individual bytes are written if the selected byte writes $\overline{SBx}$ are asserted with $\overline{SW}$. All bytes are written if either $\overline{SGW}$ is asserted or if all $\overline{SBx}$ and $\overline{SW}$ are asserted.

For read cycles, a flow–through SRAM allows output data to simply flow freely from the memory array.

The MCM69F737 operates from a 3.3 V core power supply and all outputs operate on a 2.5 V power supply. All inputs and outputs are JEDEC standard JESD8–5 compatible.

- MCM69F737 Speed Options

Speed	t_{KHKH}	Flow–Through t_{KHQV}	Setup	Hold	I_{DD}
117 MHz	8.5 ns	7.5 ns	2 ns	0.5 ns	350 mA
100 MHz	10 ns	8 ns	2 ns	0.5 ns	325 mA
90 MHz	11 ns	8.5 ns	2 ns	0.5 ns	300 mA

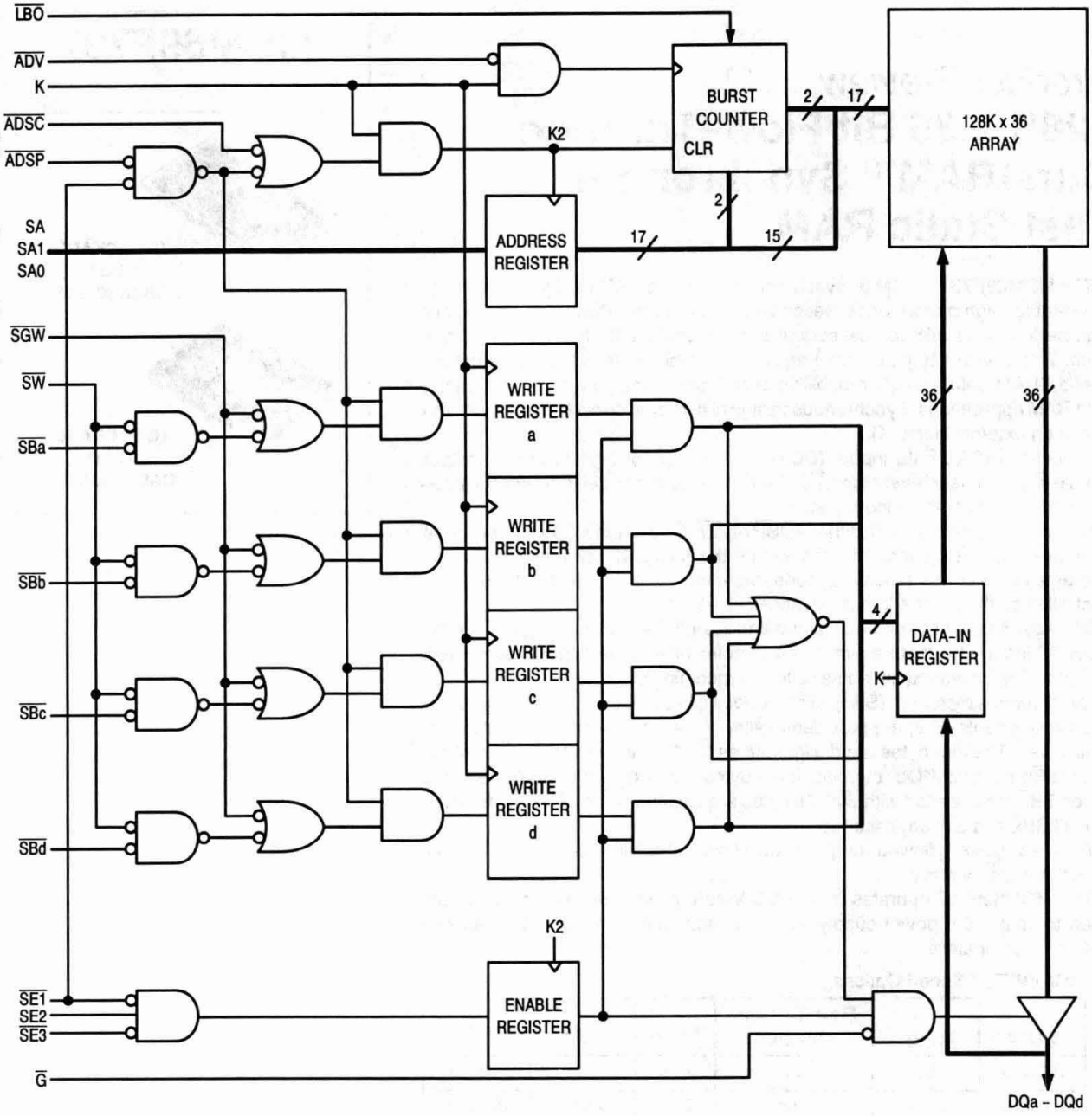
- 3.3 V + 10%, – 5% Core Power Supply, 2.5 V I/O Supply
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Selectable Burst Sequencing Order (Linear/Interleaved)
- Single–Cycle Deselect Timing
- Internally Self–Timed Write Cycle
- Byte Write and Global Write Control
- JEDEC Standard 119 Pin PBGA and 100 Pin TQFP Packages

BurstRAM is a trademark of Motorola, Inc.
The PowerPC name is a trademark of IBM Corp., used under licencse therefrom.

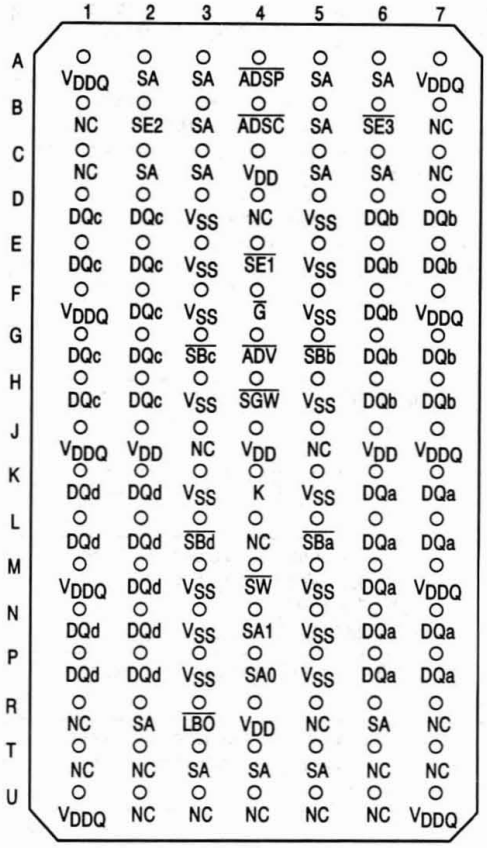
This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

REV 2
4/9/97

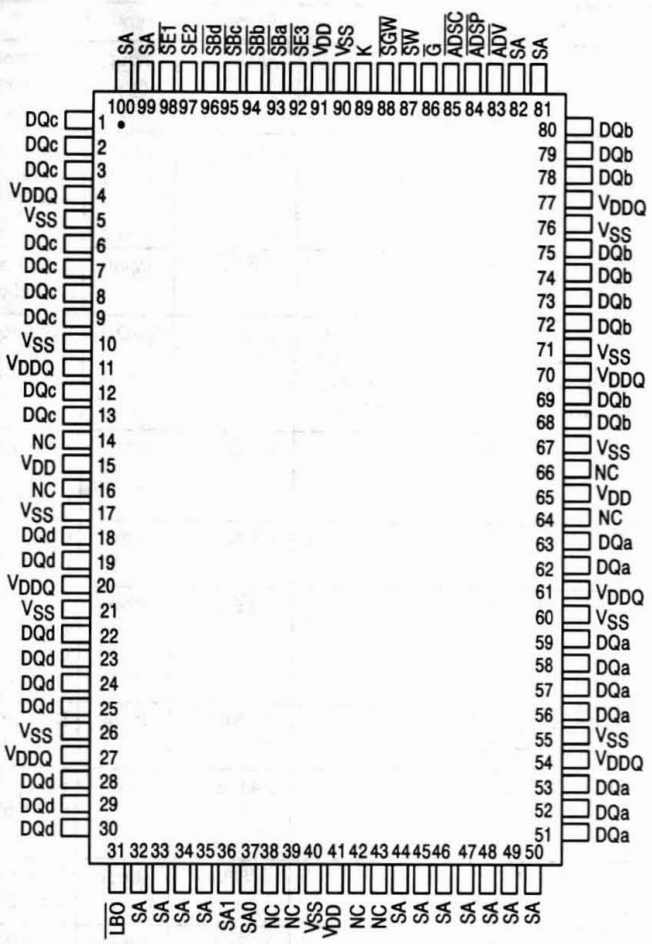
FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENTS


1 2 3 4 5 6 7
A VDDQ SA SA ADSP SA SA VDDQ
B NC SE2 SA ADSC SA SE3 NC
C NC SA SA VDD SA SA NC
D DQc DQc VSS NC VSS DQb DQb
E DQc DQc VSS SE1 VSS DQb DQb
F VDDQ DQc VSS G VSS DQb VDDQ
G DQc DQc SBc ADV SBb DQb DQb
H DQc DQc VSS SGW VSS DQb DQb
J VDDQ VDD NC VDD NC VDD VDDQ
K DQd DQd VSS K VSS DQa DQa
L DQd DQd SBd NC SBa DQa DQa
M VDDQ DQd VSS SW VSS DQa VDDQ
N DQd DQd VSS SA1 VSS DQa DQa
P DQd DQd VSS SA0 VSS DQa DQa
R NC SA LBO VDD NC SA NC
T NC NC SA SA SA NC NC
U VDDQ NC NC NC NC NC VDDQ

TOP VIEW 119 BUMP PBGA



TOP VIEW 100 PIN TQFP

Not to Scale

4

PBGA PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
4B	$\overline{ADSC}$	Input	Synchronous Address Status Controller: Active low, is used to latch a new external address. Used to initiate a READ, WRITE, or chip deselect.
4A	$\overline{ADSP}$	Input	Synchronous Address Status Processor: Active low, interrupts any ongoing burst and latches a new external address. Used to initiate a new READ or chip deselect (exception — chip deselect does not occur when $\overline{ADSP}$ is asserted and $\overline{SE1}$ is high).
4G	$\overline{ADV}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
(a) 6K, 7K, 6L, 7L, 6M, 6N, 7N, 6P, 7P (b) 6D, 7D, 6E, 7E, 6F, 6G, 7G, 6H, 7H (c) 1D, 2D, 1E, 2E, 2F, 1G, 2G, 1H, 2H (d) 1K, 2K, 1L, 2L, 2M, 1N, 2N, 1P, 2P	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b, c, d).
4F	$\overline{G}$	Input	Asynchronous Output Enable Input: Low — enables output buffers (DQx pins). High — DQx pins are high impedance.
4K	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$ and $\overline{LBO}$.
3R	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst counter (68K/PowerPC). High — interleaved burst counter (486/i960/Pentium).
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 2R, 6R, 3T, 4T, 5T	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
4N, 4P	SA1, SA0	Input	Synchronous Address Inputs: These pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
5L, 5G, 3G, 3L (a) (b) (c) (d)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: "x" refers to the byte being written (byte a, b, c, d). $\overline{SGW}$ overrides $\overline{SBx}$.
4E	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high — blocks $\overline{ADSP}$ or deselects chip when $\overline{ADSC}$ is asserted.
2B	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
6B	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
4H	$\overline{SGW}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the $\overline{SBx}$ and $\overline{SW}$ signals. If only byte write signals $\overline{SBx}$ are being used, tie this pin high.
4M	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{SBx}$ pins. If only byte write signals $\overline{SBx}$ are being used, tie this pin low.
4C, 2J, 4J, 6J, 4R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	I/O Power Supply.
3D, 5D, 3E, 5E, 3F, 5F, 3H, 5H, 3K, 5K, 3M, 5M, 3N, 5N, 3P, 5P	V_{SS}	Supply	Ground.
1B, 7B, 1C, 7C, 4D, 3J, 5J, 4L, 1R, 5R, 7R, 1T, 2T, 6T, 7T, 2U, 3U, 4U, 5U, 6U	NC	—	No Connection: There is no connection to the chip.

TQFP PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: Active low, is used to latch a new external address. Used to initiate a READ, WRITE, or chip deselect.
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: Active low, interrupts any ongoing burst and latches a new external address. Used to initiate a new READ or chip deselect (exception — chip deselect does not occur when $\overline{ADSP}$ is asserted and $\overline{SE1}$ is high).
83	$\overline{ADV}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
(a) 51, 52, 53, 56, 57, 58, 59, 62, 63 (b) 68, 69, 72, 73, 74, 75, 78, 79, 80 (c) 1, 2, 3, 6, 7, 8, 9, 12, 13 (d) 18, 19, 22, 23, 24, 25, 28, 29, 30	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b, c, d).
86	$\overline{G}$	Input	Asynchronous Output Enable Input: Low — enables output buffers (DQx pins). High — DQx pins are high impedance.
89	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$ and $\overline{LBO}$.
31	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst counter (68K/PowerPC). High — interleaved burst counter (486/i960/Pentium).
32, 33, 34, 35, 44, 45, 46, 47, 48, 49, 50, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
36, 37	SA1, SA0	Input	Synchronous Address Inputs: These pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
93, 94, 95, 96 (a) (b) (c) (d)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: "x" refers to the byte being written (byte a, b, c, d). $\overline{SGW}$ overrides $\overline{SBx}$.
98	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high — blocks $\overline{ADSP}$ or deselects chip when $\overline{ADSC}$ is asserted.
97	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
92	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
88	$\overline{SGW}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the $\overline{SBx}$ and $\overline{SW}$ signals. If only byte write signals $\overline{SBx}$ are being used, tie this pin high.
87	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{SBx}$ pins. If only byte write signals $\overline{SBx}$ are being used, tie this pin low.
15, 41, 65, 91	V_{DD}	Supply	Core Power Supply.
4, 11, 20, 27, 54, 61, 70, 77	V_{DDQ}	Supply	I/O Power Supply.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground.
14, 16, 38, 39, 42, 43, 64, 66	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE (See Notes 1 Through 5)

Next Cycle	Address Used	$\overline{SE1}$	SE2	$\overline{SE3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{G}$ [3]	DQx	Write [2, 4]
Deselect	None	1	X	X	X	0	X	X	High–Z	X
Deselect	None	0	X	1	0	X	X	X	High–Z	X
Deselect	None	0	0	X	0	X	X	X	High–Z	X
Deselect	None	X	X	1	1	0	X	X	High–Z	X
Deselect	None	X	0	X	1	0	X	X	High–Z	X
Begin Read	External	0	1	0	0	X	X	0	High–Z	X[5]
Begin Read	External	0	1	0	1	0	X	0	High–Z	READ[5]
Continue Read	Next	X	X	X	1	1	0	1	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	0	DQ	READ
Continue Read	Next	1	X	X	X	1	0	1	High–Z	READ
Continue Read	Next	1	X	X	X	1	0	0	DQ	READ
Suspend Read	Current	X	X	X	1	1	1	1	High–Z	READ
Suspend Read	Current	X	X	X	1	1	1	0	DQ	READ
Suspend Read	Current	1	X	X	X	1	1	1	High–Z	READ
Suspend Read	Current	1	X	X	X	1	1	0	DQ	READ
Begin Write	External	0	1	0	1	0	X	X	High–Z	WRITE
Continue Write	Next	X	X	X	1	1	0	X	High–Z	WRITE
Continue Write	Next	1	X	X	X	1	0	X	High–Z	WRITE
Suspend Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Suspend Write	Current	1	X	X	X	1	1	X	High–Z	WRITE

NOTES:
1. X = Don't Care. 1 = logic high. 0 = logic low.
2. Write is defined as either 1) any $\overline{SBx}$ and $\overline{SW}$ low or 2) $\overline{SGW}$ is low.
3. $\overline{G}$ is an asynchronous signal and is not sampled by the clock K. $\overline{G}$ drives the bus immediately (t_{GLQX}) following $\overline{G}$ going low.
4. On write cycles that follow read cycles, $\overline{G}$ must be negated prior to the start of the write cycle to ensure proper write data setup times. $\overline{G}$ must also remain negated at the completion of the write cycle to ensure proper write data hold times.
5. This read assumes the RAM was previously deselected.

LINEAR BURST ADDRESS TABLE ($\overline{LBO}$ = V_{SS})

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X10	X . . . X11	X . . . X00
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X00	X . . . X01	X . . . X10

INTERLEAVED BURST ADDRESS TABLE ($\overline{LBO}$ = V_{DD})

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00

WRITE TRUTH TABLE

Cycle Type	$\overline{SGW}$	$\overline{SW}$	$\overline{SBa}$	$\overline{SBb}$	$\overline{SBc}$	$\overline{SBd}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte a	H	L	L	H	H	H
Write Byte b	H	L	H	L	H	H
Write Byte c	H	L	L	H	L	H
Write Byte d	H	L	H	L	H	L
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	V_{SS} – 0.5 to + 4.6	V
I/O Supply Voltage (See Note 2)	V_{DDQ}	V_{SS} – 0.5 to V_{DD}	V
Input Voltage Relative to V_{SS} for Any Pin Except V_{DD} (See Note 2)	V_{in}, V_{out}	V_{SS} – 0.5 to V_{DD} + 0.5	V
Input Voltage (Three–State I/O) (See Note 2)	V_{IT}	V_{SS} – 0.5 to V_{DDQ} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Package Power Dissipation (See Note 3)	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to 85	°C
Storage Temperature	T_{stg}	– 55 to 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. This is a steady–state DC parameter that is in effect after the power supply has achieved its nominal operating level. Power sequencing is not necessary.
3. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

4

PACKAGE THERMAL CHARACTERISTICS — PBGA

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	38 22	°C/W	1, 2
Junction to Board (Bottom)		$R_{\theta JB}$	14	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	5	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

PACKAGE THERMAL CHARACTERISTICS — TQFP (See Note 1)

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	40 25	°C/W	2
Junction to Board (Bottom)		$R_{\theta JB}$	17	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(3.6 V ≥ V_{DD} ≥ 3.1 V, 110°C ≥ T_J ≥ 20°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.1	3.3	3.6	V
Operating Temperature	T_J	20	—	110	°C
Input Low Voltage	V_{IL}	– 0.3	—	0.7	V
Input High Voltage	V_{IH}	1.7	—	V_{DD} + 0.3	V
Input High Voltage I/O Pins	V_{IH2}	1.7	—	V_{DDQ} + 0.3	V
I/O Supply Voltage	V_{DDQ}	2.375	2.5	V_{DD}	V

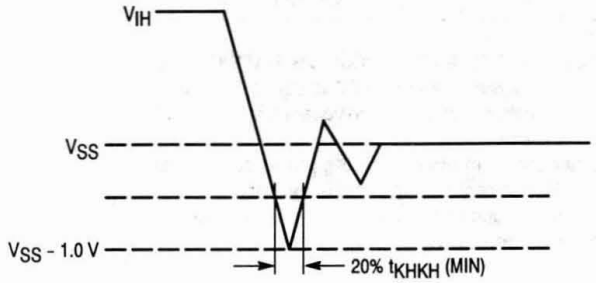


Figure 1. Undershoot Voltage

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input Leakage Current (0 V ≤ V_{in} ≤ V_{DD})	$I_{lkg(I)}$	—	—	± 1	µA	
Output Leakage Current (0 V ≤ V_{in} ≤ V_{DDQ})	$I_{lkg(O)}$	—	—	± 1	µA	
AC Supply Current (Device Selected, All Outputs Open, Cycle Time = t_{KHKH} Min) Includes V_{DD} and V_{DDQ} — MCM69F737–7.5 / MCM69F737–8 / MCM69F737–8.5	I_{DDA}	—	—	350 / 325 / 300	mA	1, 2, 3
CMOS Standby Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH})	I_{SB1}	—	—	190	mA	1, 2, 3, 4
Clock Running Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}, All Other Inputs Held to Static CMOS Levels V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{DD} – 0.2 V)	I_{SB2}	—	—	85	mA	4
Output Low Voltage (I_{OL} = 2 mA) (See Figure 4)	V_{OL}	—	—	0.7	V	
Output High Voltage (I_{OL} = – 2 mA) (See Figure 4)	V_{OH}	1.7	—	—	V	
Output Low Voltage (I_{OL} = 2 mA) V_{DDQ} = 3.3 V	V_{OL2}	—	—	0.4	V	
Output High Voltage (I_{OL} = – 2 mA) V_{DDQ} = 3.3 V	V_{OH2}	2.4	—	—	V	
Desk Top Suspend Current (Selected, All Inputs ≤ 0.2 V, Freq. = Max, V_{DD} = Max, $\overline{ADSP}$ and $\overline{ADSC}$ = Logic High, Outputs Disabled)	I_{DS1}	—	—	TBD	mA	
Desk Top Idle Current (Selected, All Inputs ≤ 0.2 V, Freq. = 0, V_{DD} = Max, $\overline{ADSP}$ and $\overline{ADSC}$ = Logic High, Outputs Disabled)	I_{DS1A}	—	—	TBD	mA	
Desk Top Standby Current (Deselected, All Inputs ≤ 0.2 V, Freq. = 0, V_{DDQ} = Max, Outputs Disabled)	I_{DS2}	—	—	TBD	mA	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing.
2. All addresses transition simultaneously low (LSB) then high (MSB).
3. Data states are all zero.
4. Device is deselected as defined by the Truth Table.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, 110°C ≥ T_J ≥ 20°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	4	5	pF
Input/Output Capacitance	$C_{I/O}$	—	7	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(3.6 V ≥ V_{DD} ≥ 3.1 V, 110°C ≥ T_J ≥ 20°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.25 V
Input Pulse Levels ..... 0 to 2.5 V
Input Slew Rate (See Note 1) ..... 1.0 V/ns

Output Timing Reference Level ..... 1.25 V
Output Load ..... See Figure 2 Unless Otherwise Noted
Output Rise/Fall Times (max) ..... 1.8 ns

READ/WRITE CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM69F737–7.5 117 MHz		MCM69F737–8 100 MHz		MCM69F737–8.5 90 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	8.5	—	10	—	11	—	ns	
Clock High Pulse Width	t_{KHKL}	3	—	4	—	4.5	—	ns	
Clock Low Pulse Width	t_{KLKH}	3	—	4	—	4.5	—	ns	
Clock Access Time	t_{KHQV}	—	7.5	—	8	—	8.5	ns	3
Output Enable to Output Valid	t_{GLQV}	—	3.5	—	3.5	—	3.5	ns	3
Clock High to Output Active	t_{KHQX1}	0	—	0	—	0	—	ns	3, 4, 5, 6
Clock High to Output Change	t_{KHQX2}	2	—	2	—	2	—	ns	4, 5
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	3, 4, 5
Output Disable to Q High–Z	t_{GHQZ}	—	3.5	—	3.5	—	3.5	ns	3, 4, 5
Clock High to Q High–Z	t_{KHQZ}	2	3.5	2	3.5	2	3.5	ns	3, 4, 5, 6
Setup Times: Address	t_{ADKH}	2.0	—	2.0	—	2.0	—	ns	3
$\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$	t_{ADSKH}								
Data In	t_{DVKH}								
Write	t_{WVKH}								
Chip Enable	t_{EVKH}								
Hold Times: Address	t_{KHAX}	0.5	—	0.5	—	0.5	—	ns	3
$\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$	t_{KHADSX}								
Data In	t_{KHDX}								
Write	t_{KHWX}								
Chip Enable	t_{KHEX}								

NOTES:
1. Write is defined as either any $\overline{SBx}$ and $\overline{SW}$ low or $\overline{SGW}$ is low. Chip Enable is defined as $\overline{SE1}$ low, SE2 high, and $\overline{SE3}$ low whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. Tested per AC Test Load, Figure 2.
4. Measured at ± 200 mV from steady state.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX1} min for a given device and from device to device.

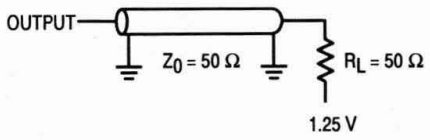
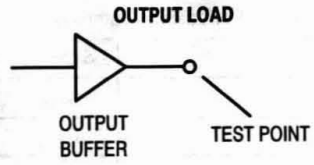
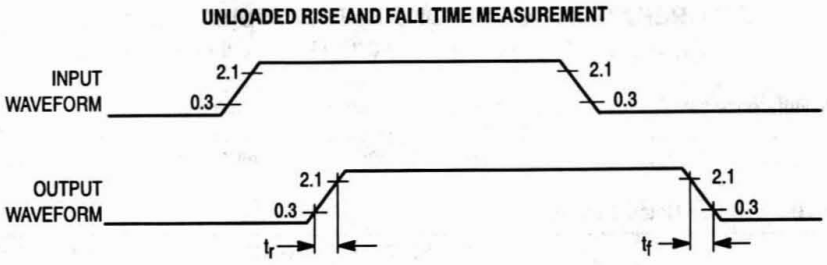


Figure 2. AC Test Load

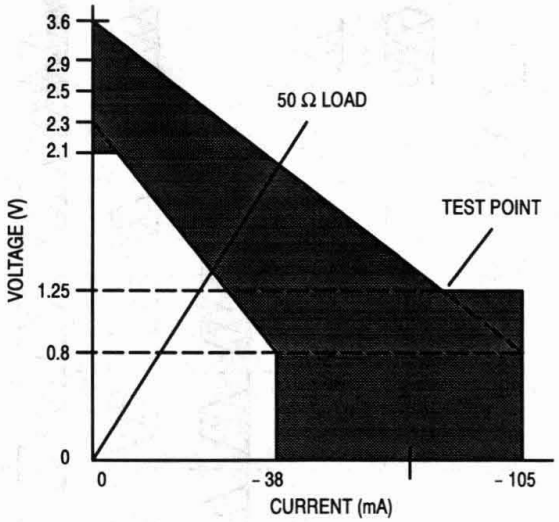




NOTES:
1. Input waveform has a slew rate of 1 V/ns.
2. Rise time is measured from 0.3 to 2.1 V unloaded.
3. Fall time is measured from 2.1 to 0.3 V unloaded.

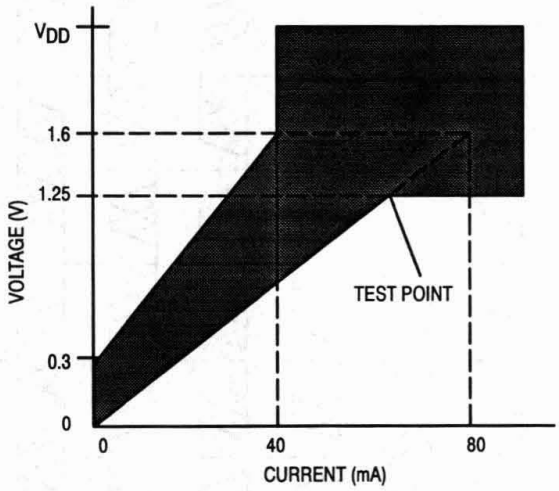
Figure 3. Unloaded Rise and Fall Time Characterization

PULL-UP		
VOLTAGE (V)	I (mA) MIN	I (mA) MAX
- 0.5	- 38	- 105
0	- 38	- 105
0.8	- 38	- 105
1.25	- 26	- 83
1.5	- 20	- 70
2.3	0	- 30
2.7	0	- 10
2.9	0	0
3.4	0	0
3.6	0	0



(a) Pull–Up

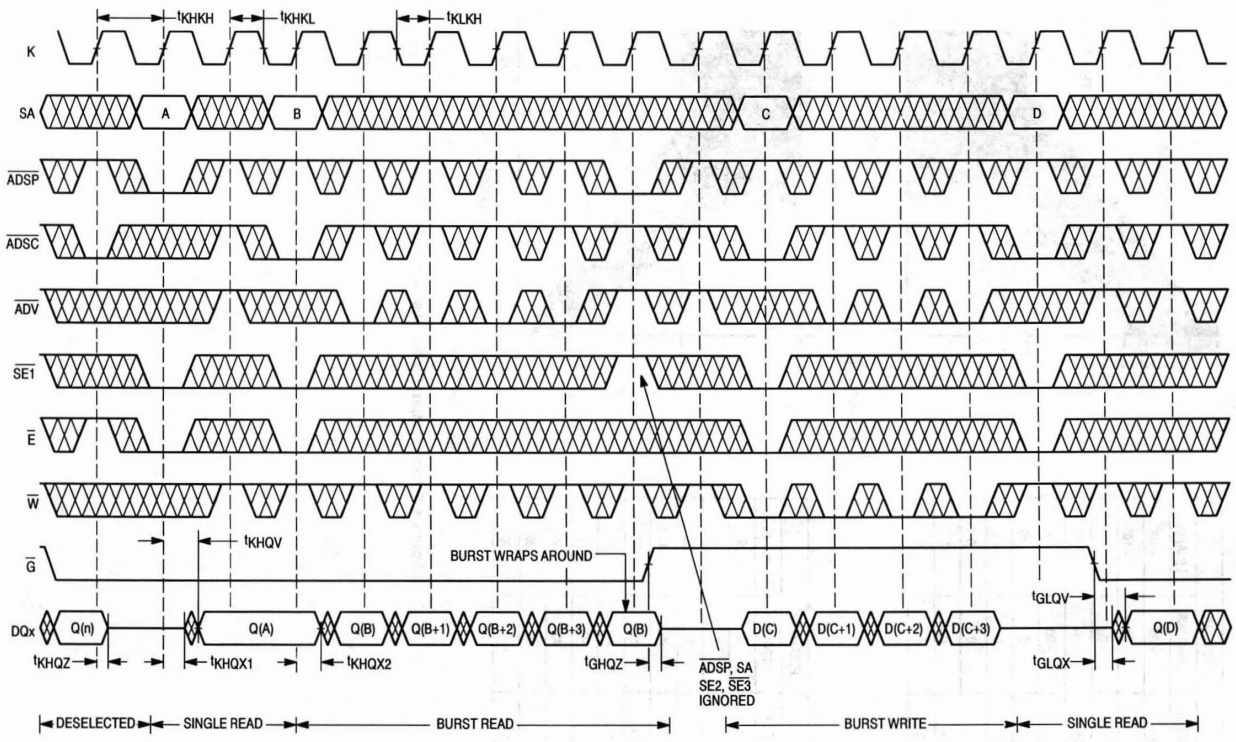
PULL-DOWN		
VOLTAGE (V)	I (mA) MIN	I (mA) MAX
- 0.5	0	0
0	0	0
0.4	10	20
0.8	20	40
1.25	31	63
1.6	40	80
2.8	40	80
3.2	40	80
3.4	40	80
3.6	46	80



(b) Pull–Down

Figure 4. Typical Output Buffer Characteristics

READ/WRITE CYCLES



NOTE: $\overline{E}$ low = SE2 high and $\overline{SE3}$ low.
$\overline{W}$ low = $\overline{SGW}$ low and/or $\overline{SW}$ and $\overline{SBx}$ low.

APPLICATION INFORMATION

STOP CLOCK OPERATION

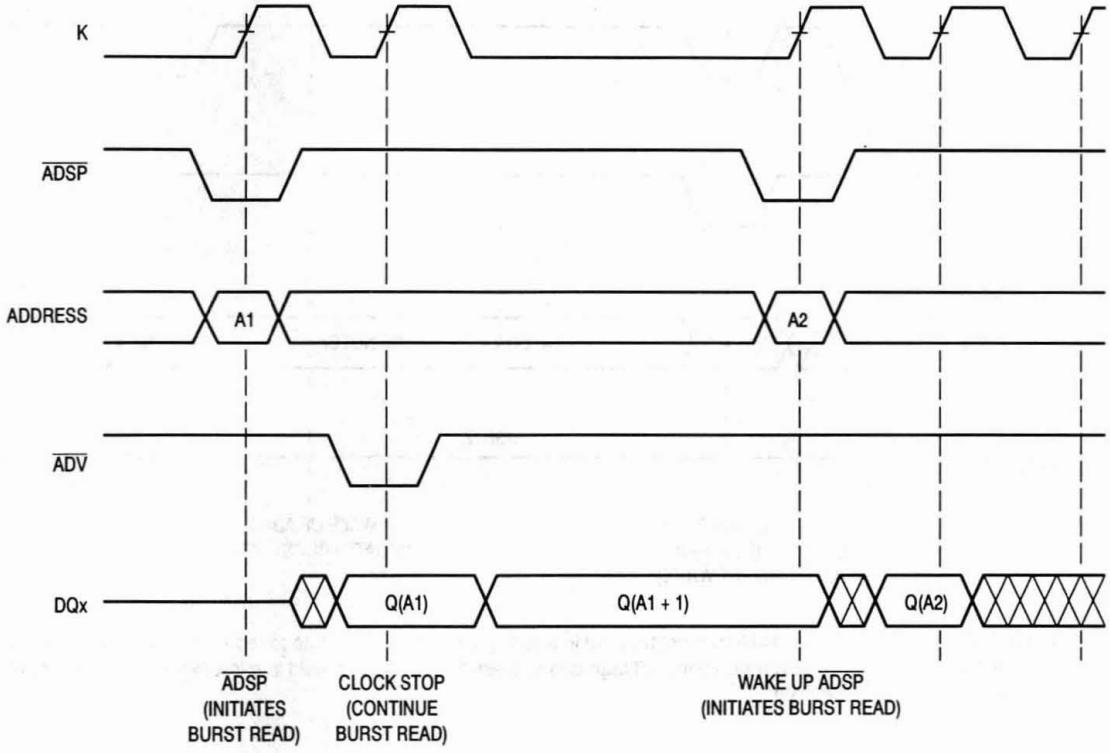
In the stop clock mode of operation, the SRAM will hold all state and data values even though the clock is not running (full static operation). The SRAM design allows the clock to start with $\overline{ADSP}$ and $\overline{ADSC}$, and stops the clock after the last write data is latched, or the last read data is driven out.

When starting and stopping the clock, the AC clock timing and parametrics must be strictly maintained. For example, clock pulse width and edge rates must be guaranteed when starting and stopping the clocks.

To achieve the lowest power operation for all three stop clock modes, stop read, stop write, and stop deselect:

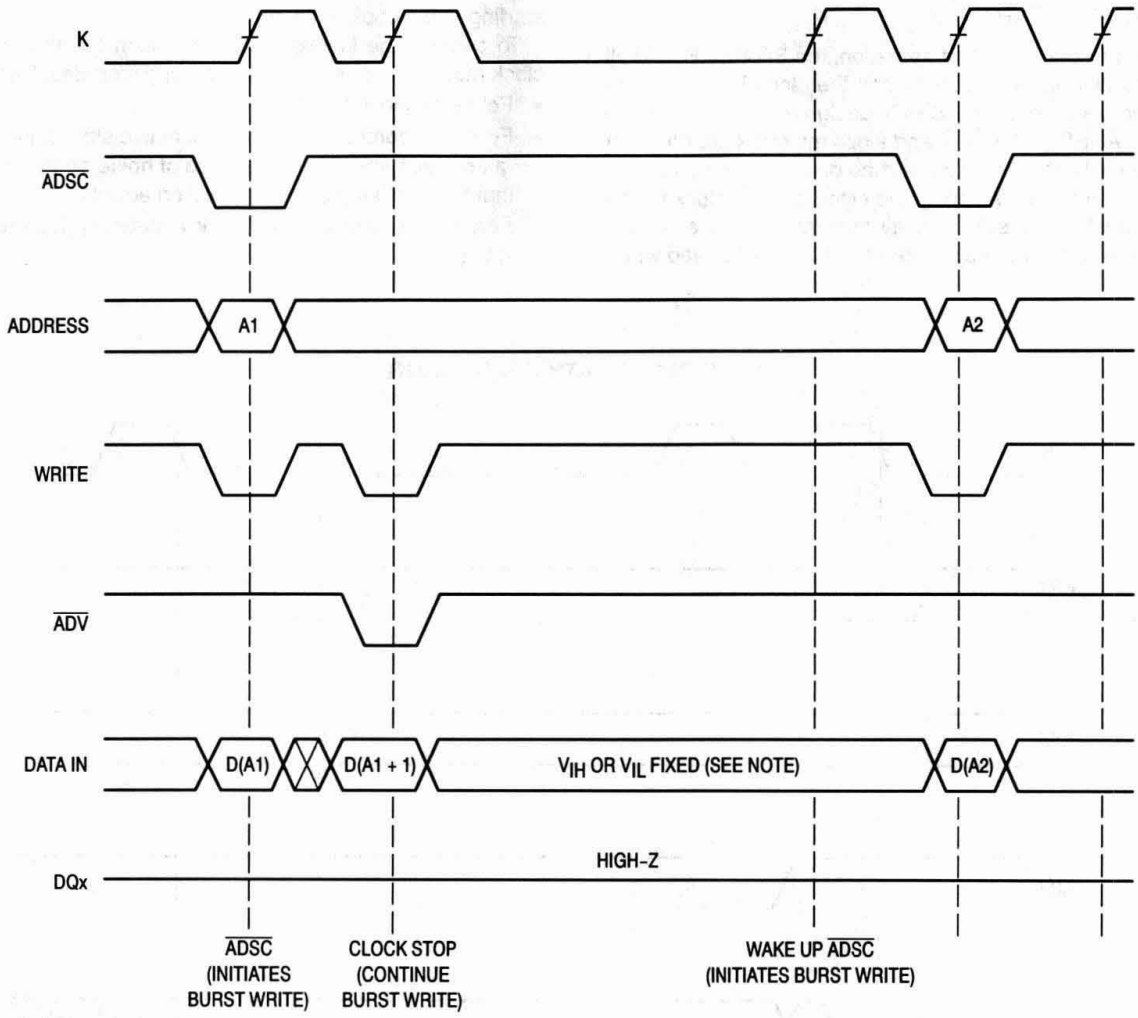
- Force the clock to a low state.
- Force the control signals to an inactive state (this guarantees any potential source of noise on the clock input will not start an unplanned on activity).
- Force the address inputs to a low state (V_{IL}), preferably < 0.2 V.

STOP CLOCK WITH READ TIMING



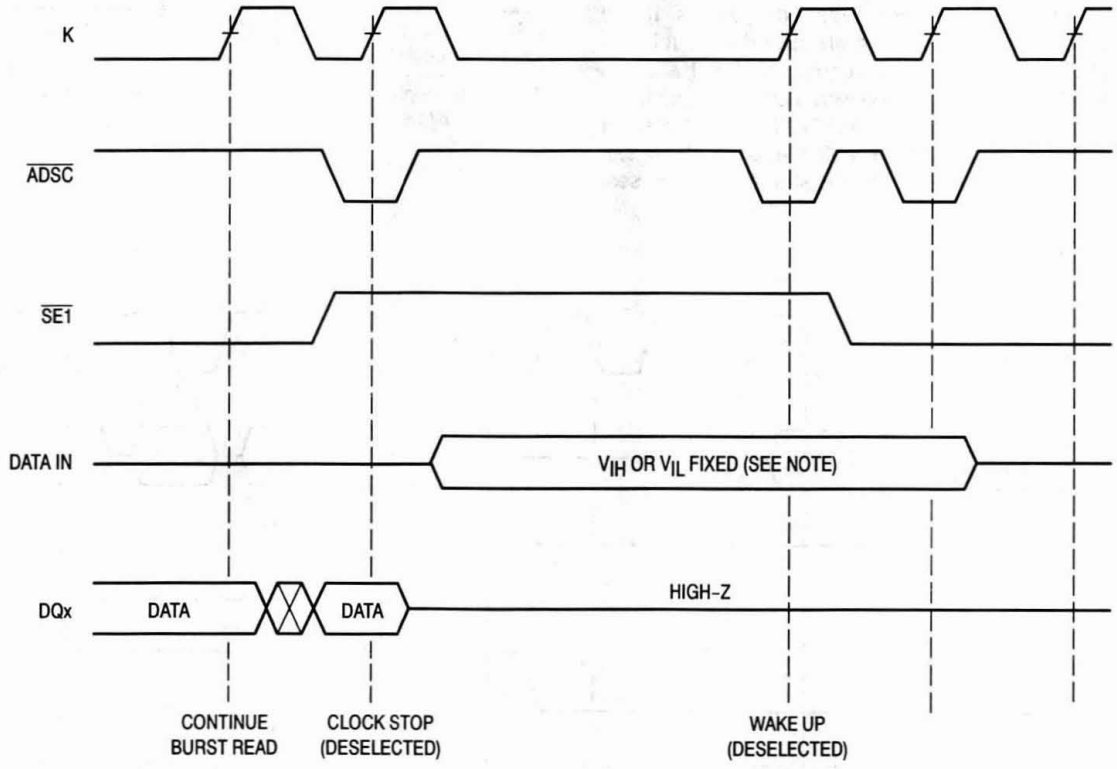
NOTE: For lowest possible power consumption during stop clock, the addresses should be driven to a low state (V_{IL}). Best results are obtained if V_{IL} < 0.2 V.

STOP CLOCK WITH WRITE TIMING



NOTE: While the clock is stopped, DATA IN must be fixed in a high (V_{IH}) or low (V_{IL}) state to reduce the DC current of the input buffers. For lowest power operation, all data and address lines should be held in a low (V_{IL}) state and control lines held in an inactive state.

STOP CLOCK WITH DESELECT OPERATION TIMING



NOTE: While the clock is stopped, DATA IN must be fixed in a high (V_{IH}) or low (V_{IL}) state to reduce the DC current of the input buffers. For lowest power operation, all data and address lines should be held in a low (V_{IL}) state and control lines held in an inactive state.

NON–BURST SYNCHRONOUS OPERATION

Although this BurstRAM has been designed for PowerPC–based and other high end MPU–based systems, these SRAMs can be used in other high speed L2 cache or memory applications that do not require the burst address feature. Most L2 caches designed with a synchronous interface can make use of the MCM69F737. The burst counter feature of the BurstRAM can be disabled, and the SRAM can be configured to act upon a continuous stream of addresses. See Figure 5.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

Non–Burst	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
Sync Non–Burst, Flow–Through SRAM	H	L	H	L	X

NOTE: Although X is specified in the table as a don't care, the pin must be tied either high or low.

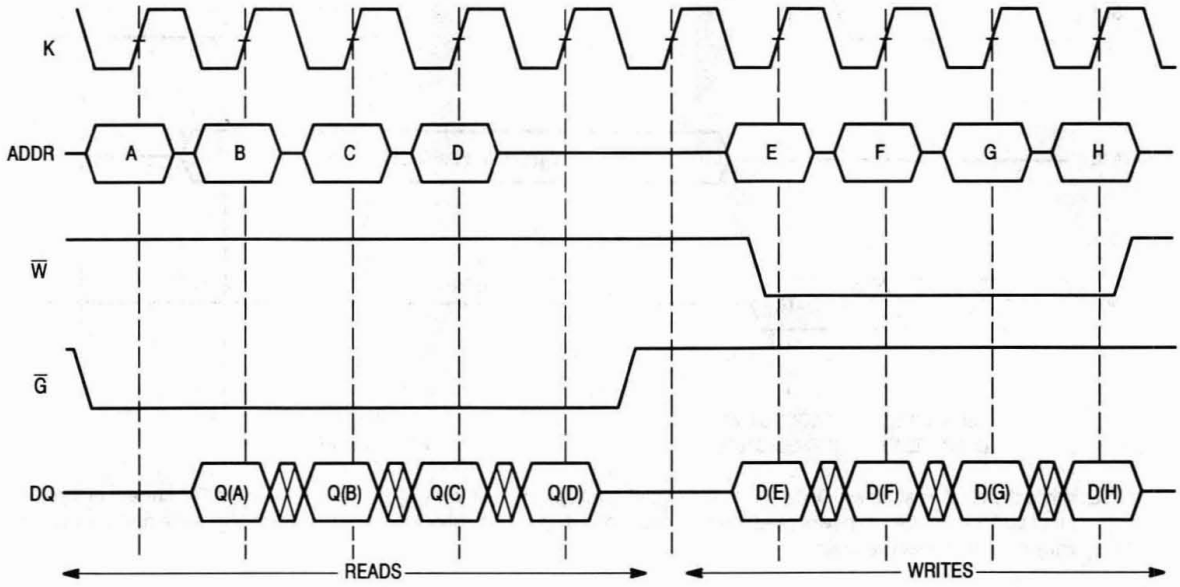


Figure 5. Configured as Non–Burst Synchronous SRAM

ORDERING INFORMATION
(Order by Full Part Number)

MCM 69F737 XX X X

- MCM: Motorola Memory Prefix
- 69F737: Part Number
- XX: Package (ZP = PBGA, TQ = TQFP)
- X: Speed (7.5 = 7.5 ns, 8 = 8 ns, 8.5 = 8.5 ns)
- X: Blank = Trays, R = Tape and Reel

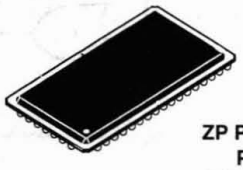
Full Part Numbers —

MCM69F737ZP7.5	MCM69F737ZP8	MCM69F737ZP8.5
MCM69F737ZP7.5R	MCM69F737ZP8R	MCM69F737ZP8.5R
MCM69F737TQ7.5	MCM69F737TQ8	MCM69F737TQ8.5
MCM69F737TQ7.5R	MCM69F737TQ8R	MCM69F737TQ8.5R

MCM69P737

Product Preview

128K x 36 Bit Pipelined BurstRAM™ Synchronous Fast Static RAM



ZP PACKAGE
PBGA
CASE 999–01

TQ PACKAGE
TQFP
CASE 983A–01

The MCM69P737 is a 4M bit synchronous fast static RAM designed to provide a burstable, high performance, secondary cache for the PowerPC™ and other high performance microprocessors. It is organized as 128K words of 36 bits each. This device integrates input registers, an output register, a 2–bit address counter, and high speed SRAM onto a single monolithic circuit for reduced parts count in cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K).

Addresses (SA), data inputs (DQx), and all control signals except output enable ($\overline{G}$) and linear burst order ($\overline{LBO}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ input pins. Subsequent burst addresses can be generated internally by the MCM69P737 (burst sequence operates in linear or interleaved mode dependent upon the state of $\overline{LBO}$) and controlled by the burst address advance ($\overline{ADV}$) input pin.

Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased timing flexibility for incoming signals.

Synchronous byte write ($\overline{SBx}$), synchronous global write ($\overline{SGW}$), and synchronous write enable ($\overline{SW}$) are provided to allow writes to either individual bytes or to all bytes. The four bytes are designated as "a", "b", "c", and "d". $\overline{SBa}$ controls DQa, $\overline{SBb}$ controls DQb, etc. Individual bytes are written if the selected byte writes $\overline{SBx}$ are asserted with $\overline{SW}$. All bytes are written if either $\overline{SGW}$ is asserted or if all $\overline{SBx}$ and $\overline{SW}$ are asserted.

For read cycles, pipelined SRAMs output data is temporarily stored by an edge–triggered output register and then released to the output buffers at the next rising edge of clock (K).

The MCM69P737 operates from a 3.3 V core power supply and all outputs operate on a 2.5 V power supply. All inputs and outputs are JEDEC standard JESD8–5 compatible.

- MCM69P737 Speed Options

Speed	t_{KHKH}	Pipelined t_{KHQV}	Setup	Hold	I_{DD}	Pkg
166 MHz	6 ns	3.5 ns	1.5 ns	0.5 ns	425 mA	PBGA
150 MHz	6.7 ns	3.8 ns	1.5 ns	0.5 ns	400 mA	PBGA
133 MHz	7.5 ns	4 ns	1.5 ns	0.5 ns	375 mA	PBGA/TQFP

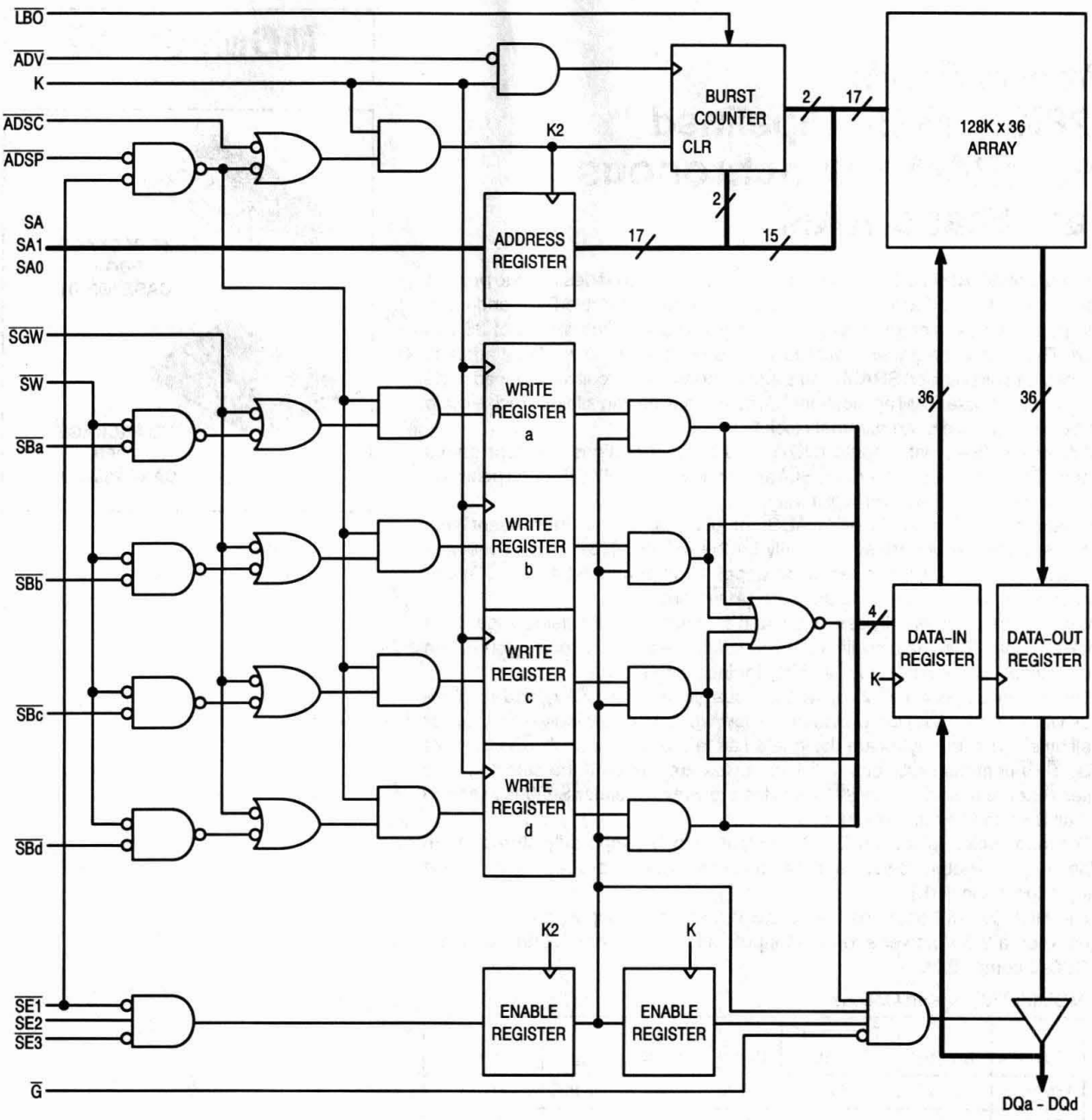
- 3.3 V + 10%, – 5% Core Power Supply, 2.5 V I/O Supply
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Selectable Burst Sequencing Order (Linear/Interleaved)
- Single–Cycle Deselect Timing
- Internally Self–Timed Write Cycle
- Byte Write and Global Write Control
- JEDEC Standard 119 Pin PBGA and 100 Pin TQFP Packages

BurstRAM is a trademark of Motorola, Inc.
The PowerPC name is a trademark of IBM Corp., used under license therefrom.

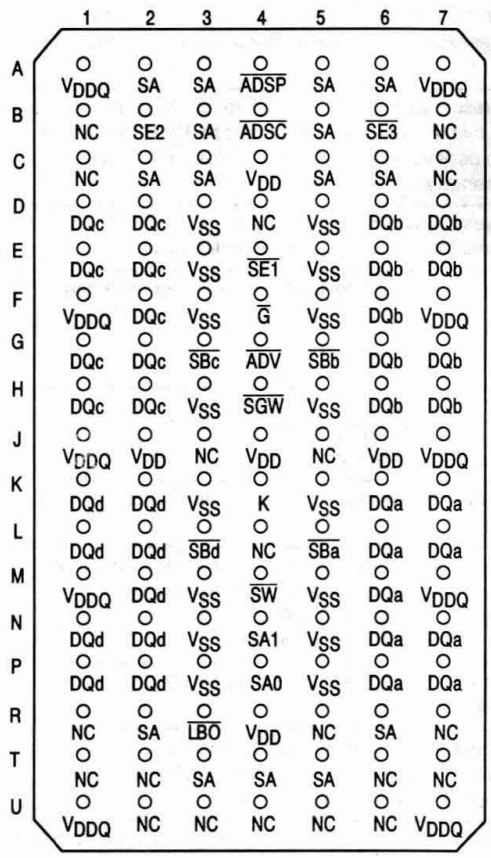
This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

REV 2
4/9/97

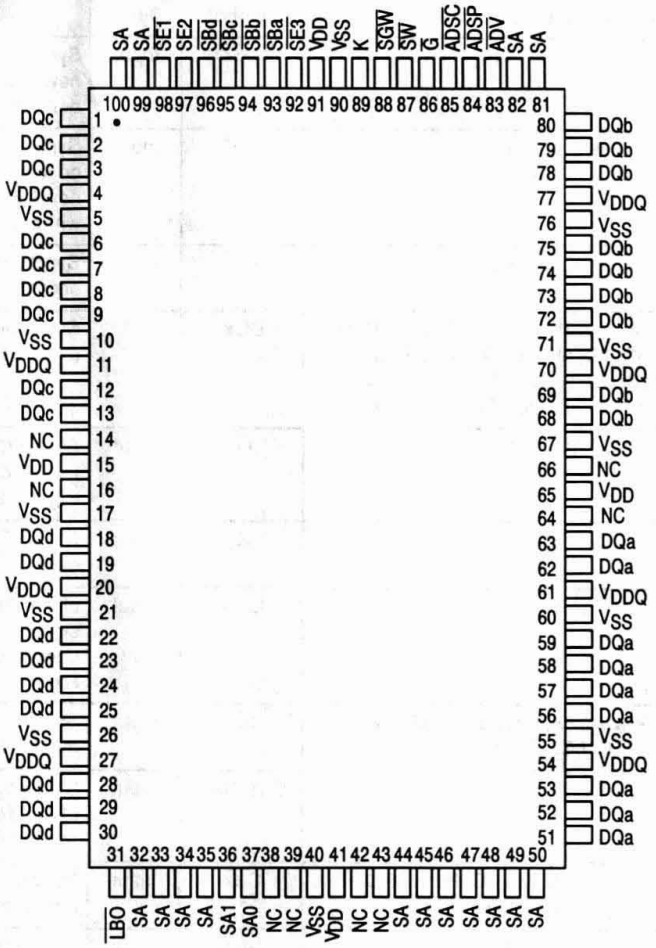
FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENTS


1 2 3 4 5 6 7
A VDDQ SA SA ADSP SA SA VDDQ
B NC SE2 SA ADSC SA SE3 NC
C NC SA SA VDD SA SA NC
D DQc DQc VSS NC VSS DQb DQb
E DQc DQc VSS SE1 VSS DQb DQb
F VDDQ DQc VSS G VSS DQb VDDQ
G DQc DQc SBc ADV SBb DQb DQb
H DQc DQc VSS SGW VSS DQb DQb
J VDDQ VDD NC VDD NC VDD VDDQ
K DQd DQd VSS K VSS DQa DQa
L DQd DQd SBd NC SBa DQa DQa
M VDDQ DQd VSS SW VSS DQa VDDQ
N DQd DQd VSS SA1 VSS DQa DQa
P DQd DQd VSS SA0 VSS DQa DQa
R NC SA LBO VDD NC SA NC
T NC NC SA SA SA NC NC
U VDDQ NC NC NC NC NC VDDQ

TOP VIEW 119 BUMP PBGA



TOP VIEW 100 PIN TQFP

Not to Scale

4

PBGA PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
4B	$\overline{ADSC}$	Input	Synchronous Address Status Controller: Active low, is used to latch a new external address. Used to initiate a READ, WRITE, or chip deselect.
4A	$\overline{ADSP}$	Input	Synchronous Address Status Processor: Active low, interrupts any ongoing burst and latches a new external address. Used to initiate a new READ or chip deselect (exception — chip deselect does not occur when $\overline{ADSP}$ is asserted and $\overline{SE1}$ is high).
4G	$\overline{ADV}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
(a) 6K, 7K, 6L, 7L, 6M, 6N, 7N, 6P, 7P (b) 6D, 7D, 6E, 7E, 6F, 6G, 7G, 6H, 7H (c) 1D, 2D, 1E, 2E, 2F, 1G, 2G, 1H, 2H (d) 1K, 2K, 1L, 2L, 2M, 1N, 2N, 1P, 2P	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b, c, d).
4F	$\overline{G}$	Input	Asynchronous Output Enable Input: Low — enables output buffers (DQx pins). High — DQx pins are high impedance.
4K	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$ and $\overline{LBO}$.
3R	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst counter (68K/PowerPC). High — interleaved burst counter (486/i960/Pentium).
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 2R, 6R, 3T, 4T, 5T	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
4N, 4P	SA1, SA0	Input	Synchronous Address Inputs: These pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
5L, 5G, 3G, 3L (a) (b) (c) (d)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: "x" refers to the byte being written (byte a, b, c, d). $\overline{SGW}$ overrides $\overline{SBx}$.
4E	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high — blocks $\overline{ADSP}$ or deselects chip when $\overline{ADSC}$ is asserted.
2B	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
6B	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
4H	$\overline{SGW}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the $\overline{SBx}$ and $\overline{SW}$ signals. If only byte write signals $\overline{SBx}$ are being used, tie this pin high.
4M	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{SBx}$ pins. If only byte write signals $\overline{SBx}$ are being used, tie this pin low.
4C, 2J, 4J, 6J, 4R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	I/O Power Supply.
3D, 5D, 3E, 5E, 3F, 5F, 3H, 5H, 3K, 5K, 3M, 5M, 3N, 5N, 3P, 5P	V_{SS}	Supply	Ground.
1B, 7B, 1C, 7C, 4D, 3J, 5J, 4L, 1R, 5R, 7R, 1T, 2T, 6T, 7T, 2U, 3U, 4U, 5U, 6U	NC	—	No Connection: There is no connection to the chip.

TQFP PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: Active low, is used to latch a new external address. Used to initiate a READ, WRITE, or chip deselect.
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: Active low, interrupts any ongoing burst and latches a new external address. Used to initiate a new READ or chip deselect (exception — chip deselect does not occur when $\overline{ADSP}$ is asserted and $\overline{SE1}$ is high).
83	$\overline{ADV}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
(a) 51, 52, 53, 56, 57, 58, 59, 62, 63 (b) 68, 69, 72, 73, 74, 75, 78, 79, 80 (c) 1, 2, 3, 6, 7, 8, 9, 12, 13 (d) 18, 19, 22, 23, 24, 25, 28, 29, 30	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b, c, d).
86	$\overline{G}$	Input	Asynchronous Output Enable Input: Low — enables output buffers (DQx pins). High — DQx pins are high impedance.
89	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$ and $\overline{LBO}$.
31	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst counter (68K/PowerPC). High — interleaved burst counter (486/i960/Pentium).
32, 33, 34, 35, 44, 45, 46, 47, 48, 49, 50, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
36, 37	SA1, SA0	Input	Synchronous Address Inputs: these pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
93, 94, 95, 96 (a) (b) (c) (d)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: "x" refers to the byte being written (byte a, b, c, d). $\overline{SGW}$ overrides $\overline{SBx}$.
98	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high — blocks $\overline{ADSP}$ or deselects chip when $\overline{ADSC}$ is asserted.
97	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
92	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
88	$\overline{SGW}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the $\overline{SBx}$ and $\overline{SW}$ signals. If only byte write signals $\overline{SBx}$ are being used, tie this pin high.
87	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{SBx}$ pins. If only byte write signals $\overline{SBx}$ are being used, tie this pin low.
15, 41, 65, 91	V_{DD}	Supply	Core Power Supply.
4, 11, 20, 27, 54, 61, 70, 77	V_{DDQ}	Supply	I/O Power Supply.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground.
14, 16, 38, 39, 42, 43, 64, 66	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE (See Notes 1 Through 5)

Next Cycle	Address Used	$\overline{SE1}$	SE2	$\overline{SE3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{G}$ [3]	DQx	Write [2, 4]
Deselect	None	1	X	X	X	0	X	X	High–Z	X
Deselect	None	0	X	1	0	X	X	X	High–Z	X
Deselect	None	0	0	X	0	X	X	X	High–Z	X
Deselect	None	X	X	1	1	0	X	X	High–Z	X
Deselect	None	X	0	X	1	0	X	X	High–Z	X
Begin Read	External	0	1	0	0	X	X	X	High–Z	X[5]
Begin Read	External	0	1	0	1	0	X	X	High–Z	READ[5]
Continue Read	Next	X	X	X	1	1	0	1	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	0	DQ	READ
Continue Read	Next	1	X	X	X	1	0	1	High–Z	READ
Continue Read	Next	1	X	X	X	1	0	0	DQ	READ
Suspend Read	Current	X	X	X	1	1	1	1	High–Z	READ
Suspend Read	Current	X	X	X	1	1	1	0	DQ	READ
Suspend Read	Current	1	X	X	X	1	1	1	High–Z	READ
Suspend Read	Current	1	X	X	X	1	1	0	DQ	READ
Begin Write	External	0	1	0	1	0	X	X	High–Z	WRITE
Continue Write	Next	X	X	X	1	1	0	X	High–Z	WRITE
Continue Write	Next	1	X	X	X	1	0	X	High–Z	WRITE
Suspend Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Suspend Write	Current	1	X	X	X	1	1	X	High–Z	WRITE

NOTES:
1. X = Don't Care. 1 = logic high. 0 = logic low.
2. Write is defined as either 1) any $\overline{SBx}$ and $\overline{SW}$ low or 2) $\overline{SGW}$ is low.
3. $\overline{G}$ is an asynchronous signal and is not sampled by the clock K. $\overline{G}$ drives the bus immediately (t_{GLQX}) following $\overline{G}$ going low.
4. On write cycles that follow read cycles, $\overline{G}$ must be negated prior to the start of the write cycle to ensure proper write data setup times. $\overline{G}$ must also remain negated at the completion of the write cycle to ensure proper write data hold times.
5. This read assumes the RAM was previously deselected.

LINEAR BURST ADDRESS TABLE ($\overline{LBO} = V_{SS}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X10	X . . . X11	X . . . X00
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X00	X . . . X01	X . . . X10

INTERLEAVED BURST ADDRESS TABLE ($\overline{LBO} = V_{DD}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00

WRITE TRUTH TABLE

Cycle Type	$\overline{SGW}$	$\overline{SW}$	$\overline{SBa}$	$\overline{SBb}$	$\overline{SBc}$	$\overline{SBd}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte a	H	L	L	H	H	H
Write Byte b	H	L	H	L	H	H
Write Byte c	H	L	L	H	L	H
Write Byte d	H	L	H	L	H	L
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	V_{SS} – 0.5 to + 4.6	V
I/O Supply Voltage (See Note 2)	V_{DDQ}	V_{SS} – 0.5 to V_{DD}	V
Input Voltage Relative to V_{SS} for Any Pin Except V_{DD} (See Note 2)	V_{in}, V_{out}	V_{SS} – 0.5 to V_{DD} + 0.5	V
Input Voltage (Three–State I/O) (See Note 2)	V_{IT}	V_{SS} – 0.5 to V_{DDQ} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Package Power Dissipation (See Note 3)	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to 85	°C
Storage Temperature	T_{stg}	– 55 to 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. This is a steady–state DC parameter that is in effect after the power supply has achieved its nominal operating level. Power sequencing is not necessary.
3. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

4

PACKAGE THERMAL CHARACTERISTICS — PBGA

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	38 22	°C/W	1, 2
Junction to Board (Bottom)		$R_{\theta JB}$	14	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	5	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

PACKAGE THERMAL CHARACTERISTICS — TQFP (See Note 1)

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	40 25	°C/W	2
Junction to Board (Bottom)		$R_{\theta JB}$	17	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(3.6 V ≥ V_{DD} ≥ 3.1 V, 110°C ≥ T_J ≥ 20°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.1	3.3	3.6	V
Operating Temperature	T_J	20	—	110	°C
Input Low Voltage	V_{IL}	– 0.3	—	0.8	V
Input High Voltage	V_{IH}	1.7	—	V_{DD} + 0.3	V
Input High Voltage I/O Pins	V_{IH2}	1.7	—	V_{DDQ} + 0.3	V
I/O Supply Voltage	V_{DDQ}	2.375	2.5	V_{DD}	V

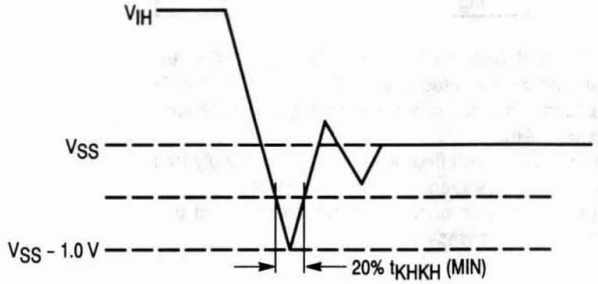


Figure 1. Undershoot Voltage

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input Leakage Current (0 V ≤ V_{in} ≤ V_{DD})	$I_{lkg(I)}$	—	—	± 1	µA	
Output Leakage Current (0 V ≤ V_{in} ≤ V_{DDQ})	$I_{lkg(O)}$	—	—	± 1	µA	
AC Supply Current (Device Selected, All Outputs Open, Cycle Time ≥ t_{KHKH} Min) Includes V_{DD} and V_{DDQ} — MCM69P737–3.5 / MCM69P737–3.8 / MCM69P737–4	I_{DDA}	—	—	425 / 400 / 375	mA	1, 2, 3
CMOS Standby Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH})	I_{SB1}	—	—	190	mA	1, 2, 3, 4
Clock Running Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}, All Other Inputs Held to Static CMOS Levels V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{DD} – 0.2 V)	I_{SB2}	—	—	85	mA	4
Output Low Voltage (I_{OL} = 2 mA) (See Figure 5)	V_{OL}	—	—	0.7	V	
Output High Voltage (I_{OL} = – 2 mA) (See Figure 5)	V_{OH}	1.7	—	—	V	
Output Low Voltage (I_{OL} = 2 mA) V_{DDQ} = 3.3 V	V_{OL2}	—	—	0.4	V	
Output High Voltage (I_{OL} = – 2 mA) V_{DDQ} = 3.3 V	V_{OH2}	2.4	—	—	V	
Desk Top Suspend Current (Selected, All Inputs ≤ 0.2 V, Freq. = Max, V_{DD} = Max, $\overline{ADSP}$ and $\overline{ADSC}$ = Logic High, Outputs Disabled)	I_{DS1}	—	—	TBD	mA	
Desk Top Idle Current (Selected, All Inputs ≤ 0.2 V, Freq. = 0, V_{DD} = Max, $\overline{ADSP}$ and $\overline{ADSC}$ = Logic High, Outputs Disabled)	I_{DS1A}	—	—	TBD	mA	
Desk Top Standby Current (Deselected, All Inputs ≤ 0.2 V, Freq. = 0, V_{DDQ} = Max, Outputs Disabled)	I_{DS2}	—	—	TBD	mA	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing.
2. All addresses transition simultaneously low (LSB) then high (MSB).
3. Data states are all zero.
4. Device is deselected as defined by the Truth Table.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, 110°C ≥ T_J ≥ 20°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	4	5	pF
Input/Output Capacitance	$C_{I/O}$	—	7	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(3.6 V ≥ V_{DD} ≥ 3.1 V, 110°C ≥ T_J ≥ 20°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.25 V
Input Pulse Levels ..... 0 to 2.5 V
Input Slew Rate (See Note 1) ..... 1.0 V/ns
Output Timing Reference Level ..... 1.25 V
Output Load ..... See Figure 2 Unless Otherwise Noted
Output Rise/Fall Times (max) ..... 1.8 ns

READ/WRITE CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM69P737–3.5 166 MHz		MCM69P737–3.8 150 MHz		MCM69P737–4 133 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	6	—	6.7	—	7.5	—	ns	
Clock High Pulse Width	t_{KHKL}	2.4	—	2.6	—	2.8	—	ns	3, 6
Clock Low Pulse Width	t_{KLKH}	2.4	—	2.6	—	2.8	—	ns	3, 6
Clock Low	t_{KL}	1.5	—	1.7	—	1.9	—	ns	3, 6
Clock High	t_{KH}	1.3	—	1.5	—	1.7	—	ns	3, 6
Clock Access Time	t_{KHQV}	—	3.5	—	3.8	—	4	ns	3
Output Enable to Output Valid	t_{GLQV}	—	3.5	—	3.5	—	3.8	ns	3
Clock High to Output Active	t_{KHQX1}	0	—	0	—	0	—	ns	3, 4, 5
Clock High to Output Change	t_{KHQX2}	1.5	—	1.5	—	1.5	—	ns	3, 5
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	3, 4, 5
Output Disable to Q High–Z	t_{GHQZ}	—	3.5	—	3.5	—	3.8	ns	3, 4, 5
Clock High to Q High–Z	t_{KHQZ}	1.5	6	1.5	6.7	1.5	7.5	ns	3, 4, 5
Setup Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	t_{ADKH} t_{ADSKH} t_{DVKH} t_{WVKH} t_{EVKH}	1.5	—	1.5	—	1.5	—	ns	3
Hold Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	t_{KHAX} t_{KHADSX} t_{KHDX} t_{KHWX} t_{KHEX}	0.5	—	0.5	—	0.5	—	ns	3

NOTES:

1. Write is defined as either any $\overline{SBx}$ and $\overline{SW}$ low or $\overline{SGW}$ is low. Chip Enable is defined as $\overline{SE1}$ low, SE2 high, and $\overline{SE3}$ low whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. Tested per AC Test Load, Figure 2.
4. Measured at ± 200 mV from steady state.
5. This parameter is sampled and not 100% tested.
6. In order to reduce test correlation issues and to reduce the effects of application specific input edge rate variations on correlation between data sheet parameters and actual system performance, FSRAM AC parametric specifications are always specified at $V_{DDQ}/2$. In some design exercises, it is desirable to evaluate timing using other reference levels. Since the maximum test input edge rate is known and is given in the AC Test Conditions section of the data sheet as 1 V/ns, one can easily interpolate timing values to other reference levels. Figure 3 shows interpolation to DC V_{IH} and DC V_{IL} levels.

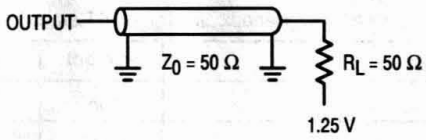


Figure 2. AC Test Load

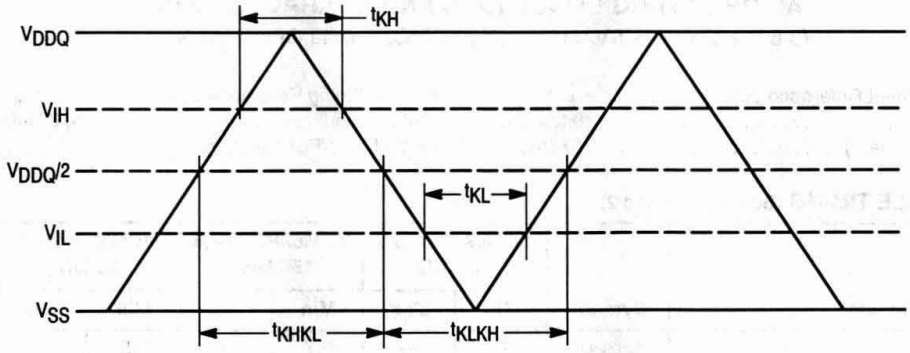


Figure 3. Interpolation to DC V_{IH} and DC V_{IL} Levels

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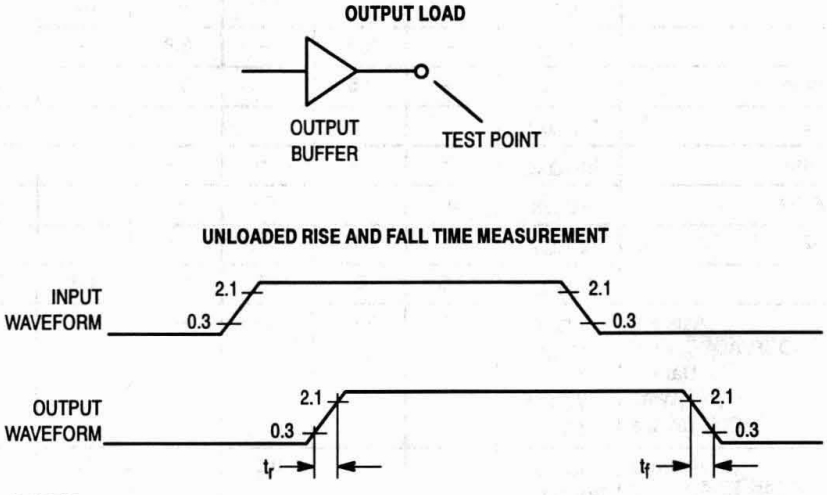
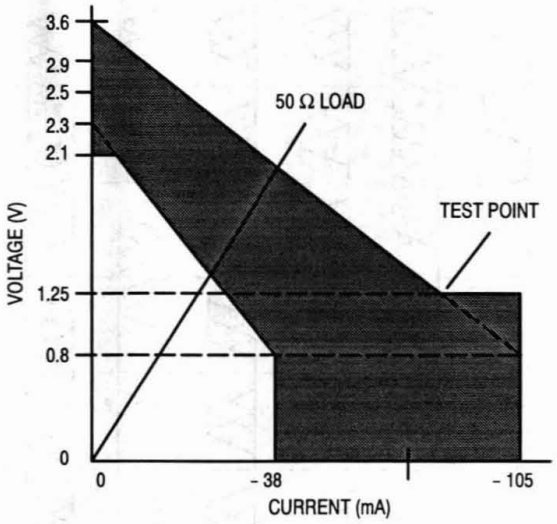


NOTES:
1. Input waveform has a slew rate of 1 V/ns.
2. Rise time is measured from 0.3 to 2.1 V unloaded.
3. Fall time is measured from 2.1 to 0.3 V unloaded.

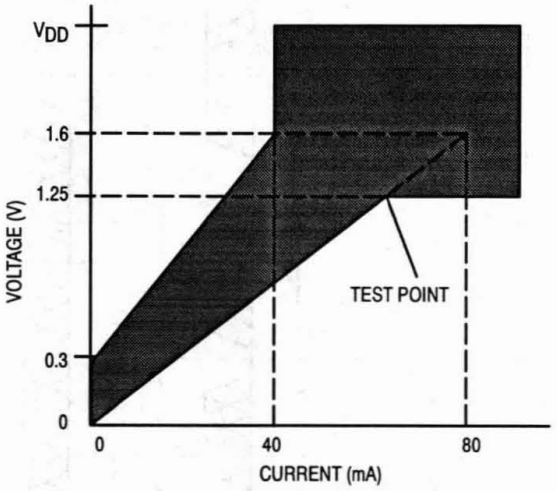
Figure 4. Unloaded Rise and Fall Time Characterization

PULL-UP		
VOLTAGE (V)	I (mA) MIN	I (mA) MAX
- 0.5	- 38	- 105
0	- 38	- 105
0.8	- 38	- 105
1.25	- 26	- 83
1.5	- 20	- 70
2.3	0	- 30
2.7	0	- 10
2.9	0	0
3.4	0	0
3.6	0	0



(a) Pull–Up

PULL-DOWN		
VOLTAGE (V)	I (mA) MIN	I (mA) MAX
- 0.5	0	0
0	0	0
0.4	10	20
0.8	20	40
1.25	31	63
1.6	40	80
2.8	40	80
3.2	40	80
3.4	40	80
3.6	46	80



(b) Pull–Down

Figure 5. Typical Output Buffer Characteristics

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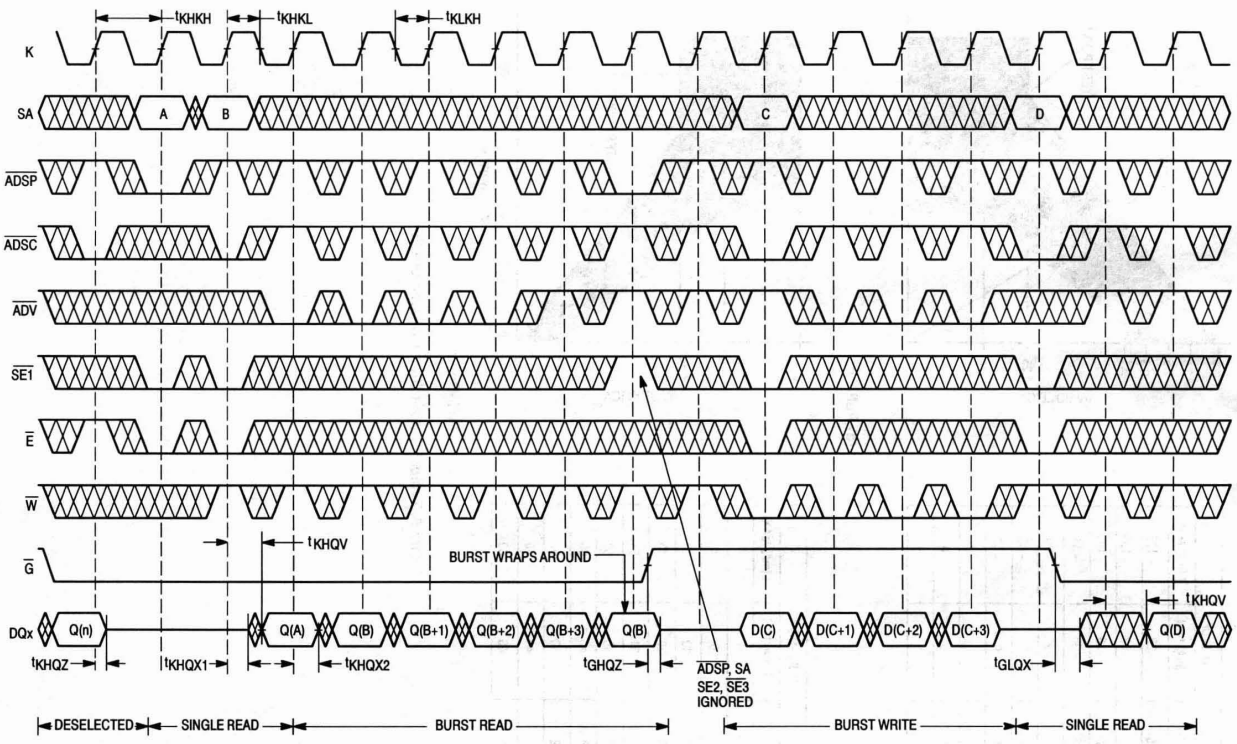
READ/WRITE CYCLES



NOTE: $\overline{E}$ low = SE2 high and $\overline{SE3}$ low.
$\overline{W}$ low = $\overline{SGW}$ low and/or $\overline{SW}$ and $\overline{SBx}$ low.

STOP CLOCK OPERATION

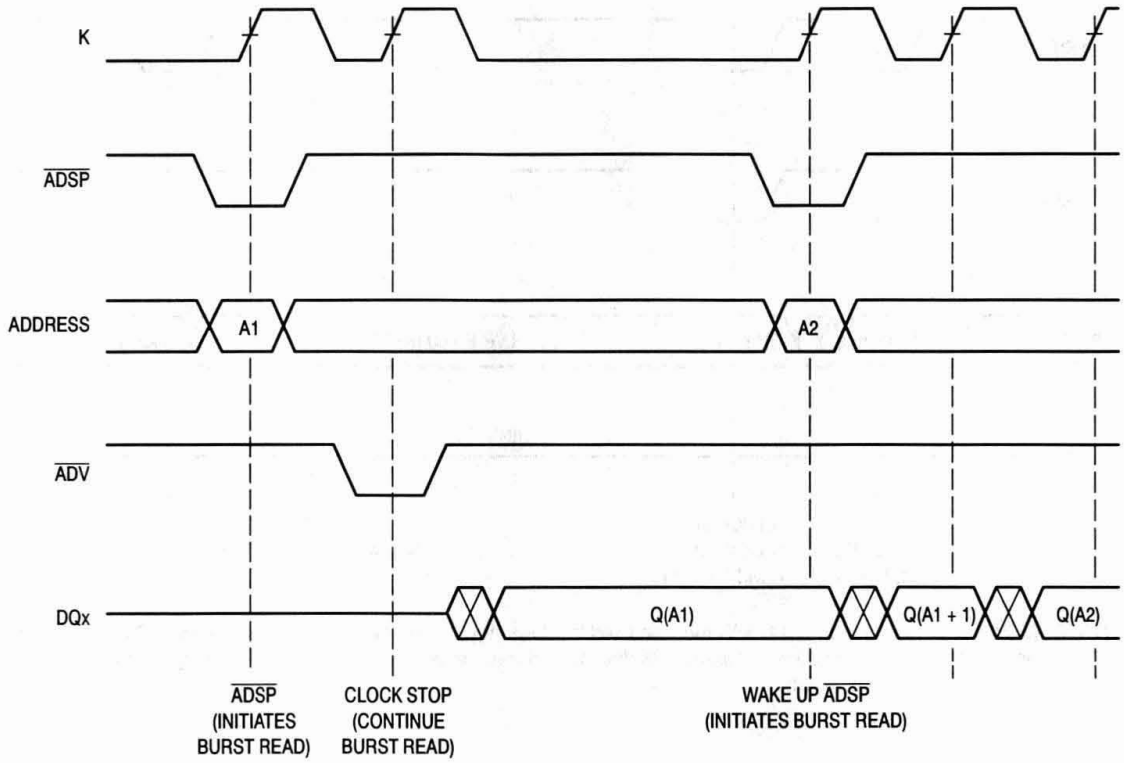
In the stop clock mode of operation, the SRAM will hold all state and data values even though the clock is not running (full static operation). The SRAM design allows the clock to start with $\overline{ADSP}$ and $\overline{ADSC}$, and stops the clock after the last write data is latched, or the last read data is driven out.

When starting and stopping the clock, the AC clock timing and parametrics must be strictly maintained. For example, clock pulse width and edge rates must be guaranteed when starting and stopping the clocks.

To achieve the lowest power operation for all three stop clock modes, stop read, stop write, and stop deselect:

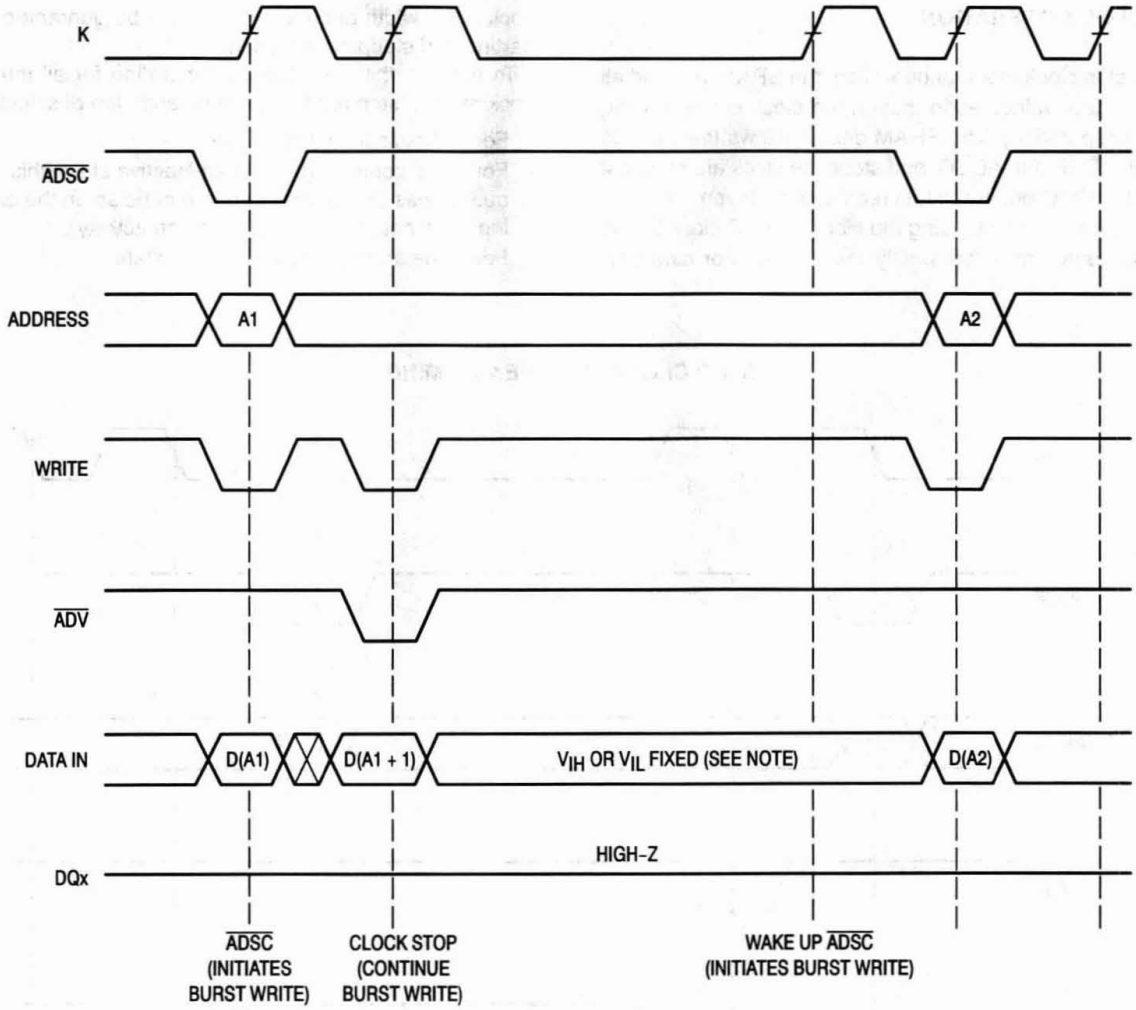
- Force the clock to a low state.
- Force the control signals to an inactive state (this guarantees any potential source of noise on the clock input will not start an unplanned on activity).
- Force the address inputs to a low state.

STOP CLOCK WITH READ TIMING



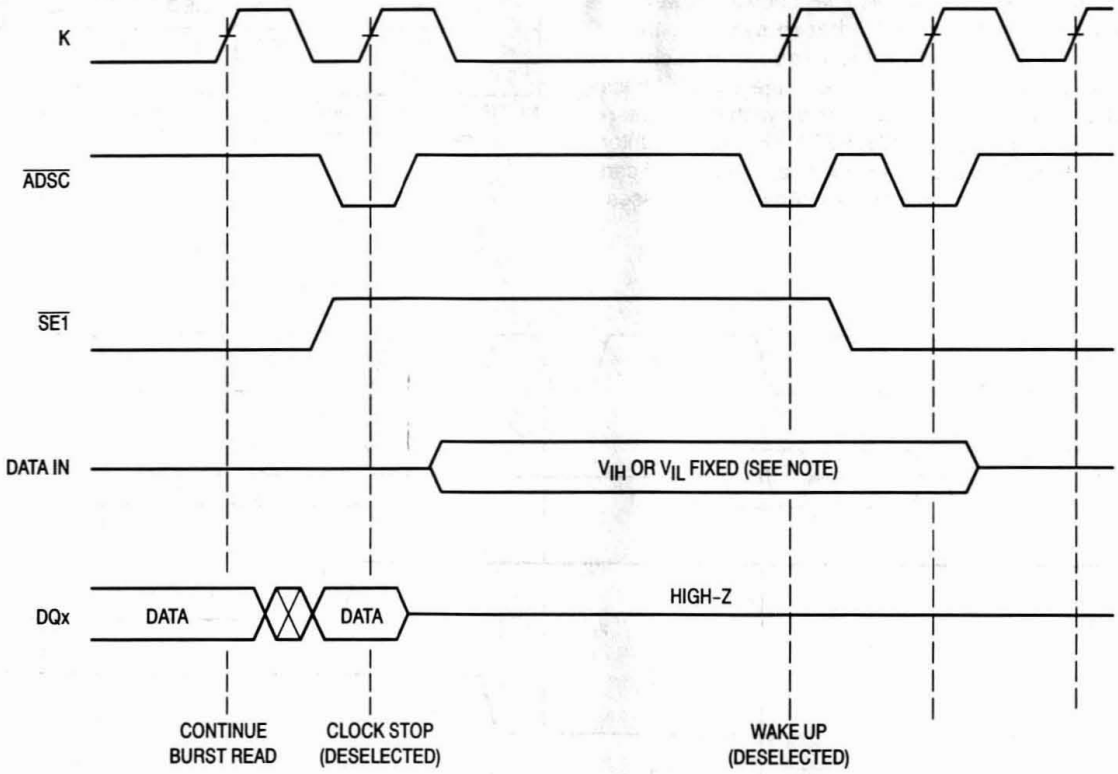
NOTE: For lowest possible power consumption during stop clock, the addresses should be driven to a low state (V_{IL}). Best results are obtained if $V_{IL} < 0.2$ V.

STOP CLOCK WITH WRITE TIMING



NOTE: While the clock is stopped, DATA IN must be fixed in a high (V_{IH}) or low (V_{IL}) state to reduce the DC current of the input buffers. For lowest power operation, all data and address lines should be held in a low (V_{IL}) state and control lines held in an inactive state.

STOP CLOCK WITH DESELECT OPERATION TIMING



NOTE: While the clock is stopped, DATA IN must be fixed in a high (V_{IH}) or low (V_{IL}) state to reduce the DC current of the input buffers. For lowest power operation, all data and address lines should be held in a low (V_{IL}) state and control lines held in an inactive state.

NON–BURST SYNCHRONOUS OPERATION

Although this BurstRAM has been designed for PowerPC–based and other high end MPU–based systems, these SRAMs can be used in other high speed L2 cache or memory applications that do not require the burst address feature. Most L2 caches designed with a synchronous interface can make use of the MCM69P737. The burst counter feature of the BurstRAM can be disabled, and the SRAM can be configured to act upon a continuous stream of addresses. See Figure 6.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

Non–Burst	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
Sync Non–Burst, Pipelined SRAM	H	L	H	L	X

NOTE: Although X is specified in the table as a don't care, the pin must be tied either high or low.

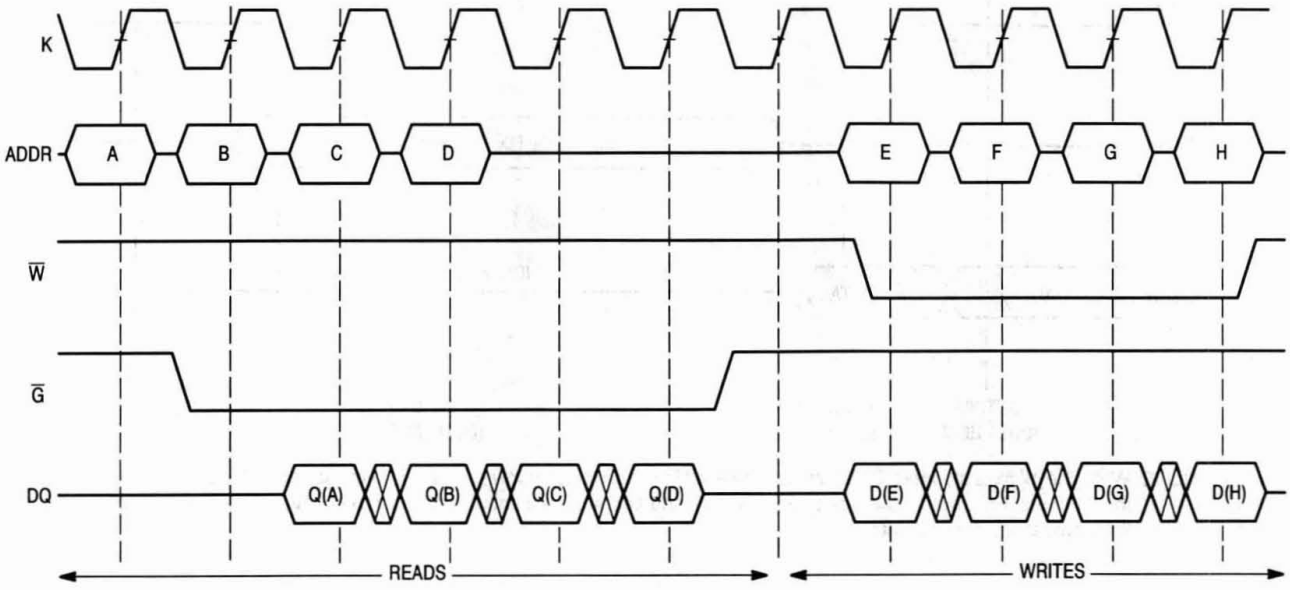


Figure 6. Configured as Non–Burst Synchronous SRAM

ORDERING INFORMATION
(Order by Full Part Number)

MCM 69P737 XX X X

- MCM: Motorola Memory Prefix
- 69P737: Part Number
- XX: Package (ZP = PBGA, TQ = TQFP)
- X: Speed (3.5 = 3.5 ns, 3.8 = 3.8 ns, 4 = 4 ns)
- X: Blank = Trays, R = Tape and Reel

Full Part Numbers —
MCM69P737ZP3.5
MCM69P737ZP3.5R
MCM69P737ZP3.8
MCM69P737ZP3.8R
MCM69P737ZP4
MCM69P737ZP4R
MCM69P737TQ4
MCM69P737TQ4R

MCM63P631

Advance Information

64K x 32 Bit Pipelined BurstRAM™ Synchronous Fast Static RAM

TQ PACKAGE
TQFP
CASE 983A–01

The MCM63P631 is a 2M bit synchronous fast static RAM designed to provide a burstable, high performance, secondary cache for the 68K Family, PowerPC™, and Pentium™ microprocessors. It is organized as 64K words of 32 bits each. This device integrates input registers, an output register, a 2–bit address counter, and high speed SRAM onto a single monolithic circuit for reduced parts count in cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (SA), data inputs (DQx), and all control signals except output enable ($\overline{G}$), sleep mode (ZZ), and Linear Burst Order ($\overline{LBO}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ input pins. Subsequent burst addresses can be generated internally by the MCM63P631 (burst sequence operates in linear or interleaved mode dependent upon state of $\overline{LBO}$) and controlled by the burst address advance ($\overline{ADV}$) input pin.

Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased timing flexibility for incoming signals.

Synchronous byte write ($\overline{SBx}$), synchronous global write ($\overline{SGW}$), and synchronous write enable $\overline{SW}$ are provided to allow writes to either individual bytes or to all bytes. The four bytes are designated as "a", "b", "c", and "d". $\overline{SBa}$ controls DQa, $\overline{SBb}$ controls DQb, etc. Individual bytes are written if the selected byte writes $\overline{SBx}$ are asserted with $\overline{SW}$. All bytes are written if either $\overline{SGW}$ is asserted or if all $\overline{SBx}$ and $\overline{SW}$ are asserted.

For read cycles, pipelined SRAMs output data is temporarily stored by an edge–triggered output register and then released to the output buffers at the next rising edge of clock (K).

The MCM63P631 operates from a 3.3 V power supply, all inputs and outputs are LVTTL compatible.

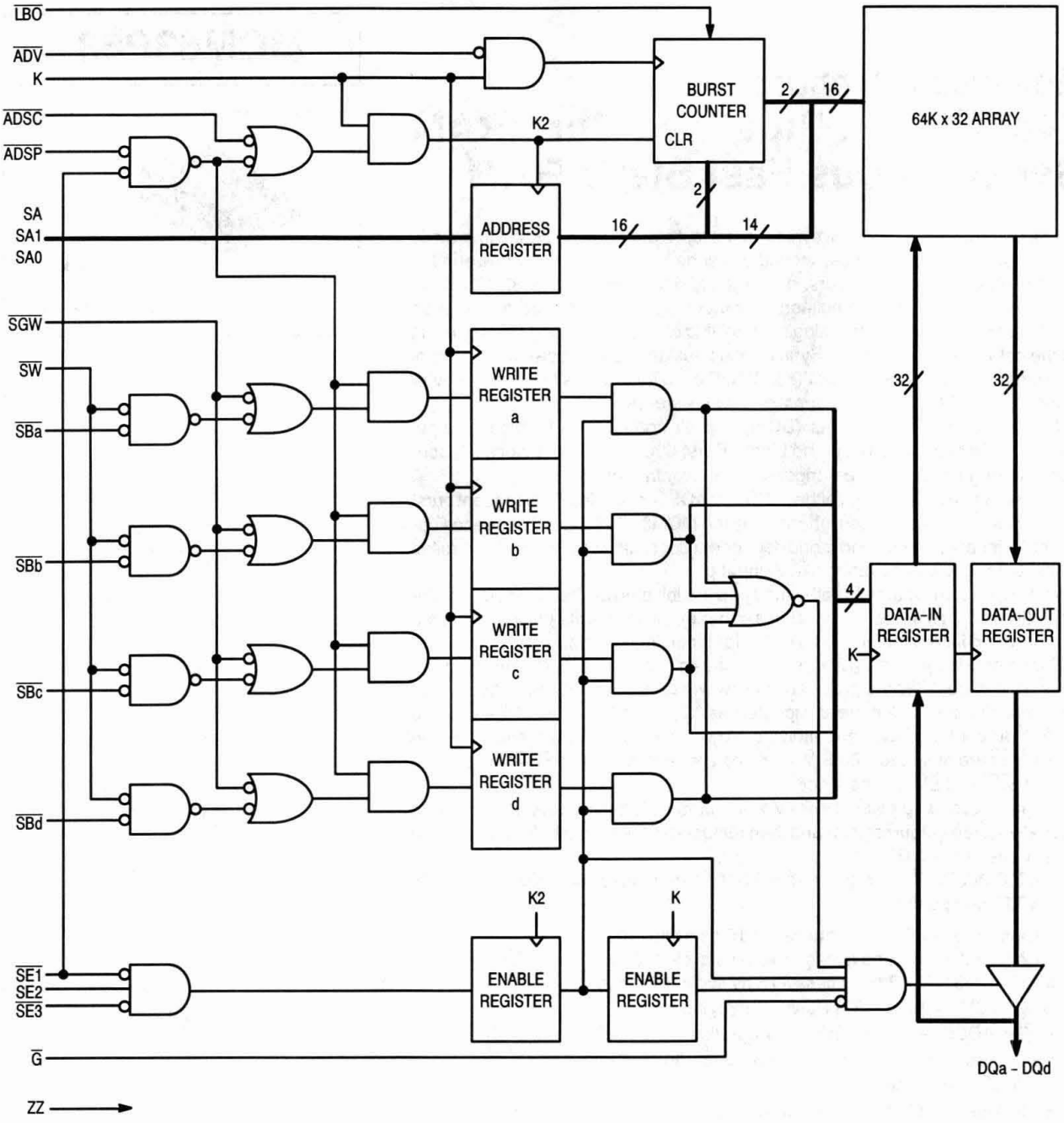
- MCM63P631–4.5 = 4.5 ns access / 10 ns cycle (100 MHz)
  MCM63P631–7 = 7 ns access / 13.3 ns cycle (75 MHz)
  MCM63P631–8 = 8 ns access / 15 ns cycle (66 MHz)
- Single 3.3 V + 10%, – 5% Power Supply
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Selectable Burst Sequencing Order (Linear/Interleaved)
- Internally Self–Timed Write Cycle
- Byte Write and Global Write Control
- Sleep Mode (ZZ)
- Intel PBSRAM 2.0 Compliant
- Single–Cycle Deselect Timing
- 100 Pin TQFP Package

BurstRAM is a trademark of Motorola, Inc.
The PowerPC name is a trademark of IBM Corp., used under license therefrom.
Pentium is a trademark of Intel Corp.

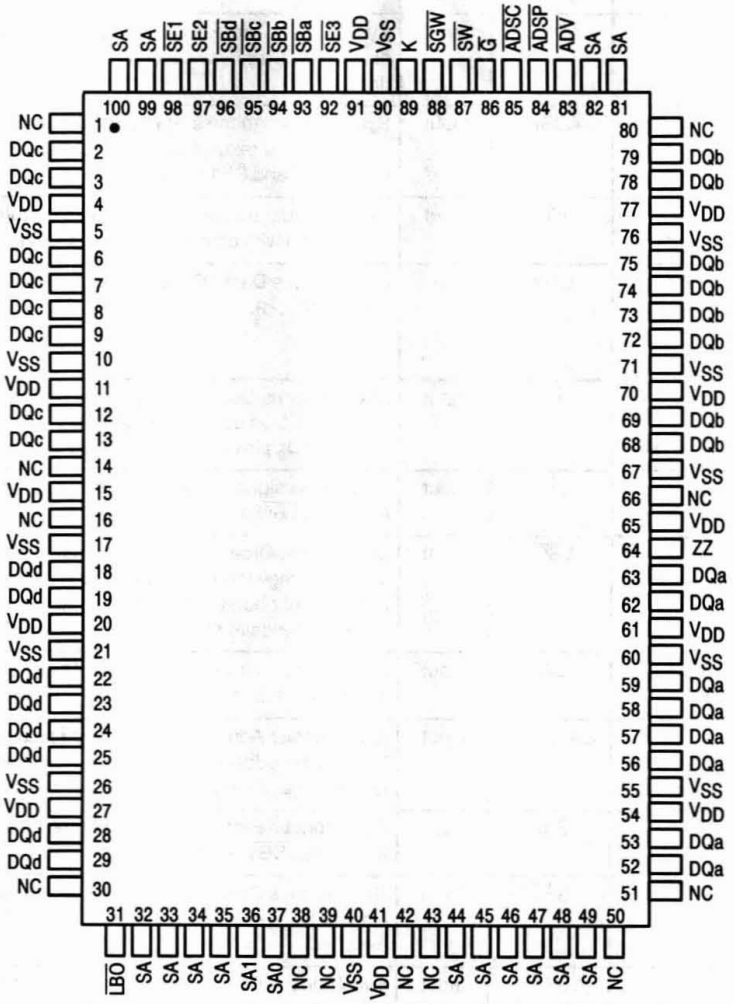
This document contains information on a new product. Motorola reserves the right to change or discontinue this product without notice.

REV 1
2/28/97

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENT



PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: Active low, is used to latch a new external address. Used to initiate a READ, WRITE or chip deselect.
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: Initiates READ or chip deselect cycle (exception — chip deselect does not occur when $\overline{ADSP}$ is asserted and $\overline{SE1}$ is high).
83	$\overline{ADV}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
(a) 52, 53, 56, 57, 58, 59, 62, 63 (b) 68, 69, 72, 73, 74, 75, 78, 79 (c) 2, 3, 6, 7, 8, 9, 12, 13 (d) 18, 19, 22, 23, 24, 25, 28, 29	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b, c, d).
86	$\overline{G}$	Input	Asynchronous Output Enable Input: Low — enables output buffers (DQx pins). High — DQx pins are high impedance.
89	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$, $\overline{LBO}$, and ZZ.
31	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst counter (68K/PowerPC). High — interleaved burst counter (486/i960/Pentium).
32, 33, 34, 35, 44, 45, 46, 47, 48, 49, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
36, 37	SA1, SA0	Input	Synchronous Address Inputs: These pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
93, 94, 95, 96 (a) (b) (c) (d)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: "x" refers to the byte being written (byte a, b, c, d). $\overline{SGW}$ overrides $\overline{SBx}$.
98	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high — blocks $\overline{ADSP}$ or deselects chip when $\overline{ADSC}$ is asserted.
97	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
92	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
88	$\overline{SGW}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the $\overline{SBx}$ and $\overline{SW}$ signals. If only byte write signals $\overline{SBx}$ are being used, tie this pin high.
87	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{SBx}$ pins. If only byte write signals $\overline{SBx}$ are being used, tie this pin low.
64	ZZ	Input	Sleep Mode: This active high asynchronous signal places the RAM into the lowest power mode. The ZZ pin disables the RAMs internal clock when placed in this mode. When ZZ is negated, the RAM remains in low power mode until it is commanded to READ or WRITE. Data integrity is maintained upon returning to normal operation.
4, 11, 15, 20, 27, 41, 54, 61, 65, 70, 77, 91	V_{DD}	Supply	Power Supply: 3.3 V + 10%, – 5%.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground.
1, 14, 16, 30, 38, 39, 42, 43, 50, 51, 66, 80	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE (See Notes 1 through 5)

Next Cycle	Address Used	$\overline{SE1}$	SE2	$\overline{SE3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{G}$ [3]	DQx	Write [2, 4]
Deselect	None	1	X	X	X	0	X	X	High–Z	X
Deselect	None	0	X	1	0	X	X	X	High–Z	X
Deselect	None	0	0	X	0	X	X	X	High–Z	X
Deselect	None	X	X	1	1	0	X	X	High–Z	X
Deselect	None	X	0	X	1	0	X	X	High–Z	X
Begin Read	External	0	1	0	0	X	X	X	High–Z	READ[5]
Begin Read	External	0	1	0	1	0	X	X	High–Z	READ[5]
Continue Read	Next	X	X	X	1	1	0	1	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	0	DQ	READ
Continue Read	Next	1	X	X	X	1	0	1	High–Z	READ
Continue Read	Next	1	X	X	X	1	0	0	DQ	READ
Suspend Read	Current	X	X	X	1	1	1	1	High–Z	READ
Suspend Read	Current	X	X	X	1	1	1	0	DQ	READ
Suspend Read	Current	1	X	X	X	1	1	1	High–Z	READ
Suspend Read	Current	1	X	X	X	1	1	0	DQ	READ
Begin Write	External	0	1	0	1	0	X	X	High–Z	WRITE
Continue Write	Next	X	X	X	1	1	0	X	High–Z	WRITE
Continue Write	Next	1	X	X	X	1	0	X	High–Z	WRITE
Suspend Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Suspend Write	Current	1	X	X	X	1	1	X	High–Z	WRITE

NOTES:
1. X = Don't Care. 1 = logic high. 0 = logic low.
2. Write is defined as either 1) any $\overline{SBx}$ and $\overline{SW}$ low or 2) $\overline{SGW}$ is low.
3. $\overline{G}$ is an asynchronous signal and is not sampled by the clock K. $\overline{G}$ drives the bus immediately (t_{GLQX}) following $\overline{G}$ going low.
4. On write cycles that follow read cycles, $\overline{G}$ must be negated prior to the start of the write cycle to ensure proper write data setup times. $\overline{G}$ must also remain negated at the completion of the write cycle to ensure proper write data hold times.
5. This READ assumes the RAM was previously deselected.

4

ASYNCHRONOUS TRUTH TABLE

Operation	ZZ	$\overline{G}$	I/O Status
Read	L	L	Data Out (DQx)
Read	L	H	High–Z
Write	L	X	High–Z
Deselected	L	X	High–Z
Sleep	H	X	High–Z

LINEAR BURST ADDRESS TABLE ($\overline{LBO}$ = V_{SS})

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X10	X . . . X11	X . . . X00
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X00	X . . . X01	X . . . X10

INTERLEAVED BURST ADDRESS TABLE ($\overline{LBO}$ = V_{DD})

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00

WRITE TRUTH TABLE

Cycle Type	$\overline{SGW}$	$\overline{SW}$	$\overline{SBa}$	$\overline{SBb}$	$\overline{SBc}$	$\overline{SBd}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte a	H	L	L	H	H	H
Write Byte b	H	L	H	L	H	H
Write Byte c	H	L	H	H	L	H
Write Byte d	H	L	H	H	H	L
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

DC ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{DD}	V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Package Power Dissipation (See Note 2)	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to 85	°C
Storage Temperature	T_{stg}	– 55 to 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Thermal Resistance		—	—	—	1
Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	40 25	°C/W	2
Junction to Board (Bottom)		$R_{\theta JB}$	17	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter		Symbol	Min	Typ	Max	Unit
Supply Voltage		V_{DD}	3.135	3.3	3.63	V
Operating Temperature		T_J	20	—	110	°C
Input Low Voltage		V_{IL}	– 0.5*	—	0.8	V
Input High Voltage	Address and Control Inputs	V_{IH}	2.0**	—	V_{DD} + 0.5	V

* $V_{IL} \geq -1$ V for $t \leq t_{KHKH}/2$.
** $V_{IH} \leq V_{DD} + 1$ V for $t \leq t_{KHKH}/2$.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Input Leakage Current (0 V ≤ V_{in} ≤ V_{DD})		$I_{lkg}(I)$	—	—	± 1	µA	6, 7
Output Leakage Current (0 V ≤ V_{in} ≤ V_{DD})		$I_{lkg}(O)$	—	—	± 1	µA	
AC Supply Current (Device Selected, Freq = Max, V_{DD} = Max, All Inputs Toggling at $V_{in} \leq V_{IL}$ or $\geq V_{IH}$, I_{out} = 0)	MCM63P631–4.5	I_{DDA}	—	—	275	mA	3, 4, 5
	MCM63P631–7 MCM63P631–8	I_{DDA}	—	—	220 200		
CMOS Standby Supply Current (Deselected, Freq = 0, V_{DD} = Max, All Inputs Static at CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or $\geq V_{DD}$ – 0.2 V)		I_{SB2}	—	—	2	mA	1
Sleep Mode Supply Current (Sleep Mode, Freq = Max, V_{DD} = Max, All Other Inputs Static at $V_{in} \leq V_{SS}$ + 0.2 or $\geq V_{DD}$ – 0.2 V, ZZ ≥ V_{DD} – 0.2 V)		I_{ZZ}	—	—	2	mA	2
TTL Standby (Device Deselected, Freq = 0, V_{DD} = Max, All Inputs Static at ≤ V_{IL} or ≥ V_{IH})		I_{SB3}	—	—	25	mA	1
Clock Running (Device Deselected, Freq = Max, V_{CC} = Max, All Inputs Toggling at ≤ V_{SS} + 0.2 or ≥ V_{DD} – 0.2)	MCM63P631–4.5	I_{SB4}	—	—	145	mA	1
	MCM63P631–7 MCM63P631–8	I_{SB4}	—	—	115 105	mA	1
Static Clock Running (Device Deselected, Freq = Max, V_{DD} = Max, All Inputs Static at ≤ V_{IL} or ≥ V_{IH})	MCM63P631–4.5	I_{SB5}	—	—	65	mA	1
	MCM63P631–7 MCM63P631–8	I_{SB5}	—	—	50	mA	1
Output Low Voltage (I_{OL} = 8 mA)		V_{OL}	—	—	0.4	V	
Output High Voltage (I_{OH} = – 4 mA)		V_{OH}	2.4	—	—	V	

NOTES:
1. Device in Deselected mode as defined by the Truth Table.
2. Device in Sleep Mode as defined by the Asynchronous Truth Table.
3. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V).
4. All addresses transition simultaneously low (LSB) and then high (MSB).
5. Data states are all zero.
6. $\overline{LBO}$ pin has an internal pullup and will exhibit leakage currents of ± 5 µA.
7. ZZ pin has an internal pulldown and will exhibit leakage currents of ± 5 µA.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_J = 20 to 110°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	3	5	pF
Input/Output Capacitance	$C_{I/O}$	—	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1 Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM63P631–4.5 100 MHz		MCM63P631–7 75 MHz		MCM63P631–8 66 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	10	—	13.3	—	15	—	ns	
Clock High Pulse Width	t_{KHKL}	3.2	—	4.5	—	5	—	ns	
Clock Low Pulse Width	t_{KLKH}	3.2	—	4.5	—	5	—	ns	
Clock Access Time	t_{KHQV}	—	4.5	—	7	—	8	ns	5
Output Enable to Output Valid	t_{GLQV}	—	4.5	—	5	—	5	ns	5
Clock High to Output Active	t_{KHQX1}	0	—	0	—	0	—	ns	5, 7
Clock High to Output Change	t_{KHQX2}	1.5	—	2	—	2	—	ns	5, 7
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	5, 7
Output Disable to Q High–Z	t_{GHQZ}	—	5.5	—	7	—	8	ns	6, 7
Clock High to Q High–Z	t_{KHQZ}	1.5	5.5	2	7	2	8	ns	6, 7
Setup Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	t_{ADKH} t_{ADSKH} t_{DVKH} t_{WVKH} t_{EVKH}	2.5	—	2.5	—	2.5	—	ns	4
Hold Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	t_{KHAX} t_{KHADSX} t_{KHDX} t_{KHWX} t_{KHEX}	0.5	—	0.5	—	0.5	—	ns	4
Sleep Mode Standby	t_{ZZS}	—	2 x t_{KHKH}	—	2 x t_{KHKH}	—	2 x t_{KHKH}	ns	
Sleep Mode Recovery	t_{ZZREC}	2 x t_{KHKH}	—	2 x t_{KHKH}	—	2 x t_{KHKH}	—	ns	
Sleep Mode High to Q High–Z	t_{ZZQZ}	—	15	—	15	—	15	ns	

NOTES:
1. Write applies to all $\overline{SBx}$, $\overline{SW}$, and $\overline{SGW}$ signals when the chip is selected and $\overline{ADSP}$ high.
2. Chip Enable applies to all $\overline{SE1}$, SE2 and $\overline{SE3}$ signals whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted.
3. All read and write cycle timings are referenced from K or $\overline{G}$.
4. $\overline{G}$ is a don't care after write cycle begins. To prevent bus contention, $\overline{G}$ should be negated prior to start of write cycle.
5. Tested per AC Test Load.
6. Measured at ± 200 mV from steady state.
7. This parameter is sampled and is not 100% tested.

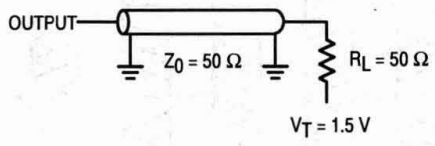
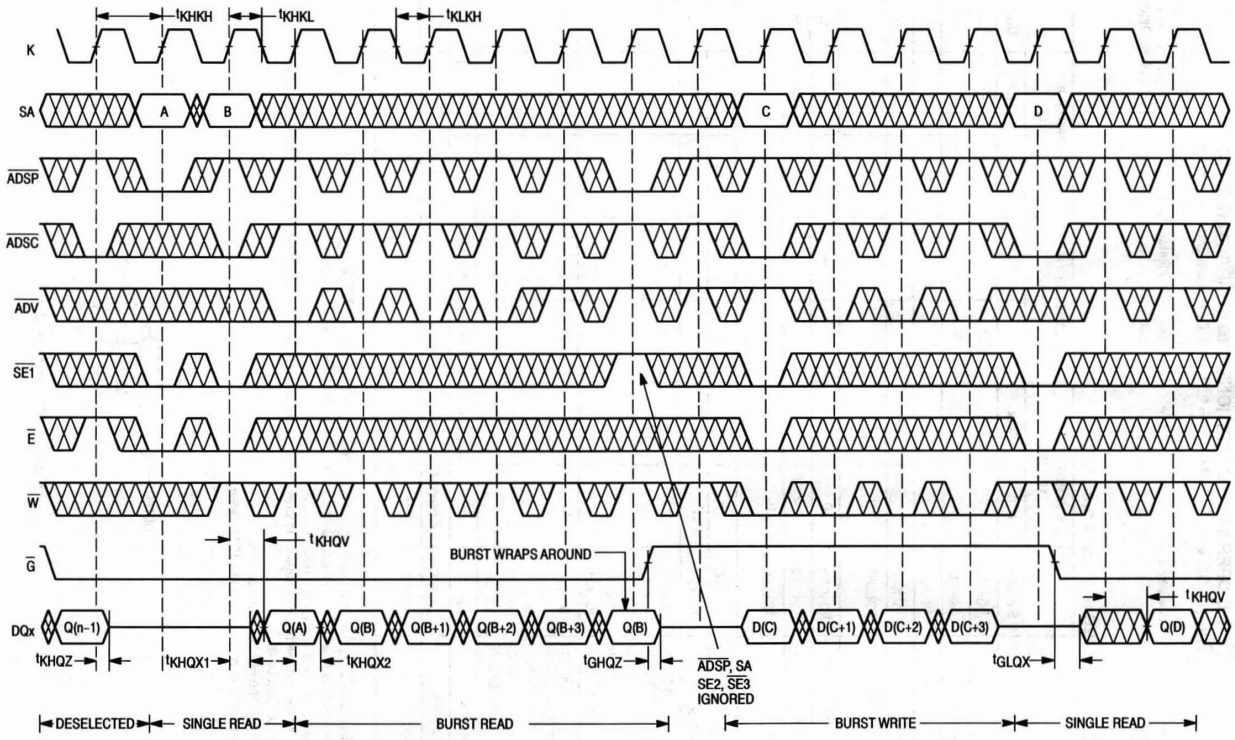


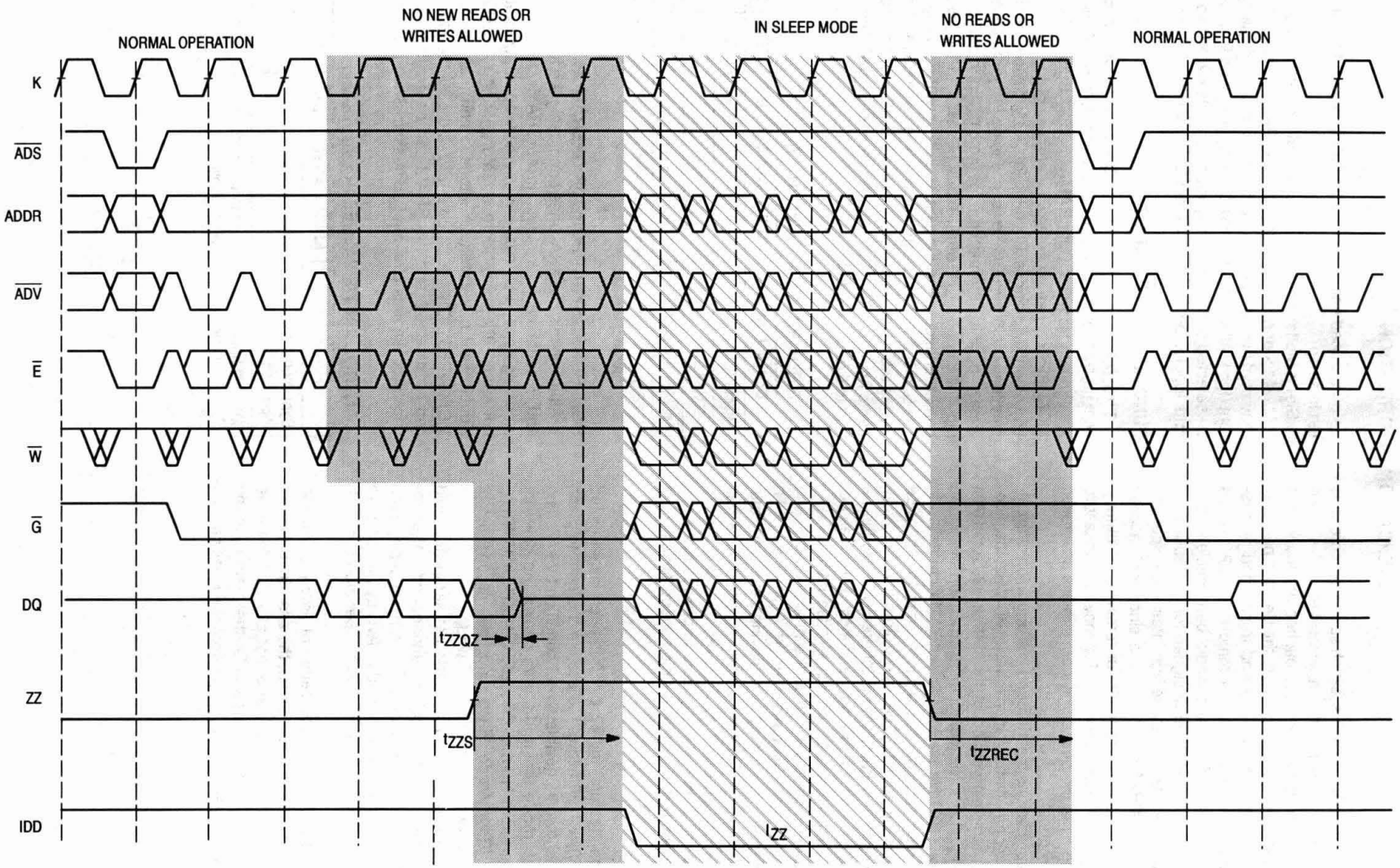
Figure 1. AC Test Load

READ/WRITE CYCLES



Note: $\overline{E}$ low = SE2 high and $\overline{SE3}$ low.
$\overline{W}$ low = $\overline{SGW}$ low and / or $\overline{SW}$ and $\overline{SBx}$ low.

SLEEP MODE TIMING



NOTE: $\overline{ADS}$ low = $\overline{ADSC}$ low or $\overline{ADSP}$ low.
$\overline{ADS}$ high = both $\overline{ADSC}$, $\overline{ADSP}$ high.
$\overline{E}$ low = $\overline{SE1}$ low, SE2 high, $\overline{SE3}$ low.

APPLICATION INFORMATION

The MCM63P631 BurstRAM is a high speed synchronous SRAM intended for use primarily in secondary or level two (L2) cache memory applications. L2 caches are found in a variety of classes of computers — from the desktop personal computer to the high–end servers and transaction processing machines. For simplicity, the majority of L2 caches today are direct mapped and are single bank implementations. These caches tend to be designed for bus speeds in the range of 33 to 66 MHz. At these bus rates, non–pipelined (flow–through) BurstRAMs can be used since their access times meet the speed requirements for a minimum–latency, zero–wait state L2 cache interface. Latency is a measure (time) of "dead" time the memory system exhibits as a result of a memory request.

For those applications that demand bus operation at greater than 66 MHz or multi–bank L2 caches at 66 MHz, the pipelined (register/register) version of the 64K x 32 BurstRAM (MCM63P631) allows the designer to maintain zero–wait state operation. Multiple banks of BurstRAMs create additional bus loading and can cause the system to otherwise miss its timing requirements. The access time (clock–to–valid–data) of a pipelined BurstRAM is inherently faster than a non–pipelined device by a few nanoseconds. This does not come without cost. The cost is latency — "dead" time.

Since most L2 caches are tied to the processor bus and bus speeds continue to increase over time, pipelined (R/R) BurstRAMs are the best choice in achieving zero–wait state L2 cache performance. For cost–sensitive applications that require zero–wait state L2 cache bus speeds of up to 75 MHz, pipelined BurstRAMs are able to provide fast clock to valid data times required of these high speed buses.

SLEEP MODE

A sleep mode feature, the ZZ pin, has been implemented on the MCM63P631. It allows the system designer to place the RAM in the lowest possible power condition by asserting ZZ. The sleep mode timing diagram shows the different modes of operation: Normal Operation, No READ/WRITE Allowed, and Sleep Mode. Each mode has its own set of constraints and conditions that are allowed.

Normal Operation: All inputs must meet setup and hold times prior to sleep and t_{ZZREC} nanoseconds after recovering from sleep. Clock (K) must also meet cycle, high, and low times during these periods. Two cycles prior to sleep, initiation of either a read or write operation is not allowed.

No READ/WRITE: During the period of time just prior to sleep and during recovery from sleep, the assertion of either $\overline{ADSC}$, $\overline{ADSP}$, or any write signal is not allowed. If a write operation occurs during these periods, the memory array may be corrupted. Validity of data out from the RAM can not be guaranteed immediately after ZZ is asserted (prior to being in sleep).

Sleep Mode: The RAM automatically deselects itself. The RAM disconnects its internal clock buffer. The external clock may continue to run without impacting the RAMs sleep current (I_{ZZ}). All inputs are allowed to toggle — the RAM will not be selected and perform any reads or writes. However, if inputs toggle, the I_{ZZ} (max) specification will not be met.

FUNCTIONAL EQUIVALENT

The following describes the configuration of the MCM63P631 as a functional equivalent to a 5 V BurstRAM. A migration from 5 V BurstRAMs to 3.3 V BurstRAMs (e.g., MCM63P631) can be somewhat confusing due to functional and pinout differences. Because the 3.3 V devices offer more pins than the 5 V PLCC devices, it is no longer necessary to supply multiple part numbers for the different burst, address pipeline support ("H" part), etc., options. The MCM63P631 can be configured to function as if it were the equivalent of two 5 V BurstRAMs, assuming parity is not required. The following table lists control pins on the MCM63P631 that can be tied off to either 3.3 V or ground in order to satisfy the migration to this 3.3 V RAM.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

5 V Device Numbers	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
MCM67C518	—	—	—	L	H
MCM67J518	—	—	—	—	H
MCM67N518	—	—	—	L	L

NOTE: If no tie value is given, then the pin should be used as intended on the 5 V device.

NON–BURST SYNCHRONOUS OPERATION

Although this BurstRAM has been designed for PowerPC– and Pentium–based systems, these SRAMs can be used in other high speed L2 cache or memory applications that do not require the burst address feature. Most L2 caches designed with a synchronous interface can make use of the MCM63P631. The burst counter feature of the BurstRAM can be disabled, and the SRAM can be configured to act upon a continuous stream of addresses. See Figure 2.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

Non–Burst	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
Sync Non–Burst, Pipelined SRAM	H	L	H	L	X

NOTE: Although X is specified in the table as a don't care, the pin must be tied either high or low.

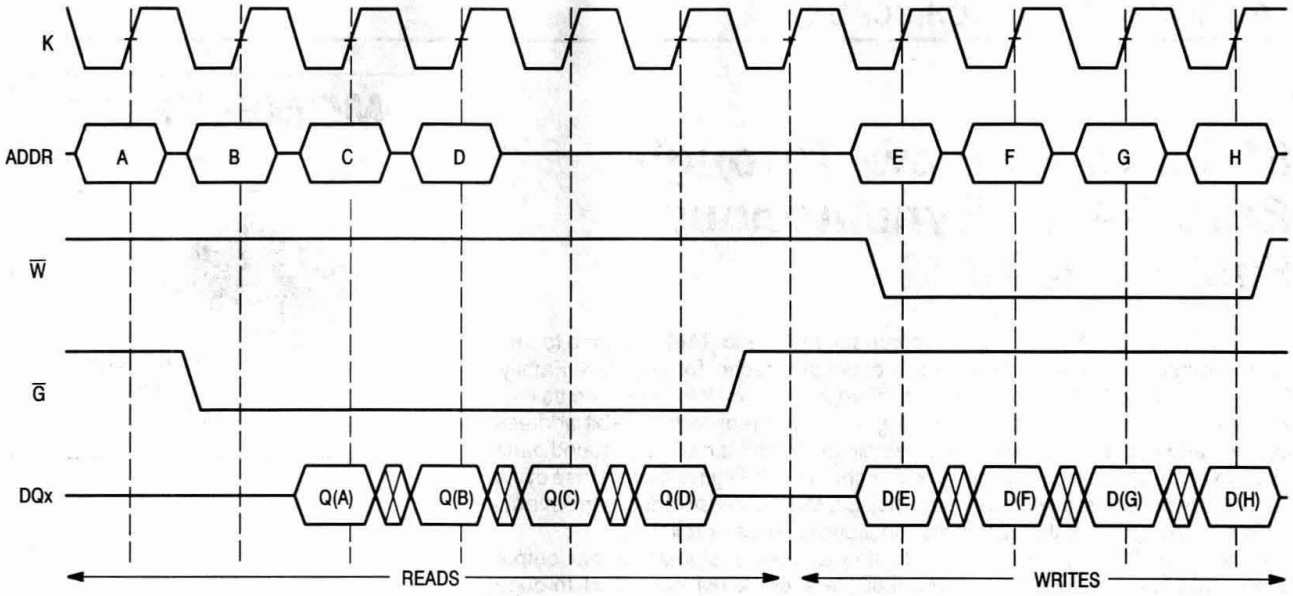


Figure 2. Configured as Non–Burst Pipelined Synchronous SRAM

4

ORDERING INFORMATION
(Order by Full Part Number)

MCM 63P631 XX X X

Motorola Memory Prefix — MCM

Part Number — 63P631

Blank = Trays, R = Tape and Reel

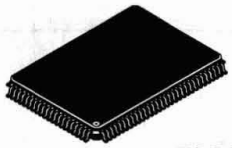
Speed (4.5 = 4.5 ns, 7 = 7 ns, 8 = 8 ns)

Package (TQ = TQFP)

Full Part Numbers — MCM63P631TQ4.5 MCM63P631TQ7 MCM63P631TQ8
MCM63P631TQ4.5R MCM63P631TQ7R MCM63P631TQ8R

MCM69F618A

64K x 18 Bit Flow–Through BurstRAM™ Synchronous Fast Static RAM



TQ PACKAGE
TQFP
CASE 983A–01

The MCM69F618A is a 1M bit synchronous fast static RAM designed to provide a burstable, high performance, secondary cache for the 68K Family, PowerPC™, 486, i960™ and Pentium™ microprocessors. It is organized as 64K words of 18 bits each. This device integrates input registers, a 2–bit address counter, and high speed SRAM onto a single monolithic circuit for reduced parts count in cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (SA), data inputs (DQx), and all control signals except output enable ($\overline{G}$) and Linear Burst Order ($\overline{LBO}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ input pins. Subsequent burst addresses can be generated internally by the MCM69F618A (burst sequence operates in linear or interleaved mode dependent upon state of $\overline{LBO}$) and controlled by the burst address advance ($\overline{ADV}$) input pin.

Write cycles are internally self–timed and initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased timing flexibility for incoming signals.

Synchronous byte write ($\overline{SBx}$), synchronous global write ($\overline{SGW}$), and synchronous write enable $\overline{SW}$ are provided to allow writes to either individual bytes or to both bytes. The two bytes are designated as "a" and "b". $\overline{SBa}$ controls DQa and $\overline{SBb}$ controls DQb. Individual bytes are written if the selected byte writes $\overline{SBx}$ are asserted with $\overline{SW}$. Both bytes are written if either $\overline{SGW}$ is asserted or if all $\overline{SBx}$ and $\overline{SW}$ are asserted.

For read cycles, a flow–through SRAM allows output data to simply flow freely from the memory array.

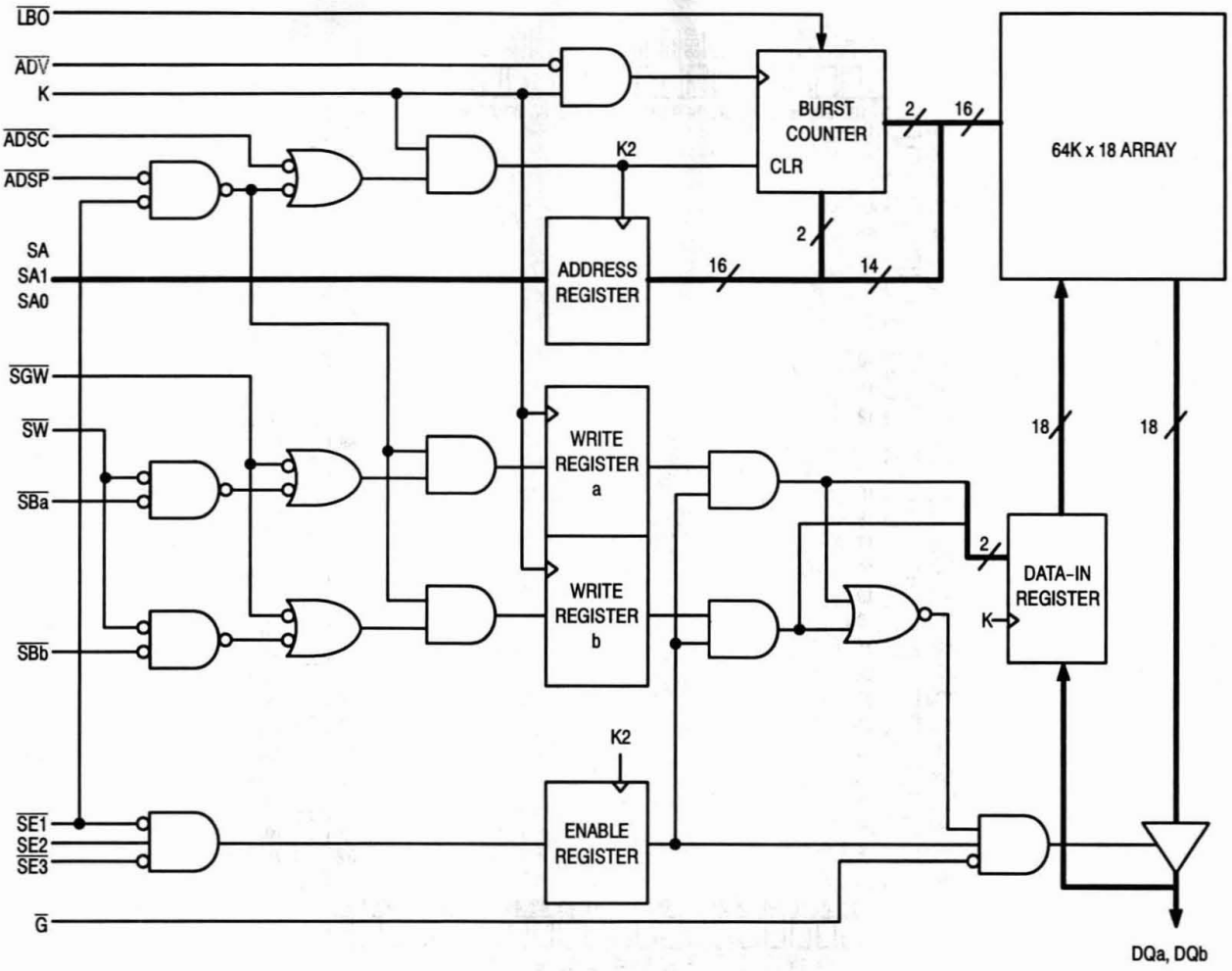
The MCM69F618A operates from a 3.3 V power supply and all inputs and outputs are LVTTL compatible.

- MCM69F618A–8.5 = 8.5 ns access / 12 ns cycle
  MCM69F618A–9 = 9 ns access / 12 ns cycle
  MCM69F618A–10 = 10 ns access / 15 ns cycle
  MCM69F618A–12= 12 ns access / 16.6 ns cycle
- Single 3.3 V + 10%, – 5% Power Supply
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Selectable Burst Sequencing Order (Linear/Interleaved)
- Internally Self–Timed Write Cycle
- Byte Write and Global Write Control
- 100 Pin TQFP Package

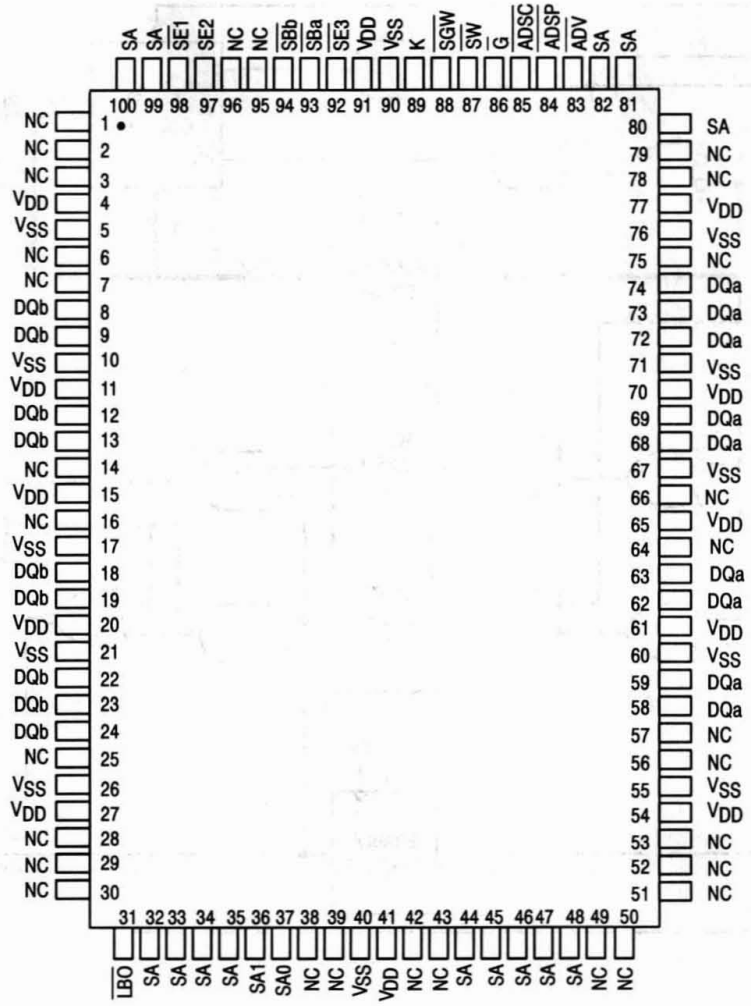
BurstRAM is a trademark of Motorola, Inc.
The PowerPC name is a trademark of IBM Corp., used under license therefrom.
i960 and Pentium are trademarks of Intel Corp.

REV 3
4/10/97

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENT



PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: Initiates READ, WRITE or chip deselect cycle.
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: Initiates READ, WRITE or chip deselect cycle (exception – chip deselect does not occur when $\overline{ADSP}$ is asserted and $\overline{SE1}$ is high).
83	$\overline{ADV}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
(a) 58, 59, 62, 63, 68, 69, 72, 73, 74 (b) 8, 9, 12, 13, 18, 19, 22, 23, 24	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b).
86	$\overline{G}$	Input	Asynchronous Output Enable Input: Low–enables output buffers (DQx pins). High – DQx pins are high impedance.
89	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$ and $\overline{LBO}$.
31	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low–linear burst counter (68K/PowerPC) High–interleaved burst counter (486/i960/Pentium)
32, 33, 34, 35, 44, 45, 46, 47, 48, 80, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
36, 37	SA1,SA0	Input	Synchronous Address Inputs: these pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
93, 94 (a) (b)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: "x" refers to the byte being written (byte a, b). $\overline{SGW}$ overrides $\overline{SBx}$.
98	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high–blocks $\overline{ADSP}$ or deselects chip when $\overline{ADSC}$ is asserted.
97	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
92	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
88	$\overline{SGW}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the $\overline{SBx}$ and $\overline{SW}$ signals. If only byte write signals $\overline{SBx}$ are being used, tie this pin high.
87	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{SBx}$ pins. If only byte write signals $\overline{SBx}$ are being used, tie this pin low.
4, 11, 15, 20, 27, 41, 54, 61, 65, 70, 77, 91	V_{DD}	Supply	Power Supply: 3.3 V + 10%, – 5%
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground
64	NC	Input	No Connection: There is no connection to the chip. For compatibility reasons, it is recommended that this pin be tied low for system designs that do not have a sleep mode associated with the cache/memory controller. Other vendors' RAMs may have implemented this Sleep Mode (ZZ) feature.
1, 2, 3, 6, 7, 14, 16, 25, 28, 29, 30, 38, 39, 42, 43, 49, 50, 51, 52, 53, 56, 57, 66, 75, 78, 79, 95, 96	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE (See Notes 1 through 4)

Next Cycle	Address Used	$\overline{SE1}$	SE2	$\overline{SE3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{G}$ [3]	DQx	Write [2, 4]
Deselect	None	1	X	X	X	0	X	X	High–Z	X
Deselect	None	0	X	1	0	X	X	X	High–Z	X
Deselect	None	0	0	X	0	X	X	X	High–Z	X
Deselect	None	X	X	1	1	0	X	X	High–Z	X
Deselect	None	X	0	X	1	0	X	X	High–Z	X
Begin Read	External	0	1	0	0	X	X	0	DQ	READ
Begin Read	External	0	1	0	1	0	X	0	DQ	READ
Continue Read	Next	X	X	X	1	1	0	1	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	0	DQ	READ
Continue Read	Next	1	X	X	X	1	0	1	High–Z	READ
Continue Read	Next	1	X	X	X	1	0	0	DQ	READ
Suspend Read	Current	X	X	X	1	1	1	1	High–Z	READ
Suspend Read	Current	X	X	X	1	1	1	0	DQ	READ
Suspend Read	Current	1	X	X	X	1	1	1	High–Z	READ
Suspend Read	Current	1	X	X	X	1	1	0	DQ	READ
Begin Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Begin Write	Current	1	X	X	X	1	1	X	High–Z	WRITE
Begin Write	External	0	1	0	1	0	X	X	High–Z	WRITE
Continue Write	Next	X	X	X	1	1	0	X	High–Z	WRITE
Continue Write	Next	1	X	X	X	1	0	X	High–Z	WRITE
Suspend Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Suspend Write	Current	1	X	X	X	1	1	X	High–Z	WRITE

NOTES:
1. X = Don't Care. 1 = logic high. 0 = logic low.
2. Write is defined as either 1) any $\overline{SBx}$ and $\overline{SW}$ low or 2) $\overline{SGW}$ is low.
3. $\overline{G}$ is an asynchronous signal and is not sampled by the clock K. $\overline{G}$ drives the bus immediately (t_{GLQX}) following $\overline{G}$ going low.
4. On write cycles that follow read cycles, $\overline{G}$ must be negated prior to the start of the write cycle to ensure proper write data setup times. $\overline{G}$ must also remain negated at the completion of the write cycle to ensure proper write data hold times.

LINEAR BURST ADDRESS TABLE ($\overline{LBO} = V_{SS}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X10	X . . . X11	X . . . X00
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X00	X . . . X01	X . . . X10

INTERLEAVED BURST ADDRESS TABLE ($\overline{LBO} = V_{DD}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00

WRITE TRUTH TABLE

Cycle Type	$\overline{SGW}$	$\overline{SW}$	$\overline{SBa}$	$\overline{SBb}$
Read	H	H	X	X
Read	H	L	H	H
Write Byte a	H	L	L	H
Write Byte b	H	L	H	L
Write All Bytes	H	L	L	L
Write All Bytes	L	X	X	X

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{DD}	V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Package Power Dissipation (See Note 2)	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to 85	°C
Storage Temperature	T_{stg}	– 55 to 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Thermal Resistance Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	40 25	°C/W	2
Thermal Resistance Junction to Board (Bottom)		$R_{\theta JB}$	17	°C/W	3
Thermal Resistance Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.135	3.3	3.6	V
Operating Temperature	T_J	20	—	110	°C
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V

* $V_{IL} \geq -2$ V for $t \leq t_{KHKH}/2$.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit	Notes
Input Leakage Current (0 V ≤ V_{in} ≤ V_{DD}) (Excluding $\overline{LBO}$)		$I_{lkg(I)}$	—	± 1	µA	
Output Leakage Current (0 V ≤ V_{in} ≤ V_{DD})		$I_{lkg(O)}$	—	± 1	µA	
AC Supply Current (Device Selected, All Outputs Open, All Inputs Toggling at $V_{in} \leq V_{IL}$ or $\geq V_{IH}$, Cycle Time ≥ t_{KHKH} min)	MCM69F618A–8.5 (83 MHz) MCM69F618A–9 (83 MHz) MCM69F618A–10 (66 MHz) MCM69F618A–12 (60 MHz)	I_{DDA}	—	225 225 215 210	mA	2, 3, 4
CMOS Standby Supply Current (Deselected[1], Clock (K) Cycle Time ≥ t_{KHKH}, All Inputs Toggling at CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{DD} – 0.2 V)	MCM69F618A–8.5 (83 MHz) MCM69F618A–9 (83 MHz) MCM69F618A–10 (66 MHz) MCM69F618A–12 (60 MHz)	I_{SB1}	—	110 110 100 95	mA	
Clock Running Supply Current (Deselected[1], Clock (K) Cycle Time ≥ t_{KHKH}, All Other Inputs Held to Static CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{DD} – 0.2 V)	MCM69F618A–8.5 (83 MHz) MCM69F618A–9 (83 MHz) MCM69F618A–10 (66 MHz) MCM69F618A–12 (60 MHz)	I_{SB2}	—	40 40 35 35	mA	
Output Low Voltage (I_{OL} = 8 mA)		V_{OL}	—	0.4	V	
Output High Voltage (I_{OH} = – 4 mA)		V_{OH}	2.4	—	V	

NOTES:
1. Device in Deselected mode as defined by the Truth Table.
2. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
3. All addresses transition simultaneously low (LSB) and then high (MSB).
4. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	4	6	pF
Input/Output Capacitance	$C_{I/O}$	—	7	9	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1 Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	69F618A–8.5		69F618A–9		69F618A–10		69F618A–12		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	12	—	12	—	15	—	16.6	—	ns	
Clock High Pulse Width	t_{KHKL}	4	—	4	—	5	—	6	—	ns	
Clock Low Pulse Width	t_{KLKH}	4	—	4	—	5	—	6	—	ns	
Clock Access Time	t_{KHQV}	—	8.5	—	9	—	10	—	12	ns	4
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	5	—	6	ns	4
Clock High to Output Active	t_{KHQX1}	0	—	0	—	0	—	0	—	ns	4, 6
Clock High to Output Change	t_{KHQX2}	3	—	3	—	3	—	3	—	ns	4, 6
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	ns	4, 6
Output Disable to Q High–Z	t_{GHQZ}	—	5	—	5	—	5	—	6	ns	5, 6
Clock High to Q High–Z	t_{KHQZ}	3	5	3	5	3	5	3	6	ns	5, 6
Setup Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	t_{AVKH} t_{ADKH} t_{DVKH} t_{WVKH} t_{EVKH}	2.5	—	2.5	—	2.5	—	2.5	—	ns	
Hold Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	t_{KHAX} t_{KHADX} t_{KHDX} t_{KHWX} t_{KHEX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	

NOTES:
1. Write is defined as either any $\overline{SBx}$ and $\overline{SW}$ low or $\overline{SGW}$ is low. Chip Enable is defined as $\overline{SE1}$ low, SE2 high and $\overline{SE3}$ low whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care after write cycle begins. To prevent bus contention, $\overline{G}$ should be negated prior to start of write cycle.
4. Tested per AC Test Load (See Figure 1).
5. Measured at ± 200 mV from steady state.
6. This parameter is sampled and not 100% tested.

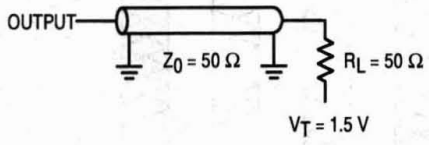
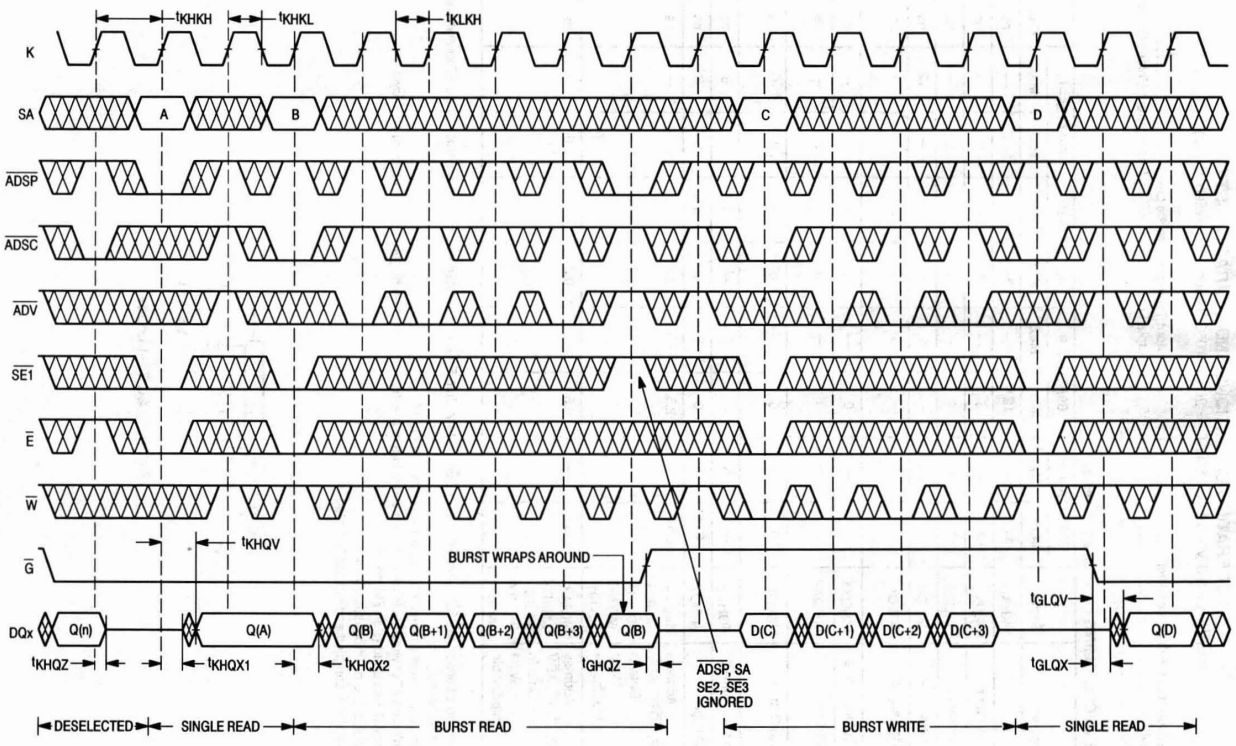


Figure 1. AC Test Loads

READ/WRITE CYCLES



Note: $\overline{E}$ low = SE2 high and $\overline{SE3}$ low.
$\overline{W}$ low = $\overline{SGW}$ low and/or $\overline{SW}$ and $\overline{SBx}$ low.

APPLICATION INFORMATION

The MCM69F618A BurstRAM is a high speed synchronous SRAM that is intended for use primarily in secondary or level two (L2) cache memory applications. L2 caches are found in a variety of classes of computers – from the desktop personal computer to the high–end servers and transaction processing machines. For simplicity, the majority of L2 caches today are direct mapped and are single bank implementations. These caches tend to be designed for bus speeds in the range of 33 to 66 MHz. At these bus rates, flow–through (non–pipelined) BurstRAMs can be used since their access times meet the speed requirements for a minimum–latency, zero–wait state L2 cache interface. Latency is a measure (time) of "dead" time the memory system exhibits as a result of a memory request.

For those applications that demand bus operation at greater than 66 MHz or multi–bank L2 caches at 66 MHz, the pipelined (register/register) version of the 64K x 18 BurstRAM (MCM69P618) allows the designer to maintain zero–wait state operation. Multiple banks of BurstRAMs create additional bus loading and can cause the system to otherwise miss its timing requirements. The access time (clock–to–valid–data) of a pipelined BurstRAM is inherently faster than a non–pipelined device by a few nanoseconds. This does not come without cost. The cost is latency – "dead" time.

For L2 cache designs that must minimize both latency and wait states, flow–through BurstRAMs are the best choice in achieving the highest performance in L2 cache design.

FUNCTIONAL EQUIVALENT

The following describes the configuration of the MCM69F618A as a functional equivalent to a 5 V BurstRAM. A migration from 5 V BurstRAMs to 3.3 V BurstRAMs (e.g. MCM69F618A) can be somewhat confusing due to functional and pinout differences. Because the 3.3 V devices offer more pins than the 5 V devices, it is no longer necessary to supply multiple part numbers for the different burst, address pipeline support ("H" part), etc., options. The MCM69F618A can be configured to function as if it were one of the 5 V BurstRAMs. The following table lists control pins on the MCM69F618A that can be tied off to either 3.3 V or ground in order to satisfy the migration to this 3.3 V RAM.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

5 V Device Numbers	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
MCM67B618	—	—	—	L	H
MCM67H618	—	—	—	—	H
MCM67M618	—	—	—	L	L

NOTE: If no tie value is given, then the pin should be used as intended on the 5 V device.

NON–BURST SYNCHRONOUS OPERATION

Although this BurstRAM has been designed for 68K–, PowerPC–, 486–, i960, and Pentium – based systems, these SRAMs can be used in other high speed L2 cache or memory applications that do not require the burst address feature. Most L2 caches designed with a synchronous interface can make use of the MCM69F618A. The burst counter feature of the BurstRAM can be disabled, and the SRAM can be configured to act upon a continuous stream of addresses. See Figure 2.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

Non–Burst	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
Sync Non–Burst Flow–Through SRAM	H	L	H	L	X

NOTE: Although X is specified in the table as a don't care, the pin must be tied either high or low.

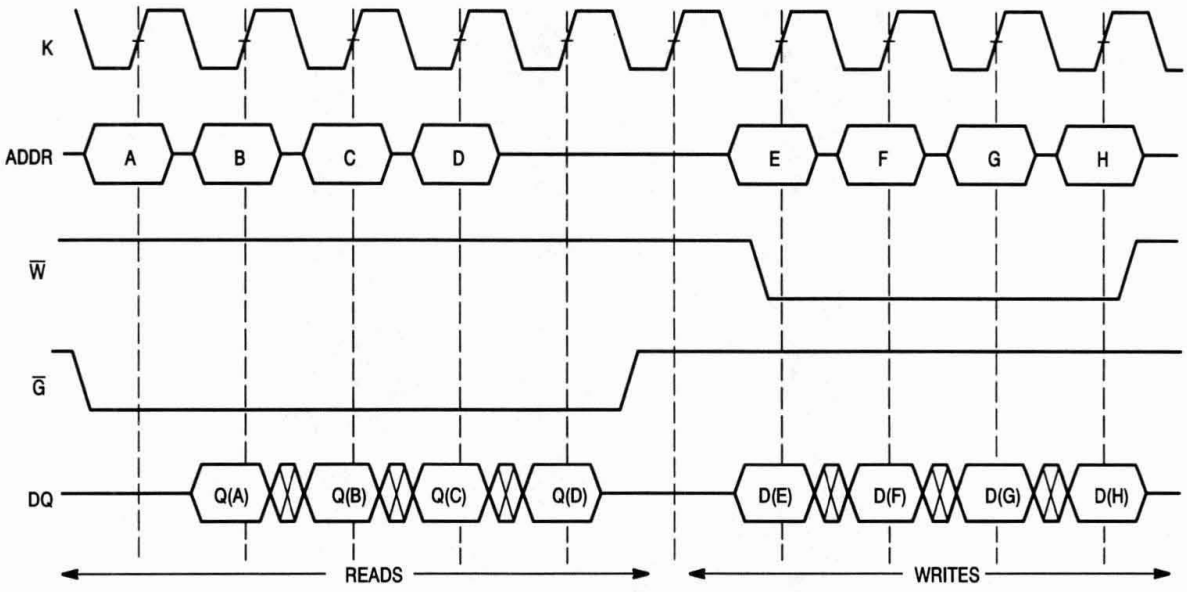
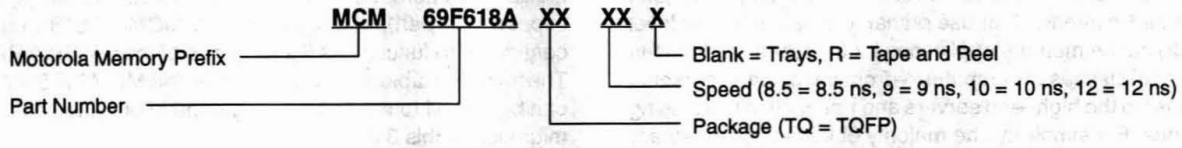


Figure 2. Configured as Non–Burst Synchronous SRAM

ORDERING INFORMATION
(Order by Full Part Number)

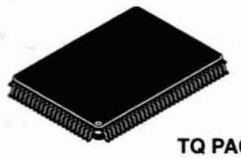

MCM 69F618A XX XX X
Motorola Memory Prefix
Part Number
Blank = Trays, R = Tape and Reel
Speed (8.5 = 8.5 ns, 9 = 9 ns, 10 = 10 ns, 12 = 12 ns)
Package (TQ = TQFP)

Full Part Numbers — MCM69F618ATQ8.5 MCM69F618ATQ9 MCM69F618ATQ10 MCM69F618ATQ12
MCM69F618ATQ8.5R MCM69F618ATQ9R MCM69F618ATQ10R MCM69F618ATQ12R

4

MCM69F618C

64K x 18 Bit Flow–Through BurstRAM™ Synchronous Fast Static RAM



TQ PACKAGE
TQFP
CASE 983A–01

The MCM69F618C is a 1M bit synchronous fast static RAM designed to provide a burstable, high performance, secondary cache for the 68K Family, PowerPC™, 486, i960™ and Pentium™ microprocessors. It is organized as 64K words of 18 bits each. This device integrates input registers, a 2–bit address counter, and high speed SRAM onto a single monolithic circuit for reduced parts count in cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (SA), data inputs (DQx), and all control signals except output enable ($\overline{G}$) and Linear Burst Order ($\overline{LBO}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ input pins. Subsequent burst addresses can be generated internally by the MCM69F618C (burst sequence operates in linear or interleaved mode dependent upon state of $\overline{LBO}$) and controlled by the burst address advance ($\overline{ADV}$) input pin.

Write cycles are internally self–timed and initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased timing flexibility for incoming signals.

Synchronous byte write ($\overline{SBx}$), synchronous global write ($\overline{SGW}$), and synchronous write enable $\overline{SW}$ are provided to allow writes to either individual bytes or to both bytes. The two bytes are designated as "a" and "b". $\overline{SBa}$ controls DQa and $\overline{SBb}$ controls DQb. Individual bytes are written if the selected byte writes $\overline{SBx}$ are asserted with $\overline{SW}$. Both bytes are written if either $\overline{SGW}$ is asserted or if all $\overline{SBx}$ and $\overline{SW}$ are asserted.

For read cycles, a flow–through SRAM allows output data to simply flow freely from the memory array.

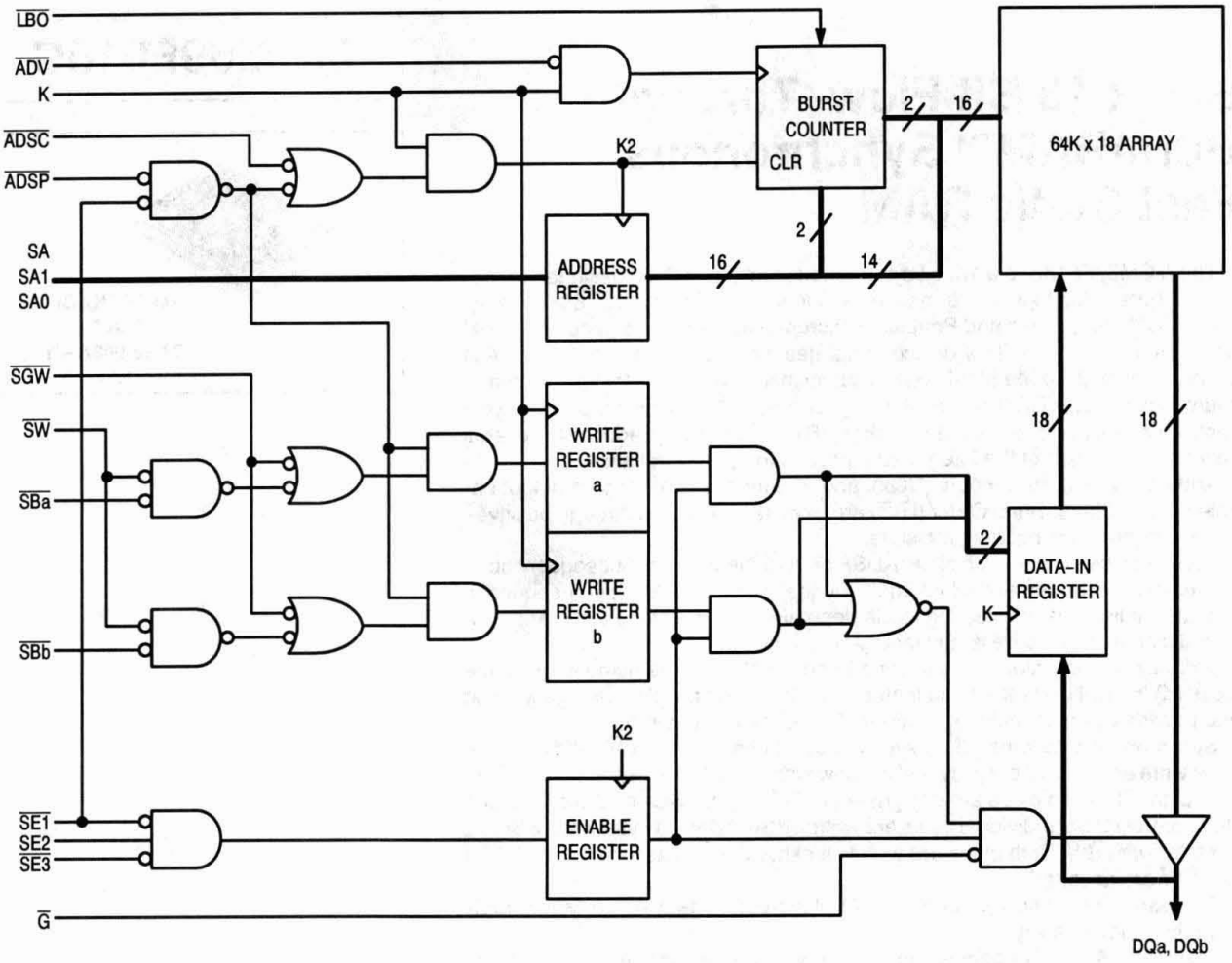
The MCM69F618C operates from a 3.3 V power supply and all inputs and outputs are LVTTL compatible and 5V tolerant.

- MCM69F618C–8.5 = 8.5 ns access / 12 ns cycle
  MCM69F618C–9 = 9 ns access / 12 ns cycle
  MCM69F618C–10 = 10 ns access / 15 ns cycle
  MCM69F618C–12= 12 ns access / 16.6 ns cycle
- Single 3.3 V + 10%, – 5% Power Supply
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Selectable Burst Sequencing Order (Linear/Interleaved)
- Internally Self–Timed Write Cycle
- Byte Write and Global Write Control
- 100 Pin TQFP Package
- 5 V Tolerant on all Pins (Inputs and I/O's)

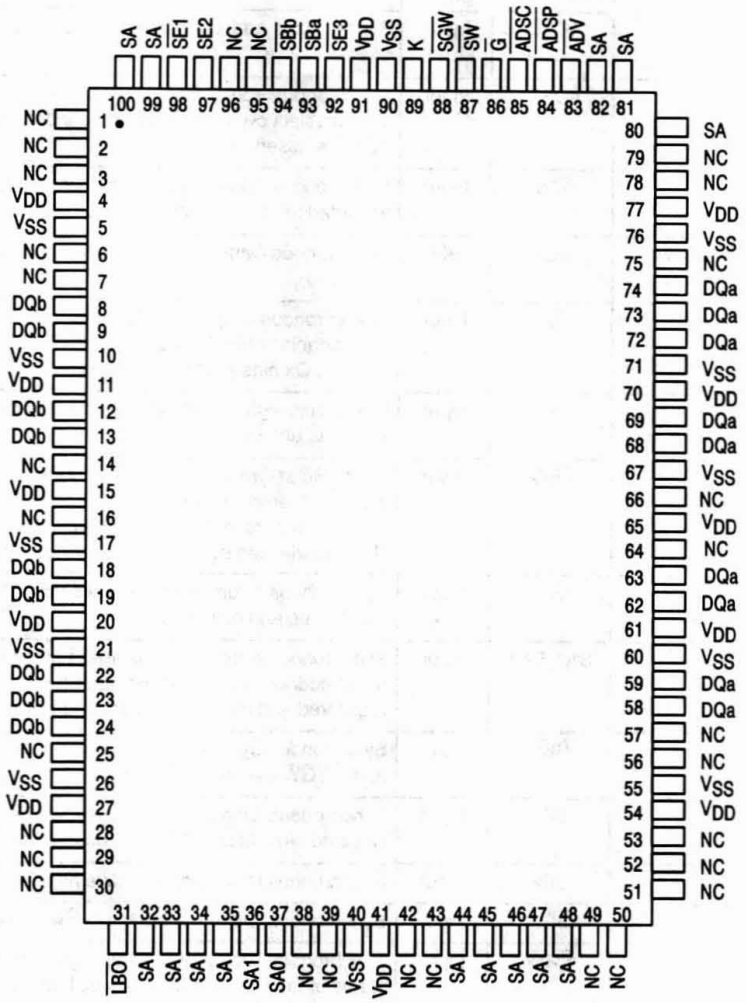
BurstRAM is a trademark of Motorola, Inc.
The PowerPC name is a trademark of IBM Corp., used under license therefrom.
i960 and Pentium are trademarks of Intel Corp.

REV 1
4/10/97

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENT



PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: Initiates READ, WRITE or chip deselect cycle.
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: Initiates READ, WRITE or chip deselect cycle (exception – chip deselect does not occur when $\overline{ADSP}$ is asserted and $\overline{SE1}$ is high).
83	$\overline{ADV}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
(a) 58, 59, 62, 63, 68, 69, 72, 73, 74 (b) 8, 9, 12, 13, 18, 19, 22, 23, 24	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b).
86	$\overline{G}$	Input	Asynchronous Output Enable Input: Low–enables output buffers (DQx pins). High – DQx pins are high impedance.
89	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$ and $\overline{LBO}$.
31	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low–linear burst counter (68K/PowerPC) High–interleaved burst counter (486/i960/Pentium)
32, 33, 34, 35, 44, 45, 46, 47, 48, 80, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
36, 37	SA1,SA0	Input	Synchronous Address Inputs: these pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
93, 94 (a) (b)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: "x" refers to the byte being written (byte a, b). $\overline{SGW}$ overrides $\overline{SBx}$.
98	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high–blocks $\overline{ADSP}$ or deselects chip when $\overline{ADSC}$ is asserted.
97	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
92	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
88	$\overline{SGW}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the $\overline{SBx}$ and $\overline{SW}$ signals. If only byte write signals $\overline{SBx}$ are being used, tie this pin high.
87	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{SBx}$ pins. If only byte write signals $\overline{SBx}$ are being used, tie this pin low.
4, 11, 15, 20, 27, 41, 54, 61, 65, 70, 77, 91	V_{DD}	Supply	Power Supply: 3.3 V + 10%, – 5%
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground
64	NC	Input	No Connection: There is no connection to the chip. For compatibility reasons, it is recommended that this pin be tied low for system designs that do not have a sleep mode associated with the cache/memory controller. Other vendors' RAMs may have implemented this Sleep Mode (ZZ) feature.
1, 2, 3, 6, 7, 14, 16, 25, 28, 29, 30, 38, 39, 42, 43, 49, 50, 51, 52, 53, 56, 57, 66, 75, 78, 79, 95, 96	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE (See Notes 1 through 4)

Next Cycle	Address Used	$\overline{SE1}$	SE2	$\overline{SE3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{G}$ [3]	DQx	Write [2, 4]
Deselect	None	1	X	X	X	0	X	X	High–Z	X
Deselect	None	0	X	1	0	X	X	X	High–Z	X
Deselect	None	0	0	X	0	X	X	X	High–Z	X
Deselect	None	X	X	1	1	0	X	X	High–Z	X
Deselect	None	X	0	X	1	0	X	X	High–Z	X
Begin Read	External	0	1	0	0	X	X	0	DQ	READ
Begin Read	External	0	1	0	1	0	X	0	DQ	READ
Continue Read	Next	X	X	X	1	1	0	1	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	0	DQ	READ
Continue Read	Next	1	X	X	X	1	0	1	High–Z	READ
Continue Read	Next	1	X	X	X	1	0	0	DQ	READ
Suspend Read	Current	X	X	X	1	1	1	1	High–Z	READ
Suspend Read	Current	X	X	X	1	1	1	0	DQ	READ
Suspend Read	Current	1	X	X	X	1	1	1	High–Z	READ
Suspend Read	Current	1	X	X	X	1	1	0	DQ	READ
Begin Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Begin Write	Current	1	X	X	X	1	1	X	High–Z	WRITE
Begin Write	External	0	1	0	1	0	X	X	High–Z	WRITE
Continue Write	Next	X	X	X	1	1	0	X	High–Z	WRITE
Continue Write	Next	1	X	X	X	1	0	X	High–Z	WRITE
Suspend Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Suspend Write	Current	1	X	X	X	1	1	X	High–Z	WRITE

NOTES: 1. X = Don't Care. 1 = logic high. 0 = logic low.
2. Write is defined as either 1) any $\overline{SBx}$ and $\overline{SW}$ low or 2) $\overline{SGW}$ is low.
3. $\overline{G}$ is an asynchronous signal and is not sampled by the clock K. $\overline{G}$ drives the bus immediately (t_{GLQX}) following $\overline{G}$ going low.
4. On write cycles that follow read cycles, $\overline{G}$ must be negated prior to the start of the write cycle to ensure proper write data setup times. $\overline{G}$ must also remain negated at the completion of the write cycle to ensure proper write data hold times.

LINEAR BURST ADDRESS TABLE ($\overline{LBO} = V_{SS}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X10	X . . . X11	X . . . X00
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X00	X . . . X01	X . . . X10

INTERLEAVED BURST ADDRESS TABLE ($\overline{LBO} = V_{DD}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00

WRITE TRUTH TABLE

Cycle Type	$\overline{SGW}$	$\overline{SW}$	$\overline{SBa}$	$\overline{SBb}$
Read	H	H	X	X
Read	H	L	H	H
Write Byte a	H	L	L	H
Write Byte b	H	L	H	L
Write All Bytes	H	L	L	L
Write All Bytes	L	X	X	X

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{DD}	V_{in}, V_{out}	– 0.5 to 6.0	V
Output Current (per I/O)	I_{out}	± 20	mA
Package Power Dissipation (See Note 2)	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to 85	°C
Storage Temperature	T_{stg}	– 55 to 125	°C

NOTES: 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

2. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Thermal Resistance Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	40 25	°C/W	1, 2
Thermal Resistance Junction to Board (Bottom)		$R_{\theta JB}$	17	°C/W	1, 3
Thermal Resistance Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	1, 4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.135	3.3	3.6	V
Operating Temperature	T_J	20	—	110	°C
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	5.5**	V

*$V_{IL} \geq -2$ V for $t \leq t_{KHKH}/2$.

**$V_{IH} \leq 6$ V for $t \leq t_{KHKH}/2$.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit	Notes
Input Leakage Current (0 V ≤ V_{in} ≤ V_{DD}) (Excluding $\overline{LBO}$)		$I_{lkg(I)}$	—	± 1	µA	
Output Leakage Current (0 V ≤ V_{in} ≤ V_{DD})		$I_{lkg(O)}$	—	± 1	µA	
AC Supply Current (Device Selected, All Outputs Open, All Inputs Toggling at $V_{in} \leq V_{IL}$ or $\geq V_{IH}$, Cycle Time ≥ t_{KHKH} min)	MCM69F618C–8.5 (83 MHz) MCM69F618C–9 (83 MHz) MCM69F618C–10 (66 MHz) MCM69F618C–12 (60 MHz)	I_{DDA}	—	225 225 215 210	mA	2, 3, 4
CMOS Standby Supply Current (Deselected[1], Clock (K) Cycle Time ≥ t_{KHKH}, All Inputs Toggling at CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{DD} – 0.2 V)	MCM69F618C–8.5 (83 MHz) MCM69F618C–9 (83 MHz) MCM69F618C–10 (66 MHz) MCM69F618C–12 (60 MHz)	I_{SB1}	—	110 110 100 95	mA	
Clock Running Supply Current (Deselected[1], Clock (K) Cycle Time ≥ t_{KHKH}, All Other Inputs Held to Static CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{DD} – 0.2 V))	MCM69F618C–8.5 (83 MHz) MCM69F618C–9 (83 MHz) MCM69F618C–10 (66 MHz MCM69F618C–12 (60 MHz)	I_{SB2}	—	40 40 35 35	mA	
Output Low Voltage (I_{OL} = 8 mA)		V_{OL}	—	0.4	V	
Output High Voltage (I_{OH} = – 4 mA)		V_{OH}	2.4	—	V	

NOTES:
1. Device in Deselected mode as defined by the Truth Table.
2. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
3. All addresses transition simultaneously low (LSB) and then high (MSB).
4. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	4	6	pF
Input/Output Capacitance	$C_{I/O}$	—	7	9	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1 Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	69F618A–8.5		69F618A–9		69F618A–10		69F618A–12		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	12	—	12	—	15	—	16.6	—	ns	
Clock High Pulse Width	t_{KHKL}	4	—	4	—	5	—	6	—	ns	
Clock Low Pulse Width	t_{KLKH}	4	—	4	—	5	—	6	—	ns	
Clock Access Time	t_{KHQV}	—	8.5	—	9	—	10	—	12	ns	4
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	5	—	6	ns	4
Clock High to Output Active	t_{KHQX1}	0	—	0	—	0	—	0	—	ns	4, 6
Clock High to Output Change	t_{KHQX2}	3	—	3	—	3	—	3	—	ns	4, 6
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	ns	4, 6
Output Disable to Q High–Z	t_{GHQZ}	—	5	—	5	—	5	—	6	ns	5, 6
Clock High to Q High–Z	t_{KHQZ}	3	5	3	5	3	5	3	6	ns	5, 6
Setup Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	t_{AVKH} t_{ADKH} t_{DVKH} t_{WVKH} t_{EVKH}	2.5	—	2.5	—	2.5	—	2.5	—	ns	
Hold Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	t_{KHAX} t_{KHADX} t_{KHDX} t_{KHWX} t_{KHEX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	

NOTES:
1. Write is defined as either any $\overline{SBx}$ and $\overline{SW}$ low or $\overline{SGW}$ is low. Chip Enable is defined as $\overline{SE1}$ low, SE2 high and $\overline{SE3}$ low whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care after write cycle begins. To prevent bus contention, $\overline{G}$ should be negated prior to start of write cycle.
4. Tested per AC Test Load (See Figure 1).
5. Measured at ± 200 mV from steady state.
6. This parameter is sampled and not 100% tested.

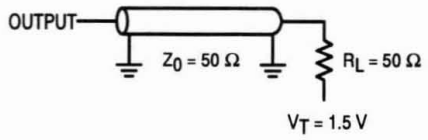
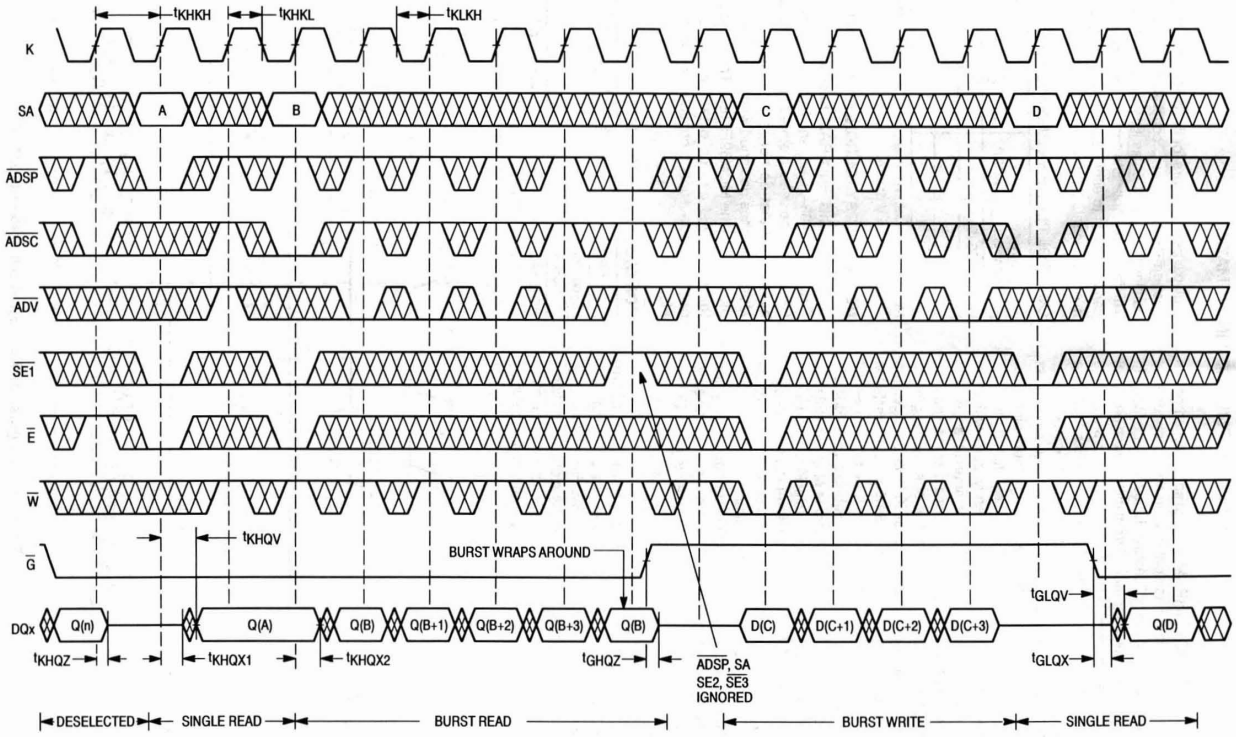


Figure 1. AC Test Loads

READ/WRITE CYCLES



Note: $\overline{E}$ low = SE2 high and $\overline{SE3}$ low.
$\overline{W}$ low = $\overline{SGW}$ low and/or $\overline{SW}$ and $\overline{SBx}$ low.

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For those applications that demand bus operation at greater than 66 MHz or multi–bank L2 caches at 66 MHz, the pipelined (register/register) version of the 64K x 18 BurstRAM (MCM69P618) allows the designer to maintain zero–wait state operation. Multiple banks of BurstRAMs create additional bus loading and can cause the system to otherwise miss its timing requirements. The access time (clock–to–valid–data) of a pipelined BurstRAM is inherently faster than a non–pipelined device by a few nanoseconds. This does not come without cost. The cost is latency – "dead" time.

For L2 cache designs that must minimize both latency and wait states, flow–through BurstRAMs are the best choice in achieving the highest performance in L2 cache design.

FUNCTIONAL EQUIVALENT

The following describes the configuration of the MCM69F618C as a functional equivalent to a 5 V BurstRAM. A migration from 5 V BurstRAMs to 3.3 V BurstRAMs (e.g. MCM69F618C) can be somewhat confusing due to functional and pinout differences. Because the 3.3 V devices offer more pins than the 5 V devices, it is no longer necessary to supply multiple part numbers for the different burst, address pipeline support ("H" part), etc., options. The MCM69F618C can be configured to function as if it were one of the 5 V BurstRAMs. The following table lists control pins on the MCM69F618C that can be tied off to either 3.3 V or ground in order to satisfy the migration to this 3.3 V RAM.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

5 V Device Numbers	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
MCM67B618	—	—	—	L	H
MCM67H618	—	—	—	—	H
MCM67M618	—	—	—	L	L

NOTE: If no tie value is given, then the pin should be used as intended on the 5 V device.

NON–BURST SYNCHRONOUS OPERATION

Although this BurstRAM has been designed for 68K–, PowerPC–, 486–, i960, and Pentium – based systems, these SRAMs can be used in other high speed L2 cache or memory applications that do not require the burst address feature. Most L2 caches designed with a synchronous interface can make use of the MCM69F618C. The burst counter feature of the BurstRAM can be disabled, and the SRAM can be configured to act upon a continuous stream of addresses. See Figure 2.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

Non–Burst	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
Sync Non–Burst Flow–Through SRAM	H	L	H	L	X

NOTE: Although X is specified in the table as a don't care, the pin must be tied either high or low.

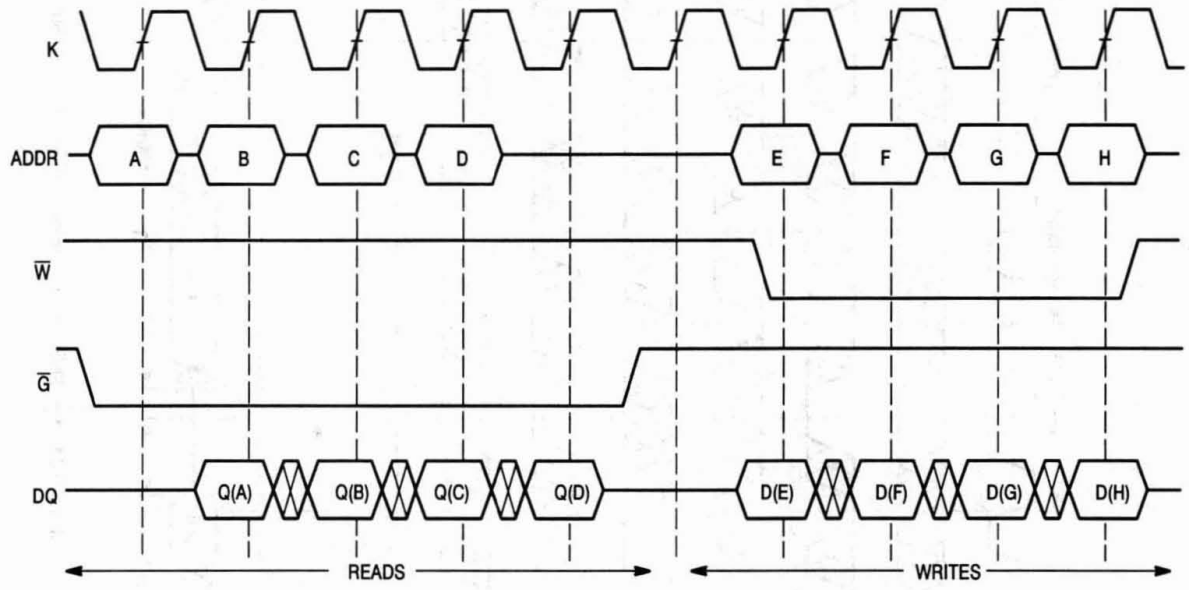
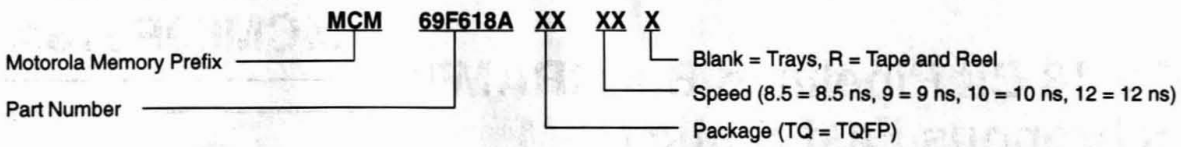


Figure 2. Configured as Non–Burst Synchronous SRAM

ORDERING INFORMATION
(Order by Full Part Number)


MCM 69F618A XX XX X
Motorola Memory Prefix
Part Number
Blank = Trays, R = Tape and Reel
Speed (8.5 = 8.5 ns, 9 = 9 ns, 10 = 10 ns, 12 = 12 ns)
Package (TQ = TQFP)

Full Part Numbers — MCM69F618CTQ8.5 MCM69F618CTQ9 MCM69F618CTQ10 MCM69F618CTQ12
MCM69F618CTQ8.5R MCM69F618CTQ9R MCM69F618CTQ10R MCM69F618CTQ12R

4

MCM69P618A

64K x 18 Bit Pipelined BurstRAM™ Synchronous Fast Static RAM

TQ PACKAGE
TQFP
CASE 983A–01

The MCM69P618A is a 1M bit synchronous fast static RAM designed to provide a burstable, high performance, secondary cache for the 68K Family, PowerPC™, 486, i960™ and Pentium™ microprocessors. It is organized as 64K words of 18 bits each. This device integrates input registers, an output register, a 2–bit address counter, and high speed SRAM onto a single monolithic circuit for reduced parts count in cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (SA), data inputs (DQx), and all control signals except output enable ($\overline{G}$) and Linear Burst Order ($\overline{LBO}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ input pins. Subsequent burst addresses can be generated internally by the MCM69P618A (burst sequence operates in linear or interleaved mode dependent upon state of $\overline{LBO}$) and controlled by the burst address advance ($\overline{ADV}$) input pin.

Write cycles are internally self–timed and initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased timing flexibility for incoming signals.

Synchronous byte write ($\overline{SBx}$), synchronous global write ($\overline{SGW}$), and synchronous write enable $\overline{SW}$ are provided to allow writes to either individual bytes or to both bytes. The two bytes are designated as "a" and "b". $\overline{SBa}$ controls DQa and $\overline{SBb}$ controls DQb. Individual bytes are written if the selected byte writes $\overline{SBx}$ are asserted with $\overline{SW}$. Both bytes are written if either $\overline{SGW}$ is asserted or if both $\overline{SBx}$ and $\overline{SW}$ are asserted.

For read cycles, pipelined SRAMs output data is temporarily stored by an edge–triggered output register and then released to the output buffers at the next rising edge of clock (K).

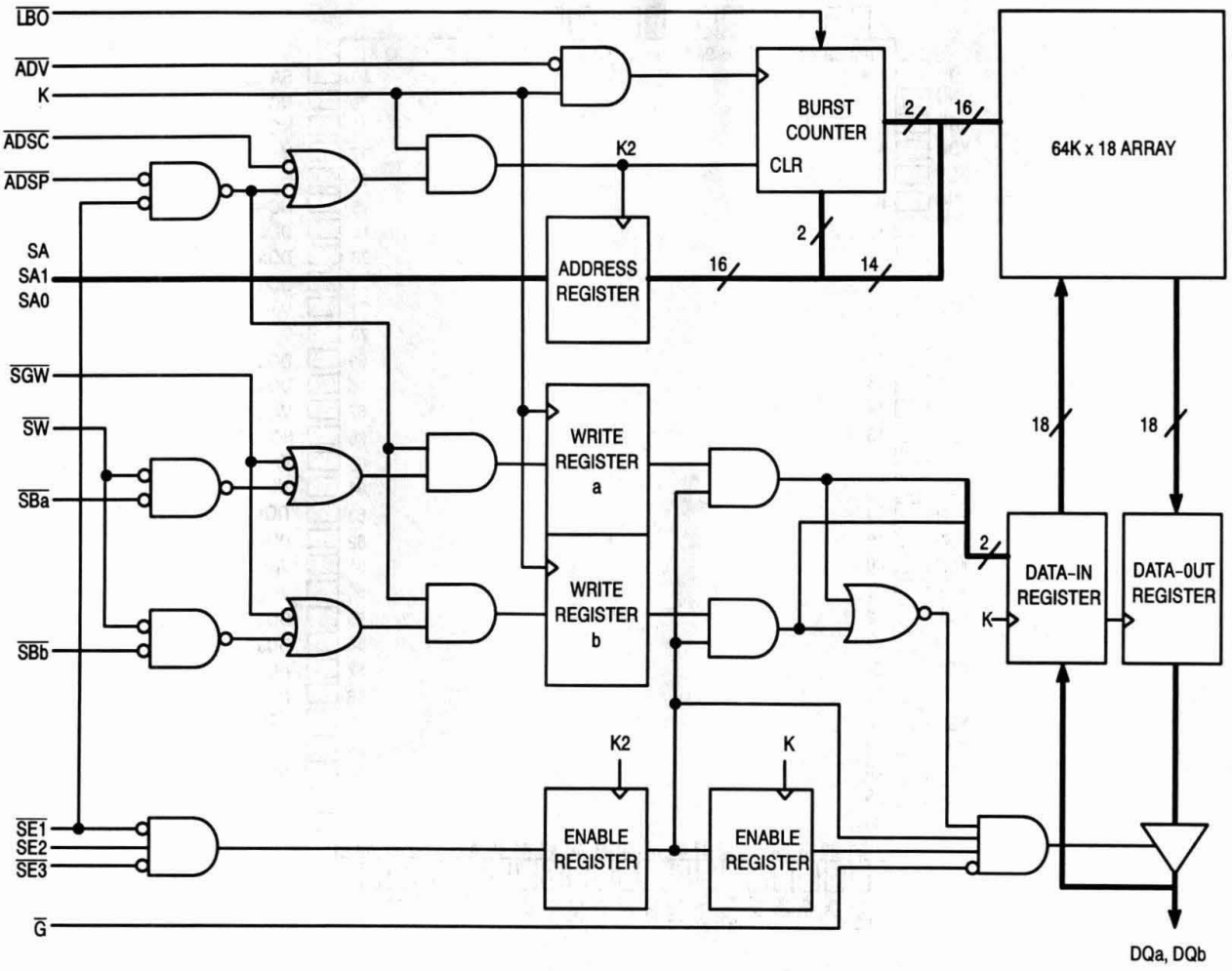
The MCM69P618A operates from a single 3.3 V power supply and all inputs and outputs are LVTTL compatible.

- MCM69P618A–4 = 4 ns access / 7.5 ns cycle
  MCM69P618A–4.5 = 4.5 ns access / 8 ns cycle
  MCM69P618A–5 = 5 ns access / 10 ns cycle
  MCM69P618A–6 = 6 ns access / 12 ns cycle
  MCM69P618A–7 = 7 ns access / 13.3 ns cycle
- Single 3.3 V + 10%, – 5% Power Supply
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Selectable Burst Sequencing Order (Linear/Interleaved)
- Internally Self–Timed Write Cycle
- Byte Write and Global Write Control
- 100 Pin TQFP Package

BurstRAM is a trademark of Motorola, Inc.
The PowerPC name is a trademark of IBM Corp., used under license therefrom.
i960 and Pentium are trademarks of Intel Corp.

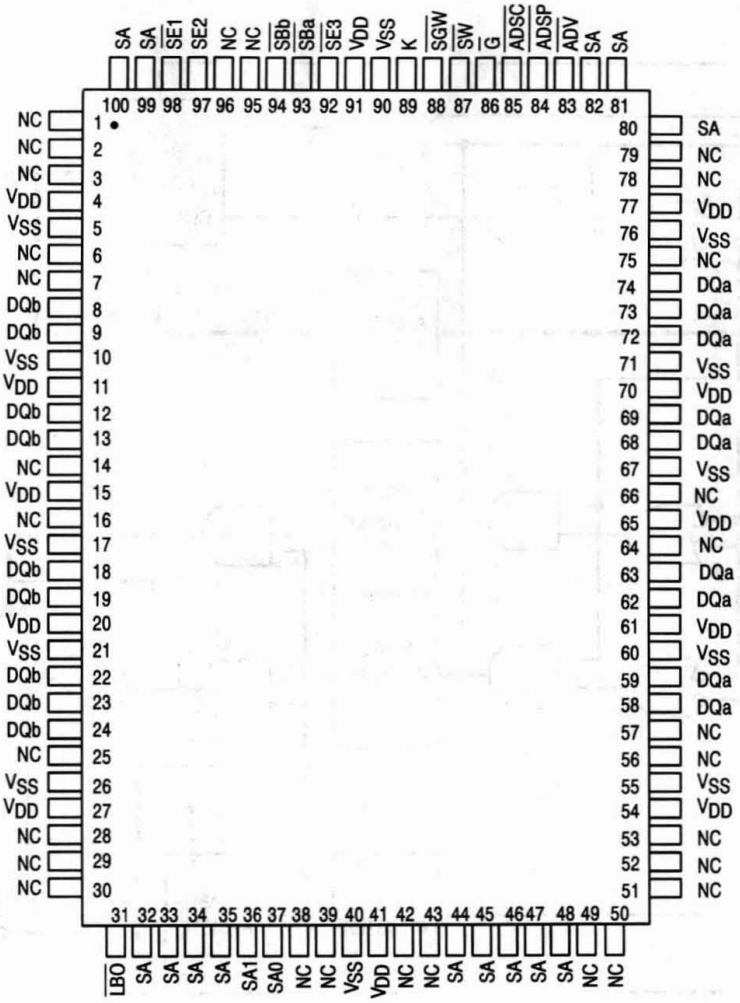
REV 4
4/10/97

FUNCTIONAL BLOCK DIAGRAM



4

PIN ASSIGNMENT



PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: Initiates READ, WRITE, or chip deselect cycle.
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: Initiates READ, WRITE, or chip deselect cycle (exception — chip deselect does not occur when $\overline{ADSP}$ is asserted and $\overline{SE1}$ is high).
83	$\overline{ADV}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
(a) 58, 59, 62, 63, 68, 69, 72, 73, 74 (b) 8, 9, 12, 13, 18, 19, 22, 23, 24	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b).
86	$\overline{G}$	Input	Asynchronous Output Enable Input: Low — enables output buffers (DQx pins). High — DQx pins are high impedance.
89	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$ and $\overline{LBO}$.
31	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst counter (68K/PowerPC). High — interleaved burst counter (486/i960/Pentium).
32, 33, 34, 35, 44, 45, 46, 47, 48, 80, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
36, 37	SA1,SA0	Input	Synchronous Address Inputs: These pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
93, 94 (a) (b)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: "x" refers to the byte being written (byte a, b). $\overline{SGW}$ overrides $\overline{SBx}$.
98	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high–blocks $\overline{ADSP}$ or deselects chip when $\overline{ADSC}$ is asserted.
97	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
92	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
88	$\overline{SGW}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the $\overline{SBx}$ and $\overline{SW}$ signals. If only byte write signals $\overline{SBx}$ are being used, tie this pin high.
87	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{SBx}$ pins. If only byte write signals $\overline{SBx}$ are being used, tie this pin low.
4, 11, 15, 20, 27, 41, 54, 61, 65, 70, 77, 91	V_{DD}	Supply	Power Supply: 3.3 V + 10%, – 5%.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground.
64	NC	Input	No Connection: There is no connection to the chip. For compatibility reasons, it is recommended that this pin be tied low for system designs that do not have a sleep mode associated with the cache/memory controller. Other vendors' RAMs may have implemented the Sleep Mode (ZZ) feature.
1, 2, 3, 6, 7, 14, 16, 25, 28, 29, 30, 38, 39, 42, 43, 49, 50, 51, 52, 53, 56, 57, 66, 75, 78, 79, 95, 96	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE (See Notes 1 through 4)

Next Cycle	Address Used	$\overline{SE1}$	SE2	$\overline{SE3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{G}$ [3]	DQx	Write [2, 4]
Deselect	None	1	X	X	X	0	X	X	High–Z	X
Deselect	None	0	X	1	0	X	X	X	High–Z	X
Deselect	None	0	0	X	0	X	X	X	High–Z	X
Deselect	None	X	X	1	1	0	X	X	High–Z	X
Deselect	None	X	0	X	1	0	X	X	High–Z	X
Begin Read	External	0	1	0	0	X	X	X	High–Z	READ
Begin Read	External	0	1	0	1	0	X	X	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	1	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	0	DQ	READ
Continue Read	Next	1	X	X	X	1	0	1	High–Z	READ
Continue Read	Next	1	X	X	X	1	0	0	DQ	READ
Suspend Read	Current	X	X	X	1	1	1	1	High–Z	READ
Suspend Read	Current	X	X	X	1	1	1	0	DQ	READ
Suspend Read	Current	1	X	X	X	1	1	1	High–Z	READ
Suspend Read	Current	1	X	X	X	1	1	0	DQ	READ
Begin Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Begin Write	Current	1	X	X	X	1	1	X	High–Z	WRITE
Begin Write	External	0	1	0	1	0	X	X	High–Z	WRITE
Continue Write	Next	X	X	X	1	1	0	X	High–Z	WRITE
Continue Write	Next	1	X	X	X	1	0	X	High–Z	WRITE
Suspend Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Suspend Write	Current	1	X	X	X	1	1	X	High–Z	WRITE

NOTES:
1. X = Don't Care. 1 = logic high. 0 = logic low.
2. Write is defined as either 1) any $\overline{SBx}$ and $\overline{SW}$ low or 2) $\overline{SGW}$ is low.
3. $\overline{G}$ is an asynchronous signal and is not sampled by the clock K. $\overline{G}$ drives the bus immediately (t_{GLQX}) following $\overline{G}$ going low.
4. On write cycles that follow read cycles, $\overline{G}$ must be negated prior to the start of the write cycle to ensure proper write data setup times. $\overline{G}$ must also remain negated at the completion of the write cycle to ensure proper write data hold times.

LINEAR BURST ADDRESS TABLE ($\overline{LBO} = V_{SS}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X10	X . . . X11	X . . . X00
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X00	X . . . X01	X . . . X10

INTERLEAVED BURST ADDRESS TABLE ($\overline{LBO} = V_{DD}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00

WRITE TRUTH TABLE

Cycle Type	$\overline{SGW}$	$\overline{SW}$	$\overline{SBa}$	$\overline{SBb}$
Read	H	H	X	X
Read	H	L	H	H
Write Byte a	H	L	L	H
Write Byte b	H	L	H	L
Write All Bytes	H	L	L	L
Write All Bytes	L	X	X	X

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{DD}	V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Package Power Dissipation (See Note 2)	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to 85	°C
Storage Temperature	T_{stg}	– 55 to 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Thermal Resistance Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	40 25	°C/W	2
Thermal Resistance Junction to Board (Bottom)		$R_{\theta JB}$	17	°C/W	3
Thermal Resistance Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.135	3.3	3.6	V
Operating Temperature	T_J	20	—	110	°C
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V

* $V_{IL} \geq -2$ V for $t \leq t_{KHKH}/2$.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit	Notes
Input Leakage Current (0 V ≤ V_{in} ≤ V_{DD}) (Excluding $\overline{LBO}$)		$I_{lkg(I)}$	—	± 1	µA	
Output Leakage Current (0 V ≤ V_{in} ≤ V_{DD})		$I_{lkg(O)}$	—	± 1	µA	
AC Supply Current (Device Selected, All Outputs Open, Cycle Time ≥ t_{KHKH} min)	MCM69P618A–4 (133 MHz) MCM69P618A–4.5 (125 MHz) MCM69P618A–5 (100 MHz) MCM69P618A–6 (83.3 MHz) MCM69P618A–7 (75 MHz)	I_{DDA}	—	TBD TBD 275 260 255	mA	2, 3, 4
CMOS Standby Supply Current (Deselected[1], Clock (K) Cycle Time ≥ t_{KHKH}, All Inputs Toggling at CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{DD} – 0.2 V)	MCM69P618A–4 (133 MHz) MCM69P618A–4.5 (125 MHz) MCM69P618A–5 (100 MHz) MCM69P618A–6 (83.3 MHz) MCM69P618A–7 (75 MHz)	I_{SB1}	—	TBD TBD 130 110 105	mA	1
Clock Running Supply Current (Deselected[1], Clock (K) Cycle Time ≥ t_{KHKH}, All Other Inputs Held to Static CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{DD} – 0.2 V)	MCM69P618A–4 (133MHz) MCM69P618A–4.5 (125 MHz) MCM69P618A–5 (100 MHz) MCM69P618A–6 (83.3 MHz) MCM69P618A–7 (75 MHz)	I_{SB2}	—	TBD TBD 45 40 40	mA	1
Output Low Voltage (I_{OL} = 8 mA)		V_{OL}	—	0.4	V	
Output High Voltage (I_{OH} = – 4 mA)		V_{OH}	2.4	—	V	

NOTES:
1. Device in Deselected mode as defined by the Truth Table.
2. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
3. All addresses transition simultaneously low (LSB) and then high (MSB).
4. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	4	6	pF
Input/Output Capacitance	$C_{I/O}$	—	7	9	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1 Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	69P618A–4		69P618A–4.5		69P618A–5		69P618A–6		69P618A–7		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	7.5	—	8	—	10	—	12	—	13.3	—	ns	6
Clock High Pulse Width	t_{KHKL}	3	—	3	—	3	—	4	—	4.5	—	ns	
Clock Low Pulse Width	t_{KLKH}	3	—	3	—	3	—	4	—	4.5	—	ns	
Clock Access Time	t_{KHQV}	—	4	—	4.5	—	5	—	6	—	7	ns	4
Output Enable to Output Valid	t_{GLQV}	—	4	—	4.5	—	5	—	5	—	6	ns	4
Clock High to Output Active	t_{KHQX1}	1.5	—	1.5	—	0	—	0	—	0	—	ns	4, 6
Clock High to Output Change	t_{KHQX2}	1.5	—	1.5	—	2	—	2	—	2	—	ns	4, 6
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	0	—	ns	4, 6
Output Disable to Q High–Z	t_{GHQZ}	—	4	—	4.5	—	5	—	5	—	5	ns	5, 6
Clock High to Q High–Z	t_{KHQZ}	2	4	2	4.5	2	5	2	5	2	5	ns	5, 6
Setup Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	t_{ADKH} t_{ADSKH} t_{DVKH} t_{WVKH} t_{EVKH}	2	—	2.5	—	2.5	—	2.5	—	2.5	—	ns	
Hold Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	t_{KHAX} t_{KHADSX} t_{KHDX} t_{KHWX} t_{KHEX}	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns	

NOTES:
1. Write is defined as either any $\overline{SBx}$ and $\overline{SW}$ low or $\overline{SGW}$ is low. Chip Enable is defined as $\overline{SE1}$ low, SE2 high and $\overline{SE3}$ low whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care after write cycle begins. To prevent bus contention, $\overline{G}$ should be negated prior to start of write cycle.
4. Tested per AC Test Load (See Figure 1).
5. Measured at ± 200 mV from steady state.
6. This parameter is sampled and not 100% tested.

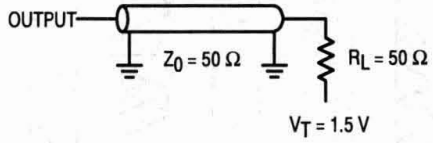
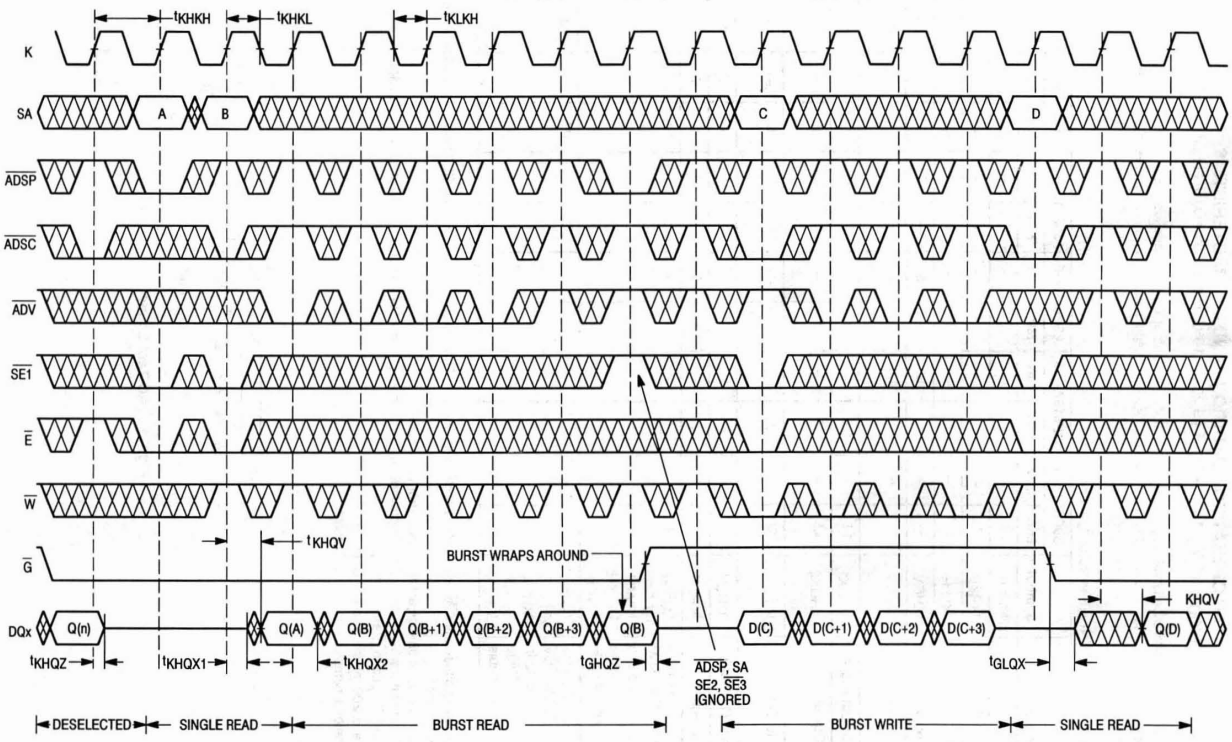


Figure 1. AC Test Loads

READ/WRITE CYCLES



Note: E low = SE2 high and SE3 low.
W low = SGW low and / or SW and SBx low.

APPLICATION INFORMATION

The MCM69P618A BurstRAM is a high speed synchronous SRAM that is intended for use primarily in secondary or level two (L2) cache memory applications. L2 caches are found in a variety of classes of computers – from the desktop personal computer to the high–end servers and transaction processing machines. For simplicity, the majority of L2 caches today are direct mapped and are single bank implementations. These caches tend to be designed for bus speeds in the range of 33 to 66 MHz. At these bus rates, non–pipelined (flow–through) BurstRAMs can be used since their access times meet the speed requirements for a minimum–latency, zero–wait state L2 cache interface. Latency is a measure (time) of "dead" time the memory system exhibits as a result of a memory request.

For those applications that demand bus operation at greater than 66 MHz or multi–bank L2 caches at 66 MHz, the pipelined (register/register) version of the 64K x 18 BurstRAM (MCM69P618A) allows the user to configure the RAM to support such designs. Multiple banks of BurstRAMs create additional bus loading and can cause the system to otherwise miss its timing requirements. The access time (clock–to–valid–data) of a pipelined BurstRAM is inherently faster than a non–pipelined device by a few nanoseconds. This does not come without cost. The cost is latency – "dead" time.

Since most L2 caches are tied to the processor bus and bus speeds continue to increase over time, pipelined (R/R) BurstRAMs are the best choice in achieving zero–wait state L2 cache performance. At bus speeds ranging from 66 MHz to 100 MHz, pipelined BurstRAMs are able to provide fast clock to valid data times required of these high speed buses.

FUNCTIONAL EQUIVALENT

The following describes the configuration of the MCM69P618A as a functional equivalent to a 5 V BurstRAM. A migration from 5 V BurstRAMs to 3.3 V BurstRAMs (e.g. MCM69P618A) can be somewhat confusing due to functional and pinout differences. Because the 3.3 V devices offer more pins than the 5 V devices, it is no longer necessary to supply multiple part numbers for the different burst, address pipelined, etc., options. The MCM69P618A can be configured to function as if it were one of the 5 V BurstRAMs. The following table lists control pins on the MCM69P618A that can be tied off to either 3.3 V or ground in order to satisfy the migration to this 3.3 V RAM.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

5 V Device Numbers	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
MCM67C618	—	—	—	L	H
MCM67J618	—	—	—	—	H
MCM67N618	—	—	—	L	L

NOTE: If no tie value is given, then the pin should be used as intended on the 5 V device.

NON–BURST SYNCHRONOUS OPERATION

Although this BurstRAM has been designed for 68K–, PowerPC–, 486–, i960, and Pentium – based systems, these SRAMs can be used in other high speed L2 cache or memory applications that do not require the burst address feature. Most L2 caches designed with a synchronous interface can make use of the MCM69P618A. The burst counter feature of the BurstRAM can be disabled, and the SRAM can be configured to act upon a continuous stream of addresses. See Figure 2.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

Non–Burst	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
Sync Non–Burst, Pipelined SRAM	H	L	H	L	X

NOTE: Although X is specified in the table as a don't care, the pin must be tied either high or low.

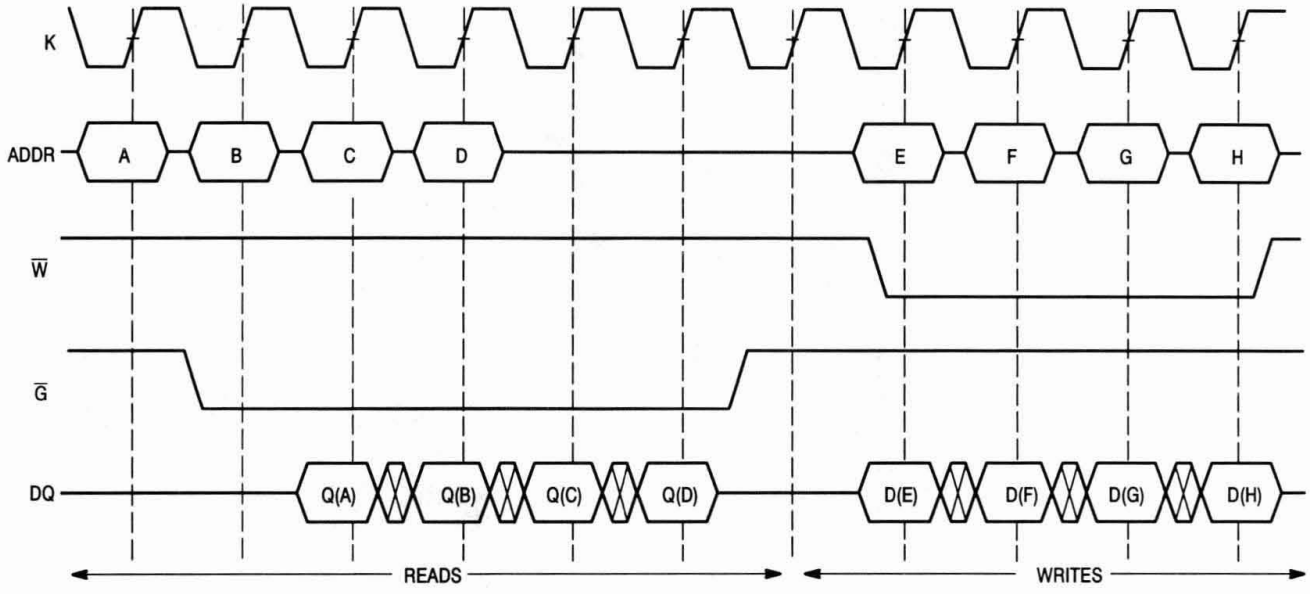
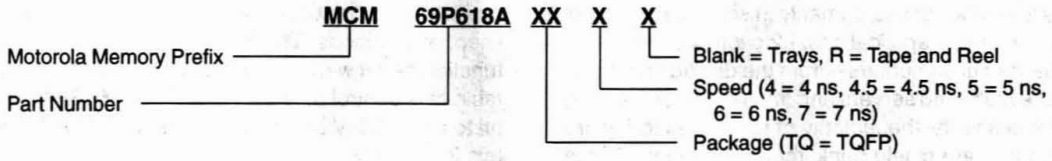


Figure 2. Configured as Non–Burst Synchronous SRAM (Register/Register Mode)

ORDERING INFORMATION
(Order by Full Part Number)

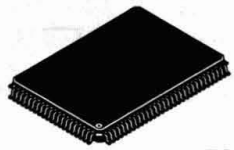

MCM 69P618A XX X X
Motorola Memory Prefix
Part Number
Blank = Trays, R = Tape and Reel
Speed (4 = 4 ns, 4.5 = 4.5 ns, 5 = 5 ns, 6 = 6 ns, 7 = 7 ns)
Package (TQ = TQFP)

Full Part Numbers —		
	MCM69P618ATQ4	MCM69P618ATQ4R
	MCM69P618ATQ4.5	MCM69P618ATQ4.5R
	MCM69P618ATQ5	MCM69P618ATQ5R
	MCM69P618ATQ6	MCM69P618ATQ6R
	MCM69P618ATQ7	MCM69P618ATQ7R

4

MCM69P618C

64K x 18 Bit Pipelined BurstRAM™ Synchronous Fast Static RAM



TQ PACKAGE
TQFP
CASE 983A–01

The MCM69P618C is a 1M bit synchronous fast static RAM designed to provide a burstable, high performance, secondary cache for the 68K Family, PowerPC™, 486, i960™ and Pentium™ microprocessors. It is organized as 64K words of 18 bits each. This device integrates input registers, an output register, a 2–bit address counter, and high speed SRAM onto a single monolithic circuit for reduced parts count in cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (SA), data inputs (DQx), and all control signals except output enable ($\overline{G}$) and Linear Burst Order ($\overline{LBO}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ input pins. Subsequent burst addresses can be generated internally by the MCM69P618C (burst sequence operates in linear or interleaved mode dependent upon state of $\overline{LBO}$) and controlled by the burst address advance ($\overline{ADV}$) input pin.

Write cycles are internally self–timed and initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased timing flexibility for incoming signals.

Synchronous byte write ($\overline{SBx}$), synchronous global write ($\overline{SGW}$), and synchronous write enable $\overline{SW}$ are provided to allow writes to either individual bytes or to both bytes. The two bytes are designated as "a" and "b". $\overline{SBa}$ controls DQa and $\overline{SBb}$ controls DQb. Individual bytes are written if the selected byte writes $\overline{SBx}$ are asserted with $\overline{SW}$. Both bytes are written if either $\overline{SGW}$ is asserted or if both $\overline{SBx}$ and $\overline{SW}$ are asserted.

For read cycles, pipelined SRAMs output data is temporarily stored by an edge–triggered output register and then released to the output buffers at the next rising edge of clock (K).

The MCM69P618C operates from a single 3.3 V power supply and all inputs and outputs are LVTTL compatible and 5V tolerant.

- MCM69P618C–4 = 4 ns access / 7.5 ns cycle
  MCM69P618C–4.5 = 4.5 ns access / 8 ns cycle
  MCM69P618C–5 = 5 ns access / 10 ns cycle
  MCM69P618C–6 = 6 ns access / 12 ns cycle
  MCM69P618C–7 = 7 ns access / 13.3 ns cycle
- Single 3.3 V + 10%, – 5% Power Supply
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Selectable Burst Sequencing Order (Linear/Interleaved)
- Internally Self–Timed Write Cycle
- Byte Write and Global Write Control
- 100 Pin TQFP Package
- 5V Tolerant on all Pins (Inputs and I/O's)
- Single–Cycle Deselect Timing

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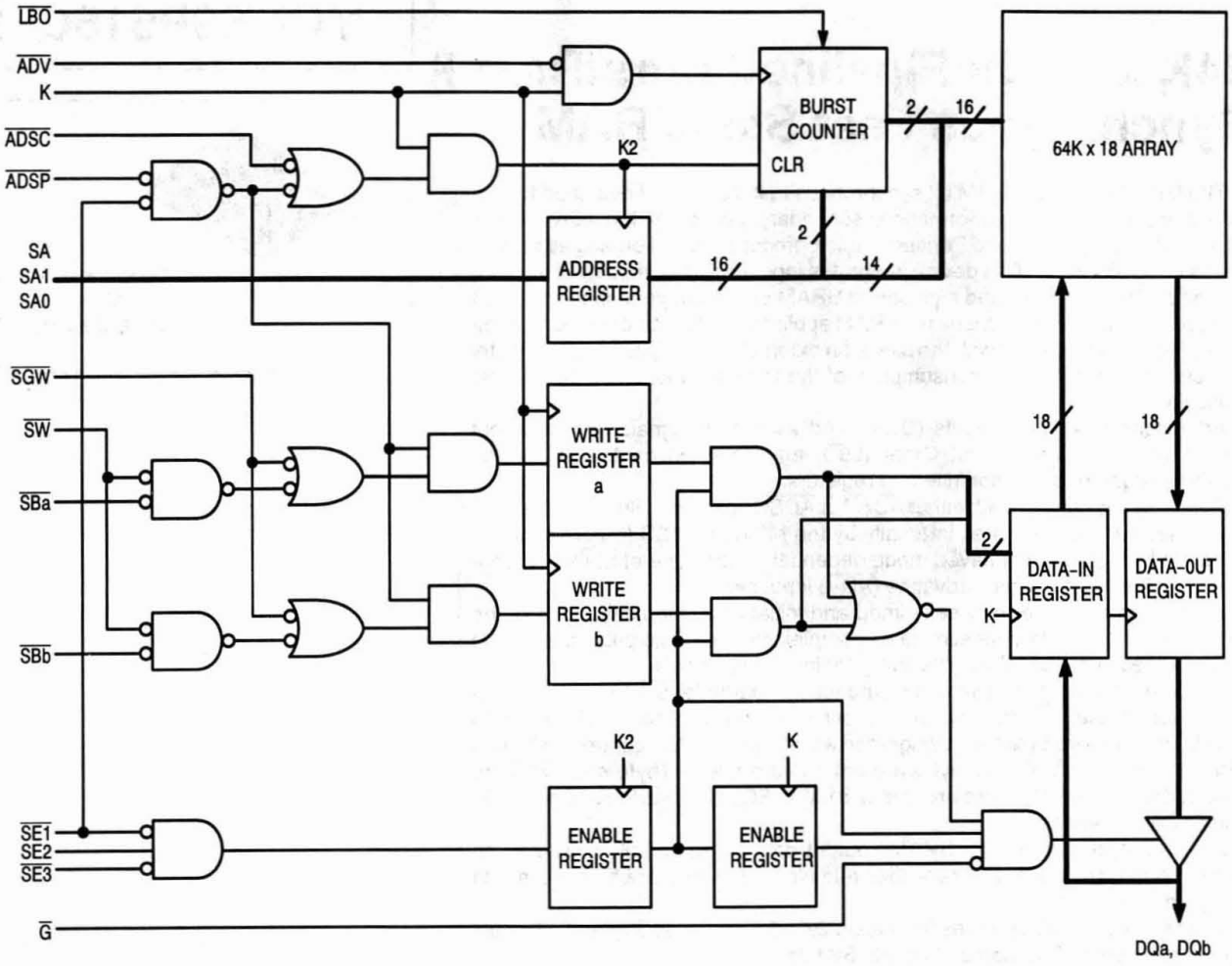
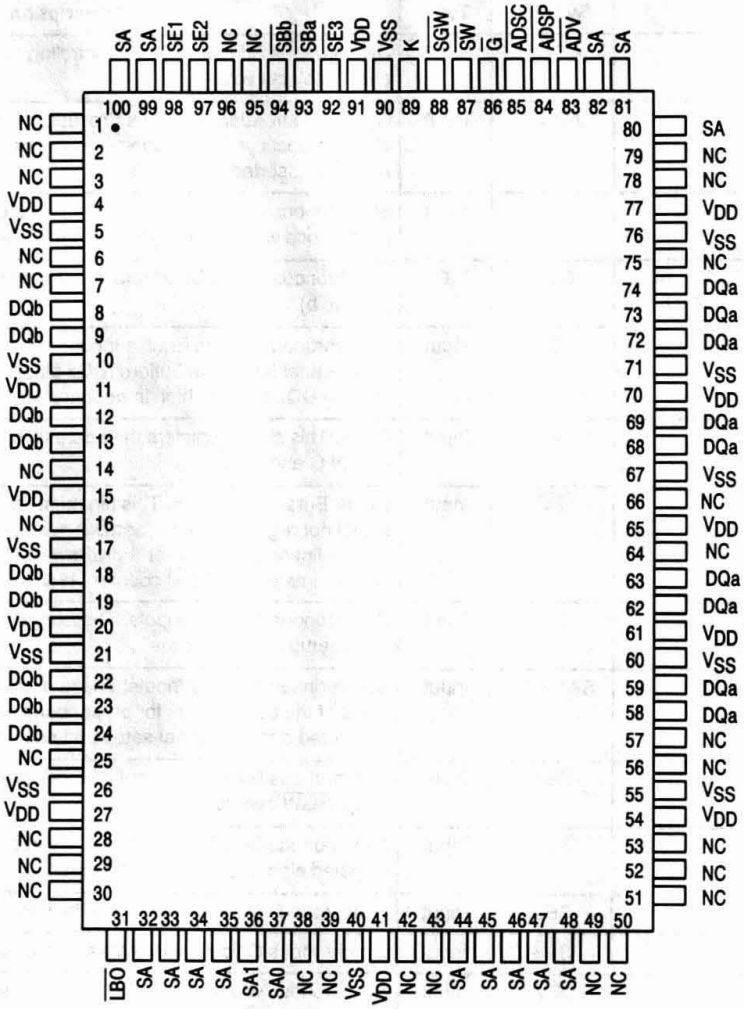
The PowerPC name is a trademark of IBM Corp., used under license therefrom.
i960 and Pentium are trademarks of Intel Corp.

REV 1
4/10/97

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENT



4

PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: Initiates READ, WRITE, or chip deselect cycle.
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: Initiates READ, WRITE, or chip deselect cycle (exception — chip deselect does not occur when $\overline{ADSP}$ is asserted and $\overline{SE1}$ is high).
83	$\overline{ADV}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
(a) 58, 59, 62, 63, 68, 69, 72, 73, 74 (b) 8, 9, 12, 13, 18, 19, 22, 23, 24	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b).
86	$\overline{G}$	Input	Asynchronous Output Enable Input: Low — enables output buffers (DQx pins). High — DQx pins are high impedance.
89	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$ and $\overline{LBO}$.
31	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst counter (68K/PowerPC). High — interleaved burst counter (486/i960/Pentium).
32, 33, 34, 35, 44, 45, 46, 47, 48, 80, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
36, 37	SA1,SA0	Input	Synchronous Address Inputs: These pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
93, 94 (a) (b)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: "x" refers to the byte being written (byte a, b). $\overline{SGW}$ overrides $\overline{SBx}$.
98	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high–blocks $\overline{ADSP}$ or deselects chip when $\overline{ADSC}$ is asserted.
97	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
92	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
88	$\overline{SGW}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the $\overline{SBx}$ and $\overline{SW}$ signals. If only byte write signals $\overline{SBx}$ are being used, tie this pin high.
87	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{SBx}$ pins. If only byte write signals $\overline{SBx}$ are being used, tie this pin low.
4, 11, 15, 20, 27, 41, 54, 61, 65, 70, 77, 91	V_{DD}	Supply	Power Supply: 3.3 V + 10%, – 5%.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground.
64	NC	Input	No Connection: There is no connection to the chip. For compatibility reasons, it is recommended that this pin be tied low for system designs that do not have a sleep mode associated with the cache/memory controller. Other vendors' RAMs may have implemented the Sleep Mode (ZZ) feature.
1, 2, 3, 6, 7, 14, 16, 25, 28, 29, 30, 38, 39, 42, 43, 49, 50, 51, 52, 53, 56, 57, 66, 75, 78, 79, 95, 96	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE (See Notes 1 through 4)

Next Cycle	Address Used	$\overline{SE1}$	SE2	$\overline{SE3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{G}$ [3]	DQx	Write [2, 4]
Deselect	None	1	X	X	X	0	X	X	High–Z	X
Deselect	None	0	X	1	0	X	X	X	High–Z	X
Deselect	None	0	0	X	0	X	X	X	High–Z	X
Deselect	None	X	X	1	1	0	X	X	High–Z	X
Deselect	None	X	0	X	1	0	X	X	High–Z	X
Begin Read	External	0	1	0	0	X	X	X	High–Z	READ
Begin Read	External	0	1	0	1	0	X	X	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	1	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	0	DQ	READ
Continue Read	Next	1	X	X	X	1	0	1	High–Z	READ
Continue Read	Next	1	X	X	X	1	0	0	DQ	READ
Suspend Read	Current	X	X	X	1	1	1	1	High–Z	READ
Suspend Read	Current	X	X	X	1	1	1	0	DQ	READ
Suspend Read	Current	1	X	X	X	1	1	1	High–Z	READ
Suspend Read	Current	1	X	X	X	1	1	0	DQ	READ
Begin Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Begin Write	Current	1	X	X	X	1	1	X	High–Z	WRITE
Begin Write	External	0	1	0	1	0	X	X	High–Z	WRITE
Continue Write	Next	X	X	X	1	1	0	X	High–Z	WRITE
Continue Write	Next	1	X	X	X	1	0	X	High–Z	WRITE
Suspend Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Suspend Write	Current	1	X	X	X	1	1	X	High–Z	WRITE

NOTES:
1. X = Don't Care. 1 = logic high. 0 = logic low.
2. Write is defined as either 1) any $\overline{SBx}$ and $\overline{SW}$ low or 2) $\overline{SGW}$ is low.
3. $\overline{G}$ is an asynchronous signal and is not sampled by the clock K. $\overline{G}$ drives the bus immediately (t_{GLQX}) following $\overline{G}$ going low.
4. On write cycles that follow read cycles, $\overline{G}$ must be negated prior to the start of the write cycle to ensure proper write data setup times. $\overline{G}$ must also remain negated at the completion of the write cycle to ensure proper write data hold times.

LINEAR BURST ADDRESS TABLE ($\overline{LBO} = V_{SS}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X10	X . . . X11	X . . . X00
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X00	X . . . X01	X . . . X10

INTERLEAVED BURST ADDRESS TABLE ($\overline{LBO} = V_{DD}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00

WRITE TRUTH TABLE

Cycle Type	$\overline{SGW}$	$\overline{SW}$	$\overline{SBa}$	$\overline{SBb}$
Read	H	H	X	X
Read	H	L	H	H
Write Byte a	H	L	L	H
Write Byte b	H	L	H	L
Write All Bytes	H	L	L	L
Write All Bytes	L	X	X	X

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{DD}	V_{in}, V_{out}	– 0.5 to 6.0	V
Output Current (per I/O)	I_{out}	± 20	mA
Package Power Dissipation (See Note 2)	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to 85	°C
Storage Temperature	T_{stg}	– 55 to 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Thermal Resistance Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	40 25	°C/W	1, 2
Thermal Resistance Junction to Board (Bottom)		$R_{\theta JB}$	17	°C/W	1, 3
Thermal Resistance Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	1, 4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.135	3.3	3.6	V
Operating Temperature	T_J	20	—	110	°C
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	5.5**	V

*$V_{IL} \geq -2$ V for $t \leq t_{KHKH}/2$.

**$V_{IH} \leq 6$ V for $t \leq t_{KHKH}/2$.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit	Notes
Input Leakage Current (0 V ≤ V_{in} ≤ V_{DD}) (Excluding $\overline{LBO}$)		$I_{lkg(I)}$	—	± 1	µA	
Output Leakage Current (0 V ≤ V_{in} ≤ V_{DD})		$I_{lkg(O)}$	—	± 1	µA	
AC Supply Current (Device Selected, All Outputs Open, Cycle Time ≥ t_{KHKH} min)	MCM69P618C–4 (133 MHz) MCM69P618C–4.5 (125 MHz) MCM69P618C–5 (100 MHz) MCM69P618C–6 (83.3 MHz) MCM69P618C–7 (75 MHz)	I_{DDA}	—	TBD TBD 275 260 255	mA	2, 3, 4
CMOS Standby Supply Current (Deselected[1], Clock (K) Cycle Time ≥ t_{KHKH}, All Inputs Toggling at CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{DD} – 0.2 V)	MCM69P618C–4 (133 MHz) MCM69P618C–4.5 (125 MHz) MCM69P618C–5 (100 MHz) MCM69P618C–6 (83.3 MHz) MCM69P618C–7 (75 MHz)	I_{SB1}	—	TBD TBD 130 110 105	mA	1
Clock Running Supply Current (Deselected[1], Clock (K) Cycle Time ≥ t_{KHKH}, All Other Inputs Held to Static CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{DD} – 0.2 V)	MCM69P618C–4 (133MHz) MCM69P618C–4.5 (125 MHz) MCM69P618C–5 (100 MHz) MCM69P618C–6 (83.3 MHz) MCM69P618C–7 (75 MHz)	I_{SB2}	—	TBD TBD 45 40 40	mA	1
Output Low Voltage (I_{OL} = 8 mA)		V_{OL}	—	0.4	V	
Output High Voltage (I_{OH} = – 4 mA)		V_{OH}	2.4	—	V	

NOTES:
1. Device in Deselected mode as defined by the Truth Table.
2. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
3. All addresses transition simultaneously low (LSB) and then high (MSB).
4. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	4	6	pF
Input/Output Capacitance	$C_{I/O}$	—	7	9	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1 Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	69P618A–4		69P618A–4.5		69P618A–5		69P618A–6		69P618A–7		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	7.5	—	8	—	10	—	12	—	13.3	—	ns	6
Clock High Pulse Width	t_{KHKL}	3	—	3	—	3	—	4	—	4.5	—	ns	
Clock Low Pulse Width	t_{KLKH}	3	—	3	—	3	—	4	—	4.5	—	ns	
Clock Access Time	t_{KHQV}	—	4	—	4.5	—	5	—	6	—	7	ns	4
Output Enable to Output Valid	t_{GLQV}	—	4	—	4.5	—	5	—	5	—	6	ns	4
Clock High to Output Active	t_{KHQX1}	1.5	—	1.5	—	0	—	0	—	0	—	ns	4, 6
Clock High to Output Change	t_{KHQX2}	1.5	—	1.5	—	2	—	2	—	2	—	ns	4, 6
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	0	—	ns	4, 6
Output Disable to Q High–Z	t_{GHQZ}	—	4	—	4.5	—	5	—	5	—	5	ns	5, 6
Clock High to Q High–Z	t_{KHQZ}	2	4	2	4.5	2	5	2	5	2	5	ns	5, 6
Setup Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	t_{ADKH} t_{ADSKH} t_{DVKH} t_{WVKH} t_{EVKH}	2	—	2.5	—	2.5	—	2.5	—	2.5	—	ns	
Hold Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	t_{KHAX} t_{KHADSX} t_{KHDX} t_{KHWX} t_{KHEX}	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns	

NOTES:
1. Write is defined as either any $\overline{SBx}$ and $\overline{SW}$ low or $\overline{SGW}$ is low. Chip Enable is defined as $\overline{SE1}$ low, SE2 high and $\overline{SE3}$ low whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care after write cycle begins. To prevent bus contention, $\overline{G}$ should be negated prior to start of write cycle.
4. Tested per AC Test Load (See Figure 1).
5. Measured at ± 200 mV from steady state.
6. This parameter is sampled and not 100% tested.

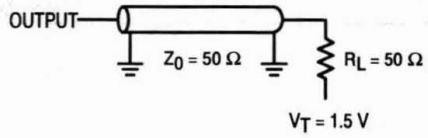
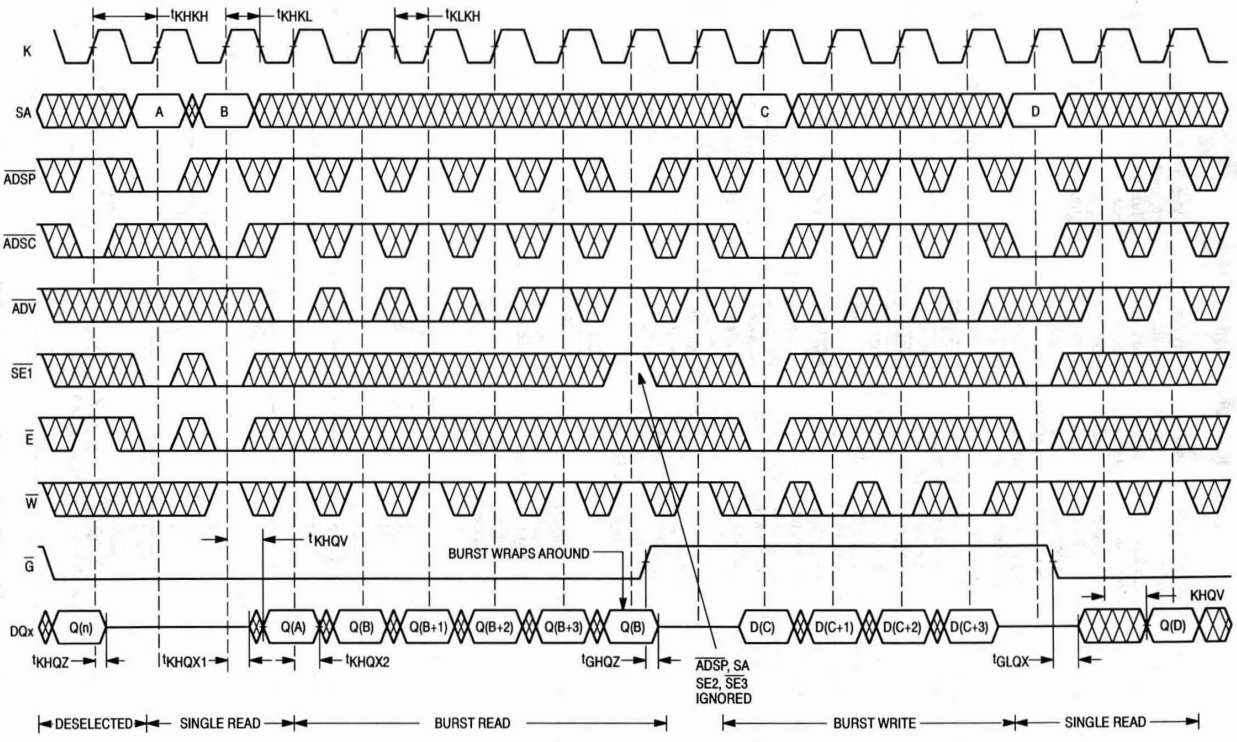


Figure 1. AC Test Loads

READ/WRITE CYCLES



Note: E low = SE2 high and SE3 low.
W low = SGW low and / or SW and SBx low.

APPLICATION INFORMATION

The MCM69P618C BurstRAM is a high speed synchronous SRAM that is intended for use primarily in secondary or level two (L2) cache memory applications. L2 caches are found in a variety of classes of computers – from the desktop personal computer to the high–end servers and transaction processing machines. For simplicity, the majority of L2 caches today are direct mapped and are single bank implementations. These caches tend to be designed for bus speeds in the range of 33 to 66 MHz. At these bus rates, non–pipelined (flow–through) BurstRAMs can be used since their access times meet the speed requirements for a minimum–latency, zero–wait state L2 cache interface. Latency is a measure (time) of "dead" time the memory system exhibits as a result of a memory request.

For those applications that demand bus operation at greater than 66 MHz or multi–bank L2 caches at 66 MHz, the pipelined (register/register) version of the 64K x 18 BurstRAM (MCM69P618C) allows the user to configure the RAM to support such designs. Multiple banks of BurstRAMs create additional bus loading and can cause the system to otherwise miss its timing requirements. The access time (clock–to–valid–data) of a pipelined BurstRAM is inherently faster than a non–pipelined device by a few nanoseconds. This does not come without cost. The cost is latency – "dead" time.

Since most L2 caches are tied to the processor bus and bus speeds continue to increase over time, pipelined (R/R) BurstRAMs are the best choice in achieving zero–wait state L2 cache performance. At bus speeds ranging from 66 MHz to 100 MHz, pipelined BurstRAMs are able to provide fast clock to valid data times required of these high speed buses.

FUNCTIONAL EQUIVALENT

The following describes the configuration of the MCM69P618C as a functional equivalent to a 5 V BurstRAM. A migration from 5 V BurstRAMs to 3.3 V BurstRAMs (e.g. MCM69P618C) can be somewhat confusing due to functional and pinout differences. Because the 3.3 V devices offer more pins than the 5 V devices, it is no longer necessary to supply multiple part numbers for the different burst, address pipelined, etc., options. The MCM69P618C can be configured to function as if it were one of the 5 V BurstRAMs. The following table lists control pins on the MCM69P618C that can be tied off to either 3.3 V or ground in order to satisfy the migration to this 3.3 V RAM.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

5 V Device Numbers	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
MCM67C618	—	—	—	L	H
MCM67J618	—	—	—	—	H
MCM67N618	—	—	—	L	L

NOTE: If no tie value is given, then the pin should be used as intended on the 5 V device.

NON–BURST SYNCHRONOUS OPERATION

Although this BurstRAM has been designed for 68K–, PowerPC–, 486–, i960, and Pentium – based systems, these SRAMs can be used in other high speed L2 cache or memory applications that do not require the burst address feature. Most L2 caches designed with a synchronous interface can make use of the MCM69P618C. The burst counter feature of the BurstRAM can be disabled, and the SRAM can be configured to act upon a continuous stream of addresses. See Figure 2.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

Non–Burst	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
Sync Non–Burst, Pipelined SRAM	H	L	H	L	X

NOTE: Although X is specified in the table as a don't care, the pin must be tied either high or low.

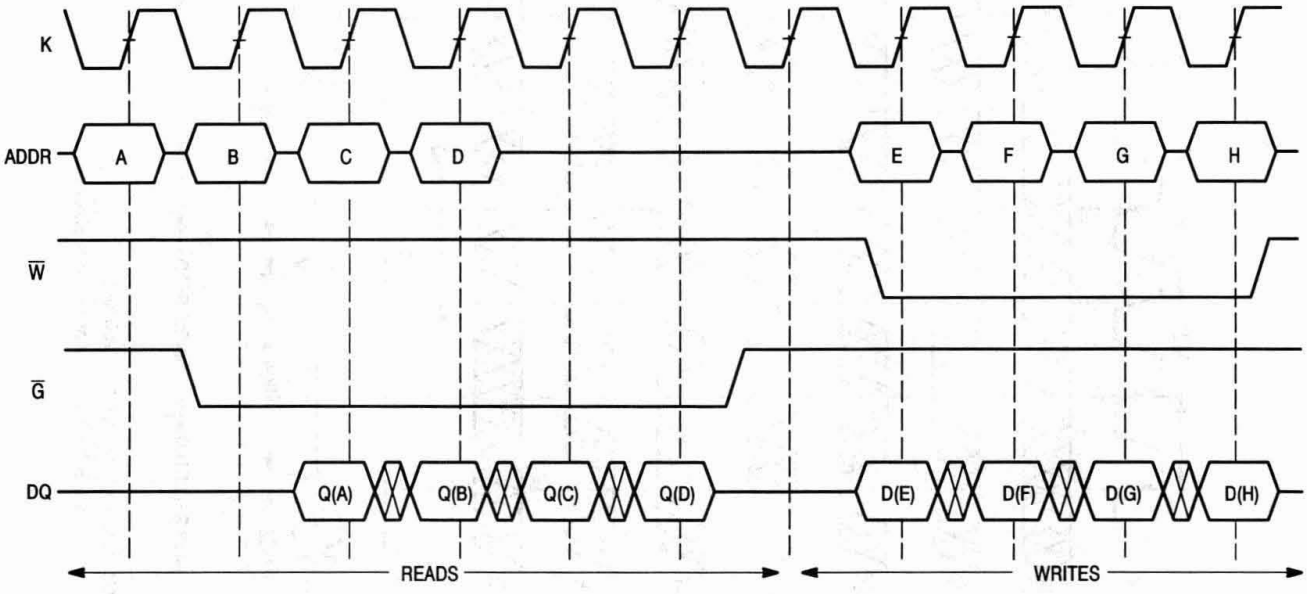
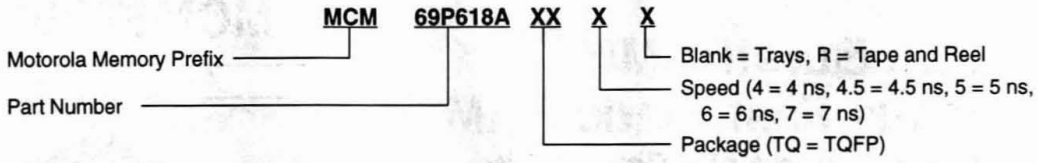


Figure 2. Configured as Non–Burst Synchronous SRAM (Register/Register Mode)

ORDERING INFORMATION
(Order by Full Part Number)


MCM 69P618A XX X X
Motorola Memory Prefix
Part Number
Blank = Trays, R = Tape and Reel
Speed (4 = 4 ns, 4.5 = 4.5 ns, 5 = 5 ns, 6 = 6 ns, 7 = 7 ns)
Package (TQ = TQFP)

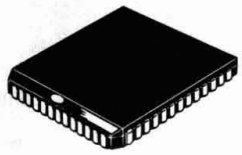
Full Part Numbers —		
	MCM69P618CTQ4	MCM69P618CTQ4R
	MCM69P618CTQ4.5	MCM69P618CTQ4.5R
	MCM69P618CTQ5	MCM69P618CTQ5R
	MCM69P618CTQ6	MCM69P618CTQ6R
	MCM69P618CTQ7	MCM69P618CTQ7R

4

MCM67B618A

64K x 18 Bit BurstRAM™ Synchronous Fast Static RAM

With Burst Counter and Self–Timed Write



FN PACKAGE
PLASTIC
CASE 778–02

The MCM67B618A is a 1,179,648 bit synchronous fast static random access memory designed to provide a burstable, high–performance, secondary cache for the i486™ and Pentium™ microprocessors. It is organized as 65,536 words of 18 bits. The device integrates input registers, a 2–bit counter, high speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A15), data inputs (D0 – D17), and all control signals except output enable ($\overline{G}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be generated internally by the MCM67B618A (burst sequence imitates that of the i486 and Pentium) and controlled by the burst address advance ($\overline{ADV}$) input pin. The following pages provide more detailed information on burst controls.

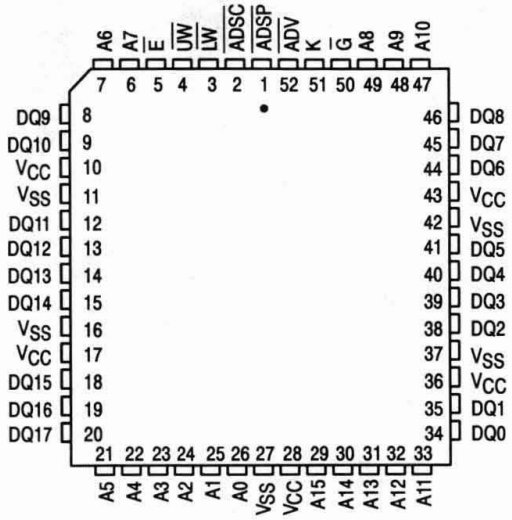
Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased flexibility for incoming signals.

Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits), while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

This device is ideally suited for systems that require wide data bus widths and cache memory. See Figure 2 for applications information.

- Single 5 V ± 5% Power Supply
- Fast Access Times: 9/10/12 ns Max
- Byte Writeable via Dual Write Enables
- Internal Input Registers (Address, Data, Control)
- Internally Self–Timed Write Cycle
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three–State Outputs
- Common Data Inputs and Data Outputs
- 3.3 V I/O Compatible
- High Board Density 52–Lead PLCC Package

PIN ASSIGNMENT



PIN NAMES	
A0 – A15	Address Inputs
K	Clock
$\overline{ADV}$	Burst Address Advance
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Upper Byte Write Enable
$\overline{ADSC}$	Controller Address Status
$\overline{ADSP}$	Processor Address Status
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

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i486 and Pentium are trademarks of Intel Corp.

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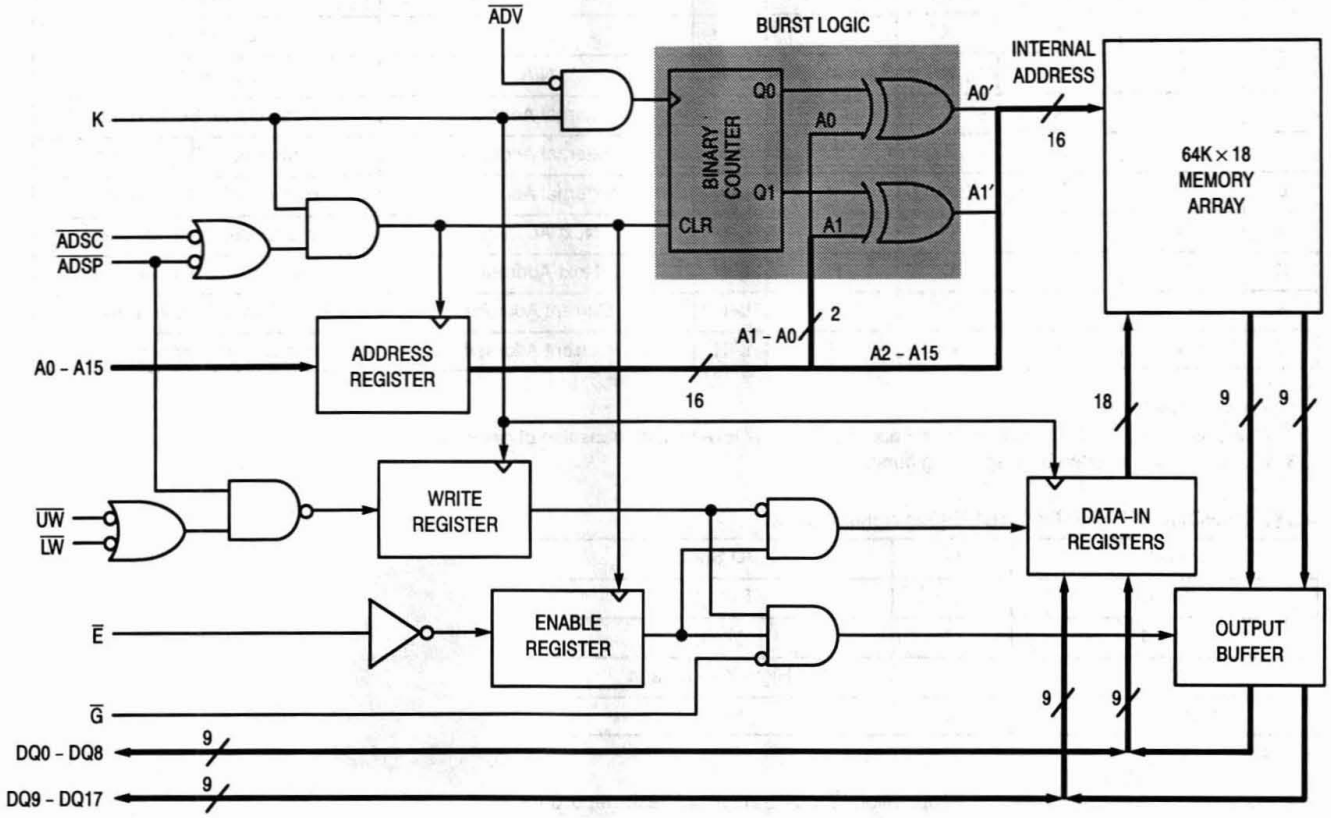
BLOCK DIAGRAM (See Note)



NOTE: All registers are positive–edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{ADSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{ADSC}$) is performed using the new external address. Alternatively, an $\overline{ADSP}$–initiated two cycle WRITE can be performed by asserting $\overline{ADSP}$ and a valid address on the first cycle, then negating both $\overline{ADSP}$ and $\overline{ADSC}$ and asserting $\overline{LW}$ and/or $\overline{UW}$ with valid data on the second cycle (see Single Write Cycle in WRITE CYCLES timing diagram).
When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{ADV}$ controls subsequent burst cycles. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE TABLE (See Note)

External Address	A15 – A2	A1	A0
1st Burst Address	A15 – A2	A1	$\overline{A0}$
2nd Burst Address	A15 – A2	$\overline{A1}$	A0
3rd Burst Address	A15 – A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{UW}$ or $\overline{LW}$	K	Address Used	Operation
H	L	X	X	X	L–H	N/A	Deselected
H	X	L	X	X	L–H	N/A	Deselected
L	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low–to–high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out
Read	H	High–Z
Write	X	High–Z — Data In
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA9} I_{CCA10} I_{CCA12}	—	275 265 250	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	95	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible i486 and Pentium bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1a Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM67B618A–9		MCM67B618A–10		MCM67B618A–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	15	—	16.6	—	20	—	ns	
Clock Access Time	t_{KHQV}	—	9	—	10	—	12	ns	5
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	6	ns	
Clock High to Output Active	t_{KHQX1}	6	—	6	—	6	—	ns	
Clock High to Output Change	t_{KHQX2}	3	—	3	—	3	—	ns	
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	
Output Disable to Q High–Z	t_{GHQZ}	—	6	—	7	—	7	ns	6
Clock High to Q High–Z	t_{KHQZ}	3	6	3	7	—	7	ns	
Clock High Pulse Width	t_{KHKL}	5	—	5	—	6	—	ns	
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	6	—	ns	
Setup Times: Address Address Status Data In Write Address Advance Chip Enable	t_{AVKH} t_{ADSVKH} t_{DVKH} t_{WVKH} t_{ADVVKH} t_{EVKH}	2.5	—	2.5	—	2.5	—	ns	7
Hold Times: Address Address Status Data In Write Address Advance Chip Enable	t_{KHAX} t_{KHADSX} t_{KHDX} t_{KHWX} t_{KHADVX} t_{KHEX}	0.5	—	0.5	—	0.5	—	ns	7

NOTES:
1. In setup and hold times, W (write) refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{ADSP}$ high for the setup and hold times.
3. All read and write cycle timings are referenced from K or $\overline{G}$.
4. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
5. Maximum access times are guaranteed for all possible i486 and Pentium external bus cycles.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1b. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of K whenever $\overline{ADSP}$ or $\overline{ADSC}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is enabled. Chip enable must be valid at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled.

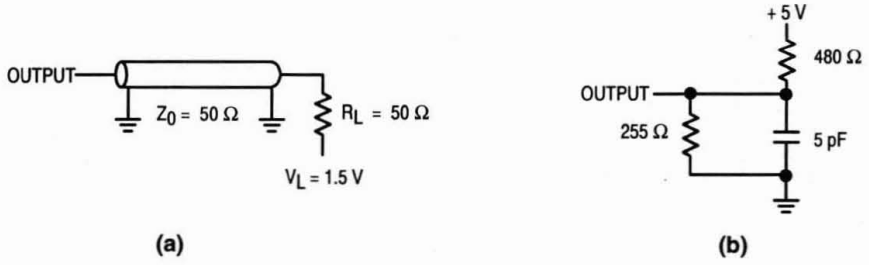
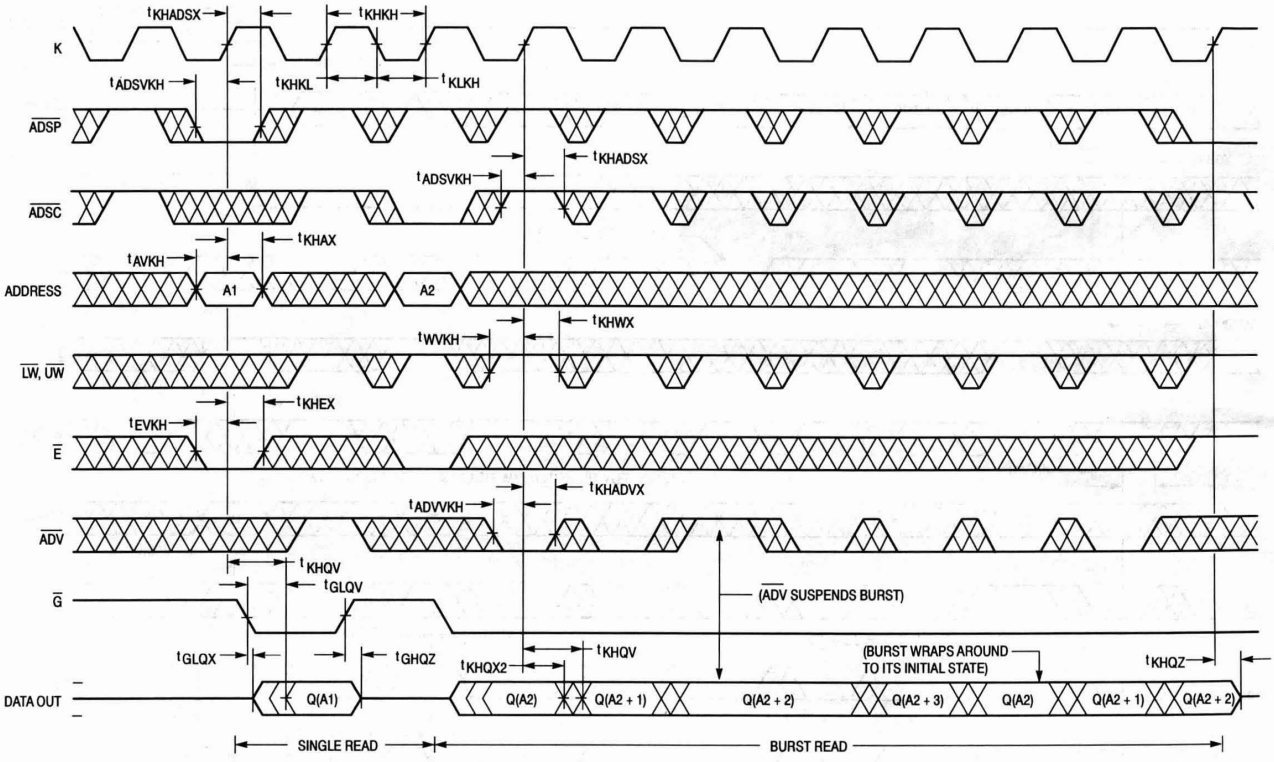


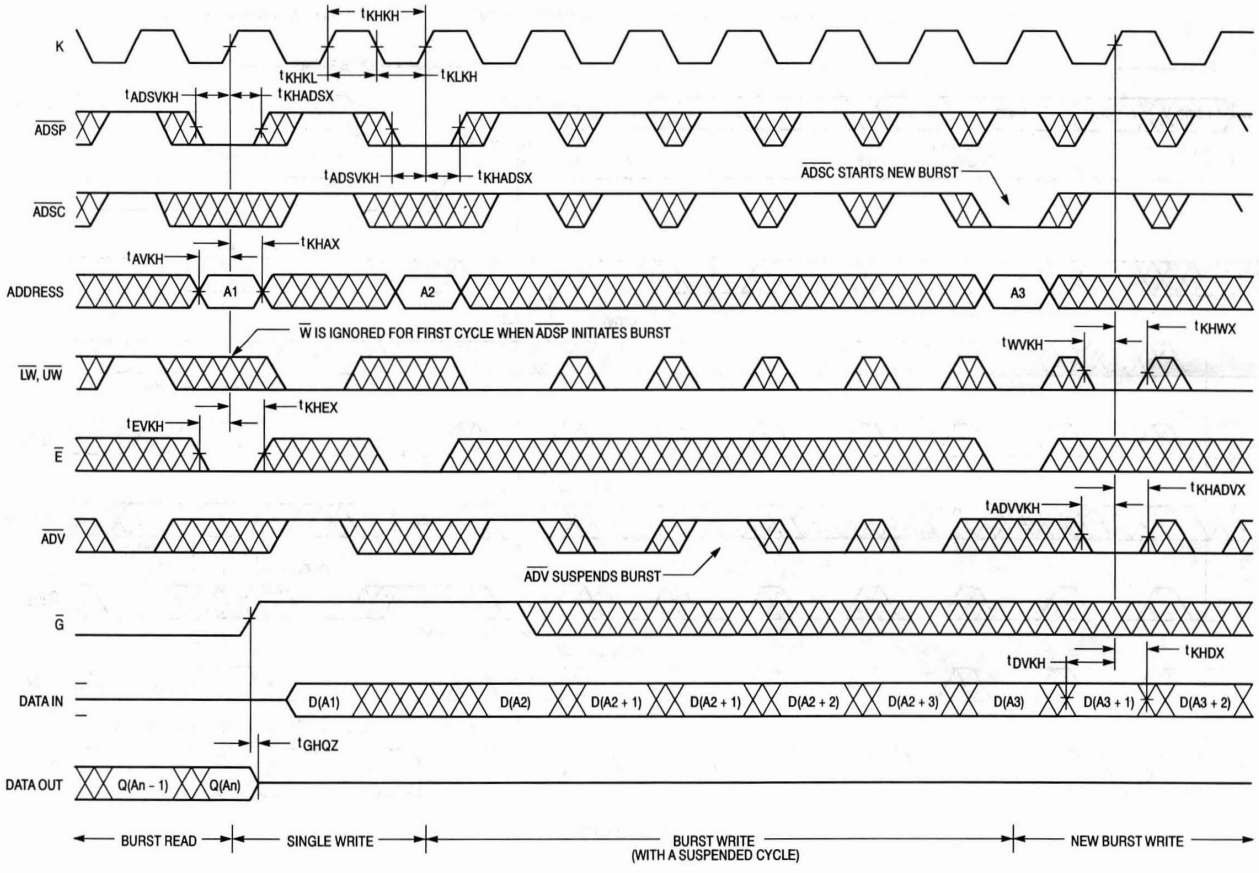
Figure 1. Test Loads

READ CYCLES

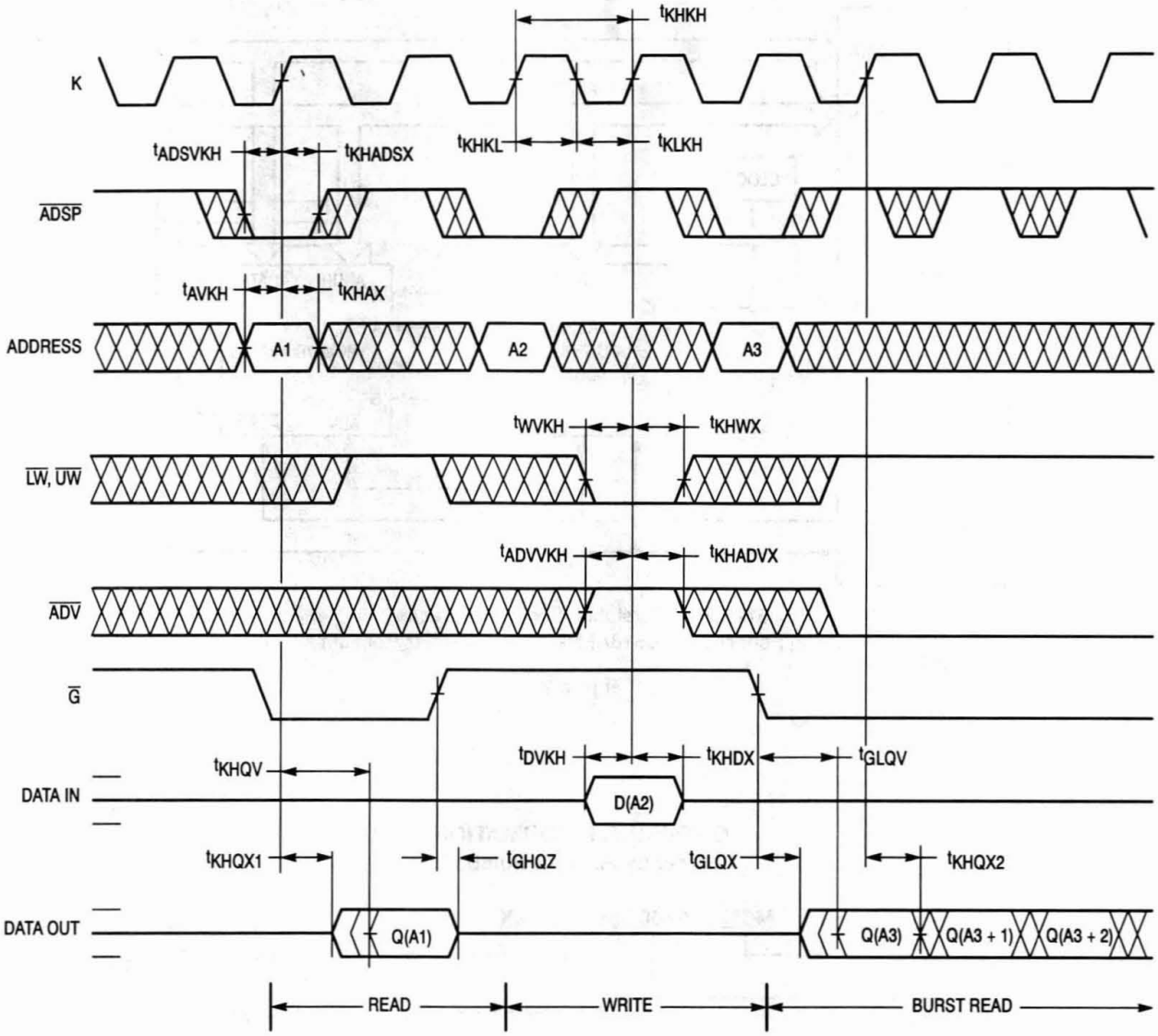


NOTE: Q(A2) represents the first output data from the base address A2; Q(A2 + 1) represents the next output data in the burst sequence with A2 as the base address.

WRITE CYCLES



COMBINATION READ/WRITE CYCLE ($\overline{E}$ low, $\overline{ADSC}$ high)



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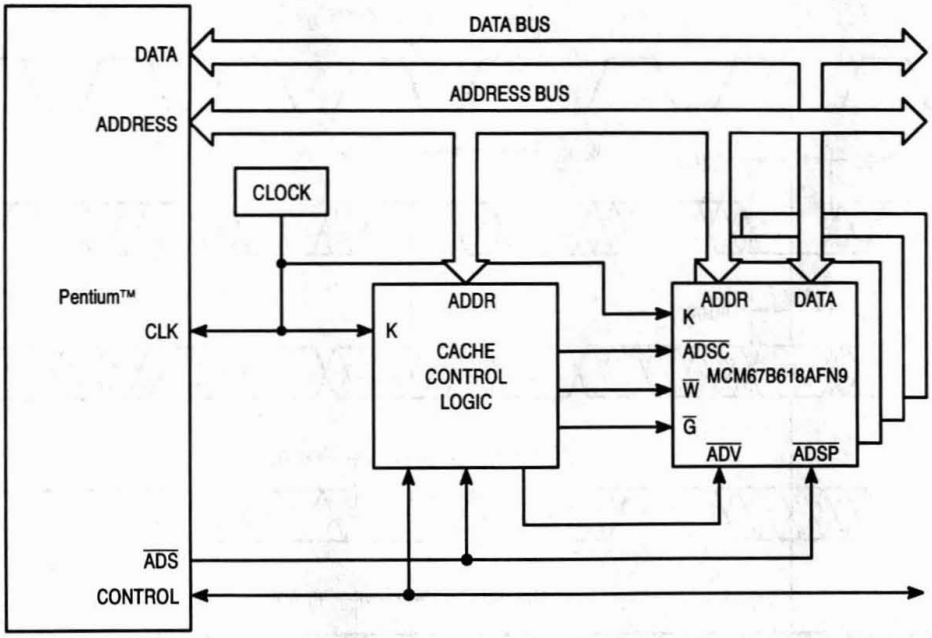
APPLICATION EXAMPLE



512K Byte Burstable, Secondary Cache
Using Four MCM67B618AFN9s with a 66 MHz Pentium

Figure 2

ORDERING INFORMATION
(Order by Full Part Number)

MCM 67B618A XX XX

Motorola Memory Prefix

Part Number

Speed (9 = 9 ns, 10 = 10 ns, 12 = 12 ns)

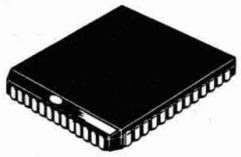
Package (FN = PLCC)

Full Part Numbers — MCM67B618AFN9 MCM67B618AFN10 MCM67B618AFN12

MCM67C618A

64K x 18 Bit BurstRAM™ Synchronous Fast Static RAM

With Burst Counter and Registered Outputs



FN PACKAGE
PLASTIC
CASE 778–02

The MCM67C618A is a 1,179,648 bit synchronous static random access memory designed to provide a burstable, high–performance, secondary cache for the i486™ and Pentium™ microprocessors. It is organized as 65,536 words of 18 bits, fabricated with Motorola's high–performance silicon–gate BiCMOS technology. The device integrates input registers, a 2–bit counter, high speed SRAM, and high drive registered output drivers onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A15), data inputs (D0 – D17), and all control signals except output enable ($\overline{G}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

This device contains output registers for pipeline operations. At the rising edge of K, the RAM provides the output data from the previous cycle.

Output enable ($\overline{G}$) is asynchronous for maximum system design flexibility.

Burst can be initiated with either address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be generated internally by the MCM67C618A (burst sequence imitates that of the i486 and Pentium) and controlled by the burst address advance ($\overline{ADV}$) input pin. The following pages provide more detailed information on burst controls.

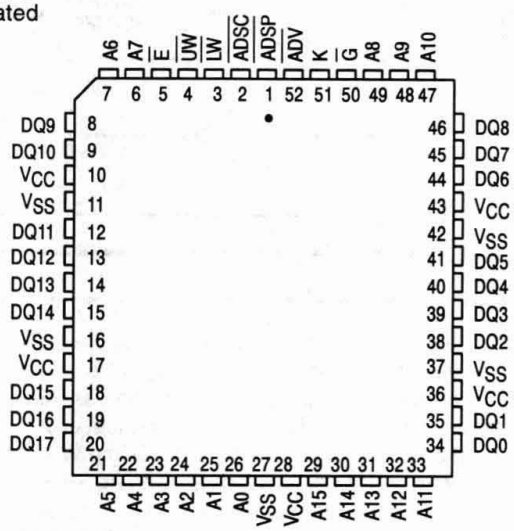
Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased flexibility for incoming signals.

Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits), while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

This device is ideally suited for systems that require wide data bus widths and cache memory. See Figure 2 for applications information.

- Single 5 V ± 5% Power Supply
- Fast Access Time/Fast Cycle Time = 5 ns/100 MHz, 7 ns/80 MHz
- Byte Writeable via Dual Write Enables
- Internal Input Registers (Address, Data, Control)
- Output Registers for Pipelined Applications
- Internally Self–Timed Write Cycle
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three–State Outputs
- Common Data Inputs and Data Outputs
- 3.3 V I/O Compatible
- High Board Density 52–Lead PLCC Package

PIN ASSIGNMENT



PIN NAMES	
A0 – A15	Address Inputs
K	Clock
$\overline{ADV}$	Burst Address Advance
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Upper Byte Write Enable
$\overline{ADSC}$	Controller Address Status
$\overline{ADSP}$	Processor Address Status
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

BurstRAM is a trademark of Motorola, Inc.
i486 and Pentium are trademarks of Intel Corp.

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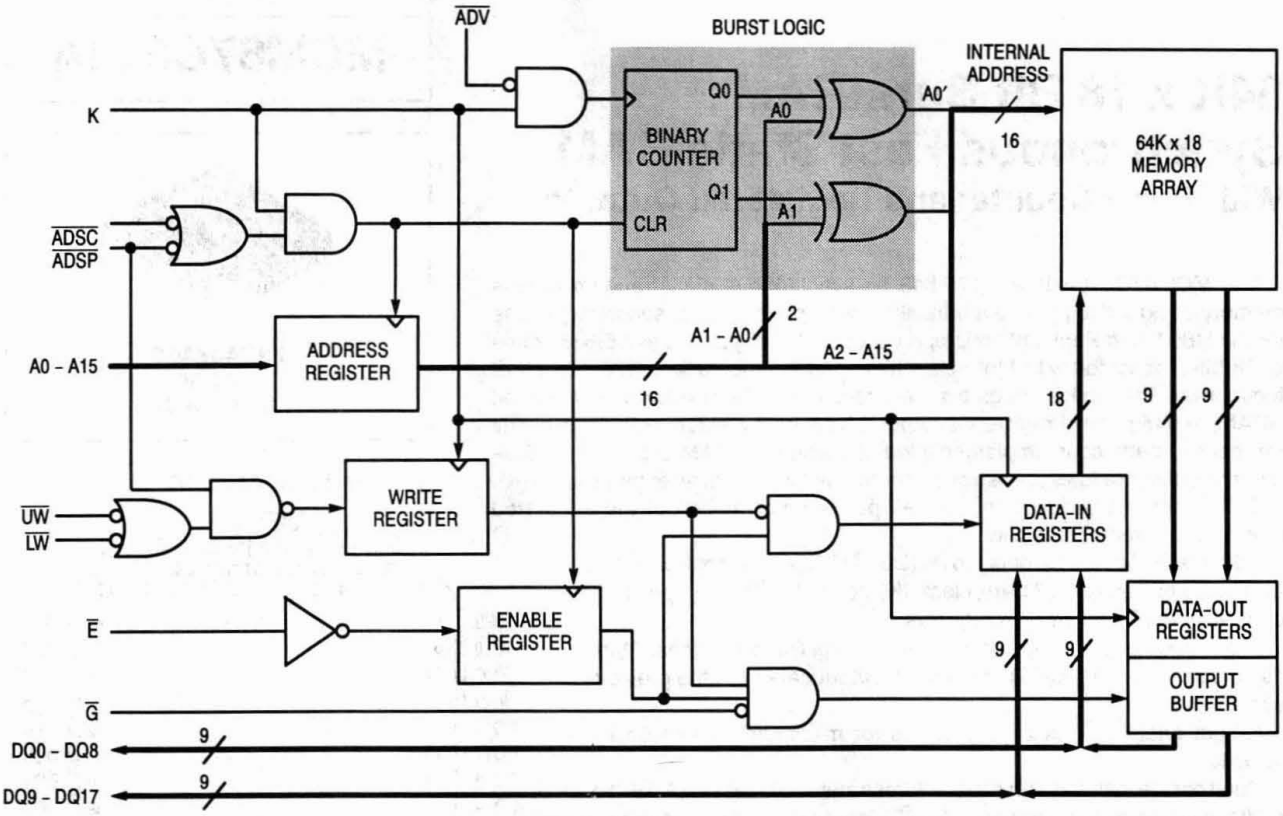
BLOCK DIAGRAM (See Note)



NOTE: All registers are positive–edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{ADSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{ADSC}$) is performed using the new external address. Alternatively, an $\overline{ADSP}$–initiated two cycle WRITE can be performed by asserting $\overline{ADSP}$ and a valid address on the first cycle, then negating both $\overline{ADSP}$ and $\overline{ADSC}$ and asserting $\overline{LW}$ and/or $\overline{UW}$ with valid data on the second cycle (see Single Write cycle in WRITE CYCLES timing diagram).
When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{ADV}$ controls subsequent burst cycles. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE TABLE (See Note)

External Address	A15 – A2	A1	A0
1st Burst Address	A15 – A2	A1	$\overline{A0}$
2nd Burst Address	A15 – A2	$\overline{A1}$	A0
3rd Burst Address	A15 – A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{UW}$ or $\overline{LW}$	K	Address Used	Operation
H	L	X	X	X	L–H	N/A	Deselected
H	X	L	X	X	L–H	N/A	Deselected
L	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low–to–high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out
Read	H	High–Z
Write	X	High–Z — Data In
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA5} I_{CCA7}	—	310 290	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	95	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible i486 and Pentium bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5% T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1a Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM67C618A–5		MCM67C618A–7		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{KHKH}	10	—	12.5	—	ns	
Clock Access Time	t_{KHQV}	—	5	—	7	ns	5
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	ns	
Clock High to Output Active	t_{KHQX1}	0	—	0	—	ns	
Clock High to Output Change	t_{KHQX2}	2	—	2	—	ns	
Output Enable to Output Active	t_{GLQX}	0	—	0	—	ns	
Output Disable to Q High–Z	t_{GHQZ}	—	6	—	6	ns	6
Clock High to Q High–Z	t_{KHQZ}	2	6	2	6	ns	
Clock High Pulse Width	t_{KHKL}	4.5	—	5	—	ns	
Clock Low Pulse Width	t_{KLKH}	4.5	—	5	—	ns	
Setup Times: Address	t_{AVKH}	2.5	—	2.5	—	ns	7
Address Status	t_{ADSVKH}						
Data In	t_{DVKH}						
Write	t_{WVKH}						
Address Advance	t_{ADVVKH}						
Chip Enable	t_{EVKH}						
Hold Times: Address	t_{KHAX}	0.5	—	0.5	—	ns	7
Address Status	t_{KHADSX}						
Data In	t_{KHDX}						
Write	t_{KHWX}						
Address Advance	t_{KHADVX}						
Chip Enable	t_{KHEX}						

NOTES:
1. In setup and hold times, W (write) refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{ADSP}$ high for the setup and hold times.
3. All read and write cycle timings are referenced from K or $\overline{G}$.
4. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
5. Maximum access times are guaranteed for all possible i486 and Pentium external bus cycles.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1b. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of K whenever $\overline{ADSP}$ or $\overline{ADSC}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is enabled. Chip enable must be valid at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled.

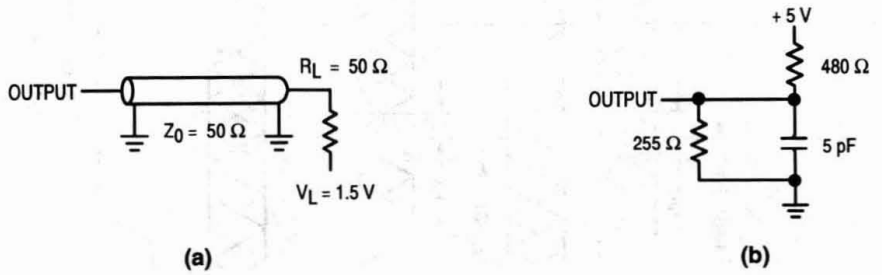
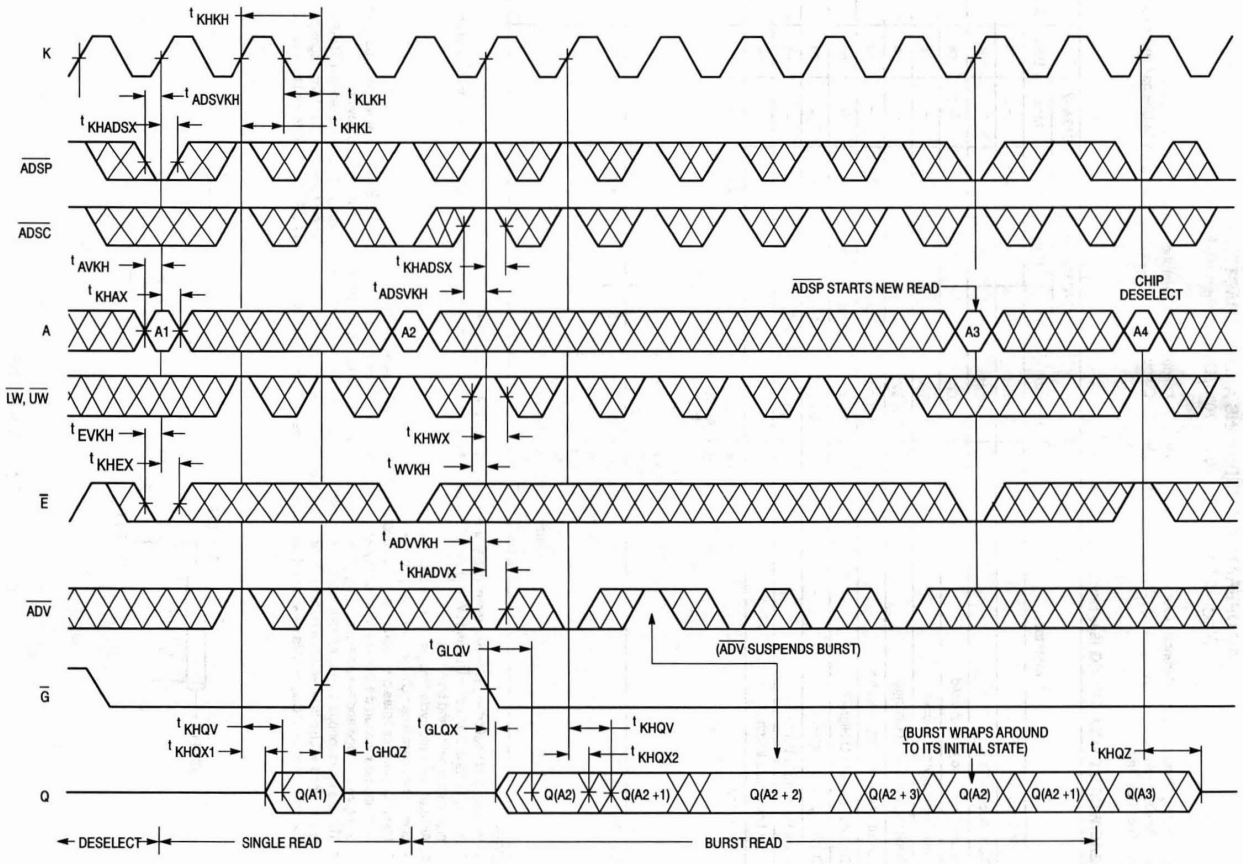
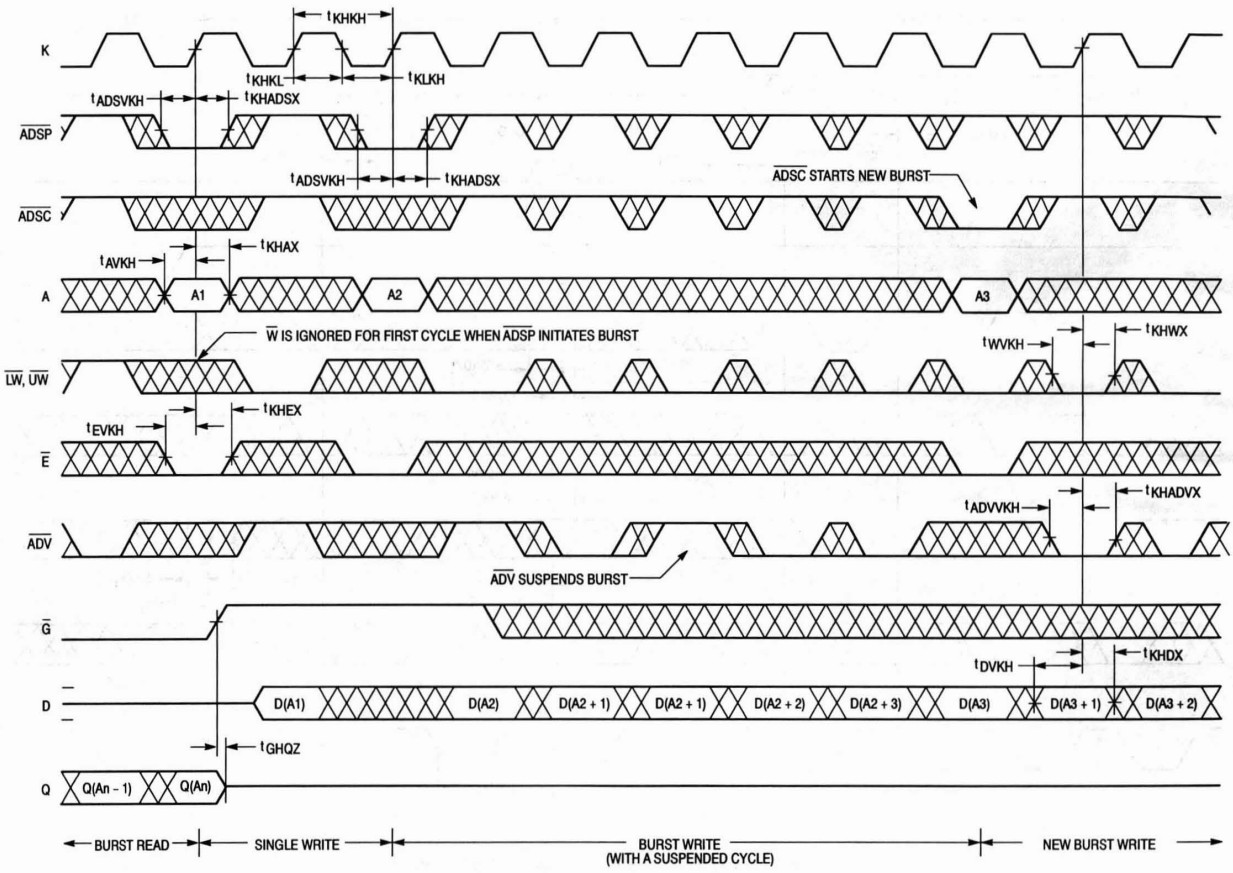


Figure 1. Test Loads

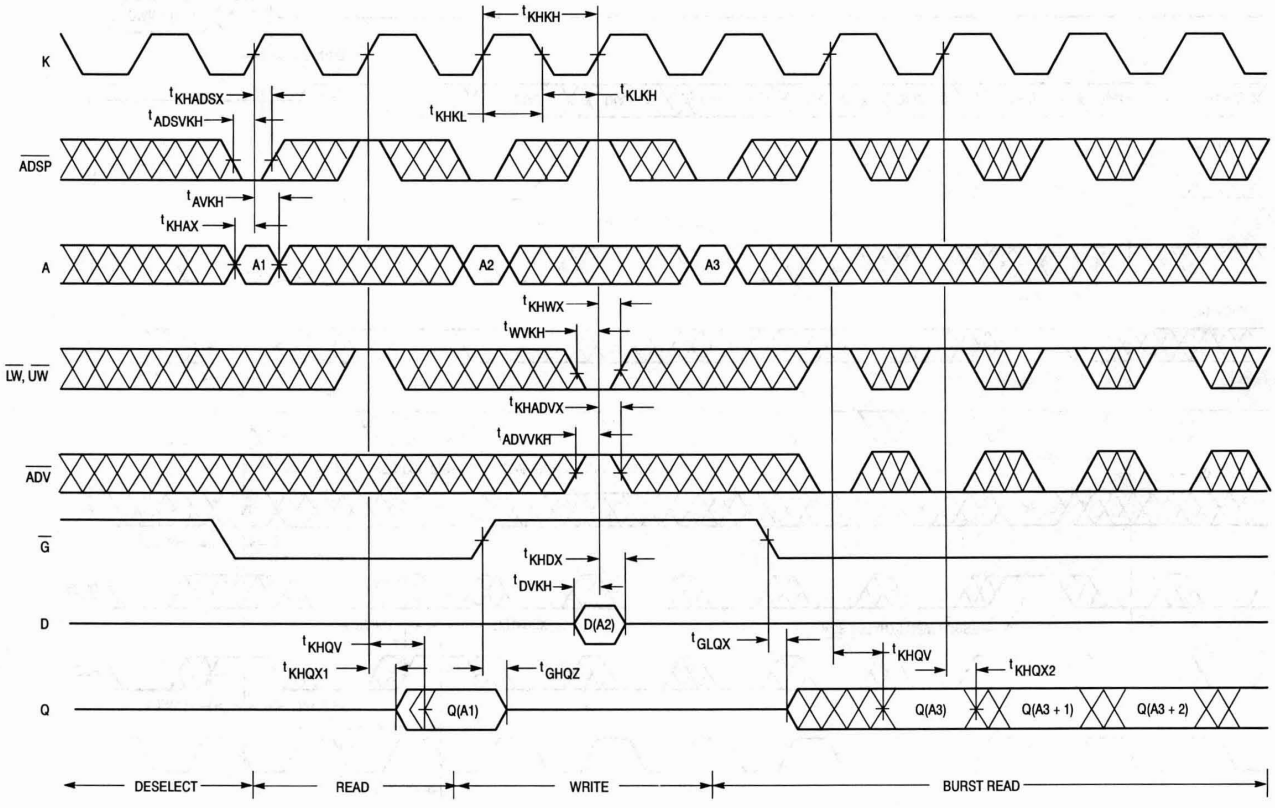
READ CYCLES


tKHKH
K
tADSVKH
tKLKH
tKHADSX
tKHKL
ADSP
ADSC
tAVKH
tKHAX
tKHADSX
tADSVKH
ADSP STARTS NEW READ
CHIP DESELECT
A
A1
A2
A3
A4
LW, UW
tEVKH
tKHEX
tKHWX
tWVKH
E
tADVVKH
tKHADVX
ADV
tGLQV
(ADV SUSPENDS BURST)
G
tKHQV
tKHQX1
tGHQZ
tGLQX
tKHQV
tKHQX2
(BURST WRAPS AROUND TO ITS INITIAL STATE)
tKHQZ
Q
Q(A1)
Q(A2)
Q(A2 +1)
Q(A2 + 2)
Q(A2 + 3)
Q(A2)
Q(A2 +1)
Q(A3)
DESELECT
SINGLE READ
BURST READ

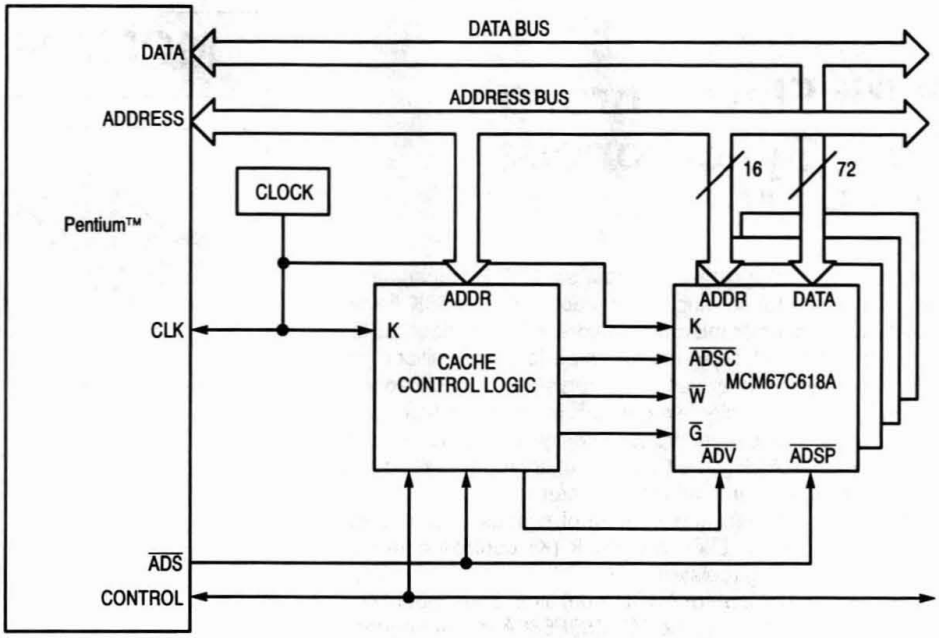
WRITE CYCLES



COMBINATION READ/WRITE CYCLES ($\overline{E}$ low, $\overline{ADSC}$ high)



APPLICATION EXAMPLE



512K Byte Burstable, Secondary Cache Using
Four MCM67C618AFN7s With a 75 MHz (bus speed) Pentium

Figure 2

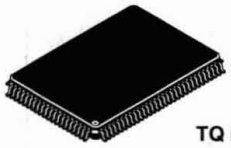
ORDERING INFORMATION
(Order by Full Part Number)

MCM	67C618A	XX	X
Motorola Memory Prefix			Speed (5 = 5 ns, 7 = 7 ns)
	Part Number		
			Package (FN = PLCC)

Full Part Numbers — MCM67C618AFN5 MCM67C618AFN7

MCM69F536A

32K x 36 Bit Flow–Through BurstRAM™ Synchronous Fast Static RAM



TQ PACKAGE
TQFP
CASE 983A–01

The MCM69F536A is a 1M bit synchronous fast static RAM designed to provide a burstable, high performance, secondary cache for the 68K Family, PowerPC™, 486, i960™ and Pentium™ microprocessors. It is organized as 32K words of 36 bits each, fabricated with Motorola's high performance silicon gate BiCMOS technology. This device integrates input registers, a 2 bit address counter, and high speed SRAM onto a single monolithic circuit for reduced parts count in cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (SA), data inputs (DQx), and all control signals except output enable ($\overline{G}$) and Linear Burst Order ($\overline{LBO}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ input pins. Subsequent burst addresses can be generated internally by the MCM69F536A (burst sequence operates in linear or interleaved mode dependent upon state of $\overline{LBO}$) and controlled by the burst address advance ($\overline{ADV}$) input pin.

Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased timing flexibility for incoming signals.

Synchronous byte write ($\overline{SBx}$) and synchronous global write ($\overline{SGW}$), and synchronous write enable $\overline{SW}$ are provided to allow writes to either individual bytes or to all bytes. The four bytes are designated as "a", "b", "c", and "d". $\overline{SBa}$ controls DQa, $\overline{SBb}$ controls DQb, and so on. Individual bytes are written if the selected byte writes $\overline{SBx}$ are asserted with $\overline{SW}$. All bytes are written if either $\overline{SGW}$ is asserted or if all $\overline{SBx}$ and $\overline{SW}$ are asserted.

For read cycles, a flow–through SRAM allows output data to simply flow freely from the memory array.

The MCM69F536A operates from a 3.3 V power supply and all inputs and outputs are LVTTL compatible.

- MCM69F536A–8.5 = 8.5 ns access / 12 ns cycle
  MCM69F536A–9 = 9 ns access / 12 ns cycle
  MCM69F536A–10 = 10 ns access / 15 ns cycle
  MCM69F536A–12 = 12 ns access / 16.6 ns cycle
- Single 3.3 V + 10%, – 5% Power Supply
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Selectable Burst Sequencing Order (Linear/Interleaved)
- Internally Self–Timed Write Cycle
- Byte Write and Global Write Control
- 100 Pin TQFP Package

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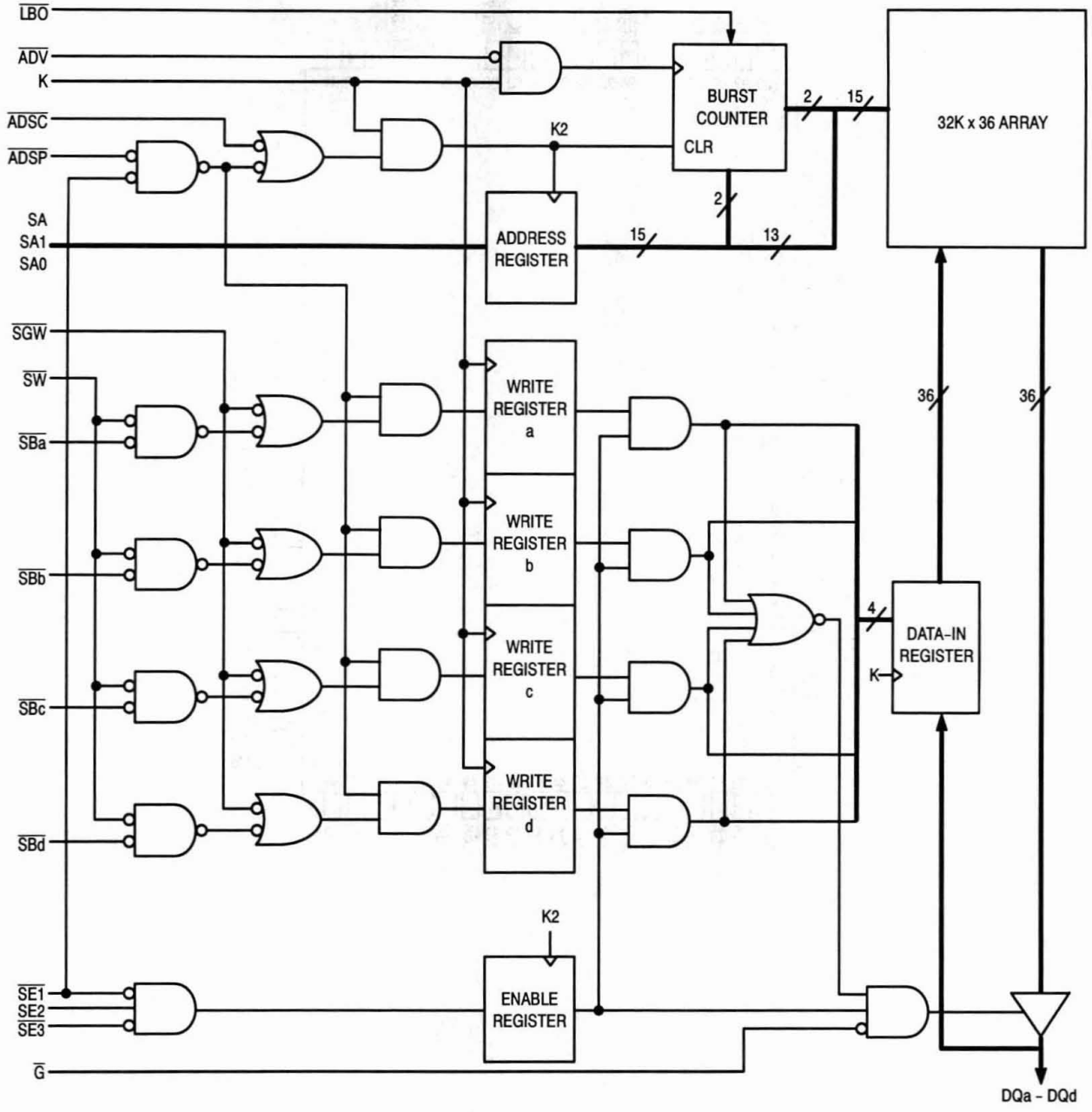
The PowerPC name is a trademark of IBM Corp., used under license therefrom.
i960 and Pentium are trademarks of Intel Corp.

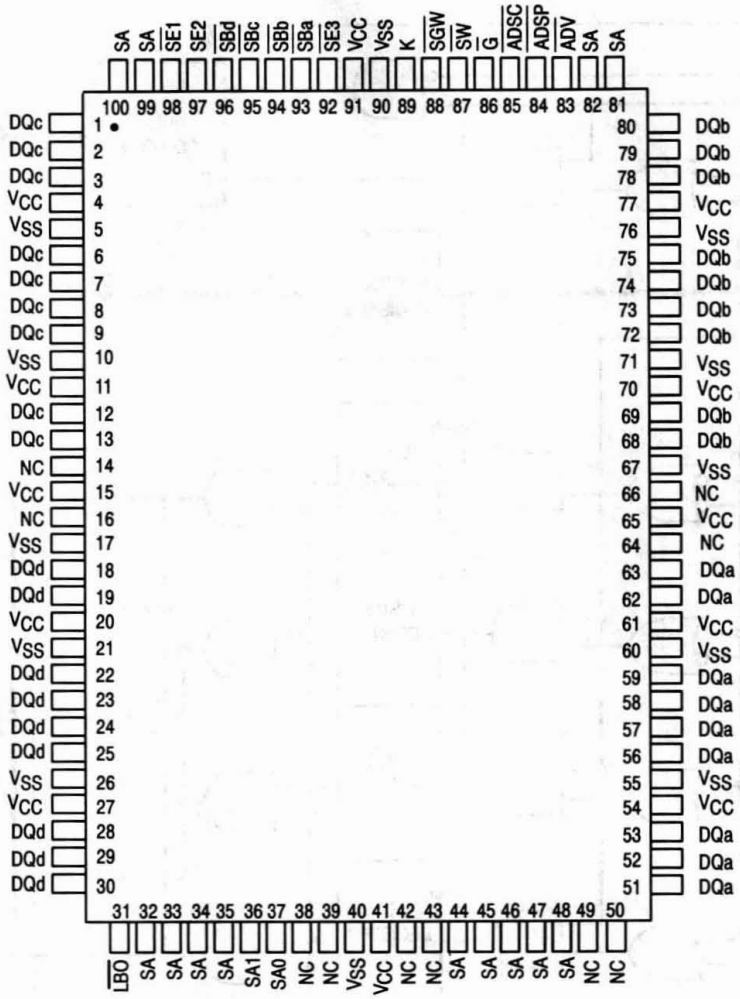
REV 1
4/10/97

FUNCTIONAL BLOCK DIAGRAM



4

PIN ASSIGNMENT



PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: Initiates READ, WRITE or chip deselect cycle
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: Initiates READ, WRITE or chip deselect cycle (exception — chip deselect does not occur when $\overline{ADSP}$ is asserted and $\overline{SE1}$ is high).
83	$\overline{ADV}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
(a) 51, 52, 53, 56, 57, 58, 59, 62, 63 (b) 68, 69, 72, 73, 74, 75, 78, 79, 80 (c) 1, 2, 3, 6, 7, 8, 9, 12, 13 (d) 18, 19, 22, 23, 24, 25, 28, 29, 30	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b, c, d).
86	$\overline{G}$	Input	Asynchronous Output Enable Input: Low — enables output buffers (DQx pins). High — DQx pins are high impedance.
89	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$ and $\overline{LBO}$.
31	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst count (68K/PowerPC). High — interleaved burst count (486/i960/Pentium).
32, 33, 34, 35, 44, 45, 46, 47, 48, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
36, 37	SA1,SA0	Input	Synchronous Address Inputs: These pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
98	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high — blocks $\overline{ADSP}$ or deselects chip when $\overline{ADSC}$ is asserted.
97	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
92	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
93, 94, 95, 96 (a) (b) (c) (d)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: "x" refers to the byte being written (byte a, b, c, d). $\overline{SGW}$ overrides $\overline{SBx}$.
88	$\overline{SGW}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the $\overline{SBx}$ and $\overline{SW}$ signals. If only byte write signals $\overline{SBx}$ are being used, tie this pin high.
87	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{SBx}$ pins. If only byte write signals $\overline{SBx}$ are being used, tie this pin low.
4, 11, 15, 20, 27, 41, 54, 61, 65, 70, 77, 91	V_{CC}	Supply	Power Supply: 3.3 V + 10%, – 5%.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground.
64	NC	Input	No Connection: There is no connection to the chip. For compatibility reasons, it is recommended that this pin be tied low for system designs that do not have a sleep mode associated with the cache/memory controller. Other vendors' RAMs may have implemented this Sleep Mode (ZZ) feature.
14, 16, 38, 39, 42, 43, 49, 50, 66	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE (See Notes 1 through 4)

Next Cycle	Address Used	$\overline{SE1}$	SE2	$\overline{SE3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{G}$ [3]	DQx	Write [2, 4]
Deselect	None	1	X	X	X	0	X	X	High–Z	X
Deselect	None	0	X	1	0	X	X	X	High–Z	X
Deselect	None	0	0	X	0	X	X	X	High–Z	X
Deselect	None	X	X	1	1	0	X	X	High–Z	X
Deselect	None	X	0	X	1	0	X	X	High–Z	X
Begin Read	External	0	1	0	0	X	X	0	DQ	READ
Begin Read	External	0	1	0	1	0	X	0	DQ	READ
Continue Read	Next	X	X	X	1	1	0	1	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	0	DQ	READ
Continue Read	Next	1	X	X	X	1	0	1	High–Z	READ
Continue Read	Next	1	X	X	X	1	0	0	DQ	READ
Suspend Read	Current	X	X	X	1	1	1	1	High–Z	READ
Suspend Read	Current	X	X	X	1	1	1	0	DQ	READ
Suspend Read	Current	1	X	X	X	1	1	1	High–Z	READ
Suspend Read	Current	1	X	X	X	1	1	0	DQ	READ
Begin Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Begin Write	Current	1	X	X	X	1	1	X	High–Z	WRITE
Begin Write	External	0	1	0	1	0	X	X	High–Z	WRITE
Continue Write	Next	X	X	X	1	1	0	X	High–Z	WRITE
Continue Write	Next	1	X	X	X	1	0	X	High–Z	WRITE
Suspend Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Suspend Write	Current	1	X	X	X	1	1	X	High–Z	WRITE

NOTES:
1. X = Don't Care. 1 = logic high. 0 = logic low.
2. Write is defined as either 1) any $\overline{SBx}$ and $\overline{SW}$ low or 2) $\overline{SGW}$ is low.
3. $\overline{G}$ is an asynchronous signal and is not sampled by the clock K. $\overline{G}$ drives the bus immediately (t_{GLQX}) following $\overline{G}$ going low.
4. On write cycles that follow read cycles, $\overline{G}$ must be negated prior to the start of the write cycle to ensure proper write data setup times. $\overline{G}$ must also remain negated at the completion of the write cycle to ensure proper write data hold times.

LINEAR BURST ADDRESS TABLE ($\overline{LBO} = V_{SS}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X10	X . . . X11	X . . . X00
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X00	X . . . X01	X . . . X10

INTERLEAVED BURST ADDRESS TABLE ($\overline{LBO} = V_{CC}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00

WRITE TRUTH TABLE

Cycle Type	$\overline{SGW}$	$\overline{SW}$	$\overline{SBa}$	$\overline{SBb}$	$\overline{SBc}$	$\overline{SBd}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte a	H	L	L	H	H	H
Write Byte b	H	L	H	L	H	H
Write Byte c	H	L	H	H	L	H
Write Byte d	H	L	H	H	H	L
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Package Power Dissipation (See Note 2)	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to 85	°C
Storage Temperature	T_{stg}	– 55 to 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Thermal Resistance Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	40 25	°C/W	1, 2
Thermal Resistance Junction to Board (Bottom)		$R_{\theta JB}$	17	°C/W	1, 3
Thermal Resistance Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	1, 4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold piate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V + 10%, – 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.135	3.3	3.6	V
Operating Temperature	T_J	20	—	110	°C
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V

* $V_{IL} \geq -2$ V for $t \leq t_{KHKH}/2$.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (0 V ≤ V_{in} ≤ V_{CC}) (Excluding $\overline{LBO}$)		$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current (0 V ≤ V_{in} ≤ V_{CC})		$I_{lkg(O)}$	—	± 1	µA
AC Supply Current (Device Selected, All Outputs Open, All Inputs Toggling at $V_{in} \leq V_{IL}$ or $\geq V_{IH}$, Cycle Time ≥ t_{KHKH} min)	MCM69F536A–8.5 (83 MHz) MCM69F536A–9 (83 MHz) MCM69F536A–10 (66 MHz) MCM69F536A–12 (60 MHz)	I_{CCA}	—	320 320 310 300	mA
CMOS Standby Supply Current (Deselected[1], Clock (K) Cycle Time ≥ t_{KHKH}, All Inputs Toggling at CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{CC} – 0.2 V)	MCM69F536A–8.5 (83 MHz) MCM69F536A–9 (83 MHz) MCM69F536A–10 (66 MHz) MCM69F536A–12 (60 MHz)	I_{SB1}	—	150 150 140 130	mA
Clock Running Supply Current (Deselected[1], Clock (K) Cycle Time ≥ t_{KHKH}, All Other Inputs Held to Static CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{CC} – 0.2 V)	MCM69F536A–8.5 (83 MHz) MCM69F536A–9 (83 MHz) MCM69F536A–10 (66 MHz) MCM69F536A–12 (60 MHz)	I_{SB2}	—	55 55 50 45	mA
Output Low Voltage (I_{OL} = 8 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4 mA)		V_{OH}	2.4	—	V

NOTE: 1. Device in Deselected mode as defined by the Truth Table.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	4	6	pF
Input/Output Capacitance	$C_{I/O}$	—	7	9	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V + 10%, – 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1 Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	69F536A–8.5		69F536A–9		69F536A–10		69F536A–12		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	12	—	12	—	15	—	16.6	—	ns	
Clock High Pulse Width	t_{KHKL}	4	—	4	—	5	—	6	—	ns	
Clock Low Pulse Width	t_{KLKH}	4	—	4	—	5	—	6	—	ns	
Clock Access Time	t_{KHQV}	—	8.5	—	9	—	10	—	12	ns	4
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	5	—	6	ns	4
Clock High to Output Active	t_{KHQX1}	0	—	0	—	0	—	0	—	ns	4
Clock High to Output Change	t_{KHQX2}	3	—	3	—	3	—	3	—	ns	4
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	ns	4
Output Disable to Q High–Z	t_{GHQZ}	—	5	—	5	—	5	—	6	ns	5
Clock High to Q High–Z	t_{KHQZ}	3	5	3	5	3	5	3	6	ns	5
Setup Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	t_{ADKH} t_{ADSKH} t_{DVKH} t_{WVKH} t_{EVKH}	2.5	—	2.5	—	2.5	—	2.5	—	ns	
Hold Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	t_{KHAX} t_{KHADSX} t_{KHDX} t_{KHWX} t_{KHEX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	

NOTES:
1. Write is defined as either any $\overline{SBx}$ and $\overline{SW}$ low or $\overline{SGW}$ is low. Chip Enable is defined as $\overline{SE1}$ low, SE2 high and $\overline{SE3}$ low whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care after write cycle begins. To prevent bus contention, $\overline{G}$ should be negated prior to start of write cycle.
4. Tested per AC Test Load (See Figure 1).
5. Measured at ± 200 mV from steady state.

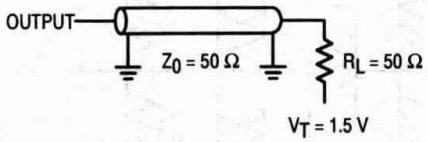
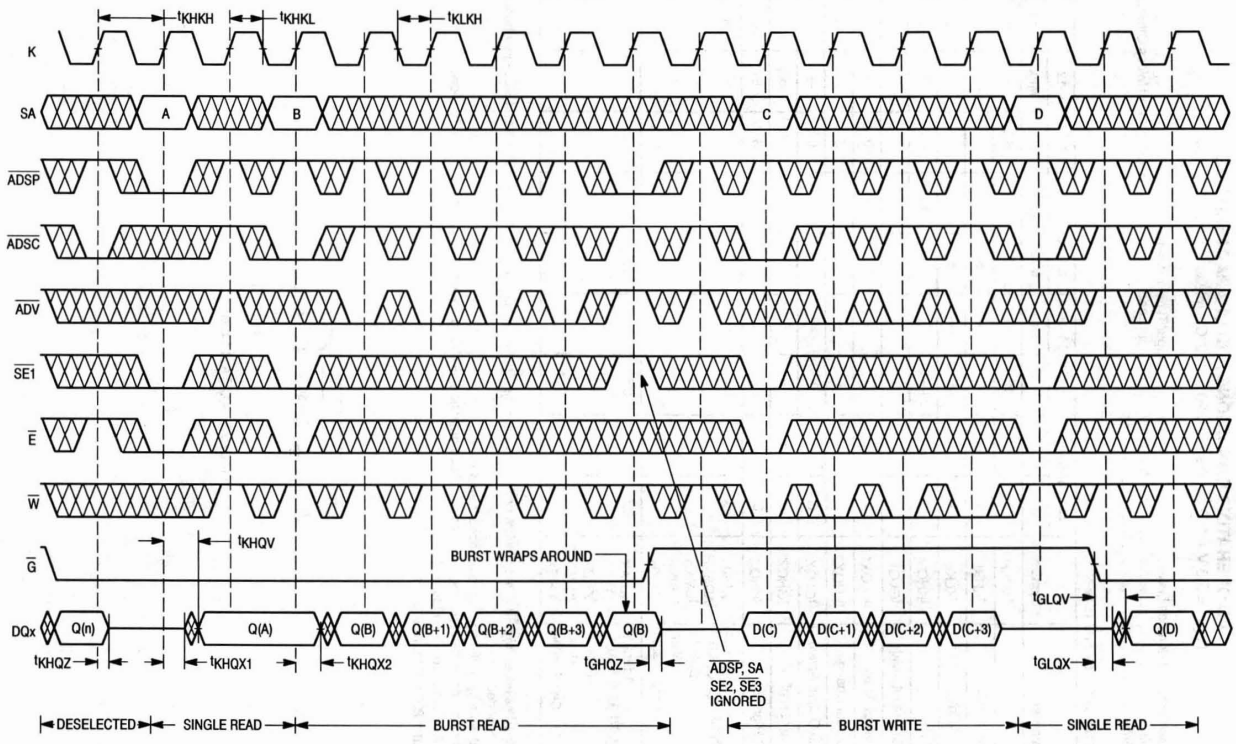


Figure 1. AC Test Loads

READ/WRITE CYCLES



NOTE: $\overline{E}$ low = SE2 high and $\overline{SE3}$ low.
$\overline{W}$ low = $\overline{SGW}$ low and/or $\overline{SW}$ and $\overline{SBx}$ low.

APPLICATION INFORMATION

The MCM69F536A BurstRAM is a high speed synchronous SRAM that is intended for use primarily in secondary or level two (L2) cache memory applications. L2 caches are found in a variety of classes of computers – from the desktop personal computer to the high–end servers and transaction processing machines. For simplicity, the majority of L2 caches today are direct mapped and are single bank implementations. These caches tend to be designed for bus speeds in the range of 33 to 66 MHz. At these bus rates, flow–through (non–pipelined) BurstRAMs can be used since their access times meet the speed requirements for a minimum–latency, zero–wait state L2 cache interface. Latency is a measure (time) of "dead" time the memory system exhibits as a result of a memory request.

For those applications that demand bus operation at greater than 66 MHz or multi–bank L2 caches at 66 MHz, the pipelined (register/register) version of the 32Kx36 BurstRAM (MCM69P536) allows the designer to maintain zero–wait state operation. Multiple banks of BurstRAMs create additional bus loading and can cause the system to otherwise miss its timing requirements. The access time (clock–to–valid–data) of a pipelined BurstRAM is inherently faster than a non–pipelined device by a few nanoseconds. This does not come without cost. The cost is latency – "dead" time.

For L2 cache designs that must minimize both latency and wait states, flow–through BurstRAMs are the best choice in achieving the highest performance in L2 cache design.

FUNCTIONAL EQUIVALENT

The following describes the configuration of the MCM69F536A as a functional equivalent to a 5 V BurstRAM. A migration from 5 V BurstRAMs to 3.3 V BurstRAMs (e.g. MCM69F536A) can be somewhat confusing due to functional and pinout differences. Because the 3.3 V devices offer more pins than the 5 V PLCC devices, it is no longer necessary to supply multiple part numbers for the different burst, address pipeline support ("H" part), etc. options. A single MCM69F536A device can replace two of the 5 V 32Kx18 devices or replace four of the 5 V 32Kx9 devices. Below is a table that lists control pins on the MCM69F536A that can be tied off to either 3.3 V or ground in order to satisfy the migration to this 3.3 V RAM.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

5 V Device Numbers	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
MCM62486B	—	—	—	L	H
MCM62940B	—	—	—	L	L
MCM67B518	—	—	—	L	H
MCM67H518	—	—	—	—	H
MCM67M518	—	—	—	L	L

NOTE: If no tie value is given, then the pin should be used as it was intended on the 5 V device.

NON–BURST SYNCHRONOUS OPERATION

Although this BurstRAM has been designed for 68K–, PowerPC–, 486–, i960, and Pentium – based systems, these SRAMs can be used in other high speed L2 cache or memory applications that do not require the burst address feature. Most L2 caches designed with a synchronous interface can make use of the MCM69F536A. The burst counter feature of the BurstRAM can be disabled, and the SRAM can be configured to act upon a continuous stream of addresses. See Figure 2.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

Desired Operation	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
Sync Non–Burst, Flow–Through SRAM	H	L	H	L	X

NOTE: Although X is specified in the table as a don't care, the pin must be tied either high or low.

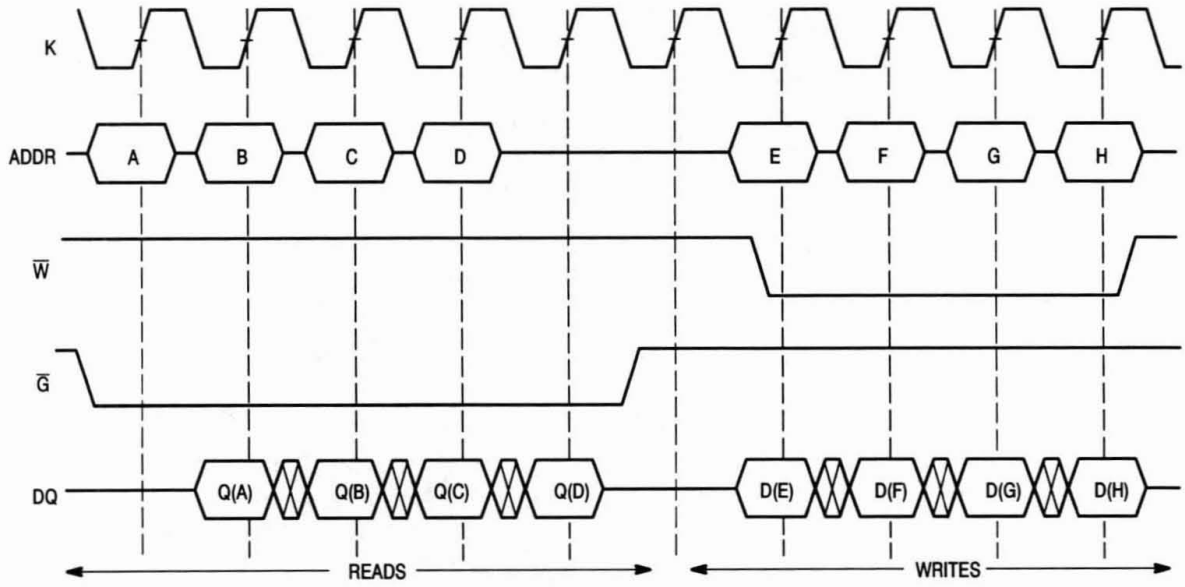
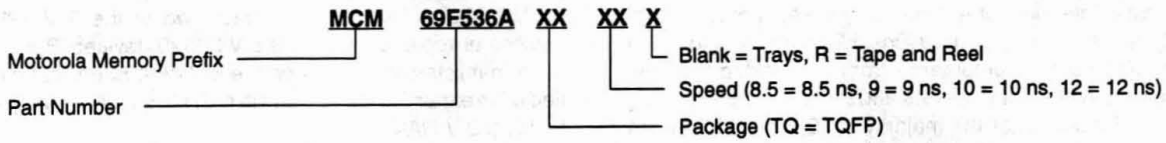


Figure 2. Configured as Non–Burst Synchronous SRAM

ORDERING INFORMATION
(Order by Full Part Number)

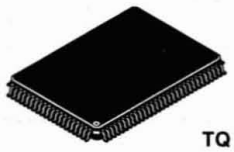

MCM 69F536A XX XX X
Motorola Memory Prefix
Part Number
Blank = Trays, R = Tape and Reel
Speed (8.5 = 8.5 ns, 9 = 9 ns, 10 = 10 ns, 12 = 12 ns)
Package (TQ = TQFP)

Full Part Numbers —				
	MCM69F536ATQ8.5	MCM69F536ATQ9	MCM69F536ATQ10	MCM69F536ATQ12
	MCM69F536ATQ8.5R	MCM69F536ATQ9R	MCM69F536ATQ10R	MCM69F536ATQ12R

4

MCM69F536B

32K x 36 Bit Flow–Through BurstRAM™ Synchronous Fast Static RAM



TQ PACKAGE
TQFP
CASE 983A–01

The MCM69F536B is a 1M bit synchronous fast static RAM designed to provide a burstable, high performance, secondary cache for the 68K Family, PowerPC™, 486, i960™ and Pentium™ microprocessors. It is organized as 32K words of 36 bits each. This device integrates input registers, a 2 bit address counter, and high speed SRAM onto a single monolithic circuit for reduced parts count in cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (SA), data inputs (DQx), and all control signals except output enable ($\overline{G}$) and Linear Burst Order ($\overline{LBO}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ input pins. Subsequent burst addresses can be generated internally by the MCM69F536B (burst sequence operates in linear or interleaved mode dependent upon state of $\overline{LBO}$) and controlled by the burst address advance ($\overline{ADV}$) input pin.

Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased timing flexibility for incoming signals.

Synchronous byte write ($\overline{SBx}$) and synchronous global write ($\overline{SGW}$), and synchronous write enable $\overline{SW}$ are provided to allow writes to either individual bytes or to all bytes. The four bytes are designated as "a", "b", "c", and "d". $\overline{SBa}$ controls DQa, $\overline{SBb}$ controls DQb, and so on. Individual bytes are written if the selected byte writes $\overline{SBx}$ are asserted with $\overline{SW}$. All bytes are written if either $\overline{SGW}$ is asserted or if all $\overline{SBx}$ and $\overline{SW}$ are asserted.

For read cycles, a flow–through SRAM allows output data to simply flow freely from the memory array.

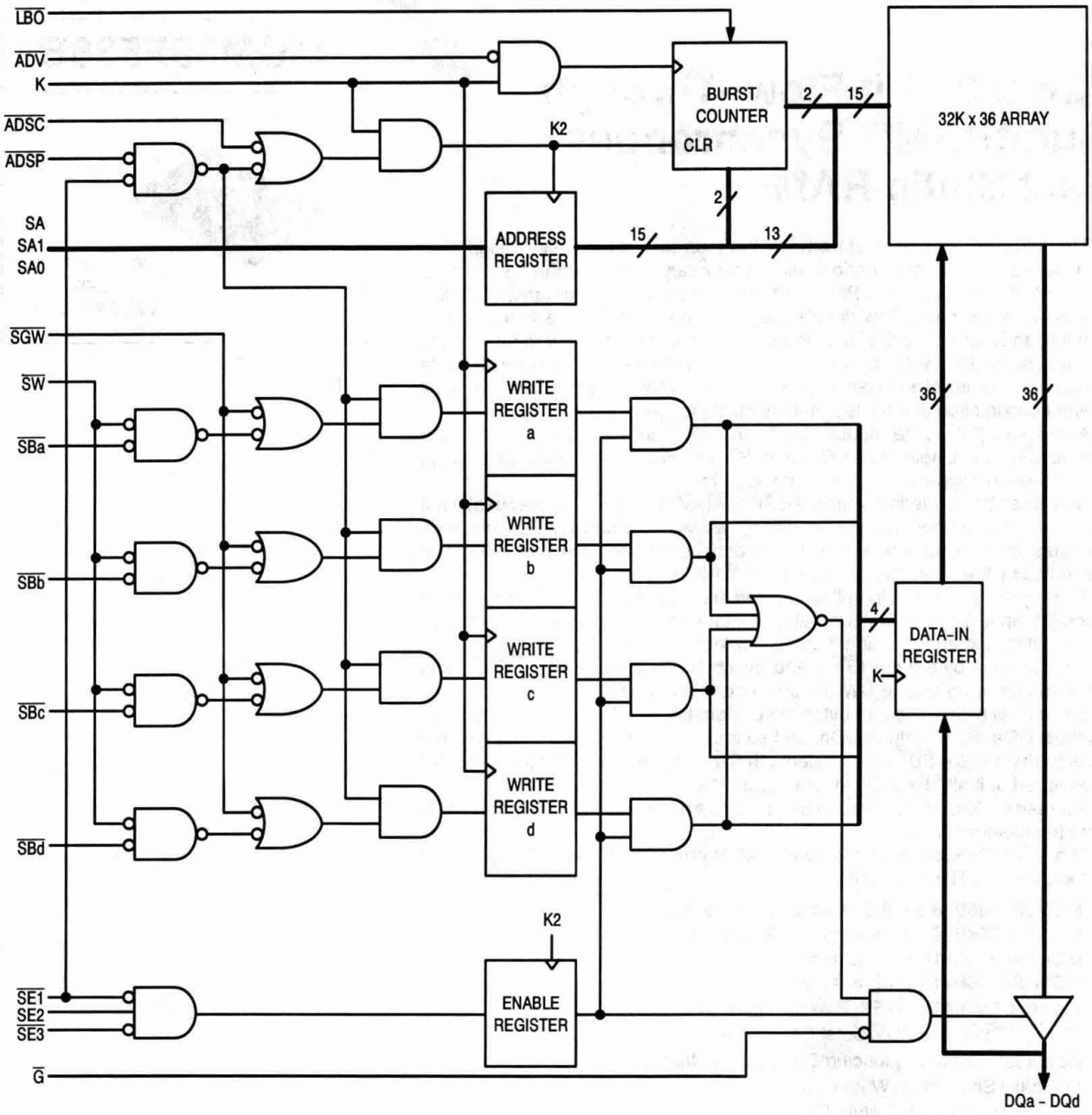
The MCM69F536B operates from a 3.3 V power supply and all inputs and outputs are LVTTL compatible.

- MCM69F536B–8.5 = 8.5 ns access / 12 ns cycle
  MCM69F536B–9 = 9 ns access / 12 ns cycle
  MCM69F536B–10 = 10 ns access / 15 ns cycle
  MCM69F536B–12 = 12 ns access / 16.6 ns cycle
- Single 3.3 V + 10%, – 5% Power Supply
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Selectable Burst Sequencing Order (Linear/Interleaved)
- Internally Self–Timed Write Cycle
- Byte Write and Global Write Control
- 5 V Tolerant Data I/Os (DQx) Only
- 100 Pin TQFP Package

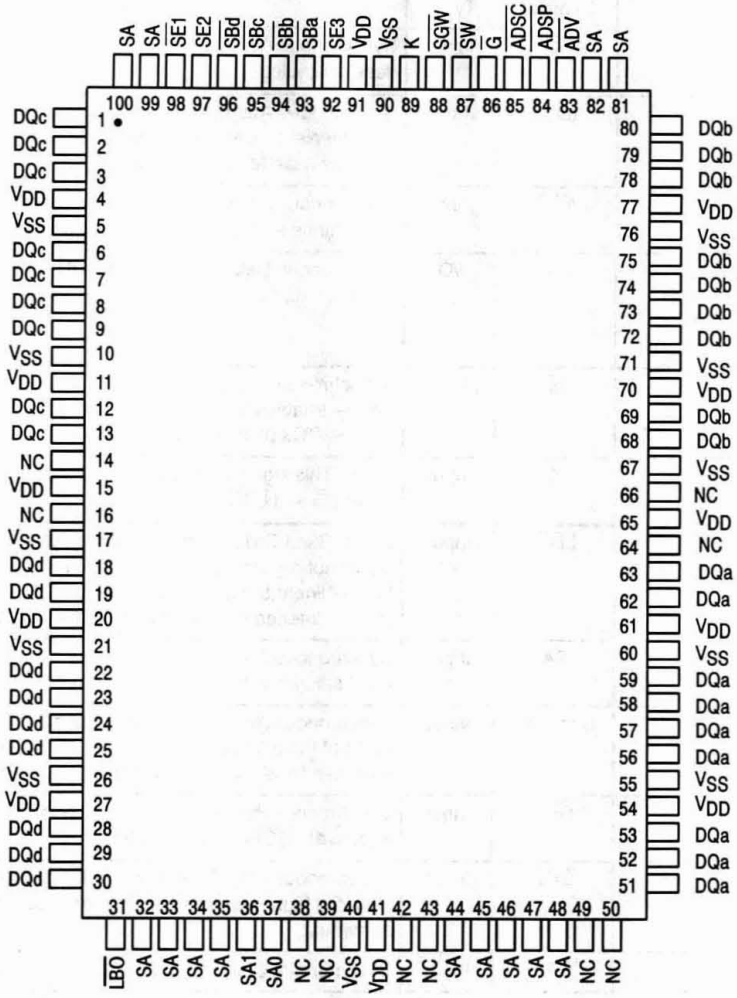
The PowerPC name is a trademark of IBM Corp., used under license therefrom.
i960 and Pentium are trademarks of Intel Corp.

REV 2
4/10/97

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENT



4

PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: Initiates READ, WRITE or chip deselect cycle.
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: Initiates READ, WRITE or chip deselect cycle (exception — chip deselect does not occur when $\overline{ADSP}$ is asserted and $\overline{SE1}$ is high).
83	$\overline{ADV}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
(a) 51, 52, 53, 56, 57, 58, 59, 62, 63 (b) 68, 69, 72, 73, 74, 75, 78, 79, 80 (c) 1, 2, 3, 6, 7, 8, 9, 12, 13 (d) 18, 19, 22, 23, 24, 25, 28, 29, 30	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b, c, d).
86	$\overline{G}$	Input	Asynchronous Output Enable Input: Low — enables output buffers (DQx pins). High — DQx pins are high impedance.
89	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$ and $\overline{LBO}$.
31	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst count (68K/PowerPC). High — interleaved burst count (486/i960/Pentium).
32, 33, 34, 35, 44, 45, 46, 47, 48, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
36, 37	SA1,SA0	Input	Synchronous Address Inputs: These pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
93, 94, 95, 96 (a) (b) (c) (d)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: "x" refers to the byte being written (byte a, b, c, d). $\overline{SGW}$ overrides $\overline{SBx}$.
98	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high — blocks $\overline{ADSP}$ or deselects chip when $\overline{ADSC}$ is asserted.
97	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
92	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
88	$\overline{SGW}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the $\overline{SBx}$ and $\overline{SW}$ signals. If only byte write signals $\overline{SBx}$ are being used, tie this pin high.
87	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{SBx}$ pins. If only byte write signals $\overline{SBx}$ are being used, tie this pin low.
4, 11, 15, 20, 27, 41, 54, 61, 65, 70, 77, 91	V_{DD}	Supply	Power Supply: 3.3 V + 10%, – 5%.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground.
64	NC	Input	No Connection: There is no connection to the chip. For compatibility reasons, it is recommended that this pin be tied low for system designs that do not have a sleep mode associated with the cache/memory controller. Other vendors' RAMs may have implemented this Sleep Mode (ZZ) feature.
14, 16, 38, 39, 42, 43, 49, 50, 66	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE (See Notes 1 through 4)

Next Cycle	Address Used	$\overline{SE1}$	SE2	$\overline{SE3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{G}$ [3]	DQx	Write [2, 4]
Deselect	None	1	X	X	X	0	X	X	High–Z	X
Deselect	None	0	X	1	0	X	X	X	High–Z	X
Deselect	None	0	0	X	0	X	X	X	High–Z	X
Deselect	None	X	X	1	1	0	X	X	High–Z	X
Deselect	None	X	0	X	1	0	X	X	High–Z	X
Begin Read	External	0	1	0	0	X	X	0	DQ	READ
Begin Read	External	0	1	0	1	0	X	0	DQ	READ
Continue Read	Next	X	X	X	1	1	0	1	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	0	DQ	READ
Continue Read	Next	1	X	X	X	1	0	1	High–Z	READ
Continue Read	Next	1	X	X	X	1	0	0	DQ	READ
Suspend Read	Current	X	X	X	1	1	1	1	High–Z	READ
Suspend Read	Current	X	X	X	1	1	1	0	DQ	READ
Suspend Read	Current	1	X	X	X	1	1	1	High–Z	READ
Suspend Read	Current	1	X	X	X	1	1	0	DQ	READ
Begin Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Begin Write	Current	1	X	X	X	1	1	X	High–Z	WRITE
Begin Write	External	0	1	0	1	0	X	X	High–Z	WRITE
Continue Write	Next	X	X	X	1	1	0	X	High–Z	WRITE
Continue Write	Next	1	X	X	X	1	0	X	High–Z	WRITE
Suspend Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Suspend Write	Current	1	X	X	X	1	1	X	High–Z	WRITE

NOTES: 1. X = Don't Care. 1 = logic high. 0 = logic low.
2. Write is defined as either 1) any $\overline{SBx}$ and $\overline{SW}$ low or 2) $\overline{SGW}$ is low.
3. $\overline{G}$ is an asynchronous signal and is not sampled by the clock K. $\overline{G}$ drives the bus immediately (t_{GLQX}) following $\overline{G}$ going low.
4. On write cycles that follow read cycles, $\overline{G}$ must be negated prior to the start of the write cycle to ensure proper write data setup times. $\overline{G}$ must also remain negated at the completion of the write cycle to ensure proper write data hold times.

LINEAR BURST ADDRESS TABLE ($\overline{LBO} = V_{SS}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X10	X . . . X11	X . . . X00
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X00	X . . . X01	X . . . X10

INTERLEAVED BURST ADDRESS TABLE ($\overline{LBO} = V_{DD}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00

WRITE TRUTH TABLE

Cycle Type	$\overline{SGW}$	$\overline{SW}$	$\overline{SBa}$	$\overline{SBb}$	$\overline{SBc}$	$\overline{SBd}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte a	H	L	L	H	H	H
Write Byte b	H	L	H	L	H	H
Write Byte c	H	L	H	H	L	H
Write Byte d	H	L	H	H	H	L
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{DD}	V_{in}	– 0.5 to V_{DD} + 0.5	V
	V_{in} (DQx), V_{out} (DQx)	– 0.5 to 6.0	V
Output Current (per I/O)	I_{out}	± 20	mA
Package Power Dissipation (See Note 2)	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to 85	°C
Storage Temperature	T_{stg}	– 55 to 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Thermal Resistance Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	40 25	°C/W	1, 2
Thermal Resistance Junction to Board (Bottom)		$R_{\theta JB}$	17	°C/W	1, 3
Thermal Resistance Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	1, 4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.135	3.3	3.6	V
Operating Temperature	T_J	20	—	110	°C
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V
Input High Voltage (except DQx)	V_{IH}	2.0	—	V_{DD} + 0.3	V
Input High Voltage (DQx)	V_{IH} (DQx)	2.0	—	5.5**	V

* $V_{IL} \geq -2$ V for $t \leq t_{KHKH}/2$.
** $V_{IH} \leq 6$ V for $t_{KHKH}/2$.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit	Notes
Input Leakage Current (0 V ≤ V_{in} ≤ V_{DD}) (Excluding $\overline{LBO}$)		$I_{lkg(I)}$	—	± 1	µA	
Output Leakage Current (0 V ≤ V_{in} ≤ V_{DD})		$I_{lkg(O)}$	—	± 1	µA	
AC Supply Current (Device Selected, All Outputs Open, All Inputs Toggling at $V_{in} \leq V_{IL}$ or $\geq V_{IH}$, Cycle Time ≥ t_{KHKH} min)	MCM69F536B–8.5 (83 MHz) MCM69F536B–9 (83 MHz) MCM69F536B–10 (66 MHz) MCM69F536B–12 (60 MHz)	I_{DDA}	—	320 320 310 300	mA	2, 3, 4
CMOS Standby Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}, All Inputs Toggling at CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{DD} – 0.2 V)	MCM69F536B–8.5 (83 MHz) MCM69F536B–9 (83 MHz) MCM69F536B–10 (66 MHz) MCM69F536B–12 (60 MHz)	I_{SB1}	—	150 150 140 130	mA	1
Clock Running Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}, All Other Inputs Held to Static CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{DD} – 0.2 V)	MCM69F536B–8.5 (83 MHz) MCM69F536B–9 (83 MHz) MCM69F536B–10 (66 MHz) MCM69F536B–12 (60 MHz)	I_{SB2}	—	55 55 50 45	mA	1
Output Low Voltage (I_{OL} = 8 mA)		V_{OL}	—	0.4	V	
Output High Voltage (I_{OH} = – 4 mA)		V_{OH}	2.4	—	V	

NOTES:
1. Device in deselected mode as defined by the Truth Table.
2. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V)
3. All addresses transition simultaneously low (LSB) and then high (HSB).
4. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	4	6	pF
Input/Output Capacitance	$C_{I/O}$	—	7	9	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1 Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	69F536B–8.5		69F536B–9		69F536B–10		69F536B–12		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	12	—	12	—	15	—	16.6	—	ns	
Clock High Pulse Width	t_{KHKL}	4	—	4	—	5	—	6	—	ns	
Clock Low Pulse Width	t_{KLKH}	4	—	4	—	5	—	6	—	ns	
Clock Access Time	t_{KHQV}	—	8.5	—	9	—	10	—	12	ns	4
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	5	—	6	ns	4
Clock High to Output Active	t_{KHQX1}	0	—	0	—	0	—	0	—	ns	4, 6
Clock High to Output Change	t_{KHQX2}	3	—	3	—	3	—	3	—	ns	4, 6
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	ns	4, 6
Output Disable to Q High–Z	t_{GHQZ}	—	5	—	5	—	5	—	6	ns	5, 6
Clock High to Q High–Z	t_{KHQZ}	3	5	3	5	3	5	3	6	ns	5, 6
Setup Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	t_{ADKH} t_{ADSKH} t_{DVKH} t_{WVKH} t_{EVKH}	2.5	—	2.5	—	2.5	—	2.5	—	ns	
Hold Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	t_{KHAX} t_{KHADSX} t_{KHDX} t_{KHWX} t_{KHEX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	

NOTES:
1. Write is defined as either any $\overline{SBx}$ and $\overline{SW}$ low or $\overline{SGW}$ is low. Chip Enable is defined as $\overline{SE1}$ low, SE2 high and $\overline{SE3}$ low whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care after write cycle begins. To prevent bus contention, $\overline{G}$ should be negated prior to start of write cycle.
4. Tested per AC Test Load (See Figure 1).
5. Measured at ± 200 mV from steady state.
6. This parameter is sampled and not 100% tested.

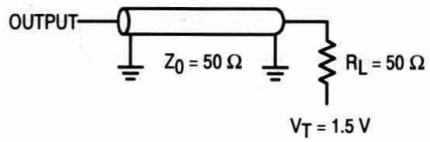
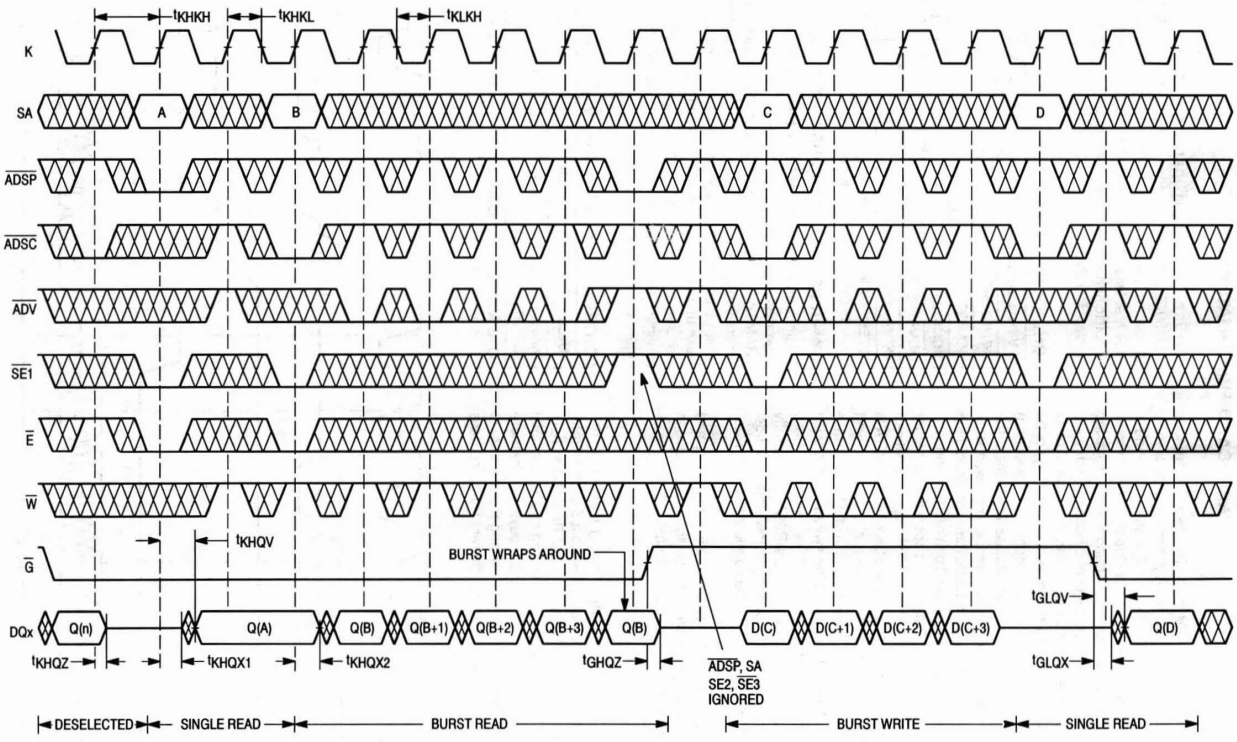


Figure 1. AC Test Loads

READ/WRITE CYCLES



NOTE: $\overline{E}$ low = SE2 high and $\overline{SE3}$ low.
$\overline{W}$ low = $\overline{SGW}$ low and/or $\overline{SW}$ and $\overline{SBx}$ low.

APPLICATION INFORMATION

The MCM69F536B BurstRAM is a high speed synchronous SRAM that is intended for use primarily in secondary or level two (L2) cache memory applications. L2 caches are found in a variety of classes of computers – from the desktop personal computer to the high–end servers and transaction processing machines. For simplicity, the majority of L2 caches today are direct mapped and are single bank implementations. These caches tend to be designed for bus speeds in the range of 33 to 66 MHz. At these bus rates, flow–through (non–pipelined) BurstRAMs can be used since their access times meet the speed requirements for a minimum–latency, zero–wait state L2 cache interface. Latency is a measure (time) of "dead" time the memory system exhibits as a result of a memory request.

For those applications that demand bus operation at greater than 66 MHz or multi–bank L2 caches at 66 MHz, the pipelined (register/register) version of the 32Kx36 BurstRAM (MCM69P536) allows the designer to maintain zero–wait state operation. Multiple banks of BurstRAMs create additional bus loading and can cause the system to otherwise miss its timing requirements. The access time (clock–to–valid–data) of a pipelined BurstRAM is inherently faster than a non–pipelined device by a few nanoseconds. This does not come without cost. The cost is latency – "dead" time.

For L2 cache designs that must minimize both latency and wait states, flow–through BurstRAMs are the best choice in achieving the highest performance in L2 cache design.

FUNCTIONAL EQUIVALENT

The following describes the configuration of the MCM69F536B as a functional equivalent to a 5 V BurstRAM. A migration from 5 V BurstRAMs to 3.3 V BurstRAMs (e.g. MCM69F536B) can be somewhat confusing due to functional and pinout differences. Because the 3.3 V devices offer more pins than the 5 V PLCC devices, it is no longer necessary to supply multiple part numbers for the different burst, address pipeline support ("H" part), etc. options. A single MCM69F536B device can replace two of the 5 V 32Kx18 devices or replace four of the 5 V 32Kx9 devices. Below is a table that lists control pins on the MCM69F536B that can be tied off to either 3.3 V or ground in order to satisfy the migration to this 3.3 V RAM.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

5 V Device Numbers	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
MCM62486B	—	—	—	L	H
MCM62940B	—	—	—	L	L
MCM67B518	—	—	—	L	H
MCM67H518	—	—	—	—	H
MCM67M518	—	—	—	L	L

NOTE: If no tie value is given, then the pin should be used as it was intended on the 5 V device.

NON–BURST SYNCHRONOUS OPERATION

Although this BurstRAM has been designed for 68K–, PowerPC–, 486–, i960, and Pentium – based systems, these SRAMs can be used in other high speed L2 cache or memory applications that do not require the burst address feature. Most L2 caches designed with a synchronous interface can make use of the MCM69F536B. The burst counter feature of the BurstRAM can be disabled, and the SRAM can be configured to act upon a continuous stream of addresses. See Figure 2.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

Desired Operation	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
Sync Non–Burst, Flow–Through SRAM	H	L	H	L	X

NOTE: Although X is specified in the table as a don't care, the pin must be tied either high or low.

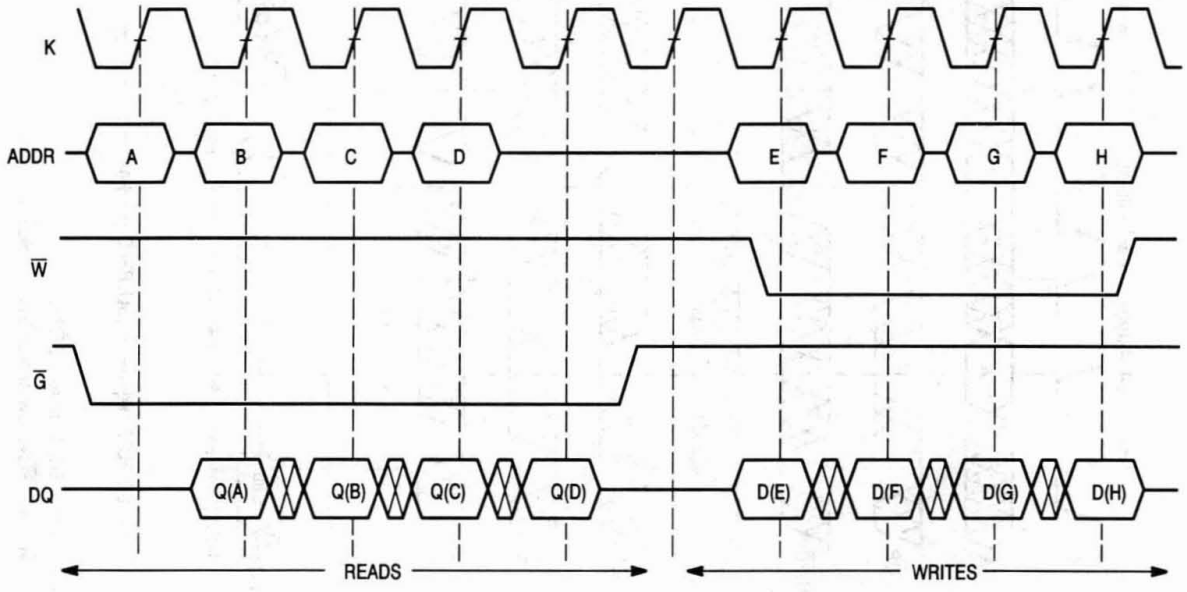
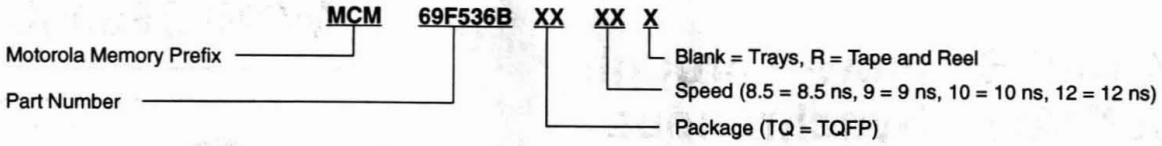


Figure 2. Configured as Non–Burst Synchronous SRAM

ORDERING INFORMATION
(Order by Full Part Number)


MCM 69F536B XX XX X
Motorola Memory Prefix
Part Number
Blank = Trays, R = Tape and Reel
Speed (8.5 = 8.5 ns, 9 = 9 ns, 10 = 10 ns, 12 = 12 ns)
Package (TQ = TQFP)

Full Part Numbers — MCM69F536BTQ8.5 MCM69F536BTQ9 MCM69F536BTQ10 MCM69F536BTQ12
MCM69F536BTQ8.5R MCM69F536BTQ9R MCM69F536BTQ10R MCM69F536BTQ12R

4

MCM69F536C

32K x 36 Bit Flow–Through BurstRAM™ Synchronous Fast Static RAM

TQ PACKAGE
TQFP
CASE 983A–01

The MCM69F536C is a 1M bit synchronous fast static RAM designed to provide a burstable, high performance, secondary cache for the 68K Family, PowerPC™, 486, i960™, and Pentium™ microprocessors. It is organized as 32K words of 36 bits each. This device integrates input registers, a 2 bit address counter, and high speed SRAM onto a single monolithic circuit for reduced parts count in cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (SA), data inputs (DQx), and all control signals except output enable ($\overline{G}$) and Linear Burst Order ($\overline{LBO}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ input pins. Subsequent burst addresses can be generated internally by the MCM69F536C (burst sequence operates in linear or interleaved mode dependent upon state of $\overline{LBO}$) and controlled by the burst address advance ($\overline{ADV}$) input pin.

Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased timing flexibility for incoming signals.

Synchronous byte write ($\overline{SBx}$) and synchronous global write ($\overline{SGW}$), and synchronous write enable $\overline{SW}$ are provided to allow writes to either individual bytes or to all bytes. The four bytes are designated as “a”, “b”, “c”, and “d”. $\overline{SBa}$ controls DQa, $\overline{SBb}$ controls DQb, and so on. Individual bytes are written if the selected byte writes $\overline{SBx}$ are asserted with $\overline{SW}$. All bytes are written if either $\overline{SGW}$ is asserted or if all $\overline{SBx}$ and $\overline{SW}$ are asserted.

For read cycles, a flow–through SRAM allows output data to simply flow freely from the memory array.

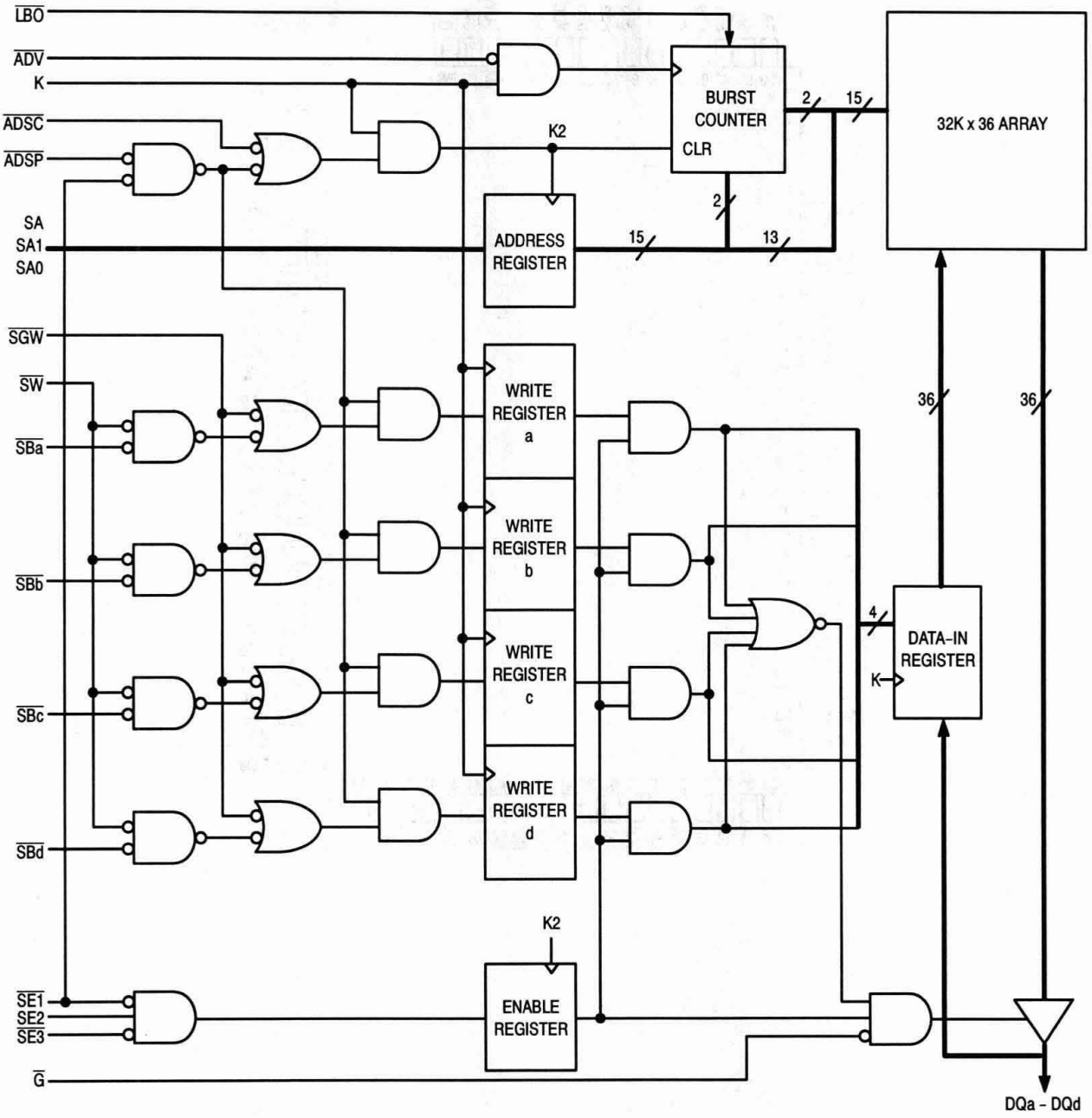
The MCM69F536C operates from a 3.3 V power supply and all inputs and outputs are LVTTL compatible.

- MCM69F536C–8.5 = 8.5 ns Access / 12 ns Cycle
  MCM69F536C–9 = 9 ns Access / 12 ns Cycle
  MCM69F536C–10 = 10 ns Access / 15 ns Cycle
  MCM69F536C–12 = 12 ns Access / 16.6 ns Cycle
- Single 3.3 V + 10%, – 5% Power Supply
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Selectable Burst Sequencing Order (Linear/Interleaved)
- Internally Self–Timed Write Cycle
- Byte Write and Global Write Control
- 5 V Tolerant on all Pins (Inputs and I/Os)
- 100 Pin TQFP Package

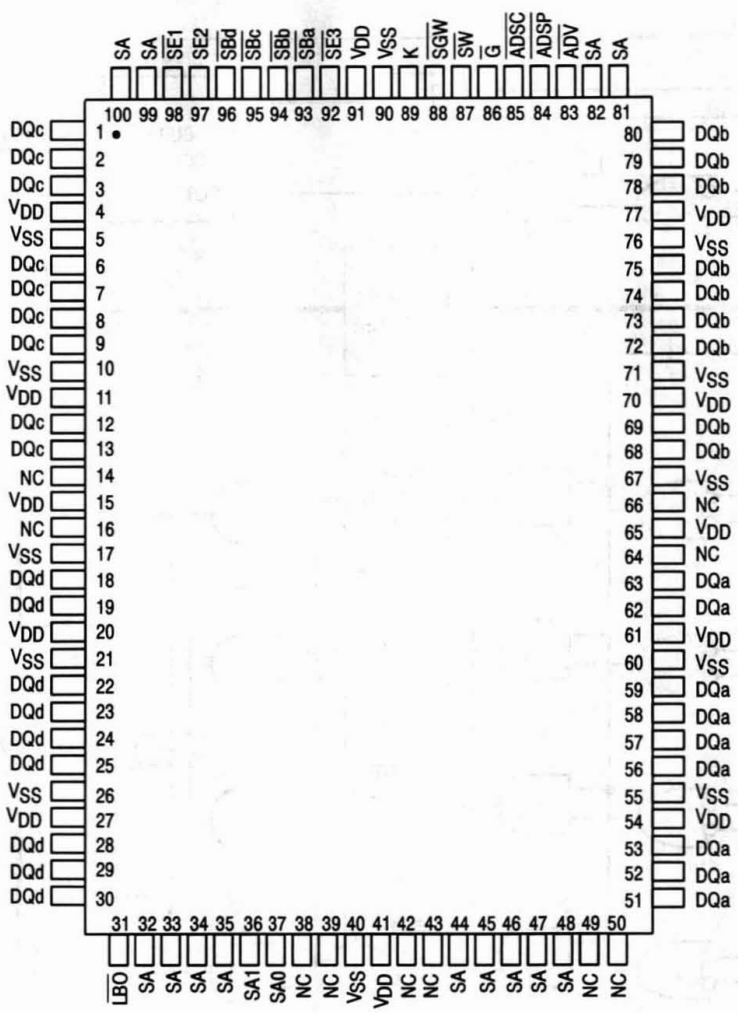
The PowerPC name is a trademark of IBM Corp., used under license therefrom.
i960 and Pentium are trademarks of Intel Corp.

REV 2
4/10/97

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENT



4

PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: Initiates READ, WRITE, or chip deselect cycle.
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: Initiates READ, WRITE, or chip deselect cycle (exception — chip deselect does not occur when $\overline{ADSP}$ is asserted and $\overline{SE1}$ is high).
83	$\overline{ADV}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
(a) 51, 52, 53, 56, 57, 58, 59, 62, 63 (b) 68, 69, 72, 73, 74, 75, 78, 79, 80 (c) 1, 2, 3, 6, 7, 8, 9, 12, 13 (d) 18, 19, 22, 23, 24, 25, 28, 29, 30	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b, c, d).
86	$\overline{G}$	Input	Asynchronous Output Enable Input: Low — enables output buffers (DQx pins). High — DQx pins are high impedance.
89	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$ and $\overline{LBO}$.
31	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst count (68K/PowerPC). High — interleaved burst count (486/i960/Pentium).
32, 33, 34, 35, 44, 45, 46, 47, 48, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
36, 37	SA1, SA0	Input	Synchronous Address Inputs: These pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
93, 94, 95, 96 (a) (b) (c) (d)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: "x" refers to the byte being written (byte a, b, c, d). $\overline{SGW}$ overrides $\overline{SBx}$.
98	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high — blocks $\overline{ADSP}$ or deselects chip when $\overline{ADSC}$ is asserted.
97	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
92	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
88	$\overline{SGW}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the $\overline{SBx}$ and $\overline{SW}$ signals. If only byte write signals $\overline{SBx}$ are being used, tie this pin high.
87	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{SBx}$ pins. If only byte write signals $\overline{SBx}$ are being used, tie this pin low.
4, 11, 15, 20, 27, 41, 54, 61, 65, 70, 77, 91	V_{DD}	Supply	Power Supply: 3.3 V + 10%, – 5%.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground.
64	NC	Input	No Connection: There is no connection to the chip. For compatibility reasons, it is recommended that this pin be tied low for system designs that do not have a sleep mode associated with the cache/memory controller. Other vendors' RAMs may have implemented this Sleep Mode (ZZ) feature.
14, 16, 38, 39, 42, 43, 49, 50, 66	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE (See Notes 1 through 4)

Next Cycle	Address Used	$\overline{SE1}$	SE2	$\overline{SE3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{G}$ [3]	DQx	Write [2, 4]
Deselect	None	1	X	X	X	0	X	X	High–Z	X
Deselect	None	0	X	1	0	X	X	X	High–Z	X
Deselect	None	0	0	X	0	X	X	X	High–Z	X
Deselect	None	X	X	1	1	0	X	X	High–Z	X
Deselect	None	X	0	X	1	0	X	X	High–Z	X
Begin Read	External	0	1	0	0	X	X	0	DQ	READ
Begin Read	External	0	1	0	1	0	X	0	DQ	READ
Continue Read	Next	X	X	X	1	1	0	1	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	0	DQ	READ
Continue Read	Next	1	X	X	X	1	0	1	High–Z	READ
Continue Read	Next	1	X	X	X	1	0	0	DQ	READ
Suspend Read	Current	X	X	X	1	1	1	1	High–Z	READ
Suspend Read	Current	X	X	X	1	1	1	0	DQ	READ
Suspend Read	Current	1	X	X	X	1	1	1	High–Z	READ
Suspend Read	Current	1	X	X	X	1	1	0	DQ	READ
Begin Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Begin Write	Current	1	X	X	X	1	1	X	High–Z	WRITE
Begin Write	External	0	1	0	1	0	X	X	High–Z	WRITE
Continue Write	Next	X	X	X	1	1	0	X	High–Z	WRITE
Continue Write	Next	1	X	X	X	1	0	X	High–Z	WRITE
Suspend Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Suspend Write	Current	1	X	X	X	1	1	X	High–Z	WRITE

NOTES: 1. X = Don't Care. 1 = logic high. 0 = logic low.
2. Write is defined as either 1) any $\overline{SBx}$ and $\overline{SW}$ low or 2) $\overline{SGW}$ is low.
3. $\overline{G}$ is an asynchronous signal and is not sampled by the clock K. $\overline{G}$ drives the bus immediately (t_{GLQX}) following $\overline{G}$ going low.
4. On write cycles that follow read cycles, $\overline{G}$ must be negated prior to the start of the write cycle to ensure proper write data setup times. $\overline{G}$ must also remain negated at the completion of the write cycle to ensure proper write data hold times.

LINEAR BURST ADDRESS TABLE ($\overline{LBO} = V_{SS}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

INTERLEAVED BURST ADDRESS TABLE ($\overline{LBO} = V_{DD}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

WRITE TRUTH TABLE

Cycle Type	SGW	SW	SBa	SBb	SBc	SBd
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte a	H	L	L	H	H	H
Write Byte b	H	L	H	L	H	H
Write Byte c	H	L	H	H	L	H
Write Byte d	H	L	H	H	H	L
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{DD}	V_{in}, V_{out}	– 0.5 to 6.0	V
Output Current (per I/O)	I_{out}	± 20	mA
Package Power Dissipation (See Note 2)	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to 85	°C
Storage Temperature	T_{stg}	– 55 to 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Thermal Resistance Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	40 25	°C/W	1, 2
Thermal Resistance Junction to Board (Bottom)		$R_{\theta JB}$	17	°C/W	1, 3
Thermal Resistance Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	1, 4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

4

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.135	3.3	3.6	V
Operating Temperature	T_J	20	—	110	°C
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	5.5**	V

*$V_{IL} \geq -2$ V for $t \leq t_{KHKH}/2$.
**$V_{IH} \leq 6$ V for $t_{KHKH}/2$.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit	Notes
Input Leakage Current (0 V ≤ V_{in} ≤ V_{DD}) (Excluding $\overline{LBO}$)		$I_{lkg(I)}$	—	± 1	µA	
Output Leakage Current (0 V ≤ V_{in} ≤ V_{DD})		$I_{lkg(O)}$	—	± 1	µA	
AC Supply Current (Device Selected, All Outputs Open, All Inputs Toggling at $V_{in} \leq V_{IL}$ or $\geq V_{IH}$, Cycle Time ≥ t_{KHKH} min)	MCM69F536C–8.5 (83 MHz) MCM69F536C–9 (83 MHz) MCM69F536C–10 (66 MHz) MCM69F536C–12 (60 MHz)	I_{DDA}	—	320 320 310 300	mA	2, 3, 4
CMOS Standby Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}, All Inputs Toggling at CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{DD} – 0.2 V)	MCM69F536C–8.5 (83 MHz) MCM69F536C–9 (83 MHz) MCM69F536C–10 (66 MHz) MCM69F536C–12 (60 MHz)	I_{SB1}	—	150 150 140 130	mA	1
Clock Running Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}, All Other Inputs Held to Static CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{DD} – 0.2 V)	MCM69F536C–8.5 (83 MHz) MCM69F536C–9 (83 MHz) MCM69F536C–10 (66 MHz) MCM69F536C–12 (60 MHz)	I_{SB2}	—	55 55 50 45	mA	1
Output Low Voltage (I_{OL} = 8 mA)		V_{OL}	—	0.4	V	
Output High Voltage (I_{OH} = – 4 mA)		V_{OH}	2.4	—	V	

NOTES:
1. Device in deselected mode as defined by the Truth Table.
2. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
3. All addresses transition simultaneously low (LSB) and then high (HSB).
4. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	4	6	pF
Input/Output Capacitance	$C_{I/O}$	—	7	9	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1 Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	69F536C–8.5		69F536C–9		69F536C–10		69F536C–12		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	12	—	12	—	15	—	16.6	—	ns	
Clock High Pulse Width	t_{KHKL}	4	—	4	—	5	—	6	—	ns	
Clock Low Pulse Width	t_{KLKH}	4	—	4	—	5	—	6	—	ns	
Clock Access Time	t_{KHQV}	—	8.5	—	9	—	10	—	12	ns	4
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	5	—	6	ns	4
Clock High to Output Active	t_{KHQX1}	0	—	0	—	0	—	0	—	ns	4, 6
Clock High to Output Change	t_{KHQX2}	3	—	3	—	3	—	3	—	ns	4, 6
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	ns	4, 6
Output Disable to Q High–Z	t_{GHQZ}	—	5	—	5	—	5	—	6	ns	5, 6
Clock High to Q High–Z	t_{KHQZ}	3	5	3	5	3	5	3	6	ns	5, 6
Setup Times: Address	t_{ADKH}	2.5	—	2.5	—	2.5	—	2.5	—	ns	
$\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$	t_{ADSKH}										
Data In	t_{DVKH}										
Write	t_{WVKH}										
Chip Enable	t_{EVKH}										
Hold Times: Address	t_{KHAX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	
$\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$	t_{KHADSX}										
Data In	t_{KHDX}										
Write	t_{KHWX}										
Chip Enable	t_{KHEX}										

NOTES:
1. Write is defined as either any $\overline{SBx}$ and $\overline{SW}$ low or $\overline{SGW}$ is low. Chip Enable is defined as $\overline{SE1}$ low, SE2 high and $\overline{SE3}$ low whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care after write cycle begins. To prevent bus contention, $\overline{G}$ should be negated prior to start of write cycle.
4. Tested per AC Test Load (See Figure 1).
5. Measured at ± 200 mV from steady state.
6. This parameter is sampled and not 100% tested.

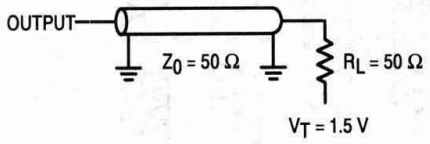
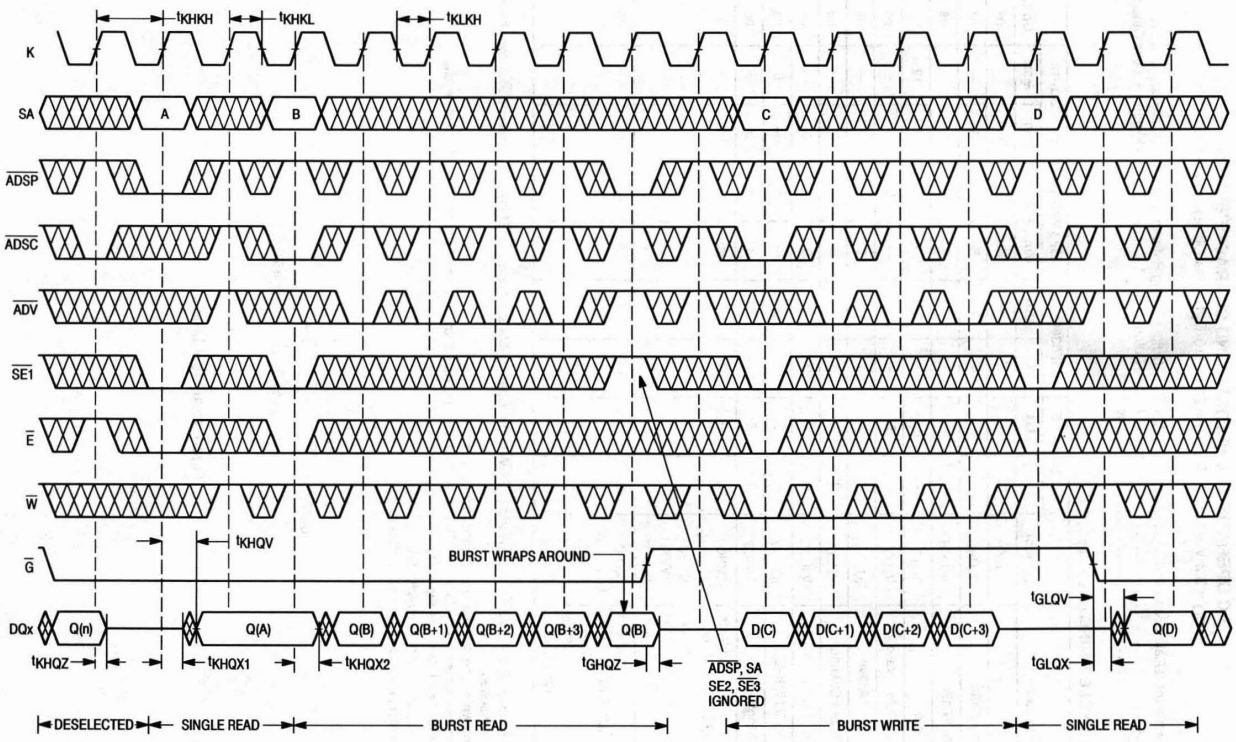


Figure 1. AC Test Loads

READ/WRITE CYCLES



NOTE: $\overline{E}$ low = SE2 high and $\overline{SE3}$ low.
$\overline{W}$ low = $\overline{SGW}$ low and/or $\overline{SW}$ and $\overline{SBx}$ low.

APPLICATION INFORMATION

The MCM69F536C BurstRAM is a high speed synchronous SRAM that is intended for use primarily in secondary or level two (L2) cache memory applications. L2 caches are found in a variety of classes of computers — from the desktop personal computer to the high–end servers and transaction processing machines. For simplicity, the majority of L2 caches today are direct mapped and are single bank implementations. These caches tend to be designed for bus speeds in the range of 33 to 66 MHz. At these bus rates, flow–through (non–pipelined) BurstRAMs can be used since their access times meet the speed requirements for a minimum–latency, zero–wait state L2 cache interface. Latency is a measure (time) of "dead" time the memory system exhibits as a result of a memory request.

For those applications that demand bus operation at greater than 66 MHz or multi–bank L2 caches at 66 MHz, the pipelined (register/register) version of the 32K x 36 BurstRAM (MCM69P536) allows the designer to maintain zero–wait state operation. Multiple banks of BurstRAMs create additional bus loading and can cause the system to otherwise miss its timing requirements. The access time (clock–to–valid–data) of a pipelined BurstRAM is inherently faster than a non–pipelined device by a few nanoseconds. This does not come without cost. The cost is latency — "dead" time.

For L2 cache designs that must minimize both latency and wait states, flow–through BurstRAMs are the best choice in achieving the highest performance in L2 cache design.

FUNCTIONAL EQUIVALENT

The following describes the configuration of the MCM69F536C as a functional equivalent to a 5 V BurstRAM. A migration from 5 V BurstRAMs to 3.3 V BurstRAMs (e.g., MCM69F536C) can be somewhat confusing due to functional and pinout differences. Because the 3.3 V devices offer more pins than the 5 V PLCC devices, it is no longer necessary to supply multiple part numbers for the different burst, address pipeline support ("H" part), etc. options. A single MCM69F536C device can replace two of the 5 V 32K x 18 devices or replace four of the 5 V 32K x 9 devices. Below is a table that lists control pins on the MCM69F536C that can be tied off to either 3.3 V or ground in order to satisfy the migration to this 3.3 V RAM.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

5 V Device Numbers	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
MCM62486B	—	—	—	L	H
MCM62940B	—	—	—	L	L
MCM67B518	—	—	—	L	H
MCM67H518	—	—	—	—	H
MCM67M518	—	—	—	L	L

NOTE: If no tie value is given, then the pin should be used as it was intended on the 5 V device.

NON–BURST SYNCHRONOUS OPERATION

Although this BurstRAM has been designed for 68K–, PowerPC–, 486–, i960–, and Pentium–based systems, these SRAMs can be used in other high speed L2 cache or memory applications that do not require the burst address feature. Most L2 caches designed with a synchronous interface can make use of the MCM69F536C. The burst counter feature of the BurstRAM can be disabled, and the SRAM can be configured to act upon a continuous stream of addresses. See Figure 2.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

Desired Operation	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
Sync Non–Burst, Flow–Through SRAM	H	L	H	L	X

NOTE: Although X is specified in the table as a don't care, the pin must be tied either high or low.

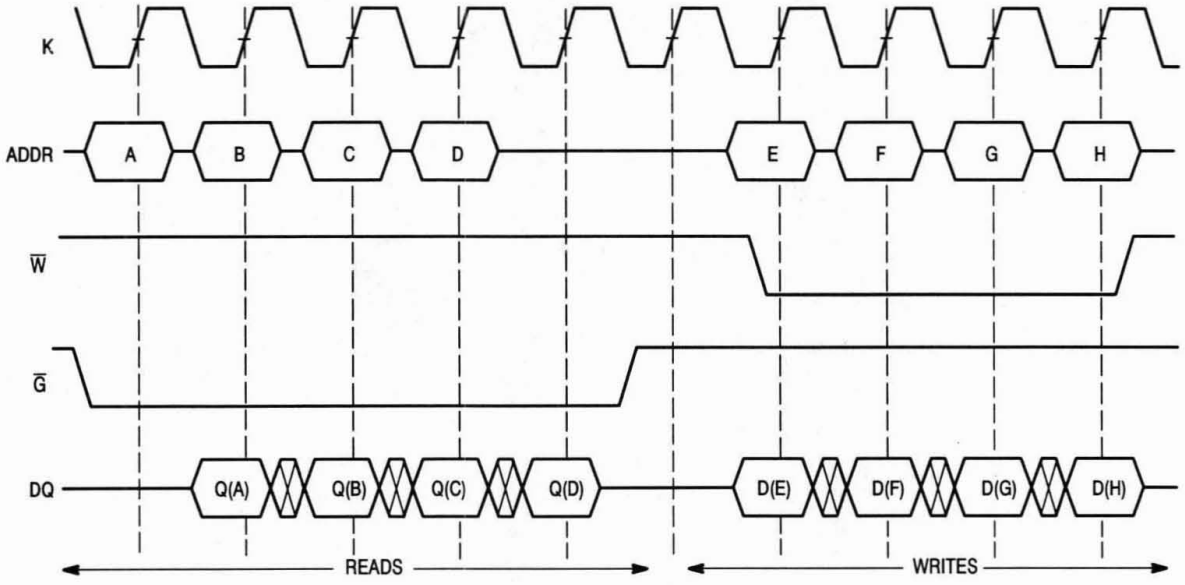
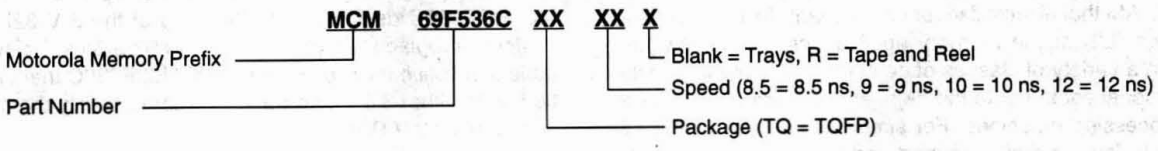


Figure 2. Configured as Non–Burst Synchronous SRAM

ORDERING INFORMATION
(Order by Full Part Number)

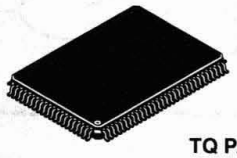

MCM 69F536C XX XX X
Motorola Memory Prefix
Part Number
Blank = Trays, R = Tape and Reel
Speed (8.5 = 8.5 ns, 9 = 9 ns, 10 = 10 ns, 12 = 12 ns)
Package (TQ = TQFP)

Full Part Numbers — MCM69F536CTQ8.5 MCM69F536CTQ9 MCM69F536CTQ10 MCM69F536CTQ12
MCM69F536CTQ8.5R MCM69F536CTQ9R MCM69F536CTQ10R MCM69F536CTQ12R

4

MCM69P536A

32K x 36 Bit Pipelined BurstRAM™ Synchronous Fast Static RAM



TQ PACKAGE
TQFP
CASE 983A–01

The MCM69P536A is a 1M bit synchronous fast static RAM designed to provide a burstable, high performance, secondary cache for the 68K Family, PowerPC™, 486, i960™ and Pentium™ microprocessors. It is organized as 32K words of 36 bits each. This device integrates input registers, an output register, a 2–bit address counter, and high speed SRAM onto a single monolithic circuit for reduced parts count in cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (SA), data inputs (DQx), and all control signals except output enable ($\overline{G}$) and Linear Burst Order ($\overline{LBO}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ input pins. Subsequent burst addresses can be generated internally by the MCM69P536A (burst sequence operates in linear or interleaved mode dependent upon state of $\overline{LBO}$) and controlled by the burst address advance ($\overline{ADV}$) input pin.

Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased timing flexibility for incoming signals.

Synchronous byte write ($\overline{SBx}$), synchronous global write ($\overline{SGW}$), and synchronous write enable $\overline{SW}$ are provided to allow writes to either individual bytes or to all bytes. The four bytes are designated as “a”, “b”, “c”, and “d”. $\overline{SBa}$ controls DQa, $\overline{SBb}$ controls DQb, etc. Individual bytes are written if the selected byte writes $\overline{SBx}$ are asserted with $\overline{SW}$. All bytes are written if either $\overline{SGW}$ is asserted or if all $\overline{SBx}$ and $\overline{SW}$ are asserted.

For read cycles, pipelined SRAMs output data is temporarily stored by an edge–triggered output register and then released to the output buffers at the next rising edge of clock (K).

The MCM69P536A operates from a 3.3 V power supply and all inputs and outputs are LVTTL compatible.

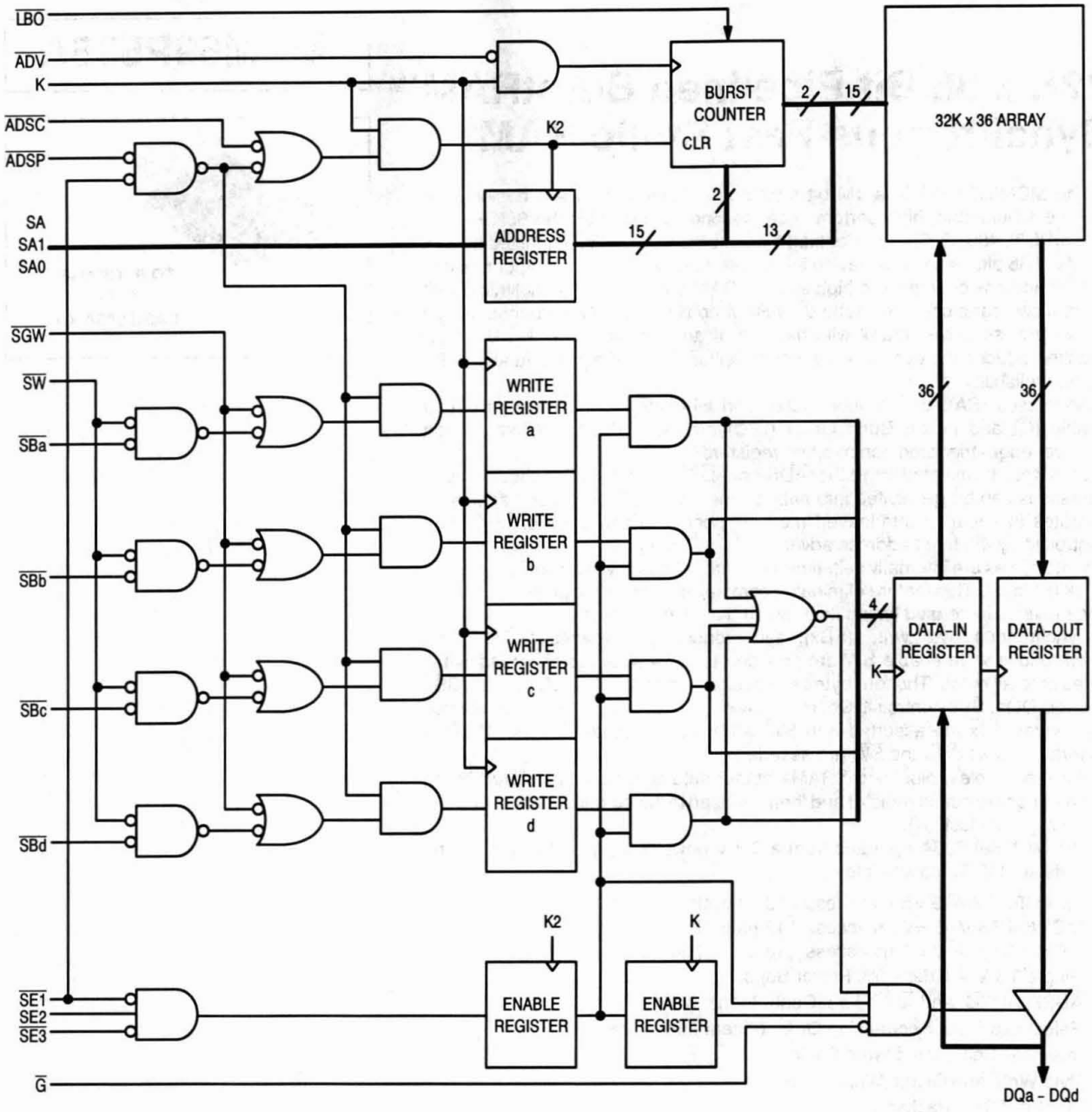
- MCM69P536A–5 = 5 ns access / 10 ns cycle
  MCM69P536A–6 = 6 ns access / 12 ns cycle
  MCM69P536A–7 = 7 ns access / 13.3 ns cycle
- Single 3.3 V + 10%, – 5% Power Supply
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Selectable Burst Sequencing Order (Linear/Interleaved)
- Internally Self–Timed Write Cycle
- Byte Write and Global Write Control
- 100 Pin TQFP Package

4

BurstRAM is a trademark of Motorola, Inc.
The PowerPC name is a trademark of IBM Corp., used under license therefrom.
i960 and Pentium are trademarks of Intel Corp.

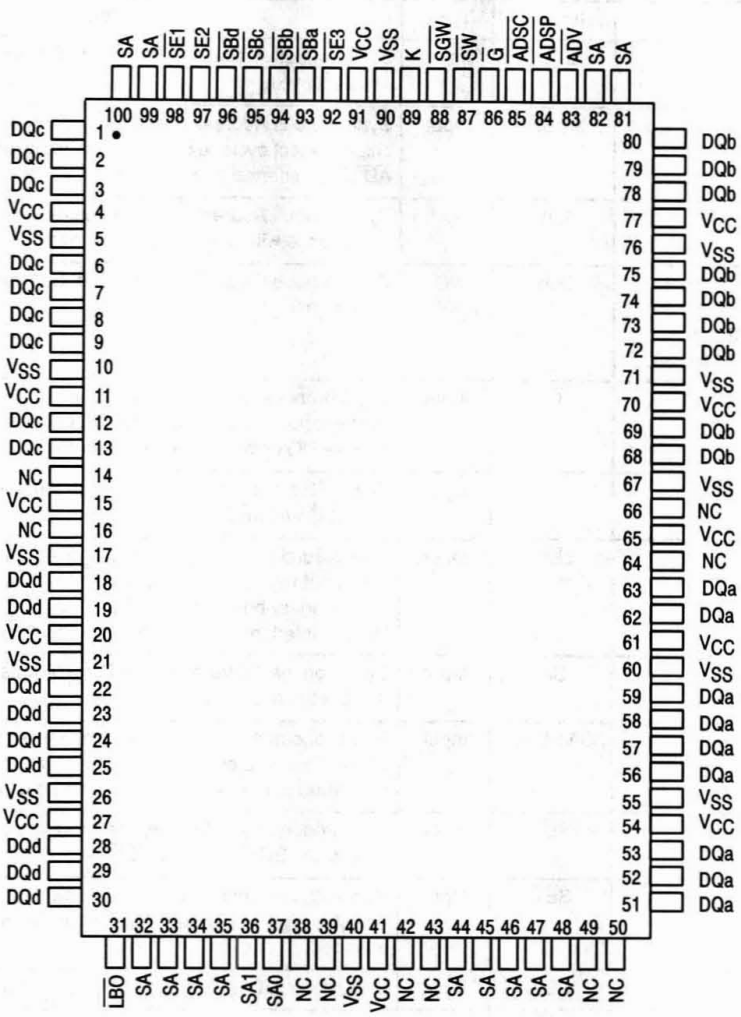
REV 2
4/10/97

FUNCTIONAL BLOCK DIAGRAM



4

PIN ASSIGNMENT



4

PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: Initiates READ, WRITE or chip deselect cycle.
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: Initiates READ, WRITE or chip deselect cycle (exception — chip deselect does not occur when $\overline{ADSP}$ is asserted and $\overline{SE1}$ is high).
83	$\overline{ADV}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
(a) 51, 52, 53, 56, 57, 58, 59, 62, 63 (b) 68, 69, 72, 73, 74, 75, 78, 79, 80 (c) 1, 2, 3, 6, 7, 8, 9, 12, 13 (d) 18, 19, 22, 23, 24, 25, 28, 29, 30	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b, c, d).
86	$\overline{G}$	Input	Asynchronous Output Enable Input: Low — enables output buffers (DQx pins). High — DQx pins are high impedance.
89	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$ and $\overline{LBO}$.
31	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst counter (68K/PowerPC). High — interleaved burst counter (486/i960/Pentium).
32, 33, 34, 35, 44, 45, 46, 47, 48, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
36, 37	SA1,SA0	Input	Synchronous Address Inputs: These pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
93, 94, 95, 96 (a) (b) (c) (d)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: "x" refers to the byte being written (byte a, b, c, d). $\overline{SGW}$ overrides $\overline{SBx}$.
98	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high — blocks $\overline{ADSP}$ or deselects chip when $\overline{ADSC}$ is asserted.
97	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
92	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
88	$\overline{SGW}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the $\overline{SBx}$ and $\overline{SW}$ signals. If only byte write signals $\overline{SBx}$ are being used, tie this pin high.
87	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{SBx}$ pins. If only byte write signals $\overline{SBx}$ are being used, tie this pin low.
4, 11, 15, 20, 27, 41, 54, 61, 65, 70, 77, 91	V_{CC}	Supply	Power Supply: 3.3 V + 10%, – 5%.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground.
64	NC	Input	No Connection: There is no connection to the chip. For compatibility reasons, it is recommended that this pin be tied low for system designs that do not have a sleep mode associated with the cache/memory controller. Other vendors' RAMs may have implemented the Sleep Mode (ZZ) feature.
14, 16, 38, 39, 42, 43, 49, 50, 66	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE (See Notes 1 through 4)

Next Cycle	Address Used	$\overline{SE1}$	SE2	$\overline{SE3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{G}$ [3]	DQx	Write [2, 4]
Deselect	None	1	X	X	X	0	X	X	High–Z	X
Deselect	None	0	X	1	0	X	X	X	High–Z	X
Deselect	None	0	0	X	0	X	X	X	High–Z	X
Deselect	None	X	X	1	1	0	X	X	High–Z	X
Deselect	None	X	0	X	1	0	X	X	High–Z	X
Begin Read	External	0	1	0	0	X	X	X	High–Z	READ
Begin Read	External	0	1	0	1	0	X	X	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	1	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	0	DQ	READ
Continue Read	Next	1	X	X	X	1	0	1	High–Z	READ
Continue Read	Next	1	X	X	X	1	0	0	DQ	READ
Suspend Read	Current	X	X	X	1	1	1	1	High–Z	READ
Suspend Read	Current	X	X	X	1	1	1	0	DQ	READ
Suspend Read	Current	1	X	X	X	1	1	1	High–Z	READ
Suspend Read	Current	1	X	X	X	1	1	0	DQ	READ
Begin Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Begin Write	Current	1	X	X	X	1	1	X	High–Z	WRITE
Begin Write	External	0	1	0	1	0	X	X	High–Z	WRITE
Continue Write	Next	X	X	X	1	1	0	X	High–Z	WRITE
Continue Write	Next	1	X	X	X	1	0	X	High–Z	WRITE
Suspend Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Suspend Write	Current	1	X	X	X	1	1	X	High–Z	WRITE

NOTES: 1. X = Don't Care. 1 = logic high. 0 = logic low.
2. Write is defined as either 1) any $\overline{SBx}$ and $\overline{SW}$ low or 2) $\overline{SGW}$ is low.
3. $\overline{G}$ is an asynchronous signal and is not sampled by the clock K. $\overline{G}$ drives the bus immediately (t_{GLQX}) following $\overline{G}$ going low.
4. On write cycles that follow read cycles, $\overline{G}$ must be negated prior to the start of the write cycle to ensure proper write data setup times. $\overline{G}$ must also remain negated at the completion of the write cycle to ensure proper write data hold times.

LINEAR BURST ADDRESS TABLE ($\overline{LBO} = V_{SS}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X10	X . . . X11	X . . . X00
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X00	X . . . X01	X . . . X10

INTERLEAVED BURST ADDRESS TABLE ($\overline{LBO} = V_{CC}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00

WRITE TRUTH TABLE

Cycle Type	$\overline{SGW}$	$\overline{SW}$	$\overline{SBa}$	$\overline{SBb}$	$\overline{SBc}$	$\overline{SBd}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte a	H	L	L	H	H	H
Write Byte b	H	L	H	L	H	H
Write Byte c	H	L	H	H	L	H
Write Byte d	H	L	H	H	H	L
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Package Power Dissipation (See Note 2)	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to 85	°C
Storage Temperature	T_{stg}	– 55 to 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Thermal Resistance Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	40 25	°C/W	1, 2
Thermal Resistance Junction to Board (Bottom)		$R_{\theta JB}$	17	°C/W	1, 3
Thermal Resistance Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	1, 4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V + 10%, – 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.135	3.3	3.6	V
Operating Temperature	T_J	20	—	110	°C
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V

* $V_{IL} \geq -2$ V for $t \leq t_{KHKH}/2$.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (0 V ≤ V_{in} ≤ V_{CC}) (Excluding $\overline{LBO}$)		$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current (0 V ≤ V_{in} ≤ V_{CC})		$I_{lkg(O)}$	—	± 1	µA
AC Supply Current (Device Selected, All Outputs Open, All Inputs Toggling at $V_{in} \leq V_{IL}$ or $\geq V_{IH}$, Cycle Time $\geq t_{KHKH}$ min)	MCM69P536A–5 (100 MHz) MCM69P536A–6 (83 MHz) MCM69P536A–7 (75 MHz)	I_{CCA}	—	320 310 300	mA
CMOS Standby Supply Current (Deselected[1], Clock (K) Cycle Time $\geq t_{KHKH}$, All Inputs Toggling at CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or $\geq V_{CC}$ – 0.2 V)	MCM69P536A–5 (100 MHz) MCM69P536A–6 (83 MHz) MCM69P536A–7 (75 MHz)	I_{SB1}	—	150 140 130	mA
Clock Running Supply Current (Deselected[1], Clock (K) Cycle Time $\geq t_{KHKH}$, All Other Inputs Held to Static CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or $\geq V_{CC}$ – 0.2 V)	MCM69P536A–5 (100 MHz) MCM69P536A–6 (83 MHz) MCM69P536A–7 (75 MHz)	I_{SB2}	—	55 50 45	mA
Output Low Voltage (I_{OL} = 8 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4 mA)		V_{OH}	2.4	—	V

NOTE: 1. Device in Deselected mode as defined by the Truth Table.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	4	6	pF
Input/Output Capacitance	$C_{I/O}$	—	7	9	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V + 10%, – 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1 Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM69P536A–5		MCM69P536A–6		MCM69P536A–7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	10	—	12	—	13.3	—	ns	
Clock High Pulse Width	t_{KHKL}	3	—	4	—	4.5	—	ns	
Clock Low Pulse Width	t_{KLKH}	3	—	4	—	4.5	—	ns	
Clock Access Time	t_{KHQV}	—	5	—	6	—	7	ns	4
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	6	ns	4
Clock High to Output Active	t_{KHQX1}	0	—	0	—	0	—	ns	4
Clock High to Output Change	t_{KHQX2}	2	—	2	—	2	—	ns	4
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4
Output Disable to Q High–Z	t_{GHQZ}	—	5	—	5	—	5	ns	5
Clock High to Q High–Z	t_{KHQZ}	2	5	2	5	2	5	ns	5
Setup Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	t_{ADKH} t_{ADSKH} t_{DVKH} t_{WVKH} t_{EVKH}	2.5	—	2.5	—	2.5	—	ns	
Hold Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	t_{KHAX} t_{KHADSX} t_{KHDX} t_{KHWX} t_{KHEX}	0.5	—	0.5	—	0.5	—	ns	

NOTES:
1. Write is defined as either any $\overline{SBx}$ and $\overline{SW}$ low or $\overline{SGW}$ is low. Chip Enable is defined as $\overline{SE1}$ low, SE2 high and $\overline{SE3}$ low whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care after write cycle begins. To prevent bus contention, $\overline{G}$ should be negated prior to start of write cycle.
4. Tested per AC Test Load (See Figure 1).
5. Measured at ± 200 mV from steady state.

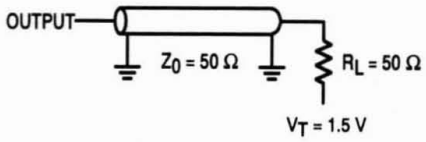
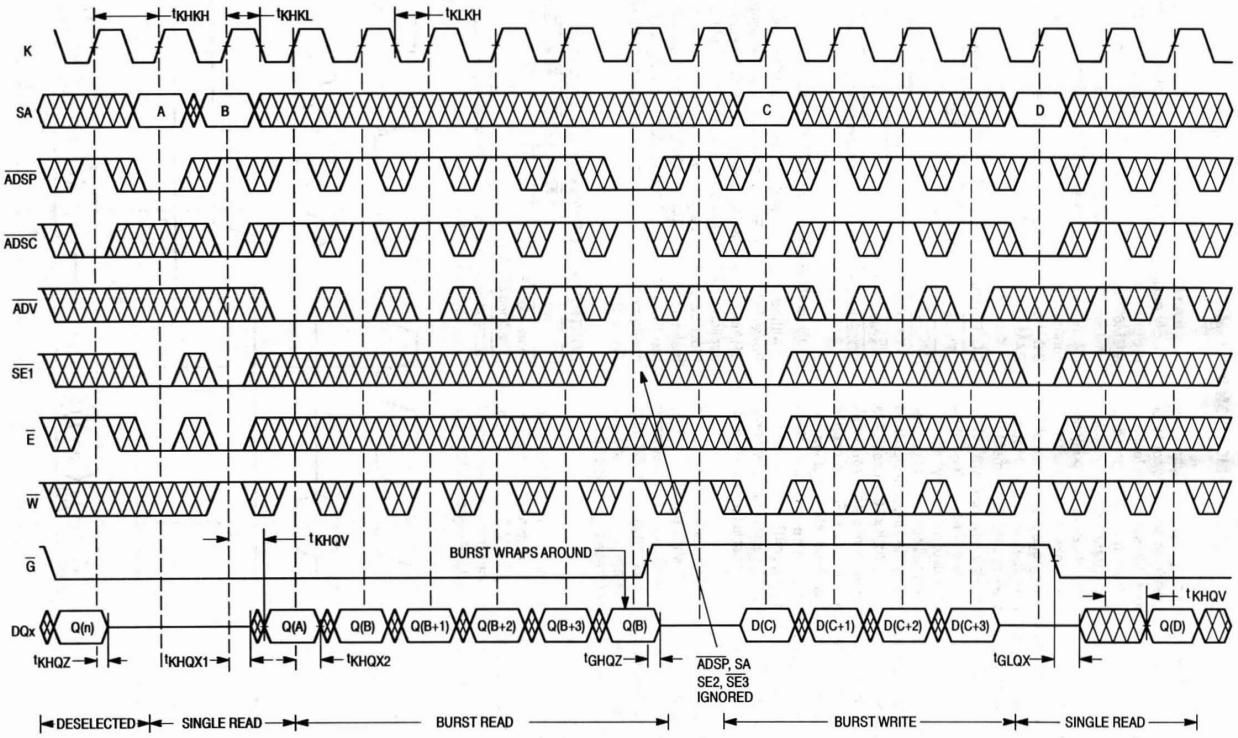


Figure 1. AC Test Loads

READ/WRITE CYCLES



Note: $\overline{E}$ low = SE2 high and $\overline{SE3}$ low.
$\overline{W}$ low = $\overline{SGW}$ low and / or $\overline{SW}$ and $\overline{SBx}$ low.

APPLICATION INFORMATION

The MCM69P536A BurstRAM is a high speed synchronous SRAM that is intended for use primarily in secondary or level two (L2) cache memory applications. L2 caches are found in a variety of classes of computers – from the desktop personal computer to the high–end servers and transaction processing machines. For simplicity, the majority of L2 caches today are direct mapped and are single bank implementations. These caches tend to be designed for bus speeds in the range of 33 to 66 MHz. At these bus rates, non–pipelined (flow–through) BurstRAMs can be used since their access times meet the speed requirements for a minimum–latency, zero–wait state L2 cache interface. Latency is a measure (time) of "dead" time the memory system exhibits as a result of a memory request.

For those applications that demand bus operation at greater than 66 MHz or multi–bank L2 caches at 66 MHz, the pipelined (register/register) version of the 32Kx36 BurstRAM (MCM69P536A) allows the designer to maintain zero–wait state operation. Multiple banks of BurstRAMs create additional bus loading and can cause the system to otherwise miss its timing requirements. The access time (clock–to–valid–data) of a pipelined BurstRAM is inherently faster than a non–pipelined device by a few nanoseconds. This does not come without cost. The cost is latency – "dead" time.

Since most L2 caches are tied to the processor bus and bus speeds continue to increase over time, pipelined (R/R) BurstRAMs are the best choice in achieving zero–wait state L2 cache performance. At bus speeds ranging from 66 MHz to 100 MHz, pipelined BurstRAMs are able to provide fast clock to valid data times required of these high speed buses.

FUNCTIONAL EQUIVALENT

The following describes the configuration of the MCM69P536A as a functional equivalent to a 5 V BurstRAM. A migration from 5 V BurstRAMs to 3.3 V BurstRAMs (e.g. MCM69P536A) can be somewhat confusing due to functional and pinout differences. Because the 3.3 V devices offer more pins than the 5 V PLCC devices, it is no longer necessary to supply multiple part numbers for the different burst, address pipeline support ("H" part), etc. options. A single MCM69P536A device can replace two of the 5 V 32K x 18 devices. The MCM69P536A can be configured to function as if it were one of the 5 V BurstRAMs. Below is a table that lists control pins on the MCM69P536A that can be tied off to either 3.3 V or ground in order to satisfy the migration to this 3.3 V RAM.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

5 V Device Numbers	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
MCM67C518	—	—	—	L	H
MCM67J518	—	—	—	—	H
MCM67N518	—	—	—	L	L

NOTE: If no tie value is given, then the pin should be used as intended on the 5 V device.

NON–BURST SYNCHRONOUS OPERATION

Although this BurstRAM has been designed for 68K–, PowerPC–, 486–, i960, and Pentium – based systems, these SRAMs can be used in other high speed L2 cache or memory applications that do not require the burst address feature. Most L2 caches designed with a synchronous interface can make use of the MCM69P536A. The burst counter feature of the BurstRAM can be disabled, and the SRAM can be configured to act upon a continuous stream of addresses. See Figure 2.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

Non–Burst	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
Sync Non–Burst, Pipelined SRAM	H	L	H	L	X

NOTE: Although X is specified in the table as a don't care, the pin must be tied either high or low.

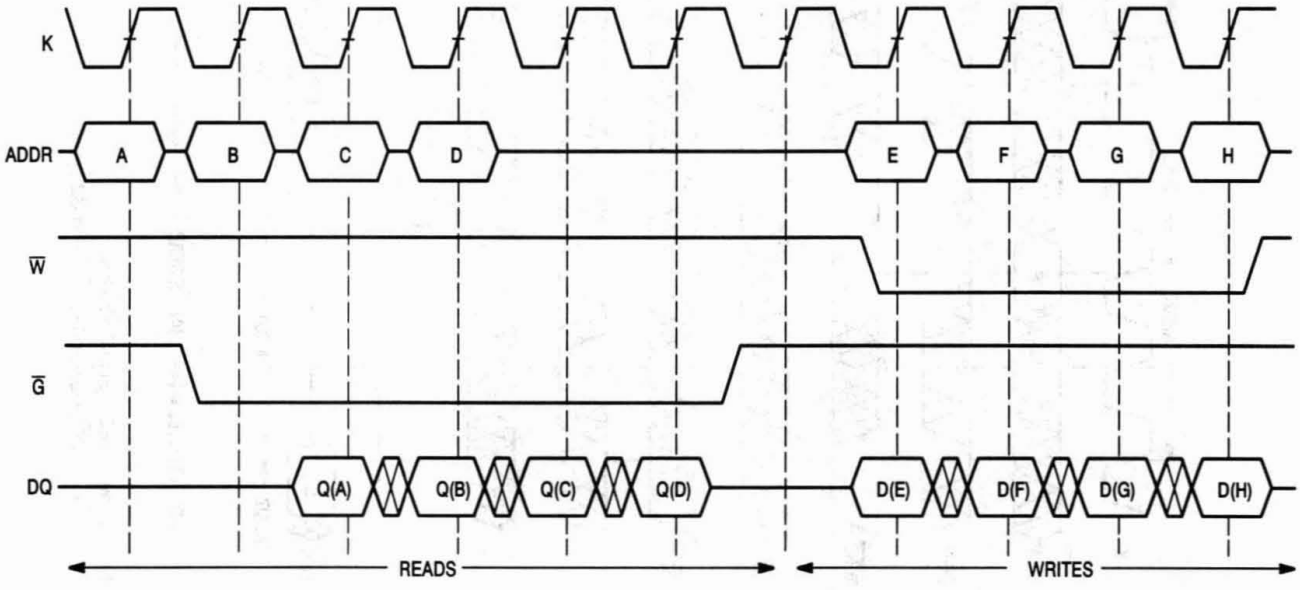
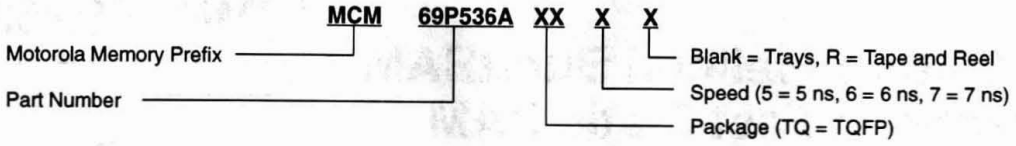


Figure 2. Configured as Non–Burst Synchronous SRAM

ORDERING INFORMATION
(Order by Full Part Number)

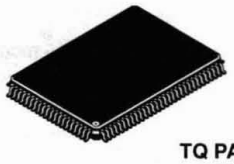


Full Part Numbers — MCM69P536ATQ5 MCM69P536ATQ6 MCM69P536ATQ7
MCM69P536ATQ5R MCM69P536ATQ6R MCM69P536ATQ7R

4

MCM69P536B

32K x 36 Bit Pipelined BurstRAM™ Synchronous Fast Static RAM



TQ PACKAGE
TQFP
CASE 983A–01

The MCM69P536B is a 1M bit synchronous fast static RAM designed to provide a burstable, high performance, secondary cache for the 68K Family, PowerPC™, 486, i960™ and Pentium™ microprocessors. It is organized as 32K words of 36 bits each. This device integrates input registers, an output register, a 2–bit address counter, and high speed SRAM onto a single monolithic circuit for reduced parts count in cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (SA), data inputs (DQx), and all control signals except output enable ($\overline{G}$) and Linear Burst Order ($\overline{LBO}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ input pins. Subsequent burst addresses can be generated internally by the MCM69P536B (burst sequence operates in linear or interleaved mode dependent upon state of $\overline{LBO}$) and controlled by the burst address advance ($\overline{ADV}$) input pin.

Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased timing flexibility for incoming signals.

Synchronous byte write ($\overline{SBx}$), synchronous global write ($\overline{SGW}$), and synchronous write enable $\overline{SW}$ are provided to allow writes to either individual bytes or to all bytes. The four bytes are designated as "a", "b", "c", and "d". $\overline{SBa}$ controls DQa, $\overline{SBb}$ controls DQb, etc. Individual bytes are written if the selected byte writes $\overline{SBx}$ are asserted with $\overline{SW}$. All bytes are written if either $\overline{SGW}$ is asserted or if all $\overline{SBx}$ and $\overline{SW}$ are asserted.

For read cycles, pipelined SRAMs output data is temporarily stored by an edge–triggered output register and then released to the output buffers at the next rising edge of clock (K).

The MCM69P536B operates from a 3.3 V power supply and all inputs and outputs are LVTTL compatible.

- MCM69P536B–4 = 4 ns access / 7.5 ns cycle
  MCM69P536B–4.5 = 4.5 ns access / 8 ns cycle
  MCM69P536B–5 = 5 ns access / 10 ns cycle
  MCM69P536B–6 = 6 ns access / 12 ns cycle
  MCM69P536B–7 = 7 ns access / 13.3 ns cycle
- Single 3.3 V + 10%, – 5% Power Supply
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Selectable Burst Sequencing Order (Linear/Interleaved)
- Internally Self–Timed Write Cycle
- Byte Write and Global Write Control
- 5 V Tolerant Data I/Os (DQx) Only
- 100 Pin TQFP Package

BurstRAM is a trademark of Motorola, Inc.
The PowerPC name is a trademark of IBM Corp., used under license therefrom.
i960 and Pentium are trademarks of Intel Corp.

REV 3
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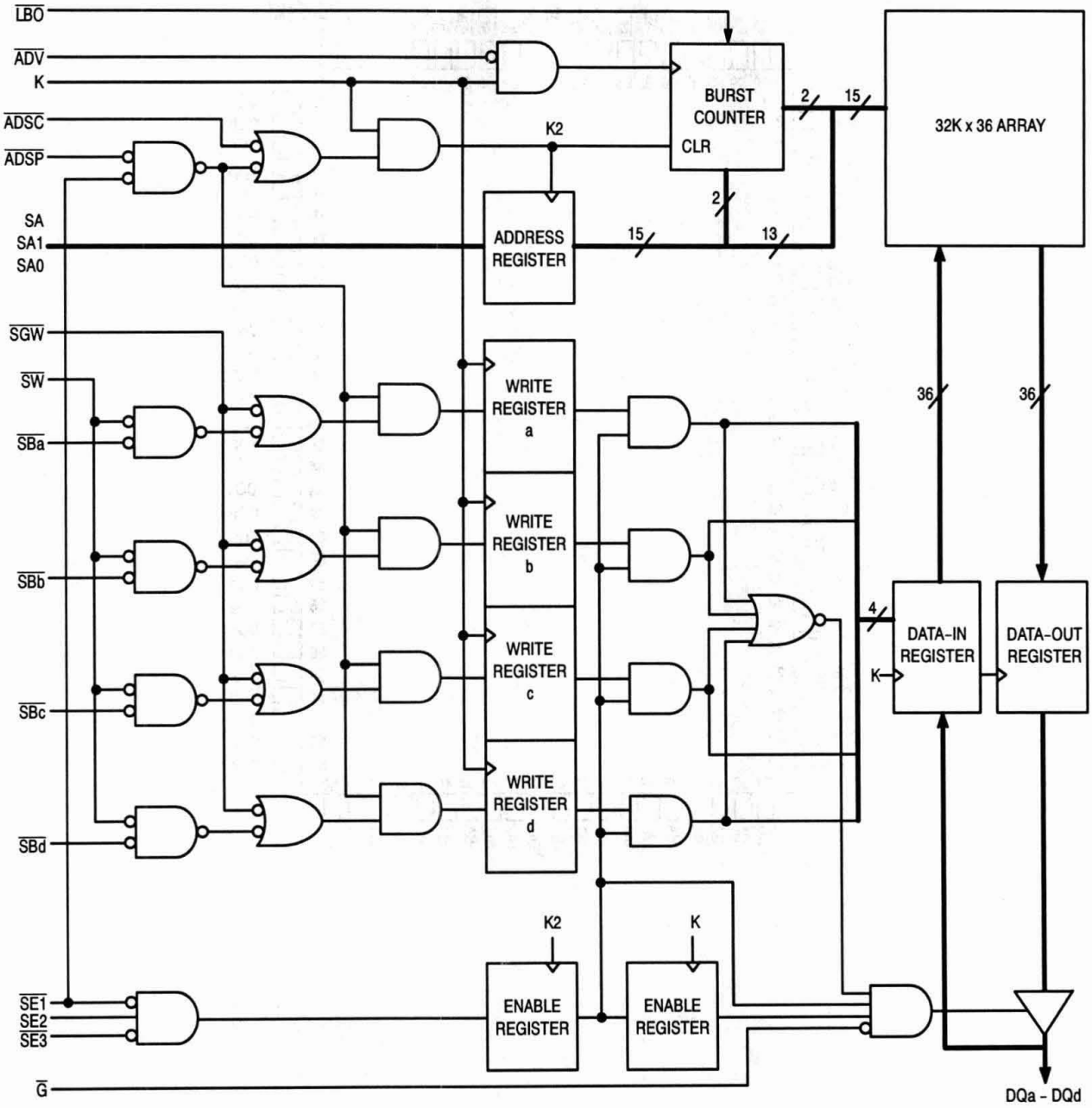
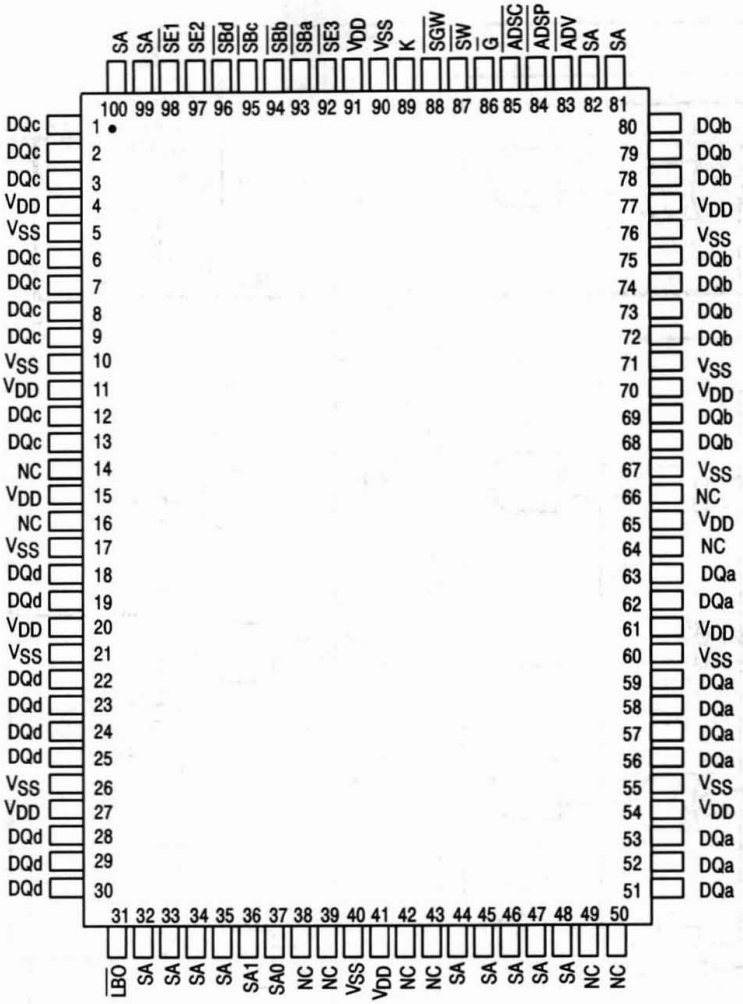
FUNCTIONAL BLOCK DIAGRAM



4

PIN ASSIGNMENT



PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: Initiates READ, WRITE or chip deselect cycle.
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: Initiates READ, WRITE or chip deselect cycle (exception — chip deselect does not occur when $\overline{ADSP}$ is asserted and $\overline{SE1}$ is high).
83	$\overline{ADV}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
(a) 51, 52, 53, 56, 57, 58, 59, 62, 63 (b) 68, 69, 72, 73, 74, 75, 78, 79, 80 (c) 1, 2, 3, 6, 7, 8, 9, 12, 13 (d) 18, 19, 22, 23, 24, 25, 28, 29, 30	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b, c, d).
86	$\overline{G}$	Input	Asynchronous Output Enable Input: Low — enables output buffers (DQx pins). High — DQx pins are high impedance.
89	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$ and $\overline{LBO}$.
31	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst counter (68K/PowerPC). High — interleaved burst counter (486/i960/Pentium).
32, 33, 34, 35, 44, 45, 46, 47, 48, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
36, 37	SA1,SA0	Input	Synchronous Address Inputs: These pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
93, 94, 95, 96 (a) (b) (c) (d)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: "x" refers to the byte being written (byte a, b, c, d). $\overline{SGW}$ overrides $\overline{SBx}$.
98	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high — blocks $\overline{ADSP}$ or deselects chip when $\overline{ADSC}$ is asserted.
97	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
92	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
88	$\overline{SGW}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the $\overline{SBx}$ and $\overline{SW}$ signals. If only byte write signals $\overline{SBx}$ are being used, tie this pin high.
87	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{SBx}$ pins. If only byte write signals $\overline{SBx}$ are being used, tie this pin low.
4, 11, 15, 20, 27, 41, 54, 61, 65, 70, 77, 91	V_{DD}	Supply	Power Supply: 3.3 V + 10%, – 5%.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground.
64	NC	Input	No Connection: There is no connection to the chip. For compatibility reasons, it is recommended that this pin be tied low for system designs that do not have a sleep mode associated with the cache/memory controller. Other vendors' RAMs may have implemented the Sleep Mode (ZZ) feature.
14, 16, 38, 39, 42, 43, 49, 50, 66	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE (See Notes 1 through 4)

Next Cycle	Address Used	$\overline{SE1}$	SE2	$\overline{SE3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{G}$ [3]	DQx	Write [2, 4]
Deselect	None	1	X	X	X	0	X	X	High–Z	X
Deselect	None	0	X	1	0	X	X	X	High–Z	X
Deselect	None	0	0	X	0	X	X	X	High–Z	X
Deselect	None	X	X	1	1	0	X	X	High–Z	X
Deselect	None	X	0	X	1	0	X	X	High–Z	X
Begin Read	External	0	1	0	0	X	X	X	High–Z	READ
Begin Read	External	0	1	0	1	0	X	X	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	1	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	0	DQ	READ
Continue Read	Next	1	X	X	X	1	0	1	High–Z	READ
Continue Read	Next	1	X	X	X	1	0	0	DQ	READ
Suspend Read	Current	X	X	X	1	1	1	1	High–Z	READ
Suspend Read	Current	X	X	X	1	1	1	0	DQ	READ
Suspend Read	Current	1	X	X	X	1	1	1	High–Z	READ
Suspend Read	Current	1	X	X	X	1	1	0	DQ	READ
Begin Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Begin Write	Current	1	X	X	X	1	1	X	High–Z	WRITE
Begin Write	External	0	1	0	1	0	X	X	High–Z	WRITE
Continue Write	Next	X	X	X	1	1	0	X	High–Z	WRITE
Continue Write	Next	1	X	X	X	1	0	X	High–Z	WRITE
Suspend Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Suspend Write	Current	1	X	X	X	1	1	X	High–Z	WRITE

NOTES: 1. X = Don't Care. 1 = logic high. 0 = logic low.
2. Write is defined as either 1) any $\overline{SBx}$ and $\overline{SW}$ low or 2) $\overline{SGW}$ is low.
3. $\overline{G}$ is an asynchronous signal and is not sampled by the clock K. $\overline{G}$ drives the bus immediately (t_{GLQX}) following $\overline{G}$ going low.
4. On write cycles that follow read cycles, $\overline{G}$ must be negated prior to the start of the write cycle to ensure proper write data setup times. $\overline{G}$ must also remain negated at the completion of the write cycle to ensure proper write data hold times.

LINEAR BURST ADDRESS TABLE ($\overline{LBO} = V_{SS}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X10	X . . . X11	X . . . X00
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X00	X . . . X01	X . . . X10

INTERLEAVED BURST ADDRESS TABLE ($\overline{LBO} = V_{DD}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00

WRITE TRUTH TABLE

Cycle Type	$\overline{SGW}$	$\overline{SW}$	$\overline{SBa}$	$\overline{SBb}$	$\overline{SBc}$	$\overline{SBd}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte a	H	L	L	H	H	H
Write Byte b	H	L	H	L	H	H
Write Byte c	H	L	H	H	L	H
Write Byte d	H	L	H	H	H	L
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{DD}	V_{in}	– 0.5 to V_{DD} + 0.5	V
	V_{in} (DQx), V_{out}(DQx)	– 0.5 to 6.0	
Output Current (per I/O)	I_{out}	± 20	mA
Package Power Dissipation (See Note 2)	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to 85	°C
Storage Temperature	T_{stg}	– 55 to 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Thermal Resistance Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	40 25	°C/W	1, 2
Thermal Resistance Junction to Board (Bottom)		$R_{\theta JB}$	17	°C/W	1, 3
Thermal Resistance Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	1, 4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

4

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.135	3.3	3.6	V
Operating Temperature	T_J	20	—	110	°C
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V
Input High Voltage (except DQx)	V_{IH}	2.0	—	V_{DD} + 0.3	V
Input High Voltage (DQx)	V_{IH} (DQx)	2.0	—	5.5**	V

*$V_{IL} \geq -2$ V for $t \leq t_{KHKH}/2$.
**$V_{IH} \leq 6$ V for $t_{KHKH}/2$.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit	Notes
Input Leakage Current (0 V ≤ V_{in} ≤ V_{DD}) (Excluding $\overline{LBO}$)		$I_{lkg(I)}$	—	± 1	µA	
Output Leakage Current (0 V ≤ V_{in} ≤ V_{DD})		$I_{lkg(O)}$	—	± 1	µA	
AC Supply Current (Device Selected, All Outputs Open, Cycle Time ≥ t_{KHKH} min)	MCM69P536B–4 (133 MHz) MCM69P536B–4.5 (125 MHz) MCM69P536B–5 (100 MHz) MCM69P536B–6 (83 MHz) MCM69P536B–7 (75 MHz)	I_{DDA}	—	TBD TBD 380 360 350	mA	2, 3, 4
CMOS Standby Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}, All Inputs Toggling at CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{DD} – 0.2 V)	MCM69P536B–4 (133 MHz) MCM69P536B–4.5 (125 MHz) MCM69P536B–5 (100 MHz) MCM69P536B–6 (83 MHz) MCM69P536B–7 (75 MHz)	I_{SB1}	—	TBD TBD 150 140 130	mA	1
Clock Running Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}, All Other Inputs Held to Static CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{DD} – 0.2 V)	MCM69P536B–4 (133 MHz) MCM69P536B–4.5 (125 MHz) MCM69P536B–5 (100 MHz) MCM69P536B–6 (83 MHz) MCM69P536B–7 (75 MHz)	I_{SB2}	—	TBD TBD 55 50 45	mA	1
Output Low Voltage (I_{OL} = 8 mA)		V_{OL}	—	0.4	V	
Output High Voltage (I_{OH} = – 4 mA)		V_{OH}	2.4	—	V	

NOTES:
1. Device in deselected mode as defined by the Truth Table.
2. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V)
3. All addresses transition simultaneously low (LSB) and then high (HSB).
4. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_J = 20 to 110°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	4	6	pF
Input/Output Capacitance	$C_{I/O}$	—	7	9	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1 Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	69P536B–4		69P536B–4.5		69P536B–5		69P536B–6		69P536B–7		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	7.5	—	8	—	10	—	12	—	13.3	—	ns	6
Clock High Pulse Width	t_{KHKL}	3	—	3	—	3	—	4	—	4.5	—	ns	
Clock Low Pulse Width	t_{KLKH}	3	—	3	—	3	—	4	—	4.5	—	ns	
Clock Access Time	t_{KHQV}	—	4	—	4.5	—	5	—	6	—	7	ns	4
Output Enable to Output Valid	t_{GLQV}	—	4	—	4.5	—	5	—	5	—	6	ns	4
Clock High to Output Active	t_{KHQX1}	1.5	—	1.5	—	0	—	0	—	0	—	ns	4, 6
Clock High to Output Change	t_{KHQX2}	1.5	—	1.5	—	2	—	2	—	2	—	ns	4, 6
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	0	—	ns	4, 6
Output Disable to Q High–Z	t_{GHQZ}	—	4	—	4.5	—	5	—	5	—	5	ns	5, 6
Clock High to Q High–Z	t_{KHQZ}	2	4	2	4.5	2	5	2	5	2	5	ns	5, 6
Setup Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	t_{ADKH} t_{ADSKH} t_{DVKH} t_{WVKH} t_{EVKH}	2	—	2.5	—	2.5	—	2.5	—	2.5	—	ns	
Hold Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	t_{KHAX} t_{KHADSX} t_{KHDX} t_{KHWX} t_{KHEX}	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns	

NOTES:
1. Write is defined as either any $\overline{SBx}$ and $\overline{SW}$ low or $\overline{SGW}$ is low. Chip Enable is defined as $\overline{SE1}$ low, SE2 high and $\overline{SE3}$ low whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care after write cycle begins. To prevent bus contention, $\overline{G}$ should be negated prior to start of write cycle.
4. Tested per AC Test Load (See Figure 1).
5. Measured at ± 200 mV from steady state.
6. This parameter is sampled and not 100% tested.

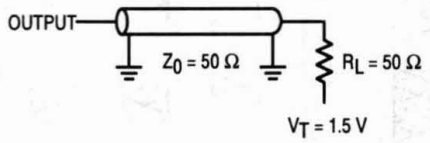
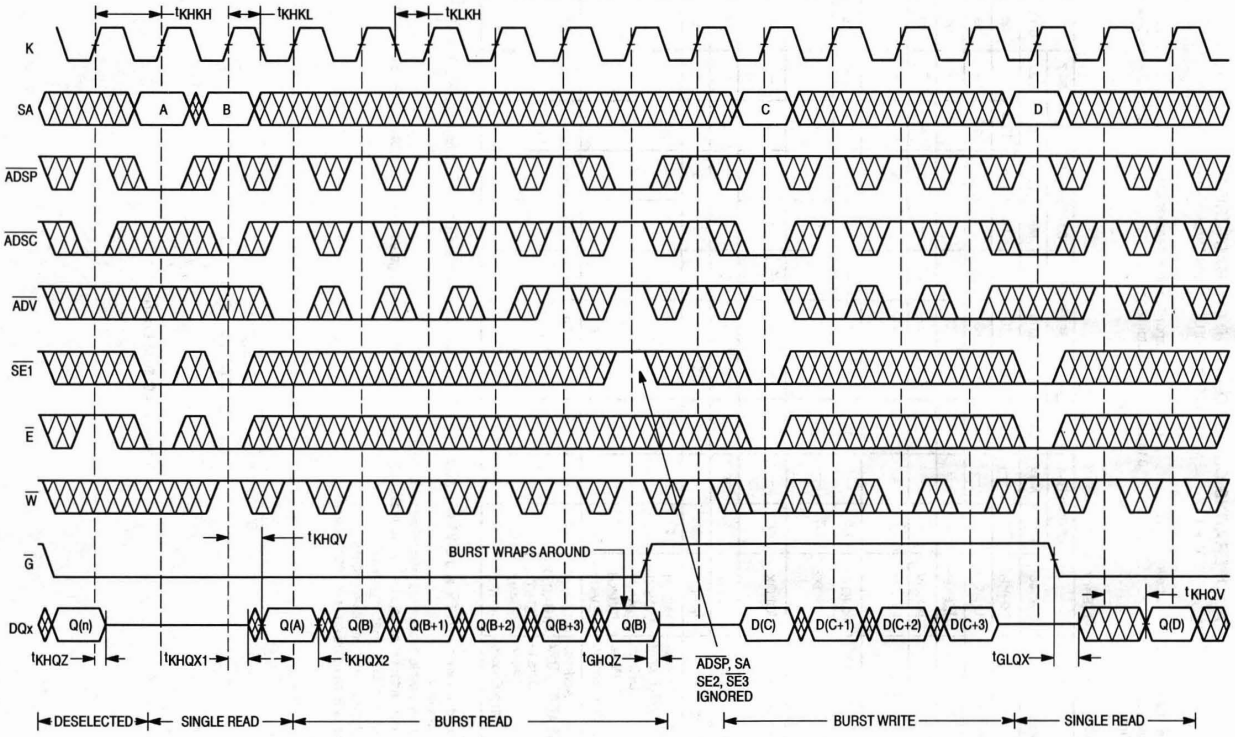


Figure 1. AC Test Loads

READ/WRITE CYCLES



Note: $\overline{E}$ low = SE2 high and $\overline{SE3}$ low.
$\overline{W}$ low = $\overline{SGW}$ low and / or $\overline{SW}$ and $\overline{SBx}$ low.

APPLICATION INFORMATION

The MCM69P536B BurstRAM is a high speed synchronous SRAM that is intended for use primarily in secondary or level two (L2) cache memory applications. L2 caches are found in a variety of classes of computers – from the desktop personal computer to the high–end servers and transaction processing machines. For simplicity, the majority of L2 caches today are direct mapped and are single bank implementations. These caches tend to be designed for bus speeds in the range of 33 to 66 MHz. At these bus rates, non–pipelined (flow–through) BurstRAMs can be used since their access times meet the speed requirements for a minimum–latency, zero–wait state L2 cache interface. Latency is a measure (time) of "dead" time the memory system exhibits as a result of a memory request.

For those applications that demand bus operation at greater than 66 MHz or multi–bank L2 caches at 66 MHz, the pipelined (register/register) version of the 32Kx36 BurstRAM (MCM69P536B) allows the designer to maintain zero–wait state operation. Multiple banks of BurstRAMs create additional bus loading and can cause the system to otherwise miss its timing requirements. The access time (clock–to–valid–data) of a pipelined BurstRAM is inherently faster than a non–pipelined device by a few nanoseconds. This does not come without cost. The cost is latency – "dead" time.

Since most L2 caches are tied to the processor bus and bus speeds continue to increase over time, pipelined (R/R) BurstRAMs are the best choice in achieving zero–wait state L2 cache performance. At bus speeds ranging from 66 MHz to 100 MHz, pipelined BurstRAMs are able to provide fast clock to valid data times required of these high speed buses.

FUNCTIONAL EQUIVALENT

The following describes the configuration of the MCM69P536B as a functional equivalent to a 5 V BurstRAM. A migration from 5 V BurstRAMs to 3.3 V BurstRAMs (e.g. MCM69P536B) can be somewhat confusing due to functional and pinout differences. Because the 3.3 V devices offer more pins than the 5 V PLCC devices, it is no longer necessary to supply multiple part numbers for the different burst, address pipeline support ("H" part), etc. options. A single MCM69P536B device can replace two of the 5 V 32K x 18 devices. The MCM69P536B can be configured to function as if it were one of the 5 V BurstRAMs. Below is a table that lists control pins on the MCM69P536B that can be tied off to either 3.3 V or ground in order to satisfy the migration to this 3.3 V RAM.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

5 V Device Numbers	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
MCM67C518	—	—	—	L	H
MCM67J518	—	—	—	—	H
MCM67N518	—	—	—	L	L

NOTE: If no tie value is given, then the pin should be used as intended on the 5 V device.

NON–BURST SYNCHRONOUS OPERATION

Although this BurstRAM has been designed for 68K–, PowerPC–, 486–, i960, and Pentium – based systems, these SRAMs can be used in other high speed L2 cache or memory applications that do not require the burst address feature. Most L2 caches designed with a synchronous interface can make use of the MCM69P536B. The burst counter feature of the BurstRAM can be disabled, and the SRAM can be configured to act upon a continuous stream of addresses. See Figure 2.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

Non–Burst	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
Sync Non–Burst, Pipelined SRAM	H	L	H	L	X

NOTE: Although X is specified in the table as a don't care, the pin must be tied either high or low.

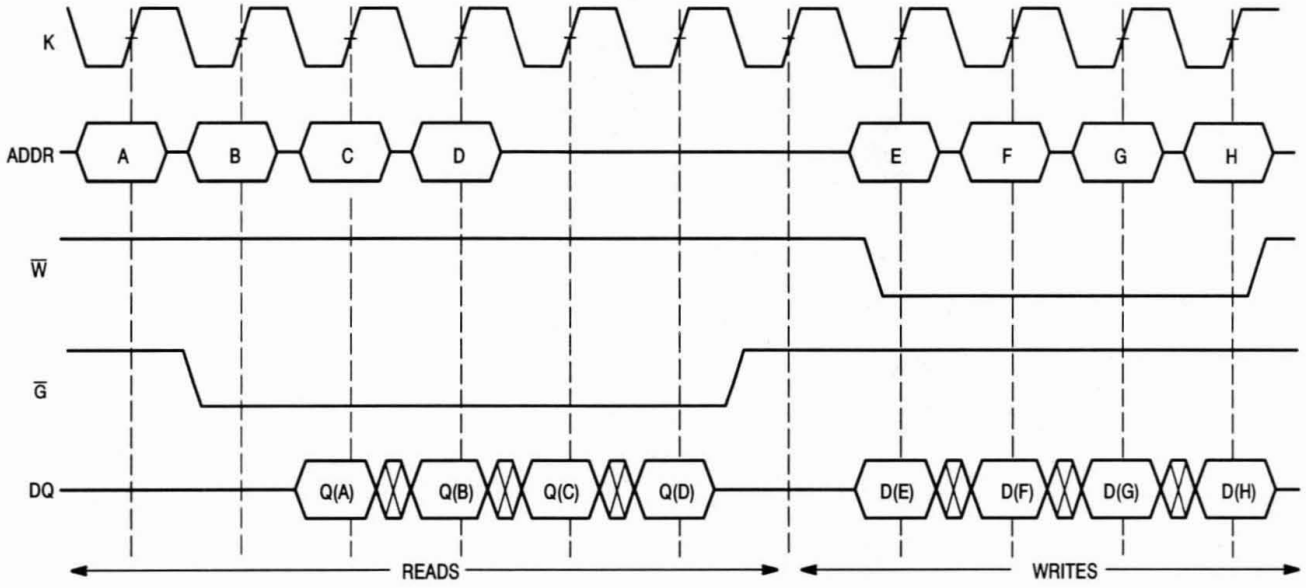
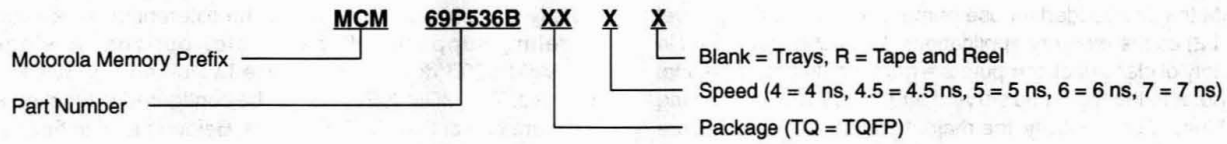


Figure 2. Configured as Non–Burst Synchronous SRAM

ORDERING INFORMATION
(Order by Full Part Number)


MCM 69P536B XX X X
Motorola Memory Prefix
Part Number
Blank = Trays, R = Tape and Reel
Speed (4 = 4 ns, 4.5 = 4.5 ns, 5 = 5 ns, 6 = 6 ns, 7 = 7 ns)
Package (TQ = TQFP)

Full Part Numbers — MCM69P536BTQ4 MCM69P536BTQ4.5 MCM69P536BTQ5 MCM69P536BTQ6 MCM69P536BTQ7
MCM69P536BTQ4R MCM69P536BTQ4.5R MCM69P536BTQ5R MCM69P536BTQ6R MCM69P536BTQ7R

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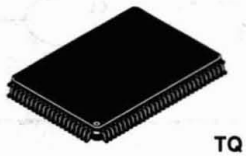
MCM69P536C

32K x 36 Bit Pipelined BurstRAM™ Synchronous Fast Static RAM



TQ PACKAGE
TQFP
CASE 983A–01

The MCM69P536C is a 1M bit synchronous fast static RAM designed to provide a burstable, high performance, secondary cache for the 68K Family, PowerPC™, 486, i960™, and Pentium™ microprocessors. It is organized as 32K words of 36 bits each. This device integrates input registers, an output register, a 2–bit address counter, and high speed SRAM onto a single monolithic circuit for reduced parts count in cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (SA), data inputs (DQx), and all control signals except output enable ($\overline{G}$) and Linear Burst Order ($\overline{LBO}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ input pins. Subsequent burst addresses can be generated internally by the MCM69P536C (burst sequence operates in linear or interleaved mode dependent upon state of $\overline{LBO}$) and controlled by the burst address advance ($\overline{ADV}$) input pin.

Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased timing flexibility for incoming signals.

Synchronous byte write ($\overline{SBx}$), synchronous global write ($\overline{SGW}$), and synchronous write enable $\overline{SW}$ are provided to allow writes to either individual bytes or to all bytes. The four bytes are designated as "a", "b", "c", and "d". $\overline{SBa}$ controls DQa, $\overline{SBb}$ controls DQb, etc. Individual bytes are written if the selected byte writes $\overline{SBx}$ are asserted with $\overline{SW}$. All bytes are written if either $\overline{SGW}$ is asserted or if all $\overline{SBx}$ and $\overline{SW}$ are asserted.

For read cycles, pipelined SRAMs output data is temporarily stored by an edge–triggered output register and then released to the output buffers at the next rising edge of clock (K).

The MCM69P536C operates from a 3.3 V power supply and all inputs and outputs are LVTTL compatible.

- MCM69P536C–4 = 4 ns Access / 7.5 ns Cycle
  MCM69P536C–4.5 = 4.5 ns Access / 8 ns Cycle
  MCM69P536C–5 = 5 ns Access / 10 ns Cycle
  MCM69P536C–6 = 6 ns Access / 12 ns Cycle
  MCM69P536C–7 = 7 ns Access / 13.3 ns Cycle
- Single 3.3 V + 10%, – 5% Power Supply
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Selectable Burst Sequencing Order (Linear/Interleaved)
- Internally Self–Timed Write Cycle
- Byte Write and Global Write Control
- 5 V Tolerant on all Pins (Inputs and I/Os)
- 100 Pin TQFP Package

BurstRAM is a trademark of Motorola, Inc.
The PowerPC name is a trademark of IBM Corp., used under license therefrom.
i960 and Pentium are trademarks of Intel Corp.

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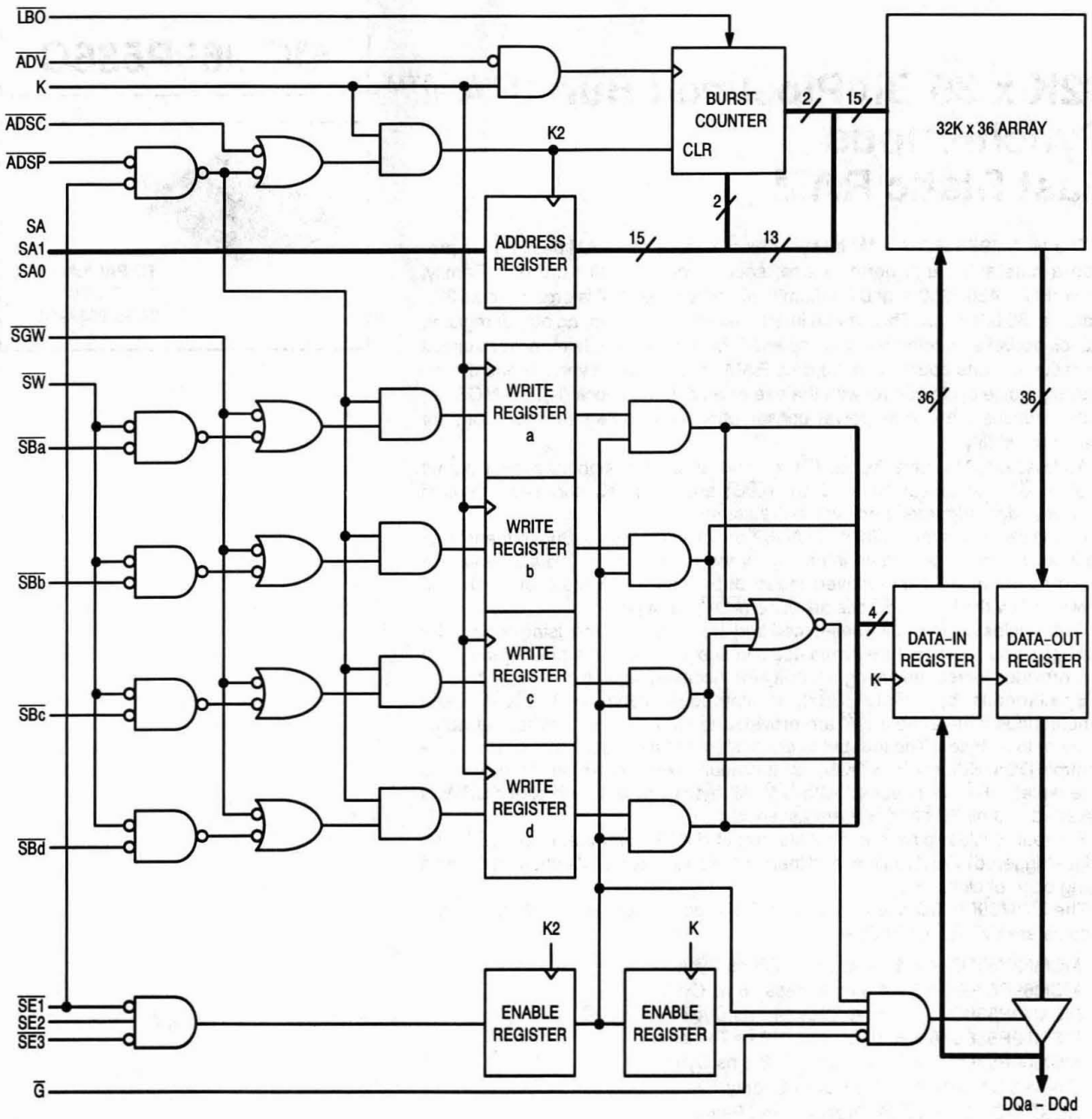
FUNCTIONAL BLOCK DIAGRAM



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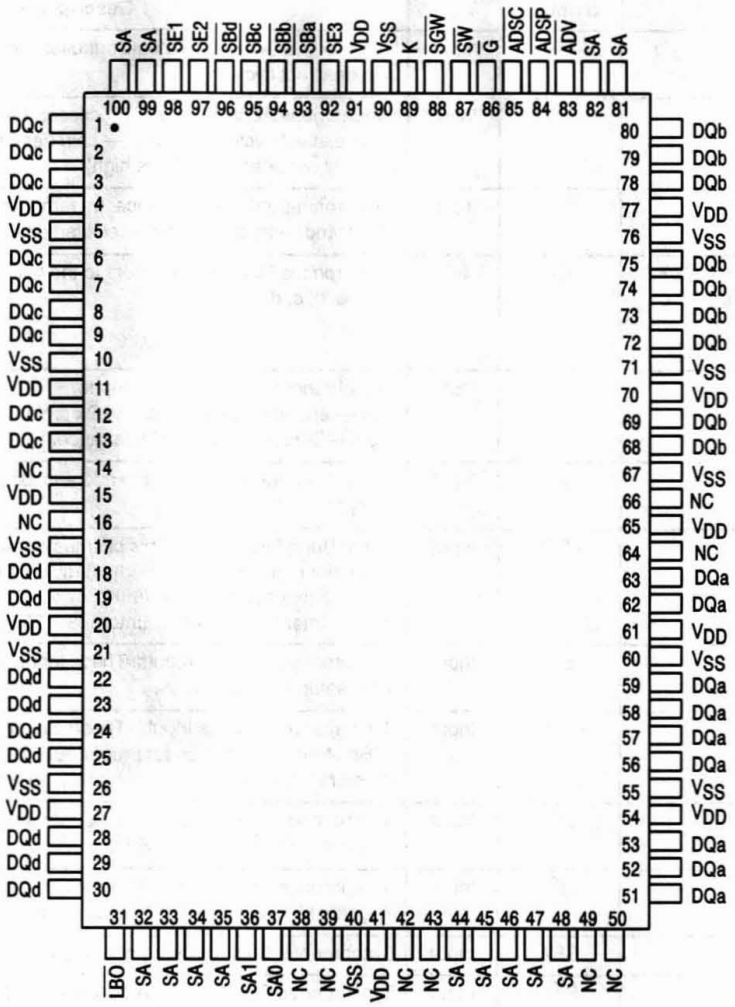
PIN ASSIGNMENT



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PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: Initiates READ, WRITE, or chip deselect cycle.
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: Initiates READ, WRITE, or chip deselect cycle (exception — chip deselect does not occur when $\overline{ADSP}$ is asserted and $\overline{SE1}$ is high).
83	$\overline{ADV}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
(a) 51, 52, 53, 56, 57, 58, 59, 62, 63 (b) 68, 69, 72, 73, 74, 75, 78, 79, 80 (c) 1, 2, 3, 6, 7, 8, 9, 12, 13 (d) 18, 19, 22, 23, 24, 25, 28, 29, 30	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b, c, d).
86	$\overline{G}$	Input	Asynchronous Output Enable Input: Low — enables output buffers (DQx pins). High — DQx pins are high impedance.
89	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$ and $\overline{LBO}$.
31	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst counter (68K/PowerPC). High — interleaved burst counter (486/i960/Pentium).
32, 33, 34, 35, 44, 45, 46, 47, 48, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
36, 37	SA1,SA0	Input	Synchronous Address Inputs: These pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
93, 94, 95, 96 (a) (b) (c) (d)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: "x" refers to the byte being written (byte a, b, c, d). $\overline{SGW}$ overrides $\overline{SBx}$.
98	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high–blocks $\overline{ADSP}$ or deselects chip when $\overline{ADSC}$ is asserted.
97	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
92	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
88	$\overline{SGW}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the $\overline{SBx}$ and $\overline{SW}$ signals. If only byte write signals $\overline{SBx}$ are being used, tie this pin high.
87	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{SBx}$ pins. If only byte write signals $\overline{SBx}$ are being used, tie this pin low.
4, 11, 15, 20, 27, 41, 54, 61, 65, 70, 77, 91	V_{DD}	Supply	Power Supply: 3.3 V + 10%, – 5%.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground.
64	NC	Input	No Connection: There is no connection to the chip. For compatibility reasons, it is recommended that this pin be tied low for system designs that do not have a sleep mode associated with the cache/memory controller. Other vendors' RAMs may have implemented the Sleep Mode (ZZ) feature.
14, 16, 38, 39, 42, 43, 49, 50, 66	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE (See Notes 1 through 4)

Next Cycle	Address Used	$\overline{SE1}$	SE2	$\overline{SE3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{G}$ [3]	DQx	Write [2, 4]
Deselect	None	1	X	X	X	0	X	X	High–Z	X
Deselect	None	0	X	1	0	X	X	X	High–Z	X
Deselect	None	0	0	X	0	X	X	X	High–Z	X
Deselect	None	X	X	1	1	0	X	X	High–Z	X
Deselect	None	X	0	X	1	0	X	X	High–Z	X
Begin Read	External	0	1	0	0	X	X	X	High–Z	READ
Begin Read	External	0	1	0	1	0	X	X	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	1	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	0	DQ	READ
Continue Read	Next	1	X	X	X	1	0	1	High–Z	READ
Continue Read	Next	1	X	X	X	1	0	0	DQ	READ
Suspend Read	Current	X	X	X	1	1	1	1	High–Z	READ
Suspend Read	Current	X	X	X	1	1	1	0	DQ	READ
Suspend Read	Current	1	X	X	X	1	1	1	High–Z	READ
Suspend Read	Current	1	X	X	X	1	1	0	DQ	READ
Begin Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Begin Write	Current	1	X	X	X	1	1	X	High–Z	WRITE
Begin Write	External	0	1	0	1	0	X	X	High–Z	WRITE
Continue Write	Next	X	X	X	1	1	0	X	High–Z	WRITE
Continue Write	Next	1	X	X	X	1	0	X	High–Z	WRITE
Suspend Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Suspend Write	Current	1	X	X	X	1	1	X	High–Z	WRITE

NOTES: 1. X = Don't Care. 1 = logic high. 0 = logic low.
2. Write is defined as either 1) any $\overline{SBx}$ and $\overline{SW}$ low or 2) $\overline{SGW}$ is low.
3. $\overline{G}$ is an asynchronous signal and is not sampled by the clock K. $\overline{G}$ drives the bus immediately (t_{GLQX}) following $\overline{G}$ going low.
4. On write cycles that follow read cycles, $\overline{G}$ must be negated prior to the start of the write cycle to ensure proper write data setup times. $\overline{G}$ must also remain negated at the completion of the write cycle to ensure proper write data hold times.

LINEAR BURST ADDRESS TABLE ($\overline{LBO} = V_{SS}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X10	X . . . X11	X . . . X00
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X00	X . . . X01	X . . . X10

INTERLEAVED BURST ADDRESS TABLE ($\overline{LBO} = V_{DD}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00

WRITE TRUTH TABLE

Cycle Type	$\overline{SGW}$	$\overline{SW}$	$\overline{SBa}$	$\overline{SBb}$	$\overline{SBc}$	$\overline{SBd}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte a	H	L	L	H	H	H
Write Byte b	H	L	H	L	H	H
Write Byte c	H	L	H	H	L	H
Write Byte d	H	L	H	H	H	L
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

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ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{DD}	V_{in}, V_{out}	– 0.5 to 6.0	V
Output Current (per I/O)	I_{out}	± 20	mA
Package Power Dissipation (See Note 2)	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to 85	°C
Storage Temperature	T_{stg}	– 55 to 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Thermal Resistance Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	40 25	°C/W	1, 2
Thermal Resistance Junction to Board (Bottom)		$R_{\theta JB}$	17	°C/W	1, 3
Thermal Resistance Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	1, 4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.135	3.3	3.6	V
Operating Temperature	T_J	20	—	110	°C
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	5.5**	V

* $V_{IL} \geq -2$ V for $t \leq t_{KHKH}/2$.
** $V_{IH} \leq 6$ V for $t_{KHKH}/2$.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit	Notes
Input Leakage Current (0 V ≤ V_{in} ≤ V_{DD}) (Excluding $\overline{LBO}$)		$I_{lkg(I)}$	—	± 1	µA	
Output Leakage Current (0 V ≤ V_{in} ≤ V_{DD})		$I_{lkg(O)}$	—	± 1	µA	
AC Supply Current (Device Selected, All Outputs Open, Cycle Time ≥ t_{KHKH} min)	MCM69P536C–4 (133 MHz) MCM69P536C–4.5 (125 MHz) MCM69P536C–5 (100 MHz) MCM69P536C–6 (83 MHz) MCM69P536C–7 (75 MHz)	I_{DDA}	—	TBD TBD 380 360 350	mA	2, 3, 4
CMOS Standby Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}, All Inputs Toggling at CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{DD} – 0.2 V)	MCM69P536C–4 (133 MHz) MCM69P536C–4.5 (125 MHz) MCM69P536C–5 (100 MHz) MCM69P536C–6 (83 MHz) MCM69P536C–7 (75 MHz)	I_{SB1}	—	TBD TBD 150 140 130	mA	1
Clock Running Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}, All Other Inputs Held to Static CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{DD} – 0.2 V)	MCM69P536C–4 (133 MHz) MCM69P536C–4.5 (125 MHz) MCM69P536C–5 (100 MHz) MCM69P536C–6 (83 MHz) MCM69P536C–7 (75 MHz)	I_{SB2}	—	TBD TBD 55 50 45	mA	1
Output Low Voltage (I_{OL} = 8 mA)		V_{OL}	—	0.4	V	
Output High Voltage (I_{OH} = – 4 mA)		V_{OH}	2.4	—	V	

NOTES:
1. Device in deselected mode as defined by the Truth Table.
2. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
3. All addresses transition simultaneously low (LSB) and then high (HSB).
4. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_J = 20 to 110°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	4	6	pF
Input/Output Capacitance	$C_{I/O}$	—	7	9	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1 Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	69P536C–4		69P536C–4.5		69P536C–5		69P536C–6		69P536C–7		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	7.5	—	8	—	10	—	12	—	13.3	—	ns	6
Clock High Pulse Width	t_{KHKL}	3	—	3	—	3	—	4	—	4.5	—	ns	
Clock Low Pulse Width	t_{KLKH}	3	—	3	—	3	—	4	—	4.5	—	ns	
Clock Access Time	t_{KHQV}	—	4	—	4.5	—	5	—	6	—	7	ns	4
Output Enable to Output Valid	t_{GLQV}	—	4	—	4.5	—	5	—	5	—	6	ns	4
Clock High to Output Active	t_{KHQX1}	1.5	—	1.5	—	0	—	0	—	0	—	ns	4, 6
Clock High to Output Change	t_{KHQX2}	1.5	—	1.5	—	2	—	2	—	2	—	ns	4, 6
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	0	—	ns	4, 6
Output Disable to Q High–Z	t_{GHQZ}	—	4	—	4.5	—	5	—	5	—	5	ns	5, 6
Clock High to Q High–Z	t_{KHQZ}	2	4	2	4.5	2	5	2	5	2	5	ns	5, 6
Setup Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	t_{ADKH} t_{ADSKH} t_{DVKH} t_{WVKH} t_{EVKH}	2	—	2.5	—	2.5	—	2.5	—	2.5	—	ns	
Hold Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	t_{KHAX} t_{KHADSX} t_{KHDX} t_{KHWX} t_{KHEX}	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns	

NOTES:
1. Write is defined as either any $\overline{SBx}$ and $\overline{SW}$ low or $\overline{SGW}$ is low. Chip Enable is defined as $\overline{SE1}$ low, SE2 high and $\overline{SE3}$ low whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care after write cycle begins. To prevent bus contention, $\overline{G}$ should be negated prior to start of write cycle.
4. Tested per AC Test Load (See Figure 1).
5. Measured at ± 200 mV from steady state.
6. This parameter is sampled and not 100% tested.

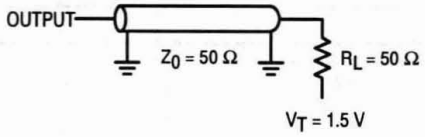
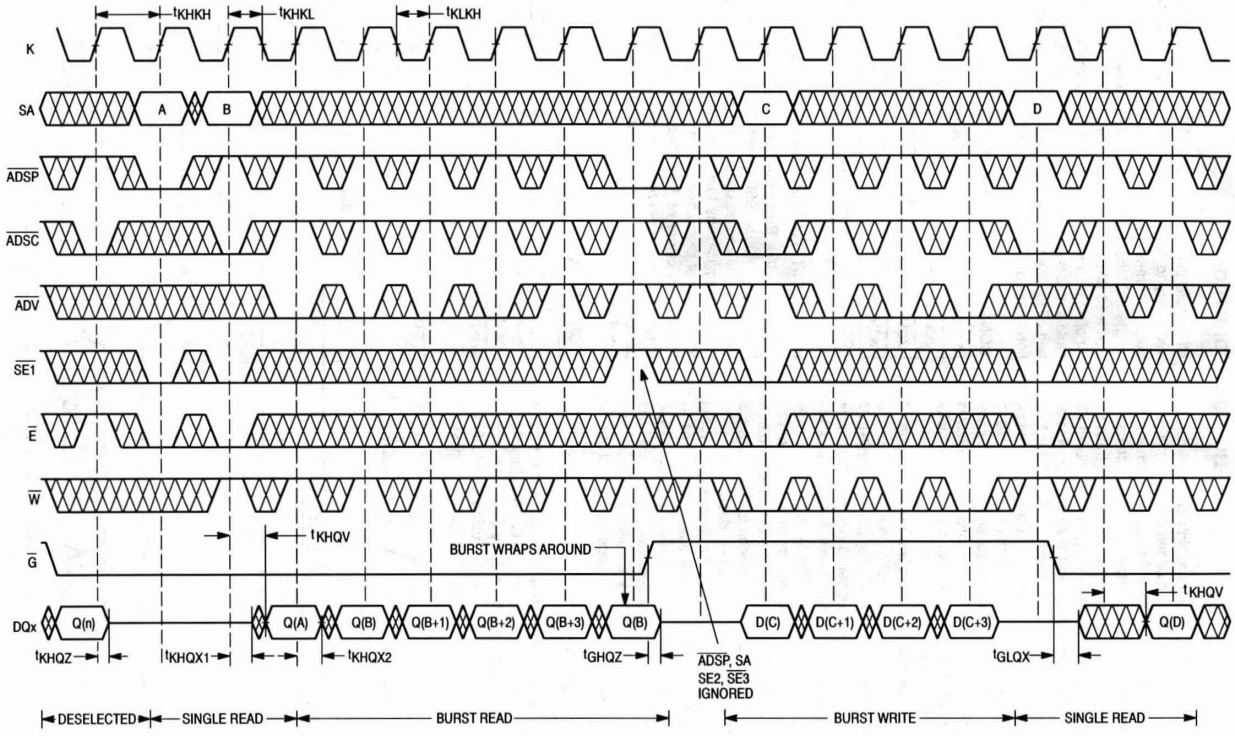


Figure 1. AC Test Loads

READ/WRITE CYCLES



NOTE: $\overline{E}$ low = SE2 high and $\overline{SE3}$ low.
$\overline{W}$ low = $\overline{SGW}$ low and / or $\overline{SW}$ and $\overline{SBx}$ low.

APPLICATION INFORMATION

The MCM69P536C BurstRAM is a high speed synchronous SRAM that is intended for use primarily in secondary or level two (L2) cache memory applications. L2 caches are found in a variety of classes of computers — from the desktop personal computer to the high–end servers and transaction processing machines. For simplicity, the majority of L2 caches today are direct mapped and are single bank implementations. These caches tend to be designed for bus speeds in the range of 33 to 66 MHz. At these bus rates, non–pipelined (flow–through) BurstRAMs can be used since their access times meet the speed requirements for a minimum–latency, zero–wait state L2 cache interface. Latency is a measure (time) of "dead" time the memory system exhibits as a result of a memory request.

For those applications that demand bus operation at greater than 66 MHz or multi–bank L2 caches at 66 MHz, the pipelined (register/register) version of the 32Kx36 BurstRAM (MCM69P536C) allows the designer to maintain zero–wait state operation. Multiple banks of BurstRAMs create additional bus loading and can cause the system to otherwise miss its timing requirements. The access time (clock–to–valid–data) of a pipelined BurstRAM is inherently faster than a non–pipelined device by a few nanoseconds. This does not come without cost. The cost is latency — "dead" time.

Since most L2 caches are tied to the processor bus and bus speeds continue to increase over time, pipelined (R/R) BurstRAMs are the best choice in achieving zero–wait state L2 cache performance. At bus speeds ranging from 66 MHz to 100 MHz, pipelined BurstRAMs are able to provide fast clock to valid data times required of these high speed buses.

FUNCTIONAL EQUIVALENT

The following describes the configuration of the MCM69P536C as a functional equivalent to a 5 V BurstRAM. A migration from 5 V BurstRAMs to 3.3 V BurstRAMs (e.g., MCM69P536C) can be somewhat confusing due to functional and pinout differences. Because the 3.3 V devices offer more pins than the 5 V PLCC devices, it is no longer necessary to supply multiple part numbers for the different burst, address pipeline support ("H" part), etc. options. A single MCM69P536C device can replace two of the 5 V 32K x 18 devices. The MCM69P536C can be configured to function as if it were one of the 5 V BurstRAMs. Below is a table that lists control pins on the MCM69P536C that can be tied off to either 3.3 V or ground in order to satisfy the migration to this 3.3 V RAM.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

5 V Device Numbers	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
MCM67C518	—	—	—	L	H
MCM67J518	—	—	—	—	H
MCM67N518	—	—	—	L	L

NOTE: If no tie value is given, then the pin should be used as intended on the 5 V device.

NON–BURST SYNCHRONOUS OPERATION

Although this BurstRAM has been designed for 68K–, PowerPC–, 486–, i960–, and Pentium–based systems, these SRAMs can be used in other high speed L2 cache or memory applications that do not require the burst address feature. Most L2 caches designed with a synchronous interface can make use of the MCM69P536C. The burst counter feature of the BurstRAM can be disabled, and the SRAM can be configured to act upon a continuous stream of addresses. See Figure 2.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

Non–Burst	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
Sync Non–Burst, Pipelined SRAM	H	L	H	L	X

NOTE: Although X is specified in the table as a don't care, the pin must be tied either high or low.

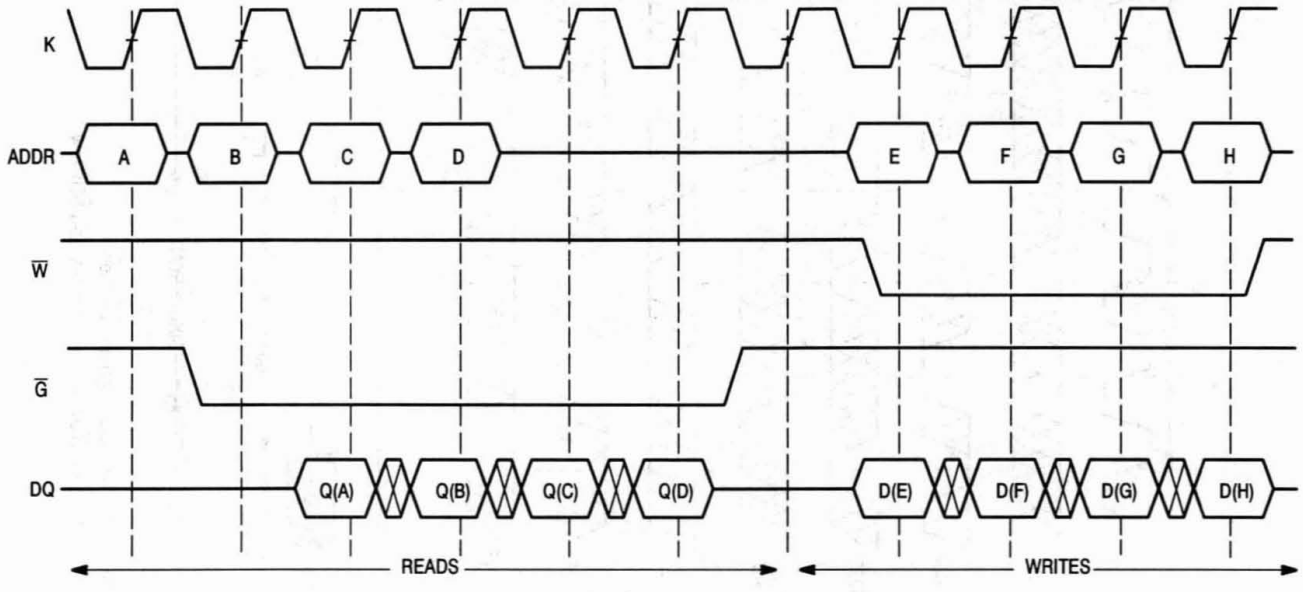
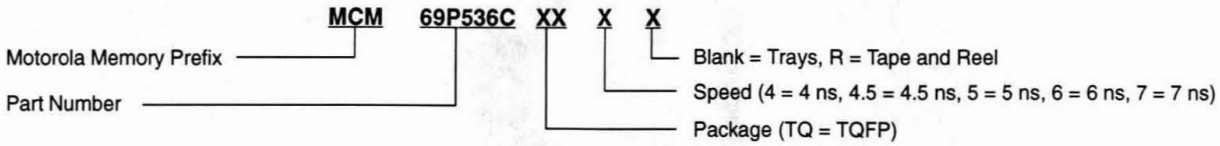


Figure 2. Configured as Non–Burst Synchronous SRAM

ORDERING INFORMATION
(Order by Full Part Number)


MCM 69P536C XX X X
Motorola Memory Prefix
Part Number
Blank = Trays, R = Tape and Reel
Speed (4 = 4 ns, 4.5 = 4.5 ns, 5 = 5 ns, 6 = 6 ns, 7 = 7 ns)
Package (TQ = TQFP)

Full Part Numbers — MCM69P536CTQ4 MCM69P536CTQ4.5 MCM69P536CTQ5 MCM69P536CTQ6 MCM69P536CTQ7
MCM69P536CTQ4R MCM69P536CTQ4.5R MCM69P536CTQ5R MCM69P536CTQ6R MCM69P536CTQ7R

4

4

Synchronous Fast SRAMs

5

Tag RAMs

MCM69T618 .... 64K x 18 .... 3.3 V 5–3
MPC27T416 .... 16K x 16 .... 5 V 5–12
MPC27T415 .... 16K x 15 .... 5 V 5–27

CAMs

MCM69C432 .... 16 x 64 ..... 3.3 V ... 5–42
MCM69C232 .... 4K x 64 ..... 3.3 V ... 5–61

Integrated Cache Solutions

MPC2605 ..... 32K x 72 .... 3.3 V ... 5–80
MPC2604GA .... 32K x 36 .... 3.3 V . 5–109

Separate and Dual I/O Devices

MCM69Q909 .... 512K x 9 .... 5 V ... 5–137
MCM69Q709 .... 128K x 9 .... 5 V ... 5–147
MCM69Q709A .. 128K x 9 .... 5V ... 5–157
MCM69Q536 .... 32K x 36 .... 3.3 V . 5–167
MCM69D536 .... 32K x 36 .... 3.3 V . 5–177
MCM69Q618 .... 64K x 18 .... 3.3 V . 5–190
MCM69D618 .... 64K x 18 .... 3.3 V . 5–200
MCM62990A .... 16K x 16 .... 5 V ... 5–213

Line Buffer

MCM62X308 .... 8K x 8 ..... 5 V ... 5–220

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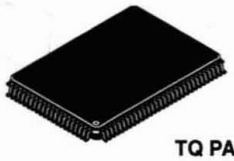
MCM69T618

64K x 18 Bit Synchronous Pipelined Cache Tag RAM

ZP PACKAGE
PBGA
CASE 999–01



TQ PACKAGE
TQFP
CASE 983A–01

The MCM69T618 is a 1M bit synchronous fast static RAM with integrated tag compare function. It is designed to address tag RAM for 512KB, 1MB, or 2MB secondary cache as well as to be used as a data RAM for 512KB caches. This device is organized as 64K words of 18 bits each. It integrates input registers, output registers, tag comparators, and high speed SRAM onto a single monolithic circuit for reduced parts count in cache tag RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (SA), data inputs (DQ), write enable ($\overline{SW}$) and chip enable (SE0 and $\overline{SE1}$) are all controlled through positive–edge–triggered noninverting registers. Data enable ($\overline{DE}$) is sampled on the rising clock edge while output enable ($\overline{G}$) and match output enable ($\overline{MG}$) are asynchronous.

Write cycles are internally self–timed and initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased timing flexibility for incoming signals.

For read cycles, pipelined SRAM output data is temporarily stored by an edge–triggered output register and then released to the output buffers at the next rising edge of clock (K).

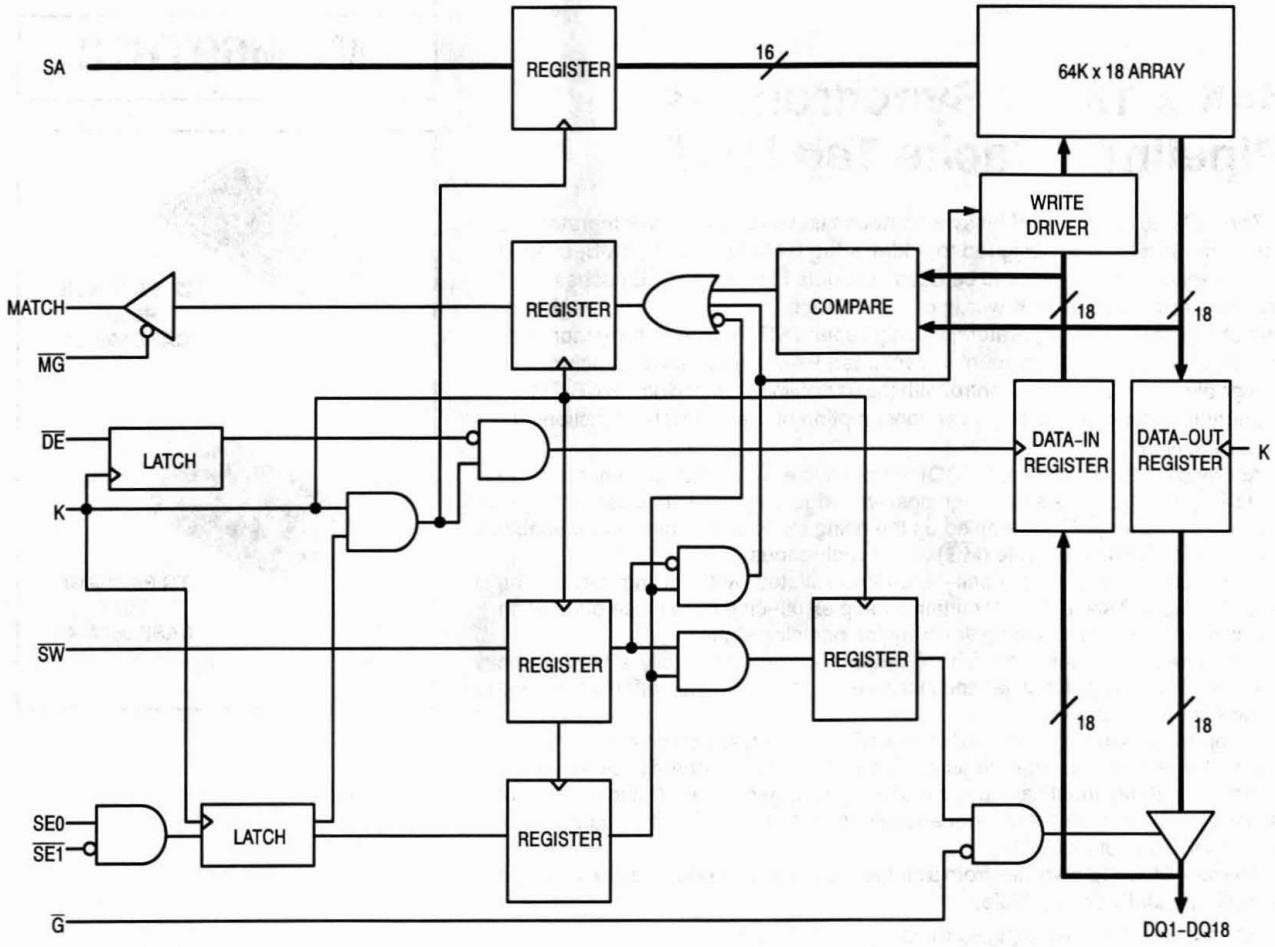
Compare cycles begin as read cycles with output disabled so compare data can be loaded into the input register. The comparator compares the read data with the registered input data, and a match signal is generated. The match output is also stored by an output register and released to the match output buffer at the next rising edge of clock (K).

The MCM69T618 operates from a single 3.3 V power supply and all inputs and outputs are LVTTL compatible.

- MCM69T618–5 = 5 ns Clock–to–Match / 10 ns cycle
  MCM69T618–6 = 6 ns Clock–to–Match / 12 ns cycle
  MCM69T618–7 = 7 ns Clock–to–Match / 13.3 ns cycle
- Single 3.3 V +10%, –5% Power Supply
- Pipelined Data Comparator
- Pipelined Chip Enable and Write Enable for Data (DQ) Output Enable Path
- 64K x 18 Organization Supports Up to 2MB Cache
- Synchronous Data Input Register Load Enable ($\overline{DE}$)
- Internally Self–Timed Write Cycle
- Asynchronous Data I/O Output Enable ($\overline{G}$)
- Asynchronous Match Output Enable ($\overline{MG}$)
- 119 Bump, 50 mil (1.27 mm) Pitch, 7 x 17 Plastic Ball Grid Array (PBGA) and 100 Pin TQFP Packages.

REV 3
4/8/97

FUNCTIONAL BLOCK DIAGRAM



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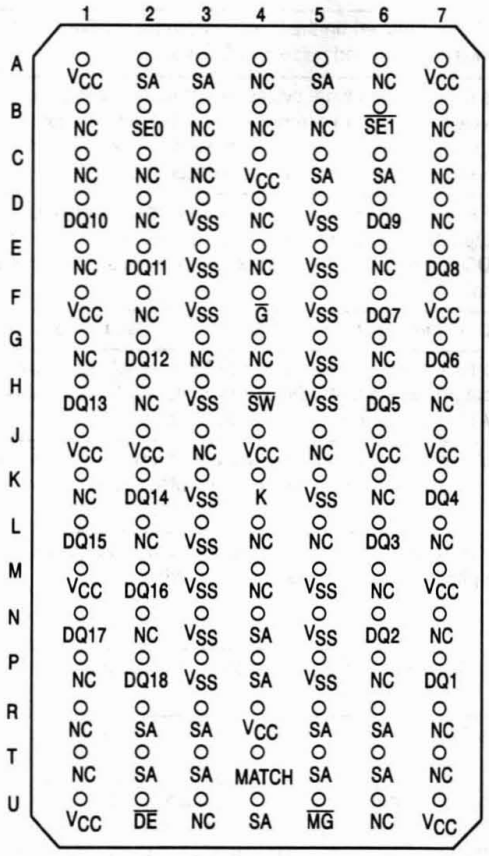
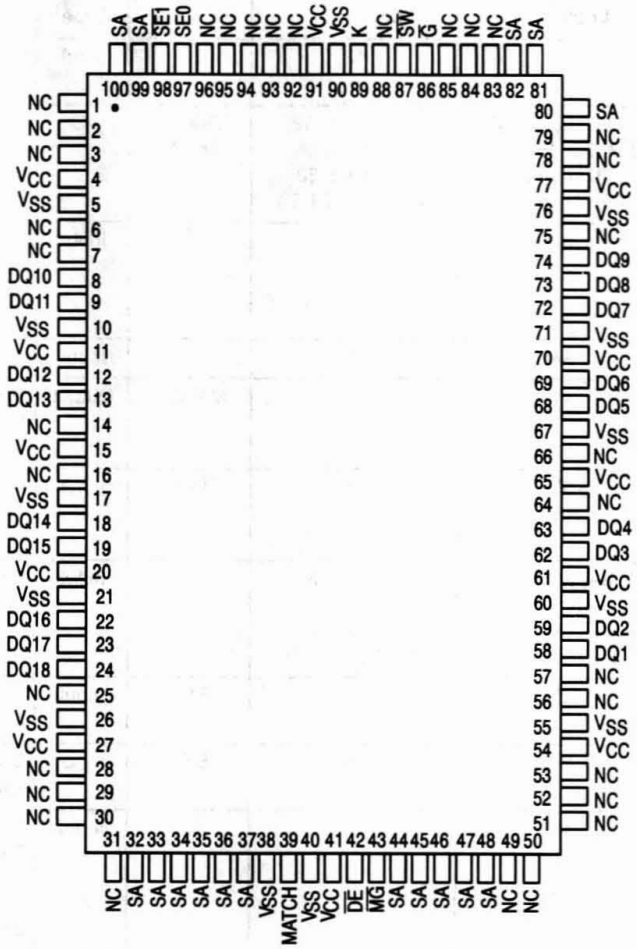
PIN ASSIGNMENTS


1 2 3 4 5 6 7
A VCC SA SA NC SA NC VCC
B NC SE0 NC NC NC SE1 NC
C NC NC NC VCC SA SA NC
D DQ10 NC VSS NC VSS DQ9 NC
E NC DQ11 VSS NC VSS NC DQ8
F VCC NC VSS G VSS DQ7 VCC
G NC DQ12 NC NC VSS NC DQ6
H DQ13 NC VSS SW VSS DQ5 NC
J VCC VCC NC VCC NC VCC VCC
K NC DQ14 VSS K VSS NC DQ4
L DQ15 NC VSS NC NC DQ3 NC
M VCC DQ16 VSS NC VSS NC VCC
N DQ17 NC VSS SA VSS DQ2 NC
P NC DQ18 VSS SA VSS NC DQ1
R NC SA SA VCC SA SA NC
T NC SA SA MATCH SA SA NC
U VCC DE NC SA MG NC VCC

TOP VIEW 119 BUMP PBGA



TOP VIEW 100 PIN TQFP

Not to Scale

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PIN DESCRIPTIONS

PBGA Pin Locations	TQFP Pin Locations	Symbol	Type	Description
2U	42	$\overline{DE}$	Input	Data Enable Input: Latched on the rising clock edge, active low. The data input register is only updated when $\overline{DE}$ is low.
1D, 6D, 2E, 7E, 6F, 2G, 7G, 1H, 6H, 2K, 7K, 1L, 6L, 2M, 1N, 6N, 2P, 7P	8, 9, 12, 13, 18, 19, 22, 23, 24, 58, 59, 62, 63, 68, 69, 72, 73, 74	DQ1 – DQ18	I/O	Synchronous Data I/O: For write cycles, registered on the rising clock edge. Two cycles after a read command, the read data is output on the DQ pins provided that $\overline{G}$ is low. On the same cycle of a write command, the write data is input on the DQ signals.
4F	86	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low. $\overline{G}$ must be low for read data to be output two cycles after a read command. If $\overline{G}$ is high, the data output DQ will remain in high impedance even if a read command occurs internally.
4K	89	K	Input	Clock: All the signals except $\overline{G}$ and $\overline{MG}$ are controlled by the clock.
4T	39	MATCH	Output	Two cycles after a compare cycle and if $\overline{MG}$ is low, MATCH will be high if the data presented to the DQ inputs matches the data stored in the RAM. MATCH will be low if the data does not match.
5U	43	$\overline{MG}$	Input	Match Output Enable: Asynchronous pin, active low. When $\overline{MG}$ is low, the MATCH output driver is on, otherwise the MATCH output driver is in high impedance.
2A, 3A, 5A, 5C, 6C, 4N, 4P, 2R, 3R, 5R, 6R, 2T, 3T, 5T, 6T, 4U	32, 33, 34, 35, 36, 37, 44, 45, 46, 47, 48, 80, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge. The address pins select one of the 64K tag entries.
2B	97	SE0	Input	Synchronous Chip Enable: Registered on the rising clock edge, active high.
6B	98	$\overline{SE1}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4H	87	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. The $\overline{SW}$ input specifies whether a read or write cycle is to occur when the chip is enabled. A write command should not be issued within three cycles of a read command unless $\overline{G}$ is high or output drive contention may occur.
1A, 7A, 4C, 1F, 7F, 1J, 2J, 4J, 6J, 7J, 1M, 7M, 4R, 1U, 7U	4, 11, 15, 20, 27, 41, 54, 61, 65, 70, 77, 91	V_{CC}	Supply	Power Supply: 3.3 V +10%, –5%. These pins act as thermal vias to pcb power plane for the PBGA package.
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P	5, 10, 17, 21, 26, 38, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground: These pins act as thermal vias to pcb ground plane for the PBGA package.
4A, 6A, 1B, 3B, 4B, 5B, 7B, 1C, 2C, 3C, 7C, 2D, 4D, 7D, 1E, 4E, 6E, 2F, 1G, 3G, 4G, 6G, 2H, 7H, 3J, 5J, 1K, 6K, 2L, 4L, 5L, 7L, 4M, 6M, 2N, 7N, 1P, 6P, 1R, 7R, 1T, 7T, 3U, 6U	1, 2, 3, 6, 7, 14, 16, 25, 28, 29, 30, 31, 49, 50, 51, 52, 53, 56, 57, 64, 66, 75, 78, 79, 83, 84, 85, 88, 92, 93, 94, 95, 96	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE (See Notes 1 through 4)

Next Cycle	$\overline{SE}$	$\overline{SW}$	$\overline{DE}$	$\overline{MG}$	$\overline{G}$	Match	DQ
Read	0	1	X	X	0	—	Data Out
Write	0	0	0	X	1	—	Data In
Compare	0	1	0	0	1	Data Out	Data In
Fill Write	0	0	1	X	1	—	High–Z
Deselected (Match Out)	1	X	X	0	X	Data High	High–Z
Deselected	1	X	X	1	X	High–Z	High–Z

NOTES:
1. X = Don't Care. 1 = logic high. 0 = logic low.
2. $\overline{SE}$ low is defined as $\overline{SE1}$ = 0 and SE0 = 1. $\overline{SE}$ high is defined as $\overline{SE1}$ = 1 or SE0 = 0.
3. $\overline{G}$ and $\overline{MG}$ are asynchronous signals and are not sampled by the clock K. $\overline{G}$ drives the bus immediately (t_{GLQX}) when $\overline{G}$ goes low.
4. On write cycles that follow read cycles, $\overline{G}$ must be negated prior to the start of the write cycle to ensure proper write data setup times. $\overline{G}$ must also remain negated at the completion of the write cycle to ensure proper write data hold times.

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}		V_{in}, V_{out}	V_{CC} + 0.5	V
Output Current (per I/O)		I_{out}	± 20	mA
Package Power Dissipation	PBGA TQFP	P_D	2.1 1.6	W
Temperature Under Bias		T_{bias}	– 10 to 85	°C
Storage Temperature		T_{stg}	– 55 to 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

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PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	PBGA	TQFP	Unit	Notes
Thermal Resistance (Still Air)			Max	Max		1
Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	41 19	40 25	°C/W	2
Junction to Board (Bottom)		$R_{\theta JB}$	11	17	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	9	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V +10%, –5%, T_J = 20 to 110°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.135	3.3	3.6	V
Operating Temperature	T_J	20	—	110	°C
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	V_{CC} + 0.5**	V

* $V_{IL} \geq -1.5$ V for $t \leq t_{KHKH}/2$.
** $V_{IH} \leq V_{CC} + 1.0$ V for $t \leq t_{KHKH}/2$.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (0 V ≤ V_{in} ≤ V_{CC})		$I_{lkg(I)}$	—	—	± 1	µA
Output Leakage Current (0 V ≤ V_{in} ≤ V_{CC})		$I_{lkg(O)}$	—	—	± 1	µA
AC Supply Current (Device Selected, All Outputs Open, All Inputs Toggling at $V_{in} \leq V_{IL}$ or $\geq V_{IH}$, Cycle Time ≥ t_{KHKH} min)	MCM69T618–5 MCM69T618–6 MCM69T618–7	I_{CCA}	— — —	— — —	240 225 220	mA
CMOS Standby Supply Current (Deselected[1], Clock (K) Cycle Time ≥ t_{KHKH}, All Inputs Toggling at CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{CC} – 0.2 V)	MCM69T618–5 MCM69T618–6 MCM69T618–7	I_{SB1}	—	—	130 110 105	mA
Clock Running Supply Current (Deselected[1], Clock (K) Cycle Time ≥ t_{KHKH}, All Other Inputs Held to Static CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{CC} – 0.2 V)	MCM69T618–5 MCM69T618–6 MCM69T618–7	I_{SB2}	— — —	— — —	45 40 40	mA
Output Low Voltage (I_{OL} = 8 mA)		V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4 mA)		V_{OH}	2.4	—	—	V

NOTE: 1. Device in Deselected mode as defined by the Truth Table.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	3	5	pF
Input/Output Capacitance	$C_{I/O}$	—	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V +10%, –5%, T_J = 20 to 110°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1 Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM69T618–5		MCM69T618–6		MCM69T618–7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	10	—	12	—	13.3	—	ns	
Clock High Pulse Width	t_{KHKL}	3.5	—	4	—	4.5	—	ns	
Clock Low Pulse Width	t_{KLKH}	3.5	—	4	—	4.5	—	ns	
Clock High to Match Valid	t_{KHMV}	—	5	—	6	—	7	ns	
Clock Access Time	t_{KHQV}	—	5	—	6	—	7	ns	4
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	5	ns	4
Match Output Enable to Match Valid	t_{MGLMV}	—	5	—	5	—	5	ns	4
Clock High to Output Active	t_{KHQX1}	0	—	0	—	0	—	ns	4. 6
Clock High to Output Change	t_{KHQX2}	1.5	—	1.5	—	1.5	—	ns	4
Clock High to Match Output Change	t_{KHMX}	1.5	—	1.5	—	1.5	—	ns	
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4, 6
Match Output Enable to Match Active	t_{MGLMX}	0	—	0	—	0	—	ns	4, 6
Output Disable to Q High–Z	t_{GHQZ}	—	5	—	5	—	5	ns	5, 6
Match Output Disable to Match High–Z	t_{MGHMZ}	—	5	—	5	—	5	ns	6
Clock High to Q High–Z	t_{KHQZ}	1.5	5	1.5	5	1.5	5	ns	5, 6
Setup Times: Address Data In Write Enable	t_{AVKH} t_{DVKH} t_{WVKH} t_{EVKH}	2.5	—	2.5	—	2.5	—	ns	
Hold Times: Address Data In Write Enable	t_{KHAX} t_{KHDX} t_{KHWX} t_{KHEX}	0.5	—	0.5	—	0.5	—	ns	

NOTES:
1. "Write" applies to the $\overline{SW}$ signal. "Enable" applies to SE0, $\overline{SE1}$, and $\overline{DE}$ signals.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care after write cycle begins. To prevent bus contention, $\overline{G}$ should be negated prior to start of write cycle.
4. Tested per AC Test Load (See Figure 1).
5. Measured at ± 200 mV from steady state.
6. This parameter is sampled and not 100% tested.

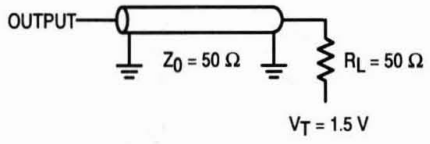
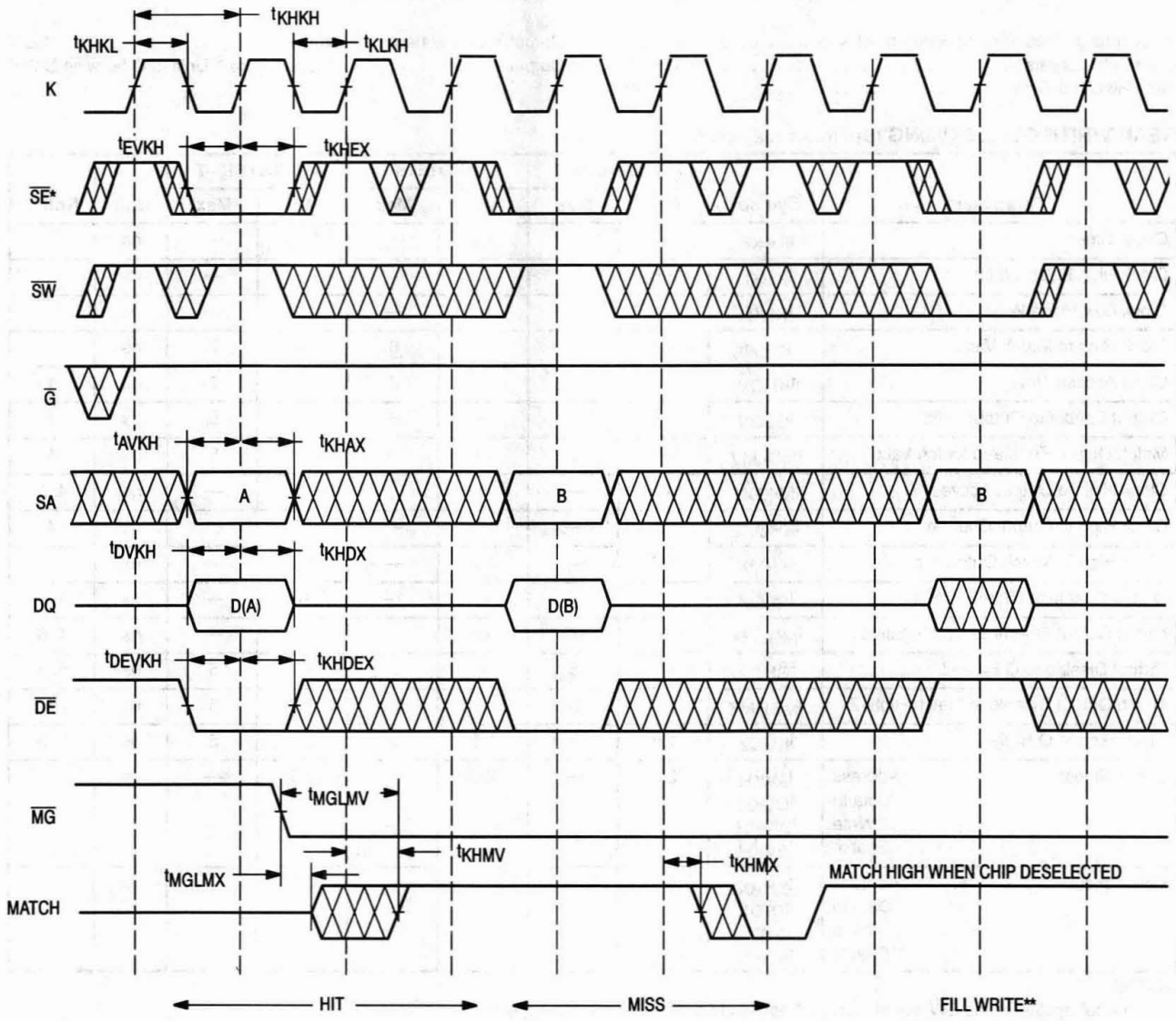


Figure 1. AC Test Loads

COMPARE/FILL WRITE CYCLES



* $\overline{SE}$ low = SE0 high and $\overline{SE1}$ low.

** During fill write sequence, tag entry is written with tag value retained in the data input register from the previous compare cycle.

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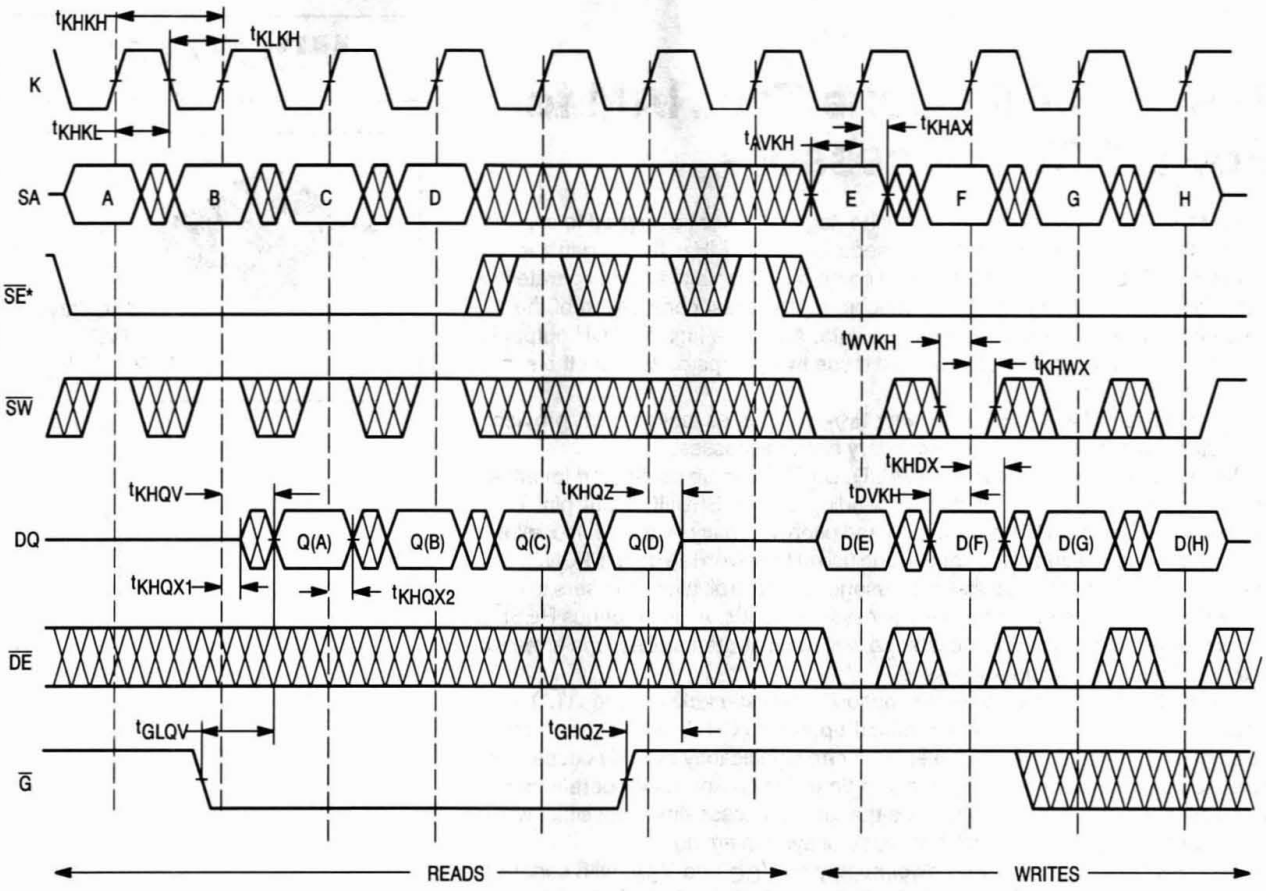
READ/WRITE CYCLES



* $\overline{SE}$ low = SE0 high and $\overline{SE1}$ low.

ORDERING INFORMATION
(Order by Full Part Number)

MCM 69T618 XX X X

- MCM — Motorola Memory Prefix
- 69T618 — Part Number
- XX — Package (ZP = PBGA, TQ = TQFP)
- X — Speed (5 = 5 ns, 6 = 6 ns, 7 = 7 ns)
- X — R = Tape and Reel, Blank = Tray

Full Part Numbers —

MCM69T618ZP5	MCM69T618ZP6	MCM69T618ZP7
MCM69T618ZP5R	MCM69T618ZP6R	MCM69T618ZP7R
MCM69T618TQ5	MCM69T618TQ6	MCM69T618TQ7
MCM69T618TQ5R	MCM69T618TQ6R	MCM69T618TQ7R

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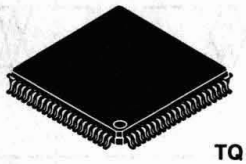
MPC27T416

16K x 16 Bit Cache Tag RAM for PowerPC™ Processors



TQ PACKAGE
TQFP
CASE 917A–02

The MPC27T416 is a 262,144 bit cache–tag static RAM designed to support PowerPC microprocessors at bus speeds up to 66 MHz. It is organized as 16K words of 16 bits each. There are 14 common I/O tag bits and 2 separate I/O status bits. A 14–bit comparator is on–chip to allow fast comparison of the 14 stored tag bits with the current tag input data. An active high MATCH output is generated when the valid bit is true and these two groups of data are the same for a given address.

This high–speed MATCH signal, with t_{AVMV} times as fast as 9 ns, provides the fastest possible enabling of secondary cache accesses.

The two separate I/O status bits (VALID, DIRTY) can be configured for either dedicated or generic functionality, depending on the SFUNC input pin. With SFUNC low, the status bits are defined and used internally by the device, allowing easier determination of the validity and use of the given tag data. SFUNC high releases the defined internal status bit usage and control, allowing users to configure the status bit information to fit their system needs. A synchronous $\overline{\text{RESET}}$ pin, when held low at a rising clock edge, will reset all status bits in the array for easy invalidation of all tag addresses.

The MPC27T416 also provides the option for transfer acknowledge ($\overline{\text{TA}}$) generation within the cache tag itself, based upon MATCH, VALID bit, and other external inputs provided by the user. This can significantly simplify cache controller logic and minimize cache decision time. Match and read operations are both asynchronous in order to provide the fastest access times possible, while write operations are synchronous for ease of system timing.

The MPC27T416 uses a 5 V power supply on V_{CC} and V_{SS}, with separate V_{CCQ} pins provided for the outputs to offer compliance with both 5 V TTL and 3.3 V LVTTL logic levels. The $\overline{\text{PWRDN}}$ pin offers a low–power standby mode, which provides significant system power savings.

The MPC27T416 is offered in a space saving 80–pin thin quad flat pack (TQFP) package.

- 16K x 16 Configuration:
  - — 14 Tag Bits
  - — Two Status Bits (Valid and Dirty)
- Valid Bit Used to Qualify Match Output
- High–Speed Address–to–Match Comparison Times — 9/10/12 ns
- $\overline{\text{TA}}$ Circuitry Included Inside the Cache–Tag for the Highest Speed Operation
- Asynchronous Read/Match Operation and Synchronous Write and Reset Operation
- Separate Write Enable Pins for Tag Bits and Status Bits
- Separate Output Enable Pins for Tag Bits, Status Bits, and $\overline{\text{TA}}$
- Synchronous $\overline{\text{RESET}}$ Pin for Invalidation of all Tag Entries
- Dual Chip Selects for Easy Depth Expansion with No Performance Degradation
- I/O Pins Both 5 V TTL and 3.3 V LVTTL Compatible with V_{CCQ} Pins
- $\overline{\text{PWRDN}}$ Pin to Place Device in Low–Power Mode
- Compatible with PowerPC Platform (CHRP)
- Packaged in an 80–Pin Thin Quad Flat Pack (TQFP)

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REV 3
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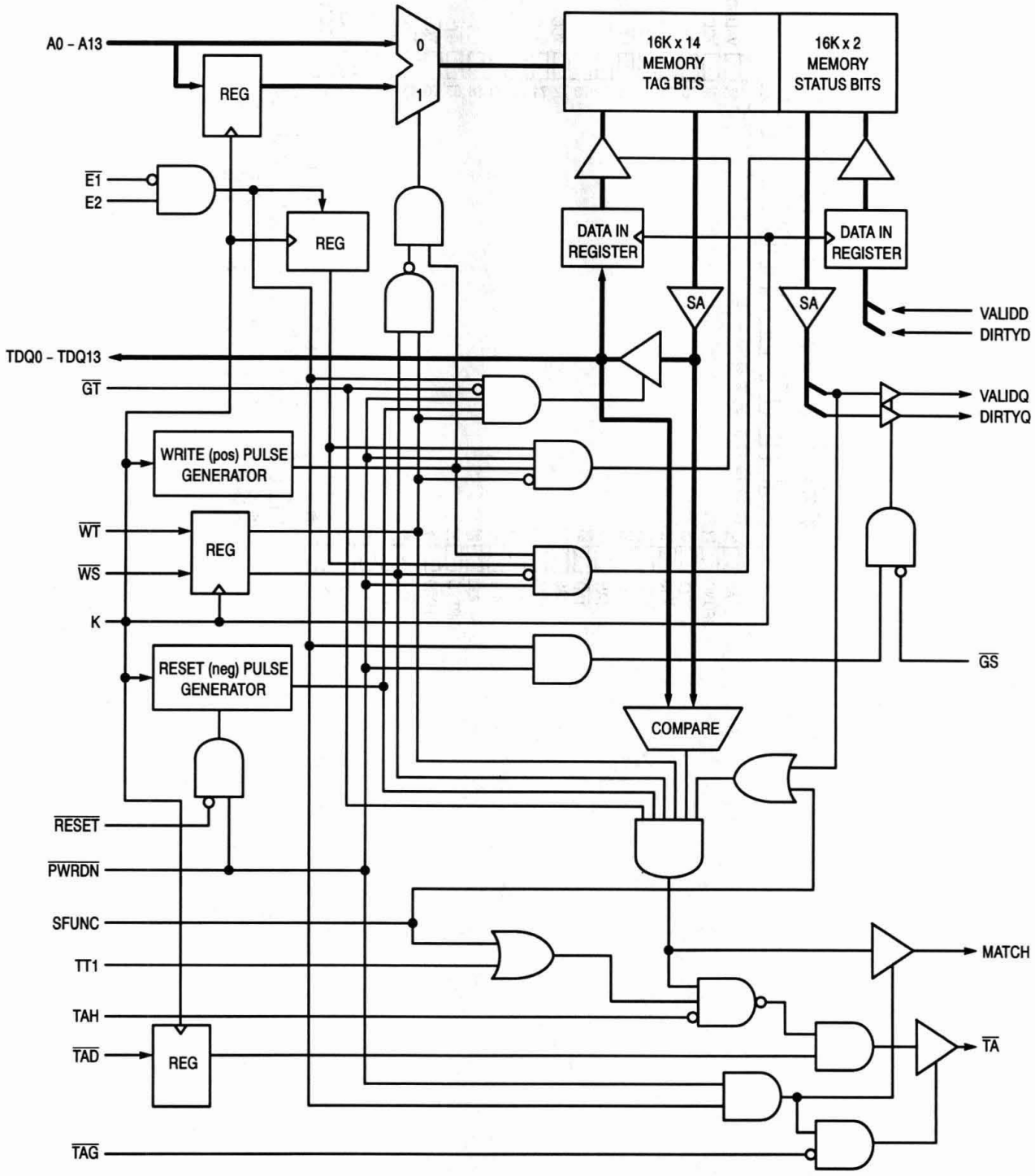
FUNCTIONAL BLOCK DIAGRAM



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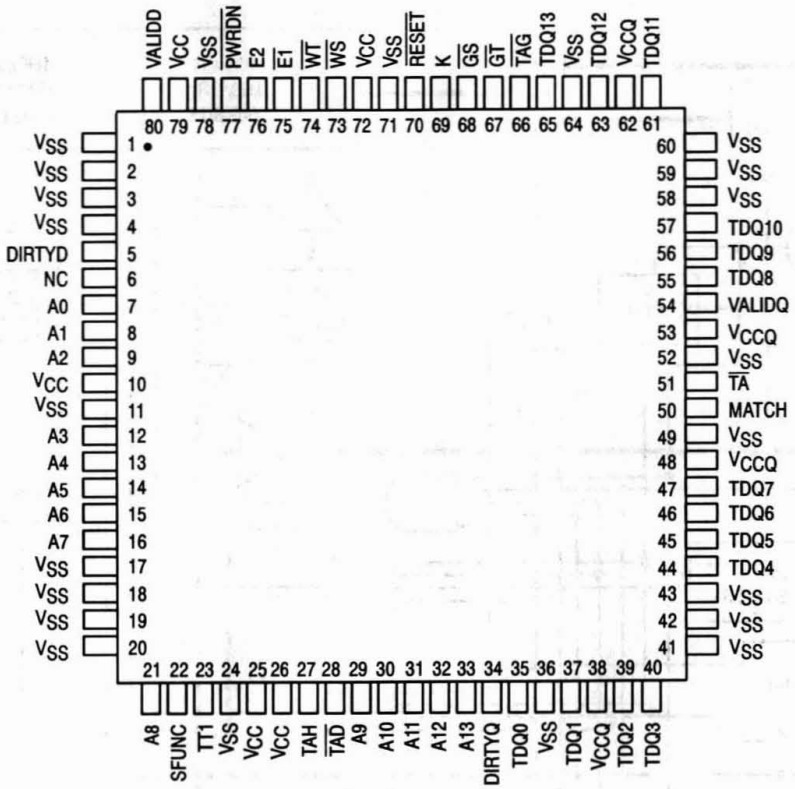
PIN ASSIGNMENT



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PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
7, 8, 9, 12, 13, 14, 15, 16, 21, 29, 30, 31, 32, 33	A0 – A13	Input	Address Inputs: These inputs are registered and must meet setup and hold times for write cycles only. For all other cycles, addresses are asynchronous.
5	DIRTYD	Input	Dirty Bit Input.
34	DIRTYQ	Output	Dirty Bit Output.
75, 76	$\overline{E1}$, E2	Input	Chip Selects: These inputs are registered and must meet setup and hold times for write cycles only. For all other cycles, $\overline{E1}$ and E2 are asynchronous.
68	$\overline{GS}$	Input	Output Enable — Status Bits: Asynchronous, active low.
67	$\overline{GT}$	Input	Output Enable — Tag Bits: Asynchronous, active low.
69	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$, TAH, TT1, SFUNC, and $\overline{PWRDN}$.
50	MATCH	Output	Match: This pin is asserted high when the selected tag's valid bit is true, and the stored tag in the RAM array matches the tag data presented on the TDQ pins.
6	NC	—	No Connection to the Chip.
77	$\overline{PWRDN}$	Input	Powerdown Mode Control Pin: This signal is asynchronous and places the RAM in standby mode.
70	$\overline{RESET}$	Input	Status Bit Reset: Reset cycle is initiated synchronously on a rising clock edge and will terminate within the Status Bit Reset Time. When $\overline{RESET}$ is returned high, the part will return to normal operation within the time specified in the $\overline{RESET}$ AC Cycle Timing table.
22	SFUNC	Input	Status Bit Function Control Pin.
51	$\overline{TA}$	Output	Transfer Acknowledge: Typically used as "ready" signal to processor for cache reads. Can also be used as an active low MATCH pin.
28	$\overline{TAD}$	Input	Additional $\overline{TA}$ Input.
66	$\overline{TAG}$	Input	$\overline{TA}$ Output Enable: Asynchronous, active low.
27	TAH	Input	$\overline{TA}$ Force High: Active high signal places $\overline{TA}$ into high–Z mode.
35, 37, 39, 40, 44, 45, 46, 47, 55, 56, 57, 61, 63, 65	TDQ0 – TDQ13	I/O	Tag Data Input/Outputs: Used as input port for compare cycles. Used as output port for tag read cycles.
23	TT1	Input	Read/Write Input from Processor.
73	$\overline{WS}$	Input	Write Enable — Status Bits: This input is registered and must meet setup and hold times for all cycles when this chip is selected.
74	$\overline{WT}$	Input	Write Enable — Tag Bits: This input is registered and must meet setup and hold times for all cycles when this chip is selected.
80	VALIDD	Input	Valid Bit Input.
54	VALIDQ	Output	Valid Bit Output.
10, 25, 26, 72, 79	V_{CC}	Supply	Power Supply: 5.0 V ± 5%.
38, 48, 53, 62	V_{CCQ}	Supply	Output Buffer Power Supply: 5 V ± 5% or 3.3 V ± 0.3 V.
1, 2, 3, 4, 11, 17, 18, 19, 20, 24, 36, 41, 42, 43, 49, 52, 58, 59, 60, 64, 71, 78	V_{SS}	Supply	Ground.

CHIP SELECT FUNCTION TRUTH TABLE (See Notes 1 and 2)

Next Cycle	$\overline{E1}$	E2	$\overline{RESET}$	$\overline{PWRDN}$	K	$\overline{WT}$	$\overline{WS}$	$\overline{TAG}$	TDQ	VALIDQ	DIRTYQ	MATCH	$\overline{TA}$	POWER
Deselect	H	X	X	H	X	X	X	X	High–Z	High–Z	High–Z	High–Z	High–Z	Active
Deselect	X	L	X	H	X	X	X	X	High–Z	High–Z	High–Z	High–Z	High–Z	Active
Select	L	H	X	H	X	X	X	X	—	—	—	—	—	Active

RESET FUNCTION TRUTH TABLE (See Notes 1 and 2)

Next Cycle	$\overline{E1}$	E2	$\overline{RESET}$	$\overline{PWRDN}$	K	$\overline{WT}$	$\overline{WS}$	$\overline{TAG}$	TDQ	VALIDQ	DIRTYQ	MATCH	$\overline{TA}$	POWER
Reset Status	L	H	L	H	↑	H	H	L	High–Z	L(3)	L(3)	L	H(4)	Active
Reset Status	L	H	L	H	↑	H	H	H	High–Z	L(3)	L(3)	L	High–Z	Active
Reset Status	H	X	L	H	↑	H	H	X	High–Z	High–Z	High–Z	High–Z	High–Z	Active
Reset Status	X	L	L	H	↑	H	H	X	High–Z	High–Z	High–Z	High–Z	High–Z	Active
Not Allowed	X	X	L	H	↑	L	X	X	—	—	—	—	—	—
Not Allowed	X	X	L	H	↑	X	L	X	—	—	—	—	—	—

POWERDOWN FUNCTION TRUTH TABLE (See Notes 1 and 2)

Next Cycle	$\overline{E1}$	E2	$\overline{RESET}$	$\overline{PWRDN}$	K	$\overline{WT}$	$\overline{WS}$	$\overline{TAG}$	TDQ	VALIDQ	DIRTYQ	MATCH	$\overline{TA}$	POWER
Standby	X	X	X	L	X	H	H	X	High–Z	High–Z	High–Z	High–Z	High–Z	Power–down

NOTES: 1. X = Don't Care, H = V_{IH}, L = V_{IL}, "—" = Undefined.
2. $\overline{GT}$, $\overline{GS}$, TT1, TAH, and SFUNC are X for this table.
3. $\overline{GS}$ is low.
4. $\overline{TA}$ output is dependent on the previous registered value of $\overline{TAD}$.

READ FUNCTION TRUTH TABLE (See Notes 1 and 2)

Cycle Type	$\overline{GT}$	$\overline{GS}$	$\overline{WT}$	$\overline{WS}$	K	TT1	TDQ	VALIDD	DIRTYD	VALIDQ	DIRTYQ	MATCH
Read Tag I/O	L	X	H	X	X	X	D_{out}	—	—	—	—	L
Read Status Bits	X	L	X	X	X	X	—	—	—	D_{out}	D_{out}	—
Tag I/O Disable	H	X	X	X	X	X	High–Z	—	—	—	—	—
Status Disable	X	H	X	X	X	X	—	—	—	High–Z	High–Z	—

WRITE FUNCTION TRUTH TABLE (See Notes 1 and 2)

Cycle Type	$\overline{GT}$	$\overline{GS}$	$\overline{WT}$	$\overline{WS}$	K	TT1	TDQ	VALIDD	DIRTYD	VALIDQ	DIRTYQ	MATCH
Write Tag I/O	H	X	L	X	↑	X	D_{in}	—	—	—	—	L
Not Allowed	L	X	L	X	↑	X	—	—	—	—	—	—
Write Status Bits	X	L	X	L	↑	X	—	D_{in}	D_{in}	D_{out}(3)	D_{out}(3)	L
Write Status Bits	X	H	X	L	↑	X	—	D_{in}	D_{in}	High–Z	High–Z	L

NOTES: 1. X = Don't Care, H = V_{IH}, L = V_{IL}, "—" = Undefined.
2. This table applies when $\overline{E1}$ is low, and E2, $\overline{RESET}$, and $\overline{PWRDN}$ are high. $\overline{TAG}$, TAH, $\overline{TAD}$, and SFUNC are X for this table.
3. D_{out} in this case is the same as D_{in}; the input data is written through to the outputs during the write operation.

MATCH FUNCTION TRUTH TABLE (See Notes 1 and 2)

Next Cycle	$\overline{E1}$	E2	SFUNC	$\overline{GT}$	$\overline{WT}$	$\overline{WS}$	TDQ	VALIDQ(3)	DIRTYQ(3)	MATCH
Deselect	H	X	X	X	X	X	High–Z	—	—	High–Z
Deselect	X	L	X	X	X	X	High–Z	—	—	High–Z
Select	L	H	X	X	X	X	—	—	—	—
Read Tag I/O	L	H	X	L	H	X	D_{out}	—	—	L
Write Tag I/O	L	H	X	H	L	X	D_{in}	—	—	L
Write Status Bits	L	H	X	X	X	L	—	D_{in}	D_{in}	L
Invalid Data–Dedicated Status Bits	L	H	L	H	H	H	TDQ_{in}	L	—	L
Match–Dedicated Status Bits	L	H	L	H	H	H	TDQ_{in}	H	—	M(4)
Match–Generic Status Bits	L	H	H	H	H	H	TDQ_{in}	X	—	M(4)

NOTES: 1. X = don't care, H = V_{IH}, L = V_{IL}, "—" = Undefined.
2. $\overline{PWRDN}$ and $\overline{RESET}$ are high for this table. TT1, TAH, $\overline{TAG}$, $\overline{TAD}$, $\overline{GS}$, and K are X.
3. This column represents the stored memory cell data for the given status bit at the selected address.
4. M = high if TDQ_{in} equals the memory contents at that address; M = low if TDQ_{in} does not equal the memory contents at that address.

$\overline{TA}$ FUNCTION TRUTH TABLE (See Notes 1, 2, 3, and 4)

Next Cycle	$\overline{TAG}$	$\overline{TAD}$(5)	$\overline{GT}$	$\overline{WT}$	$\overline{WS}$	TAH	TT1	SFUNC	TDQ	VALIDQ(6)	DIRTYQ(6)	MATCH	$\overline{TA}$
$\overline{TA}$ Disabled	H	X	X	X	X	X	X	X	—	X	—	—	High–Z
External $\overline{TA}$ Input(7)	L	L	X	X	X	X	X	X	—	X	—	—	L
Read Tag	L	H	L	H	X	X	X	X	D_{out}	X	—	L	H
Write Tag	L	H	X	L	X	X	X	X	D_{in}	X	—	L	H
Write Status	L	H	X	X	L	X	X	X	—	D_{in}	D_{in}	L	H
Force $\overline{TA}$ High	L	H	X	X	X	H	X	X	—	X	—	—	H
Invalid Tag	L	H	X	X	X	X	X	L	—	L	—	L	H
Compare	L	H	H	H	H	L	H	L	TDQ_{in}	H	—	M(2)	$\overline{M}$(2)
Compare	L	H	H	H	H	L	X	H	TDQ_{in}	X	—	M(2)	$\overline{M}$(2)

NOTES:
1. X = don't care, H = V_{IH}, L = V_{IL}, "—" = Undefined.
2. M = high if TDQ_{in} equals the memory contents at that address; M = low if TDQ_{in} does not equal the memory contents at that address.
3. $\overline{PWRDN}$ and $\overline{RESET}$ are high for this table. $\overline{GS}$ and K are X.
4. $\overline{E1}$ is low, E2 is high for this table.
5. $\overline{TAD}$, $\overline{WT}$, and $\overline{WS}$ are synchronous inputs; thus the inputs noted in the table must be applied during a rising K edge.
6. This column represents the stored memory cell data for the given status bit at the selected address.
7. $\overline{TAD}$ will be a factor in determining the $\overline{TA}$ output in all cases except when TAH is low, SFUNC and/or TT1 is high, and there is a valid MATCH. In that case, $\overline{TA}$ will be low (valid).

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}, V_{CCQ}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Package Power Dissipation (See Note 2)	P_D	1.7	W
Temperature Under Bias	T_{bias}	– 10 to 85	°C
Storage Temperature	T_{stg}	– 55 to 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

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TQFP PACKAGE THERMAL CHARACTERISTICS (See Note 1)

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	45 38	°C/W	2
Junction to Board (Leads)		$R_{\theta JB}$	27	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	12	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87. Single layer board is the normally quoted value per the specification. The result on the four layer board is an extension to that specification.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, V_{CCQ} = 5.0 V ± 5%, or 3.3 V ± 0.3 V, T_J = 20 to 110°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
5 V Output Buffers	V_{CCQ}	4.75	5.0	5.25	V
3.3 V Output Buffers	V_{CCQ}	3.0	3.3	3.6	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V

* V_{IL} (min) = – 2.0 V for pulse width of less than 10 ns, once per cycle.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit	Notes
Input Leakage Current (V_{CC} = max, V_{in} = 0 V to V_{CC})		$I_{lkg(I)}$	—	± 1	µA	
Output Leakage Current ($\overline{E1} \geq V_{IH}$, E2 ≤ V_{IL}, $\overline{G} \geq V_{IH}$, V_{CC} = max, V_{out} = 0 V to V_{CCQ}, V_{CCQ} = max)		$I_{lkg(O)}$	—	± 1	µA	
AC Supply Current ($\overline{PWRDN} \geq V_{IH}$, Outputs Open, V_{CC} = max, f = f_{max})	MPC27T416–9 MPC27T416–10 MPC27T416–12	I_{CCA}	—	260 260 260	mA	3
CMOS Standby Supply Current ($\overline{PWRDN} \leq V_{IL}$, $V_{in} \geq V_{IH}$ or ≤ V_{IL}, V_{CC} = max, f = f_{max})	MPC27T416–9 MPC27T416–10 MPC27T416–12	I_{SB1}	—	30 30 30	mA	3
Clock Running Supply Current ($\overline{PWRDN} \leq V_{IL}$, $V_{in} \geq V_{HC}$ or ≤ V_{LC}, V_{CC} = max, f = 0)	MPC27T416–9 MPC27T416–10 MPC27T416–12	I_{SB2}	—	25 25 25	mA	3, 4
Output Low Voltage (I_{OL} = 8 mA)		V_{OL}	—	0.4	V	
Output High Voltage (I_{OH} = – 4 mA)		V_{OH}	2.4	—	V	

NOTES:
1. All values are maximum guaranteed values.
2. $\overline{E1} \leq V_{IL}$, E2 ≥ V_{IH}.
3. $f_{max} = 1/t_{CYC}$ (all address inputs are cycling at f_{max}). f = 0 means no address input lines are changing.
4. $V_{HC} = V_{CC} - 0.2$ V, V_{LC} = 0.2 V.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	4	6	pF
Tag Input/Output Capacitance	$C_{I/O}$	—	8	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, V_{CCQ} = 5.0 V ± 5% or 3.3 V ± 0.3 V, T_J = 20 to 110°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1a Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Note 1)

Parameter	Symbol	MPC27T416–9		MPC27T416–10		MPC27T416–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Clock Cycle Time	t_{KHKH}	15	—	15	—	16.6	—	ns	
Address Access Time Tag Bits	t_{AVTV}	—	11	—	12	—	14	ns	
Chip Select Access Time Tag Bits	t_{CSTV}	—	9	—	10	—	12	ns	
Chip Select to Tag and Status Bits in Low–Z	t_{CSQX}	1	—	1	—	1	—	ns	2
Chip Select to Tag and Status Bits in High–Z	t_{CSQZ}	1	6	1	6	1	7	ns	2
Output Enable to Tag Bits Valid	t_{GLTV}	—	6	—	6	—	7	ns	
Output Enable to Tag Bits Low–Z	t_{GLTX}	0	—	0	—	0	—	ns	2
Output Enable to Tag Bits High–Z	t_{GHTZ}	1	6	1	6	1	7	ns	2
Tag and Status Bit Hold from Address Change	t_{AXQX}	2	—	2	—	2	—	ns	
Address Access Time Status Bits	t_{AVSV}	—	9	—	10	—	12	ns	
Chip Select Access Time Status Bits	t_{CSSV}	—	7	—	8	—	10	ns	
Clock High Read to Outputs in Low–Z	t_{KHTX}	1.5	—	1.5	—	1.5	—	ns	2
Clock High Read to Tag Bits Valid	t_{KHTV}	—	10	—	10	—	12	ns	3
Clock High Write to Status Outputs Valid	t_{KHSV}	—	9	—	9	—	10	ns	3
Status Output Hold from Clock High Write	t_{KHSX}	0	—	0	—	0	—	ns	2
Output Enable to Status Bits Valid	t_{GLSV}	—	6	—	6	—	7	ns	
Output Enable to Status Bits High–Z	t_{GHSZ}	1	6	1	6	1	7	ns	
Output Enable to Status Bits Low–Z	t_{GLSX}	0	—	0	—	0	—	ns	
$\overline{WT}$ and $\overline{WS}$ High to $\overline{PWRDN}$ Low	t_{WHPL}	5	—	5	—	5	—	ns	
$\overline{PWRDN}$ High to $\overline{WT}$ and $\overline{WS}$ Active	t_{PHWL}	50	—	50	—	50	—	ns	
Clock Pulse High	t_{KHKL}	4.5	—	4.5	—	5	—	ns	
Clock Pulse Low	t_{KLKH}	4.5	—	4.5	—	5	—	ns	
Setup Times: Address Tag Write Enable Status Write Enable Data In Chip Enable	t_{AVKH} t_{WTVKH} t_{WSVKH} t_{DVKH} t_{EVKH}	3	—	3	—	3	—	ns	
Hold Times: Address Tag Write Enable Status Write Enable Data In Chip Enable	t_{KHAX} t_{KHWTX} t_{KHWSX} t_{KHDX} t_{KHEX}	1.0	—	1.0	—	1.0	—	ns	

NOTES:
1. All Write cycles are synchronous and referenced from rising K.
2. This parameter is sampled and not 100% tested.
3. Addresses are stable prior to K transition high.

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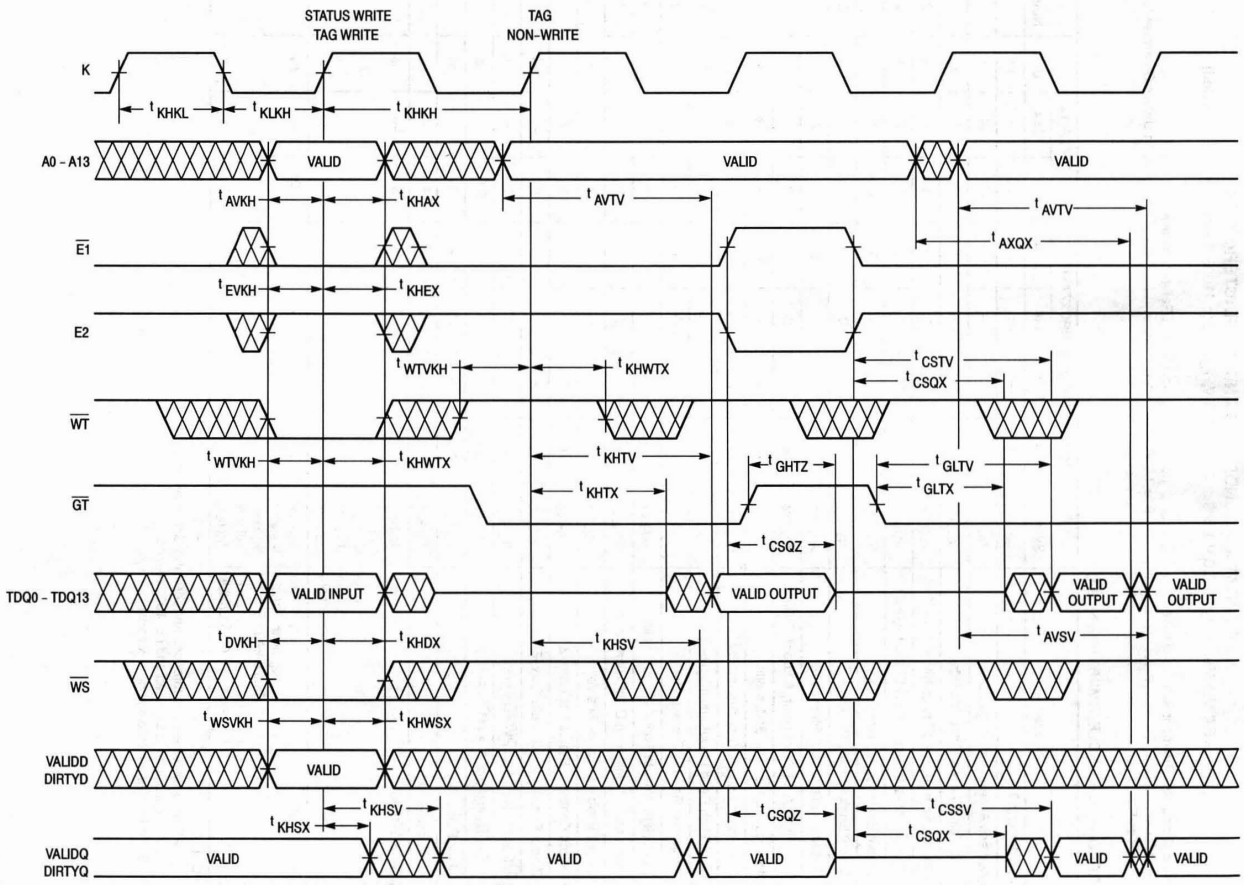
READ AND WRITE CYCLES



MATCH AND $\overline{TA}$ CYCLE TIMING

Parameter	Symbol	MPC27T416–9		MPC27T416–10		MPC27T416–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Address to MATCH Valid	t_{AVMV}	—	9	—	10	—	12	ns	
Data Input to MATCH Valid	t_{TVMV}	—	9	—	10	—	12	ns	
Chip Select to MATCH Valid	t_{CSMV}	—	9	—	10	—	12	ns	
Chip Select to MATCH in Low–Z	t_{CSMX}	1	—	1	—	1	—	ns	1
Chip Select to MATCH in High–Z	t_{CSMZ}	1	6	1	6	1	7	ns	1
MATCH Valid Hold from Address	t_{AVMX}	2	—	2	—	2	—	ns	
MATCH Valid Hold from Data	t_{TVMX}	2	—	2	—	2	—	ns	
$\overline{TA}$ Valid Hold from Address	t_{AVTAX}	2	—	2	—	2	—	ns	
$\overline{TA}$ Valid Hold from Data	t_{TVTAX}	2	—	2	—	2	—	ns	
Address to $\overline{TA}$ Valid	t_{AVTAV}	—	10	—	11	—	13	ns	
Data Input to $\overline{TA}$ Valid	t_{TVTAV}	—	10	—	11	—	13	ns	
Chip Select Low to $\overline{TA}$ Valid	t_{CSTAV}	—	10	—	11	—	13	ns	
$\overline{TAG}$ Low to $\overline{TA}$ Valid	t_{TAGTAV}	—	6	—	7	—	8	ns	
$\overline{TAG}$ Low to $\overline{TA}$ in Low–Z	t_{TAGTAX}	0	—	0	—	0	—	ns	1
$\overline{TAG}$ High to $\overline{TA}$ in High–Z	t_{TAGTAZ}	1	6	1	6	1	7	ns	1
TAH High to Force $\overline{TA}$ High	t_{TAFTAH}	—	5	—	5	—	6	ns	
TAH Low to $\overline{TA}$ Valid	t_{TAFTAV}	—	5	—	5	—	6	ns	
$\overline{TAD}$ Setup Time	t_{TADVKH}	4	—	4	—	4	—	ns	
$\overline{TAD}$ Hold Time	t_{KHTADX}	1.5	—	1.5	—	1.5	—	ns	
Clock High $\overline{TAD}$ Low to $\overline{TA}$ Low	t_{TADTAL}	—	6	—	7	—	8	ns	
Clock High $\overline{TAD}$ High to $\overline{TA}$ Valid	t_{TADTAV}	—	6	—	7	—	8	ns	
$\overline{GT}$ Low to MATCH and $\overline{TA}$ Invalid	t_{GTML}	—	7	—	7	—	8	ns	
$\overline{GT}$ High to MATCH and $\overline{TA}$ Valid	t_{GTMV}	—	8	—	8	—	10	ns	
TT1 Low to $\overline{TA}$ High	t_{TTLTAH}	—	7	—	7	—	8	ns	2
TT1 High to $\overline{TA}$ Valid	t_{TTHTAV}	—	7	—	7	—	8	ns	2
Clock High Write to MATCH and $\overline{TA}$ Invalid	t_{KHMI}	—	7	—	7	—	8	ns	
Clock High Read to MATCH and $\overline{TA}$ Valid	t_{KHMV}	—	9	—	10	—	12	ns	3
Setup Times: Tag Write Enable Status Write Enable	t_{WTVKH} t_{WSVKH}	3	—	3	—	3	—	ns	
Hold Times: Tag Write Enable Status Write Enable	t_{KHWTX} t_{KHWSK}	1.0	—	1.0	—	1.0	—	ns	

NOTES:
1. This parameter is sampled and not 100% tested.
2. These parameters only apply when SFUNC is low.
3. t_{AVMV}, t_{TVMV}, t_{CSMV}, t_{ADB}, t_{DAB}, t_{CSB} must also be satisfied.

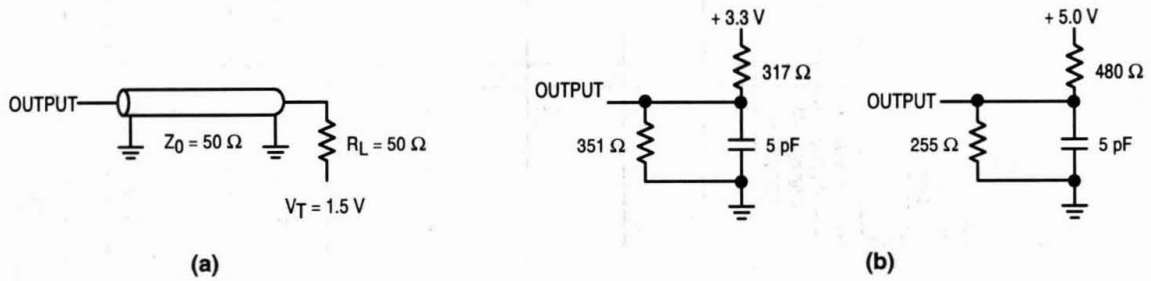
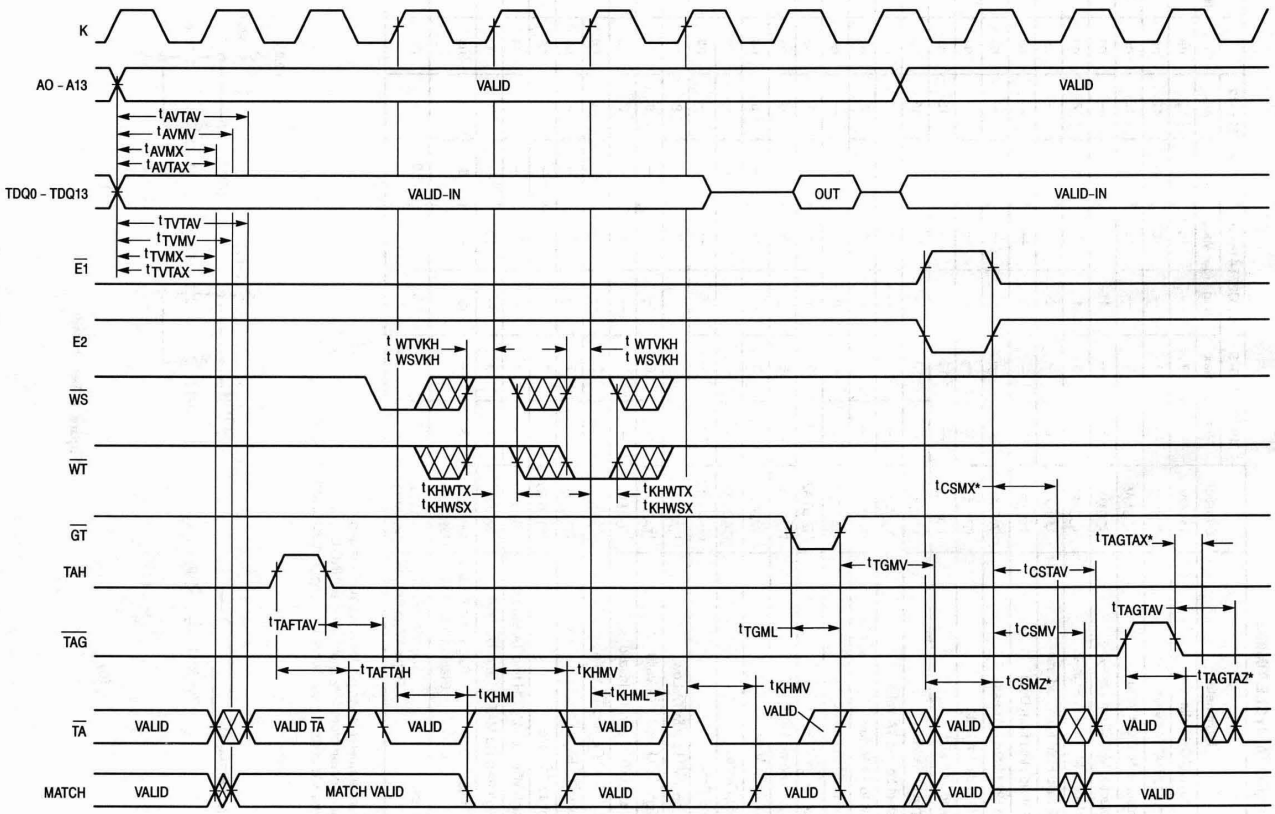


Figure 1. Test Loads

MATCH AND $\overline{TA}$ FUNCTION CYCLES



* Transition is measured plus or minus 200 mV from steady state.

$\overline{\text{RESET}}$ AND $\overline{\text{PWRDN}}$ CYCLE TIMING (See Note 1)

Parameter	Symbol	MPC27T416–9		MPC27T416–10		MPC27T416–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{\text{RESET}}$ Setup Time	t_{RLKH}	4	—	4	—	4	—	ns	
$\overline{\text{RESET}}$ Hold Time	t_{KHRH}	1	—	1	—	1	—	ns	
Status Bit Reset Time	t_{KHSL}	—	60	—	60	—	70	ns	
Status Bit Hold from $\overline{\text{RESET}}$ Low	t_{KHSX}	2	—	2	—	2	—	ns	
$\overline{\text{RESET}}$ Low to MATCH and $\overline{\text{TA}}$ Invalid	t_{KHMI}	—	10	—	10	—	12	ns	
$\overline{\text{RESET}}$ High to MATCH and $\overline{\text{TA}}$ Valid	t_{RHMV}	—	120	—	120	—	130	ns	
$\overline{\text{RESET}}$ Low to Tag Bits High–Z	t_{KHTZ}	—	10	—	10	—	12	ns	2
$\overline{\text{RESET}}$ High to Tag Bits Low–Z	t_{RHTX}	—	100	—	100	—	110	ns	2
$\overline{\text{PWRDN}}$ Setup Time (when $\overline{\text{RESET}}$ low)	t_{PHKH1}	30	—	30	—	30	—	ns	
$\overline{\text{RESET}}$ High to $\overline{\text{WT}}$ and $\overline{\text{WS}}$ Low	t_{RHWL}	95	—	95	—	105	—	ns	
$\overline{\text{PWRDN}}$ Low to Low Power Mode	t_{PLIL}	—	50	—	50	—	50	ns	2
$\overline{\text{PWRDN}}$ High to Active Power Mode	t_{PHIH}	0	—	0	—	0	—	ns	2
$\overline{\text{PWRDN}}$ Low to Outputs in High–Z	t_{PLQZ}	—	10	—	10	—	12	ns	2
$\overline{\text{PWRDN}}$ High to Outputs in Low–Z	t_{PHQX}	0	—	0	—	0	—	ns	2
$\overline{\text{PWRDN}}$ High to Outputs Valid	t_{PHQV}	—	50	—	50	—	50	ns	
$\overline{\text{WT}}$ and $\overline{\text{WS}}$ High to $\overline{\text{PWRDN}}$ Low	t_{KHPL}	5	—	5	—	5	—	ns	2
$\overline{\text{WT}}$ and $\overline{\text{WS}}$ Setup Time	t_{WVKH}	3	—	3	—	3	—	ns	
$\overline{\text{PWRDN}}$ Setup Time (first write following $\overline{\text{PWRDN}}$ cycle)	t_{PHKH2}	50	—	50	—	50	—	ns	

NOTES:
1. $\overline{\text{PWRDN}}$ mode is intended to be used during extended time periods of device inactivity.
2. This parameter is sampled and not 100% tested.

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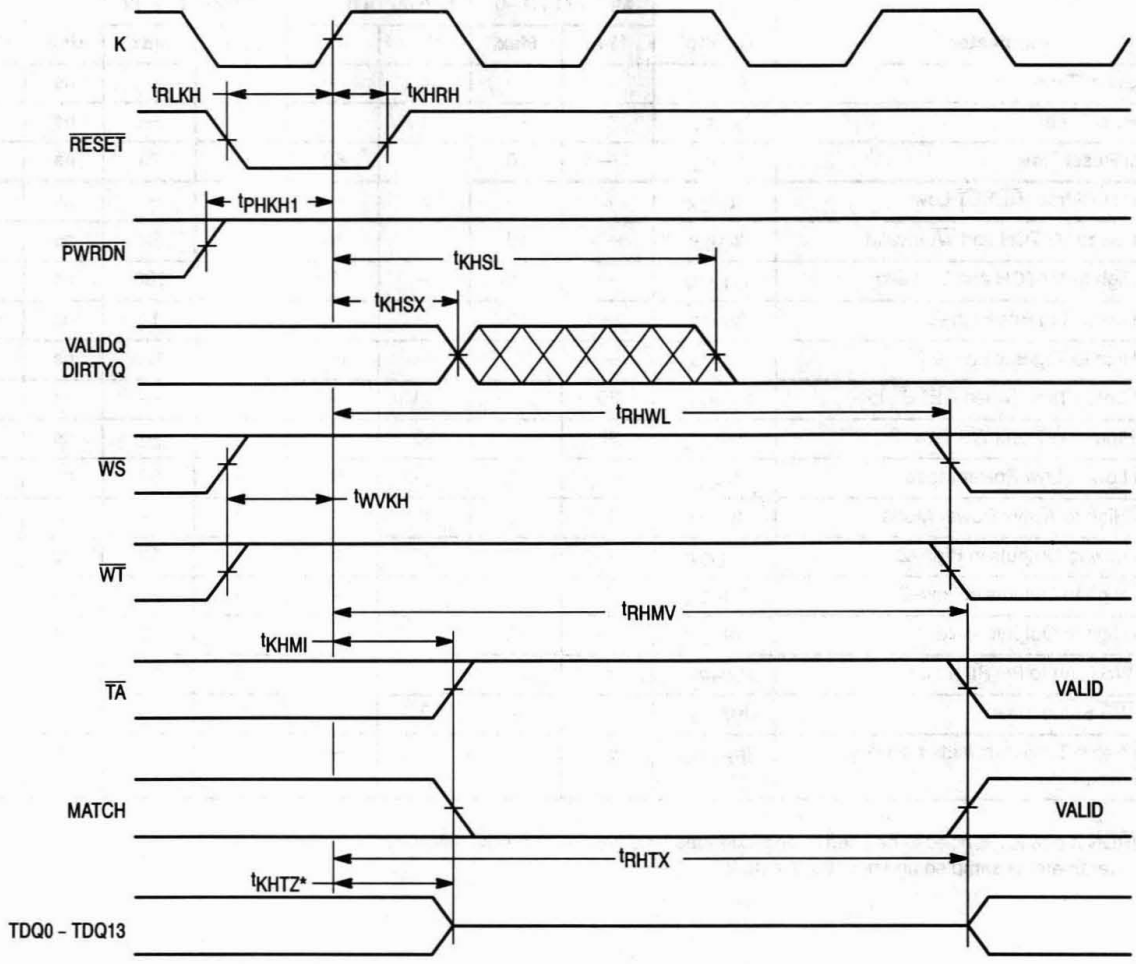
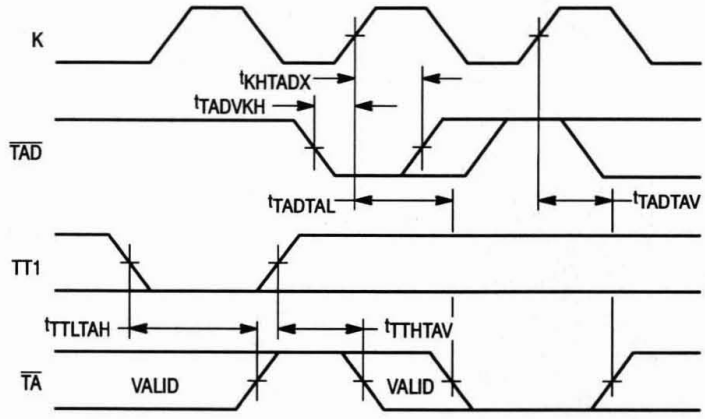
$\overline{\text{RESET}}$ FUNCTION



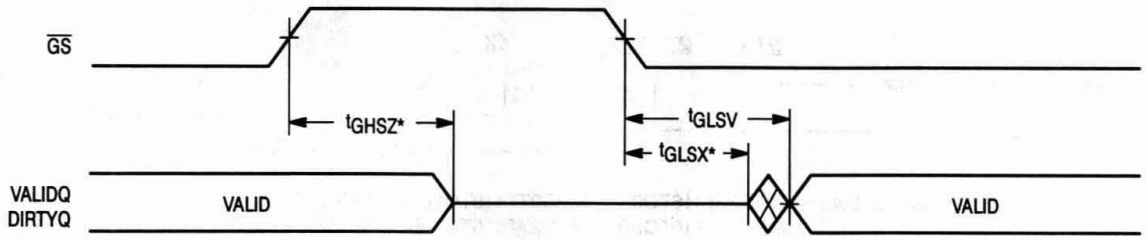
* Transition is measured plus or minus 200 mV from steady state.

$\overline{\text{TA}}$ AND TT1 SIGNAL

(SFUNC = low)

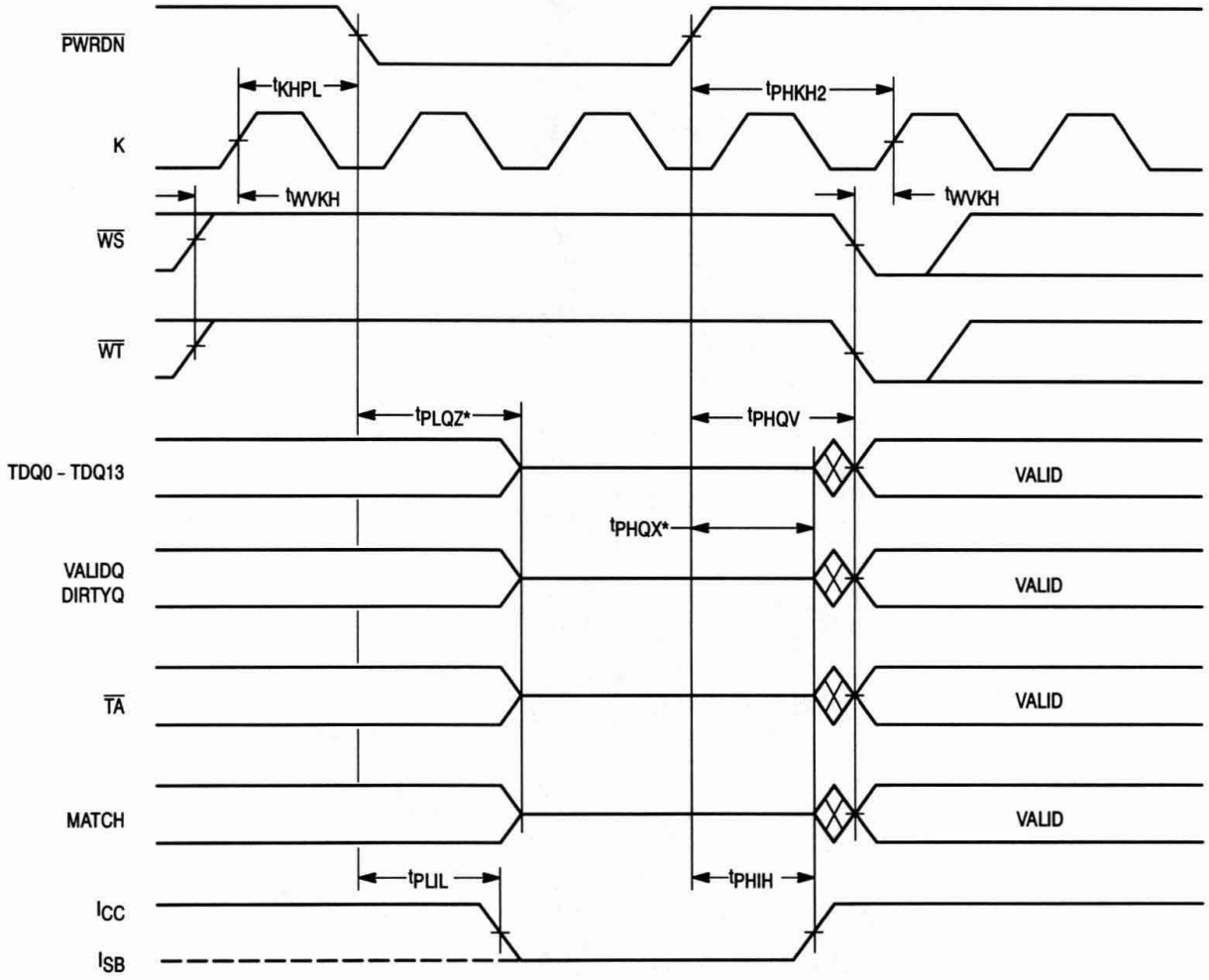


$\overline{GS}$ FUNCTION



* Transition is measured plus or minus 200 mV from steady state.

POWER DOWN FUNCTION



* Transition is measured plus or minus 200 mV from steady state.

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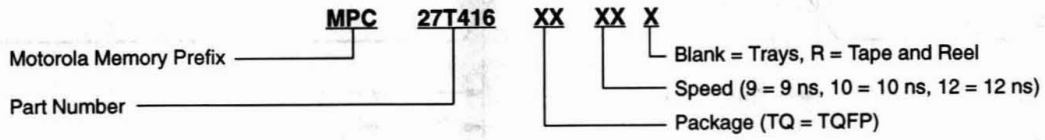
ORDERING INFORMATION
(Order by Full Part Number)


MPC 27T416 XX XX X
Motorola Memory Prefix
Part Number
Blank = Trays, R = Tape and Reel
Speed (9 = 9 ns, 10 = 10 ns, 12 = 12 ns)
Package (TQ = TQFP)

Full Part Numbers — MPC27T416TQ9 MPC27T416TQ10 MPC27T416TQ12
MPC27T416TQ9R MPC27T416TQ10R MPC27T416TQ12R

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MPC27T415

16K x 15 Bit Cache Tag RAM for PowerPC™ Processors

TQ PACKAGE
TQFP
CASE 917A–02

The MPC27T415 is a 245,760 bit cache–tag static RAM designed to support PowerPC microprocessors at bus speeds up to 66 MHz. It is organized as 16K words of 15 bits each. There are 12 common I/O tag bits and 3 separate I/O status bits. A 12–bit comparator is on–chip to allow fast comparison of the 12 stored tag bits with the current tag input data. An active high MATCH output is generated when the valid bit is true and these two groups of data are the same for a given address.

This high–speed MATCH signal, with t_{AVMV} times as fast as 9 ns, provides the fastest possible enabling of secondary cache accesses.

The three separate I/O status bits (VALID, DIRTY, and WT) can be configured for either dedicated or generic functionality, depending on the SFUNC input pin. With SFUNC low, the status bits are defined and used internally by the device, allowing easier determination of the validity and use of the given tag data. SFUNC high releases the defined internal status bit usage and control, allowing users to configure the status bit information to fit their system needs. A synchronous $\overline{\text{RESET}}$ pin, when held low at a rising clock edge, will reset all status bits in the array for easy invalidation of all tag addresses.

The MPC27T415 also provides the option for transfer acknowledge ($\overline{\text{TA}}$) generation within the cache tag itself, based upon MATCH, VALID bit, WT bit, and other external inputs provided by the user. This can significantly simplify cache controller logic and minimize cache decision time. Match and read operations are both asynchronous in order to provide the fastest access times possible, while write operations are synchronous for ease of system timing.

The MPC27T415 uses a 5 V power supply on V_{CC} and V_{SS}, with separate V_{CCQ} pins provided for the outputs to offer compliance with both 5 V TTL and 3.3 V LVTTL logic levels. The $\overline{\text{PWRDN}}$ pin offers a low–power standby mode, which provides significant system power savings.

The MPC27T415 is offered in a space saving 80–pin thin quad flat pack (TQFP) package.

- 16K x 15 Configuration:
  - — 12 Tag Bits
  - — Three Status Bits (Valid, Dirty, and WT)
- Valid Bit Used to Qualify Match Output
- High–Speed Address–to–Match Comparison Times — 9/10/12 ns
- $\overline{\text{TA}}$ Circuitry Included Inside the Cache–Tag for the Highest Speed Operation
- Asynchronous Read/Match Operation and Synchronous Write and Reset Operation
- Separate Write Enable for Tag Bits and Status Bits
- Separate Output Enable for Tag Bits, Status Bits, and $\overline{\text{TA}}$
- Synchronous $\overline{\text{RESET}}$ Pin for Invalidation of all Tag Entries
- Dual Chip Selects for Easy Depth Expansion with No Performance Degradation
- I/O Pins Both 5 V TTL and 3.3 V LVTTL Compatible with V_{CCQ} Pins
- $\overline{\text{PWRDN}}$ Pin to Place Device in Low–Power Mode
- Compatible with PowerPC Platform (CHRP)
- Drop–In Replacement for IDT71216
- Packaged in an 80–Pin Thin Quad Flat Pack (TQFP)

The PowerPC name is a trademark of IBM Corp., used under license therefrom.

REV 2
11/11/96

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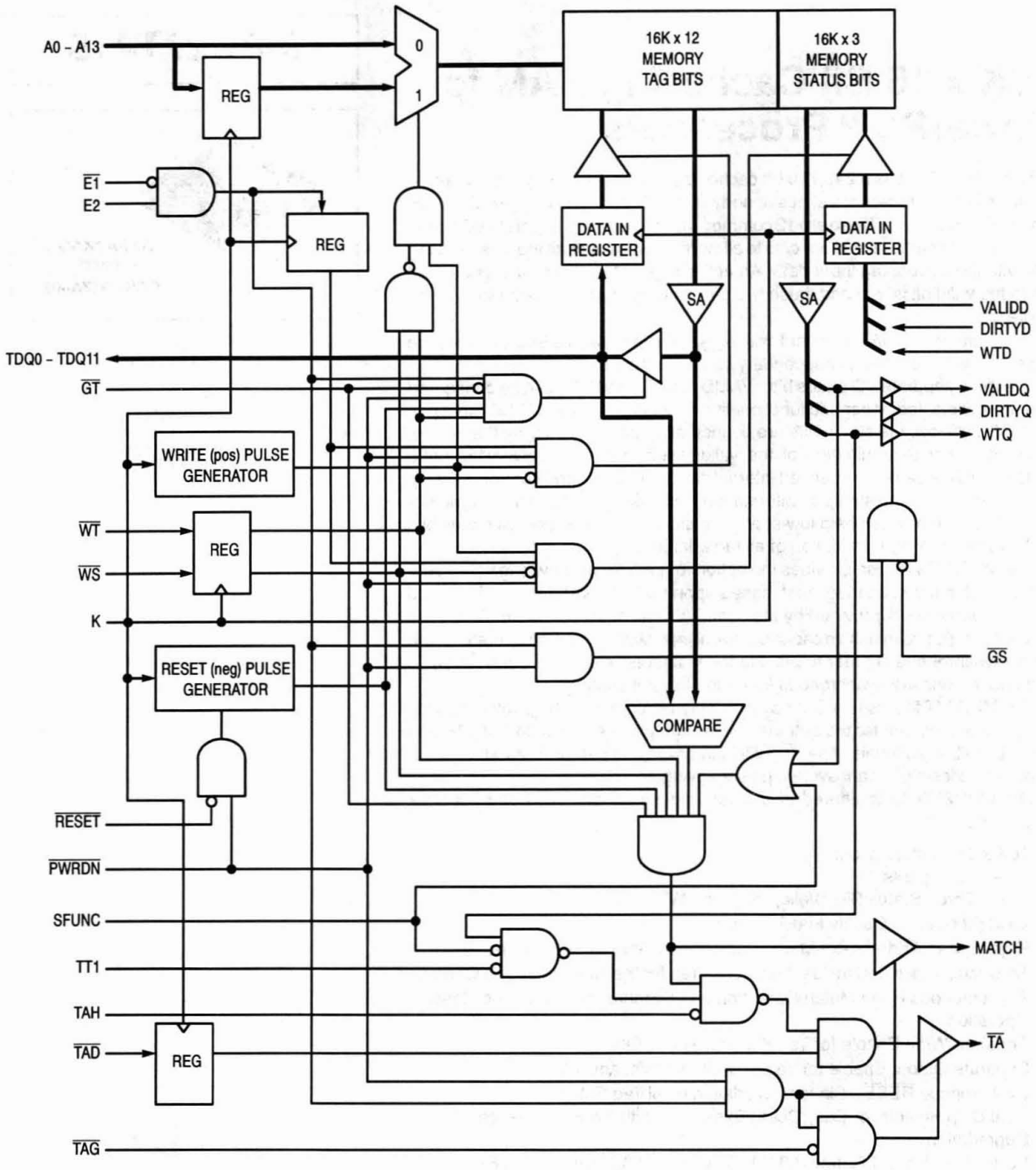
FUNCTIONAL BLOCK DIAGRAM



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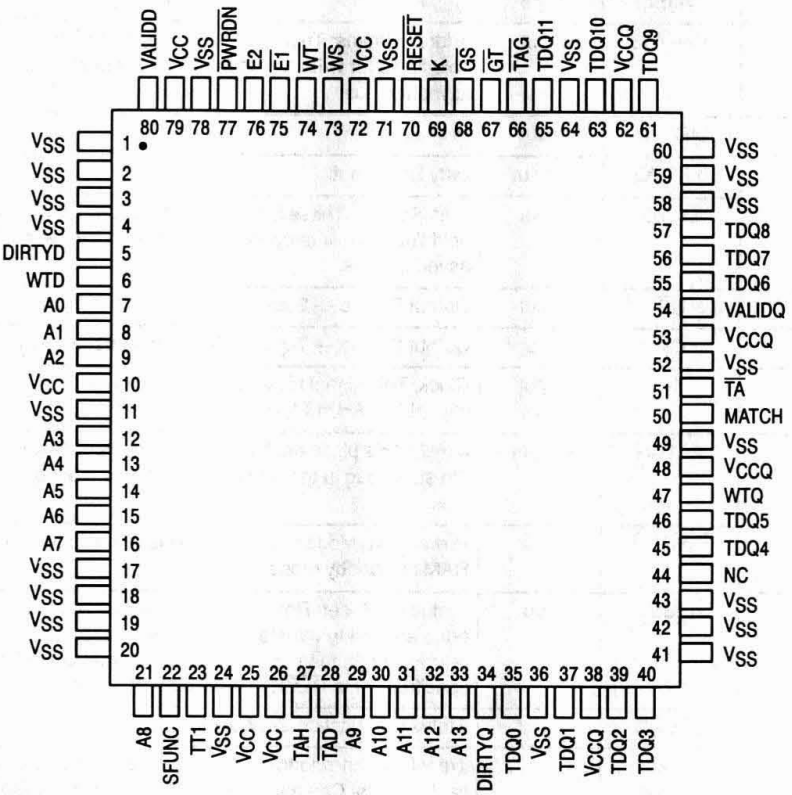
PIN ASSIGNMENT



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PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
7, 8, 9, 12, 13, 14, 15, 16, 21, 29, 30, 31, 32, 33	A0 – A13	Input	Address Inputs: These inputs are registered and must meet setup and hold times for write cycles only. For all other cycles, addresses are asynchronous.
5	DIRTYD	Input	Dirty Bit Input.
34	DIRTYQ	Output	Dirty Bit Output.
75, 76	$\overline{E1}$, E2	Input	Chip Selects: These inputs are registered and must meet setup and hold times for write cycles only. For all other cycles, $\overline{E1}$ and E2 are asynchronous.
68	$\overline{GS}$	Input	Output Enable — Status Bits: Asynchronous, active low.
67	$\overline{GT}$	Input	Output Enable — Tag Bits: Asynchronous, active low.
69	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$, TAH, TT1, SFUNC, and $\overline{PWRDN}$.
50	MATCH	Output	Match: This pin is asserted high when the selected tag's valid bit is true, and the stored tag in the RAM array matches the tag data presented on the TDQ pins.
77	$\overline{PWRDN}$	Input	Powerdown Mode Control Pin: This signal is asynchronous and places the RAM in standby mode.
70	$\overline{RESET}$	Input	Status Bit Reset: Reset cycle is initiated synchronously on a rising clock edge and will terminate within the Status Bit Reset Time. When $\overline{RESET}$ is returned high, the part will return to normal operation within the time specified in the $\overline{RESET}$ AC Cycle Timing table.
22	SFUNC	Input	Status Bit Function Control Pin.
51	$\overline{TA}$	Output	Transfer Acknowledge: Typically used as "ready" signal to processor for cache reads. Can also be used as an active low MATCH pin.
28	$\overline{TAD}$	Input	Additional $\overline{TA}$ Input.
66	$\overline{TAG}$	Input	$\overline{TA}$ Output Enable: Asynchronous, active low.
27	TAH	Input	$\overline{TA}$ Force High: Active high signal places $\overline{TA}$ into high–Z mode.
35, 37, 39, 40, 45, 46, 55, 56, 57, 61, 63, 65	TDQ0 – TDQ11	I/O	Tag Data Input/Outputs: Used as input port for compare cycles. Used as output port for tag read cycles.
23	TT1	Input	Read/Write Input from Processor.
80	VALIDD	Input	Valid Bit Input.
54	VALIDQ	Output	Valid Bit Output.
73	$\overline{WS}$	Input	Write Enable — Status Bits: This input is registered and must meet setup and hold times for all cycles when this chip is selected.
74	$\overline{WT}$	Input	Write Enable — Tag Bits: This input is registered and must meet setup and hold times for all cycles when this chip is selected.
6	WTD	Input	WT Bit Input.
47	WTQ	Output	WT Bit Output.
10, 25, 26, 72, 79	V_{CC}	Supply	Power Supply: 5.0 V ± 5%.
38, 48, 53, 62	V_{CCQ}	Supply	Output Buffer Power Supply: 5.0 V ± 5%, or 3.3 V ± 0.3 V.
1, 2, 3, 4, 11, 17, 18, 19, 20, 24, 36, 41, 42, 43, 49, 52, 58, 59, 60, 64, 71, 78	V_{SS}	Supply	Ground.
44	NC	—	No Connection to the Chip.

CHIP SELECT FUNCTION TRUTH TABLE (See Notes 1 and 2)

Next Cycle	$\overline{E1}$	E2	$\overline{RESET}$	$\overline{PWRDN}$	K	$\overline{WT}$	$\overline{WS}$	$\overline{TAG}$	TDQ	VALIDQ	DIRTYQ	WTQ	MATCH	$\overline{TA}$	POWER
Deselect	H	X	X	H	X	X	X	X	High–Z	High–Z	High–Z	High–Z	High–Z	High–Z	Active
Deselect	X	L	X	H	X	X	X	X	High–Z	High–Z	High–Z	High–Z	High–Z	High–Z	Active
Select	L	H	X	H	X	X	X	X	—	—	—	—	—	—	Active

RESET FUNCTION TRUTH TABLE (See Notes 1 and 2)

Next Cycle	$\overline{E1}$	E2	$\overline{RESET}$	$\overline{PWRDN}$	K	$\overline{WT}$	$\overline{WS}$	$\overline{TAG}$	TDQ	VALIDQ	DIRTYQ	WTQ	MATCH	$\overline{TA}$	POWER
Reset Status	L	H	L	H	↑	H	H	L	High–Z	L(3)	L(3)	L(3)	L	H(4)	Active
Reset Status	L	H	L	H	↑	H	H	H	High–Z	L(3)	L(3)	L(3)	L	High–Z	Active
Reset Status	H	X	L	H	↑	H	H	X	High–Z	High–Z	High–Z	High–Z	High–Z	High–Z	Active
Reset Status	X	L	L	H	↑	H	H	X	High–Z	High–Z	High–Z	High–Z	High–Z	High–Z	Active
Not Allowed	X	X	L	H	↑	L	X	X	—	—	—	—	—	—	—
Not Allowed	X	X	L	H	↑	X	L	X	—	—	—	—	—	—	—

POWERDOWN FUNCTION TRUTH TABLE (See Notes 1 and 2)

Next Cycle	$\overline{E1}$	E2	$\overline{RESET}$	$\overline{PWRDN}$	K	$\overline{WT}$	$\overline{WS}$	$\overline{TAG}$	TDQ	VALIDQ	DIRTYQ	WTQ	MATCH	$\overline{TA}$	POWER
Standby	X	X	X	L	X	H	H	X	High–Z	High–Z	High–Z	High–Z	High–Z	High–Z	Power–down

NOTES: 1. X = Don't Care, H = V_{IH}, L = V_{IL}, "—" = Undefined.
2. $\overline{GT}$, $\overline{GS}$, TT1, TAH, and SFUNC are X for this table.
3. $\overline{GS}$ is low.
4. $\overline{TA}$ output is dependent on the previous registered value of $\overline{TAD}$.

READ FUNCTION TRUTH TABLE (See Notes 1 and 2)

Cycle Type	$\overline{GT}$	$\overline{GS}$	$\overline{WT}$	$\overline{WS}$	K	TT1	TDQ	VALIDD	DIRTYD	WTD	VALIDQ	DIRTYQ	WTQ	MATCH
Read Tag I/O	L	X	H	X	X	X	D_{out}	—	—	—	—	—	—	L
Read Status Bits	X	L	X	X	X	X	—	—	—	—	D_{out}	D_{out}	D_{out}	—
Tag I/O Disable	H	X	X	X	X	X	High–Z	—	—	—	—	—	—	—
Status Disable	X	H	X	X	X	X	—	—	—	—	High–Z	High–Z	High–Z	—

WRITE FUNCTION TRUTH TABLE (See Notes 1 and 2)

Cycle Type	$\overline{GT}$	$\overline{GS}$	$\overline{WT}$	$\overline{WS}$	K	TT1	TDQ	VALIDD	DIRTYD	WTD	VALIDQ	DIRTYQ	WTQ	MATCH
Write Tag I/O	H	X	L	X	↑	X	D_{in}	—	—	—	—	—	—	L
Not Allowed	L	X	L	X	↑	X	—	—	—	—	—	—	—	—
Write Status Bits	X	L	X	L	↑	X	—	D_{in}	D_{in}	D_{in}	D_{out}(3)	D_{out}(3)	D_{out}(3)	L
Write Status Bits	X	H	X	L	↑	X	—	D_{in}	D_{in}	D_{in}	High–Z	High–Z	High–Z	L

NOTES: 1. X = Don't Care, H = V_{IH}, L = V_{IL}, "—" = Undefined.
2. This table applies when $\overline{E1}$ is low, and E2, $\overline{RESET}$, and $\overline{PWRDN}$ are high. $\overline{TAG}$, TAH, $\overline{TAD}$, and SFUNC are X for this table.
3. D_{out} in this case is the same as D_{in}; the input data is written through to the outputs during the write operation.

MATCH FUNCTION TRUTH TABLE (See Notes 1 and 2)

Next Cycle	$\overline{E1}$	E2	SFUNC	$\overline{GT}$	$\overline{WT}$	$\overline{WS}$	TDQ	VALIDQ(3)	DIRTYQ(3)	WTQ(3)	MATCH
Deselect	H	X	X	X	X	X	High–Z	—	—	—	High–Z
Deselect	X	L	X	X	X	X	High–Z	—	—	—	High–Z
Select	L	H	X	X	X	X	—	—	—	—	—
Read Tag I/O	L	H	X	L	H	X	D_{out}	—	—	—	L
Write Tag I/O	L	H	X	H	L	X	D_{in}	—	—	—	L
Write Status Bits	L	H	X	X	X	L	—	D_{in}	D_{in}	D_{in}	L
Invalid Data–Dedicated Status Bits	L	H	L	H	H	H	TDQ_{in}	L	—	—	L
Match–Dedicated Status Bits	L	H	L	H	H	H	TDQ_{in}	H	—	—	M(4)
Match–Generic Status Bits	L	H	H	H	H	H	TDQ_{in}	X	—	—	M(4)

NOTES: 1. X = don't care, H = V_{IH}, L = V_{IL}, "—" = Undefined.
2. $\overline{PWRDN}$ and $\overline{RESET}$ are high for this table. TT1, TAH, $\overline{TAG}$, $\overline{TAD}$, $\overline{GS}$, and K are X.
3. This column represents the stored memory cell data for the given status bit at the selected address.
4. M = high if TDQ_{in} equals the memory contents at that address; M = low if TDQ_{in} does not equal the memory contents at that address.

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$\overline{TA}$ FUNCTION TRUTH TABLE (See Notes 1, 2, 3, and 4)

Next Cycle	$\overline{TAG}$	$\overline{TAD}$(5)	$\overline{GT}$	$\overline{WT}$	$\overline{WS}$	TAH	TT1	SFUNC	TDQ	VALIDQ(6)	DIRTYQ(6)	WTQ(6)	MATCH	$\overline{TA}$
$\overline{TA}$ Disabled	H	X	X	X	X	X	X	X	—	X	—	X	—	High–Z
External $\overline{TA}$ Input(7)	L	L	X	X	X	X	X	X	—	X	—	X	—	L
Read Tag	L	H	L	H	X	X	X	X	D_{out}	X	—	X	L	H
Write Tag	L	H	X	L	X	X	X	X	D_{in}	X	—	X	L	H
Write Status	L	H	X	X	L	X	X	X	—	D_{in}	D_{in}	D_{in}	L	H
Force $\overline{TA}$ High	L	H	X	X	X	H	X	X	—	X	—	X	—	H
Invalid Tag	L	H	X	X	X	X	X	L	—	L	—	X	L	H
Write Through	L	H	X	X	X	X	L	L	—	X	—	H	X	H
Compare	L	H	H	H	H	L	X	L	TDQ_{in}	H	—	L	M(2)	$\overline{M}$(2)
Compare	L	H	H	H	H	L	H	L	TDQ_{in}	H	—	X	M(2)	$\overline{M}$(2)
Compare	L	H	H	H	H	L	X	H	TDQ_{in}	X	—	X	M(2)	$\overline{M}$(2)

NOTES:
1. X = don't care, H = V_{IH}, L = V_{IL}, "—" = Undefined.
2. M = high if TDQ_{in} equals the memory contents at that address; M = low if TDQ_{in} does not equal the memory contents at that address.
3. $\overline{PWRDN}$ and $\overline{RESET}$ are high for this table. $\overline{GS}$ and K are X.
4. $\overline{E1}$ is low, E2 is high for this table.
5. $\overline{TAD}$, $\overline{WT}$, and $\overline{WS}$ are synchronous inputs; thus the inputs noted in the table must be applied during a rising K edge.
6. This column represents the stored memory cell data for the given status bit at the selected address.
7. $\overline{TAD}$ will be a factor in determining the $\overline{TA}$ output in all cases except when TAH is low, SFUNC and/or TT1 is high, and there is a valid MATCH. In that case, $\overline{TA}$ will be low (valid).

5

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}, V_{CCQ}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Operating Temperature	T_A	0 to + 70	°C
Output Current (per I/O)	I_{out}	± 20	mA
Package Power Dissipation. (See Note 2)	P_D	1.7	W
Temperature Under Bias	T_{bias}	– 10 to 85	°C
Storage Temperature	T_{stg}	– 55 to 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

TQFP PACKAGE THERMAL CHARACTERISTICS (See Note 1)

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	45 38	°C/W	2
Junction to Board (Leads)		$R_{\theta JB}$	27	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	12	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87. Single layer board is the normally quoted value per the specification. The result on the four layer board is an extension to that specification.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, V_{CCQ} = 5.0 V ± 5%, or 3.3 V ± 0.3 V, T_J = 20 to 110°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
5 V Output Buffers	V_{CCQ}	4.75	5.0	5.25	V
3.3 V Output Buffers	V_{CCQ}	3.0	3.3	3.6	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V

* V_{IL} (min) = – 2.0 V for pulse width of less than 10 ns, once per cycle.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit	Notes
Input Leakage Current (V_{CC} = max, V_{in} = 0 V to V_{CC})		$I_{lkg(I)}$	—	± 1	µA	
Output Leakage Current ($\overline{E1} \geq V_{IH}$, E2 ≤ V_{IL}, $\overline{G} \geq V_{IH}$, V_{CC} = max, V_{out} = 0 V to V_{CCQ}, V_{CCQ} = max)		$I_{lkg(O)}$	—	± 1	µA	
AC Supply Current ($\overline{PWRDN} \geq V_{IH}$, Outputs Open, V_{CC} = max, f = f_{max})	MPC27T415–9 MPC27T415–10 MPC27T415–12	I_{CCA}	—	260 260 260	mA	3
CMOS Standby Supply Current ($\overline{PWRDN} \leq V_{IL}$, $V_{in} \geq V_{IH}$ or ≤ V_{IL}, V_{CC} = max, f = f_{max})	MPC27T415–9 MPC27T415–10 MPC27T415–12	I_{SB1}	—	30 30 30	mA	3
Clock Running Supply Current ($\overline{PWRDN} \leq V_{IL}$, $V_{in} \geq V_{HC}$ or ≤ V_{LC}, V_{CC} = max, f = 0)	MPC27T415–9 MPC27T415–10 MPC27T415–12	I_{SB2}	—	25 25 25	mA	3, 4
Output Low Voltage (I_{OL} = 8 mA)		V_{OL}	—	0.4	V	
Output High Voltage (I_{OH} = – 4 mA)		V_{OH}	2.4	—	V	

NOTES:
1. All values are maximum guaranteed values.
2. $\overline{E1} \leq V_{IL}$, E2 ≥ V_{IH}.
3. $f_{max} = 1/t_{CYC}$ (all address inputs are cycling at f_{max}). f = 0 means no address input lines are changing.
4. $V_{HC} = V_{CC} - 0.2$ V, V_{LC} = 0.2 V.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	4	6	pF
Tag Input/Output Capacitance	$C_{I/O}$	—	8	10	pF

5

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, V_{CCQ} = 5.0 V ± 5% or 3.3 V ± 0.3 V, T_J = 20 to 110°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1a Unless Otherwise Noted

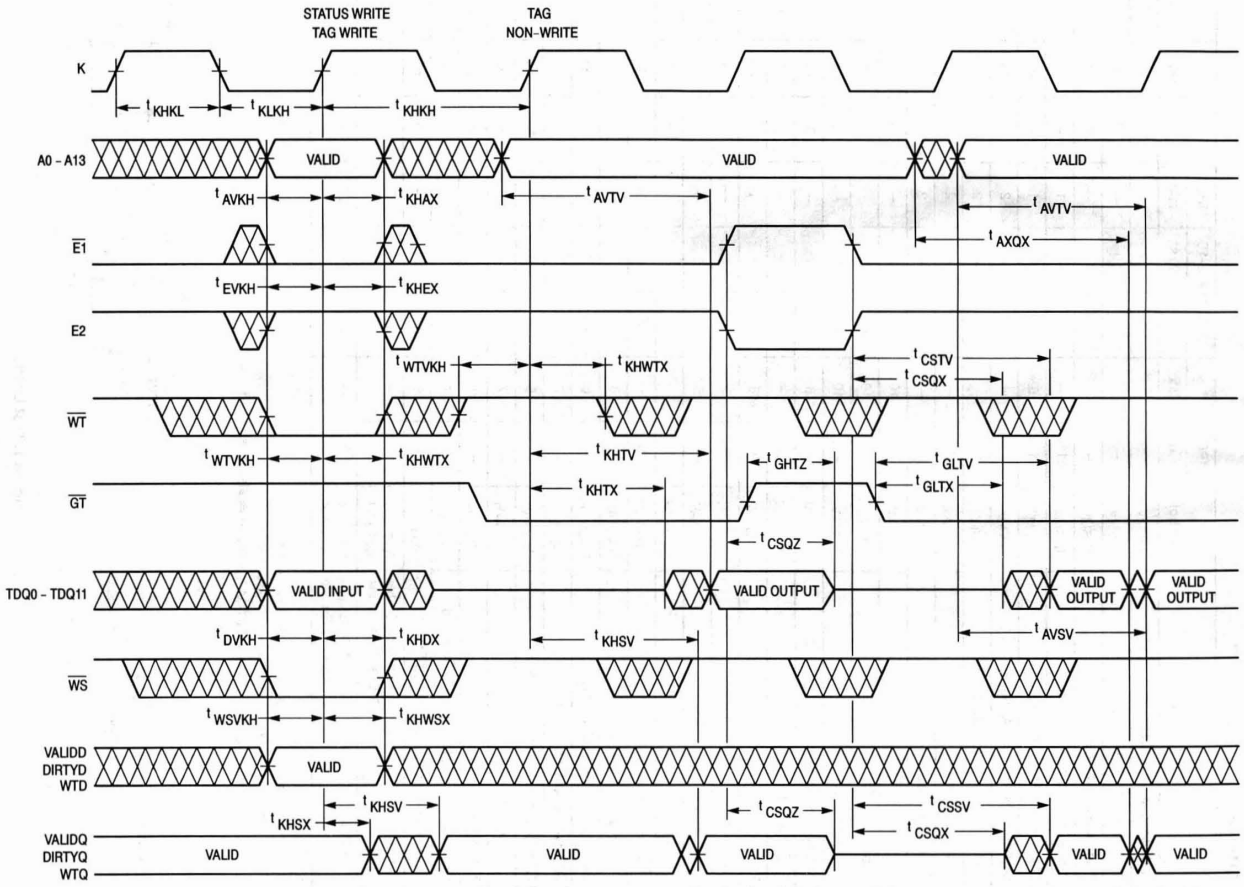
READ/WRITE CYCLE TIMING (See Note 1)

Parameter	Symbol	MPC27T415–9		MPC27T415–10		MPC27T415–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Clock Cycle Time	t_{KHKH}	15	—	15	—	16.6	—	ns	
Address Access Time Tag Bits	t_{AVTV}	—	11	—	12	—	14	ns	
Chip Select Access Time Tag Bits	t_{CSTV}	—	9	—	10	—	12	ns	
Chip Select to Tag and Status Bits in Low–Z	t_{CSQX}	1	—	1	—	1	—	ns	2
Chip Select to Tag and Status Bits in High–Z	t_{CSQZ}	1	6	1	6	1	7	ns	2
Output Enable to Tag Bits Valid	t_{GLTV}	—	6	—	6	—	7	ns	
Output Enable to Tag Bits Low–Z	t_{GLTX}	0	—	0	—	0	—	ns	2
Output Enable to Tag Bits High–Z	t_{GHTZ}	1	6	1	6	1	7	ns	2
Tag and Status Bit Hold from Address Change	t_{AXQX}	2	—	2	—	2	—	ns	
Address Access Time Status Bits	t_{AVSV}	—	9	—	10	—	12	ns	
Chip Select Access Time Status Bits	t_{CSSV}	—	7	—	8	—	10	ns	
Clock High Read to Outputs in Low–Z	t_{KHTX}	1.5	—	1.5	—	1.5	—	ns	2
Clock High Read to Tag Bits Valid	t_{KHTV}	—	10	—	10	—	12	ns	3
Clock High Write to Status Outputs Valid	t_{KHSV}	—	9	—	9	—	10	ns	3
Status Output Hold from Clock High Write	t_{KHSX}	0	—	0	—	0	—	ns	2
Output Enable to Status Bits Valid	t_{GLSV}	—	6	—	6	—	7	ns	
Output Enable to Status Bits High–Z	t_{GHSZ}	1	6	1	6	1	7	ns	
Output Enable to Status Bits Low–Z	t_{GLSX}	0	—	0	—	0	—	ns	
$\overline{WT}$ and $\overline{WS}$ High to $\overline{PWRDN}$ Low	t_{WHPL}	5	—	5	—	5	—	ns	
$\overline{PWRDN}$ High to $\overline{WT}$ and $\overline{WS}$ Active	t_{PHWL}	50	—	50	—	50	—	ns	
Clock Pulse High	t_{KHKL}	4.5	—	4.5	—	5	—	ns	
Clock Pulse Low	t_{KLKH}	4.5	—	4.5	—	5	—	ns	
Setup Times: Address Tag Write Enable Status Write Enable Data In Chip Enable	t_{AVKH} t_{WTVKH} t_{WSVKH} t_{DVKH} t_{EVKH}	3	—	3	—	3	—	ns	
Hold Times: Address Tag Write Enable Status Write Enable Data In Chip Enable	t_{KHAX} t_{KHWTX} t_{KHWSX} t_{KHDX} t_{KHEX}	1.0	—	1.0	—	1.0	—	ns	

NOTES:
1. All Write cycles are synchronous and referenced from rising K.
2. This parameter is sampled and not 100% tested.
3. Addresses are stable prior to K transition high.

5

READ AND WRITE CYCLES



MATCH AND $\overline{TA}$ CYCLE TIMING

Parameter	Symbol	MPC27T415–9		MPC27T415–10		MPC27T415–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Address to MATCH Valid	t_{AVMV}	—	9	—	10	—	12	ns	
Data Input to MATCH Valid	t_{TVMV}	—	9	—	10	—	12	ns	
Chip Select to MATCH Valid	t_{CSMV}	—	9	—	10	—	12	ns	
Chip Select to MATCH in Low–Z	t_{CSMX}	1	—	1	—	1	—	ns	1
Chip Select to MATCH in High–Z	t_{CSMZ}	1	6	1	6	1	7	ns	1
MATCH Valid Hold from Address	t_{AVMX}	2	—	2	—	2	—	ns	
MATCH Valid Hold from Data	t_{TVMX}	2	—	2	—	2	—	ns	
$\overline{TA}$ Valid Hold from Address	t_{AVTAX}	2	—	2	—	2	—	ns	
$\overline{TA}$ Valid Hold from Data	t_{TVTAX}	2	—	2	—	2	—	ns	
Address to $\overline{TA}$ Valid	t_{AVTAV}	—	10	—	11	—	13	ns	
Data Input to $\overline{TA}$ Valid	t_{TVTAV}	—	10	—	11	—	13	ns	
Chip Select Low to $\overline{TA}$ Valid	t_{CSTAV}	—	10	—	11	—	13	ns	
$\overline{TAG}$ Low to $\overline{TA}$ Valid	t_{TAGTAV}	—	6	—	7	—	8	ns	
$\overline{TAG}$ Low to $\overline{TA}$ in Low–Z	t_{TAGTAX}	0	—	0	—	0	—	ns	1
$\overline{TAG}$ High to $\overline{TA}$ in High–Z	t_{TAGTAZ}	1	6	1	6	1	7	ns	1
TAH High to Force $\overline{TA}$ High	t_{TAFTAH}	—	5	—	5	—	6	ns	
TAH Low to $\overline{TA}$ Valid	t_{TAFTAV}	—	5	—	5	—	6	ns	
$\overline{TAD}$ Setup Time	t_{TADVKH}	4	—	4	—	4	—	ns	
$\overline{TAD}$ Hold Time	t_{KHTADX}	1.5	—	1.5	—	1.5	—	ns	
Clock High $\overline{TAD}$ Low to $\overline{TA}$ Low	t_{TADTAL}	—	6	—	7	—	8	ns	
Clock High $\overline{TAD}$ High to $\overline{TA}$ Valid	t_{TADTAV}	—	6	—	7	—	8	ns	
$\overline{GT}$ Low to MATCH and $\overline{TA}$ Invalid	t_{GTML}	—	7	—	7	—	8	ns	
$\overline{GT}$ High to MATCH and $\overline{TA}$ Valid	t_{GTMV}	—	8	—	8	—	10	ns	
TT1 Low to $\overline{TA}$ High	t_{TTLTAH}	—	7	—	7	—	8	ns	2
TT1 High to $\overline{TA}$ Valid	t_{TTHTAV}	—	7	—	7	—	8	ns	2
Clock High Write to MATCH and $\overline{TA}$ Invalid	t_{KHMI}	—	7	—	7	—	8	ns	
Clock High Read to MATCH and $\overline{TA}$ Valid	t_{KHMV}	—	9	—	10	—	12	ns	3
Setup Times: Tag Write Enable Status Write Enable	t_{WTVKH} t_{WSVKH}	3	—	3	—	3	—	ns	
Hold Times: Tag Write Enable Status Write Enable	t_{KHWTX} t_{KHWSK}	1.0	—	1.0	—	1.0	—	ns	

NOTES:
1. This parameter is sampled and not 100% tested.
2. These parameters only apply when SFUNC is low.
3. t_{AVMV}, t_{TVMV}, t_{CSMV}, t_{AVTAV}, t_{TVTAV}, t_{CSTAV} must also be satisfied.

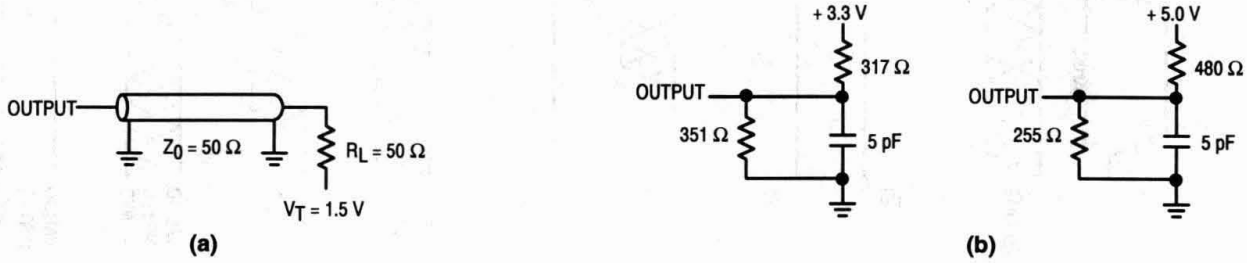
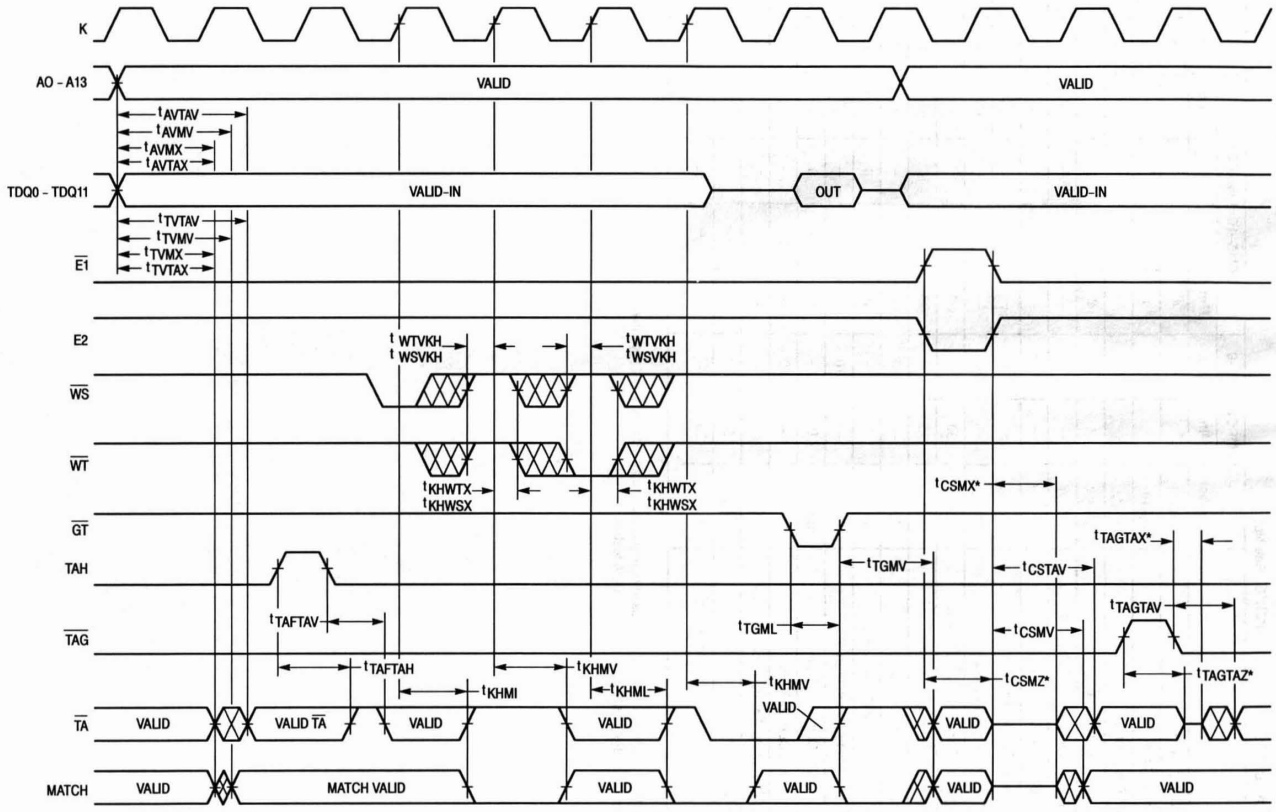


Figure 1. Test Loads

MATCH AND $\overline{TA}$ FUNCTION CYCLES



* Transition is measured plus or minus 200 mV from steady state.

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$\overline{\text{RESET}}$ AND $\overline{\text{PWRDN}}$ CYCLE TIMING (See Note 1)

Parameter	Symbol	MPC27T415–9		MPC27T415–10		MPC27T415–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{\text{RESET}}$ Setup Time	t_{RLKH}	4	—	4	—	4	—	ns	
$\overline{\text{RESET}}$ Hold Time	t_{KHRH}	1	—	1	—	1	—	ns	
Status Bit Reset Time	t_{KHSL}	—	60	—	60	—	70	ns	
Status Bit Hold from $\overline{\text{RESET}}$ Low	t_{KHSX}	2	—	2	—	2	—	ns	
$\overline{\text{RESET}}$ Low to MATCH and $\overline{\text{TA}}$ Invalid	t_{KHMI}	—	10	—	10	—	12	ns	
$\overline{\text{RESET}}$ High to MATCH and $\overline{\text{TA}}$ Valid	t_{RHMV}	—	120	—	120	—	130	ns	
$\overline{\text{RESET}}$ Low to Tag Bits High–Z	t_{KHTZ}	—	10	—	10	—	12	ns	2
$\overline{\text{RESET}}$ High to Tag Bits Low–Z	t_{RHTX}	—	100	—	100	—	110	ns	2
$\overline{\text{PWRDN}}$ Setup Time (when $\overline{\text{RESET}}$ low)	t_{PHKH1}	30	—	30	—	30	—	ns	
$\overline{\text{RESET}}$ High to $\overline{\text{WT}}$ and $\overline{\text{WS}}$ Low	t_{RHWL}	95	—	95	—	105	—	ns	
$\overline{\text{PWRDN}}$ Low to Low Power Mode	t_{PLIL}	—	50	—	50	—	50	ns	2
$\overline{\text{PWRDN}}$ High to Active Power Mode	t_{PHIH}	0	—	0	—	0	—	ns	2
$\overline{\text{PWRDN}}$ Low to Outputs in High–Z	t_{PLQZ}	—	10	—	10	—	12	ns	2
$\overline{\text{PWRDN}}$ High to Outputs in Low–Z	t_{PHQX}	0	—	0	—	0	—	ns	2
$\overline{\text{PWRDN}}$ High to Outputs Valid	t_{PHQV}	—	50	—	50	—	50	ns	
$\overline{\text{WT}}$ and $\overline{\text{WS}}$ High to $\overline{\text{PWRDN}}$ Low	t_{KHPL}	5	—	5	—	5	—	ns	2
$\overline{\text{WT}}$ and $\overline{\text{WS}}$ Setup Time	t_{WVKH}	3	—	3	—	3	—	ns	
$\overline{\text{PWRDN}}$ Setup Time (first write following $\overline{\text{PWRDN}}$ cycle)	t_{PHKH2}	50	—	50	—	50	—	ns	

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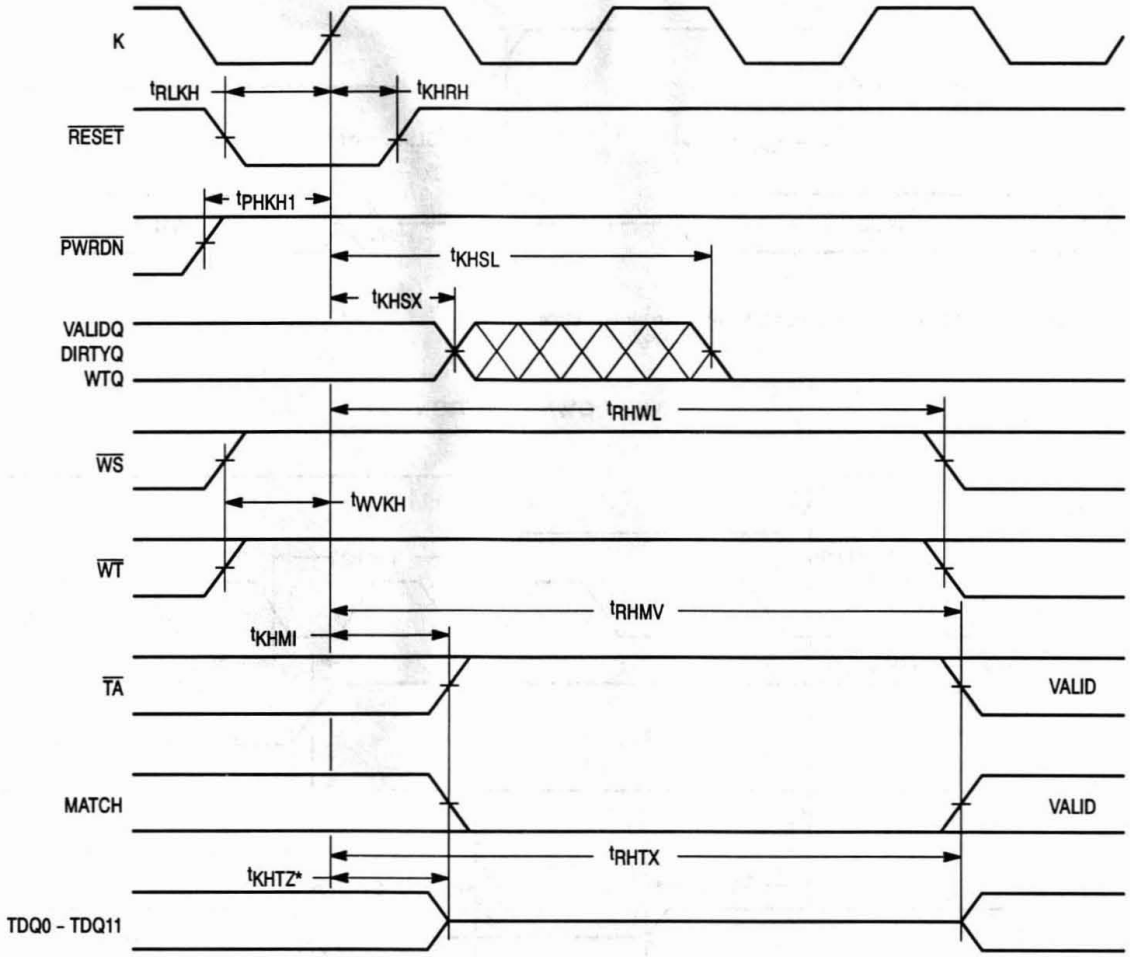
NOTES:
1. $\overline{\text{PWRDN}}$ mode is intended to be used during extended time periods of device inactivity.
2. This parameter is sampled and not 100% tested.

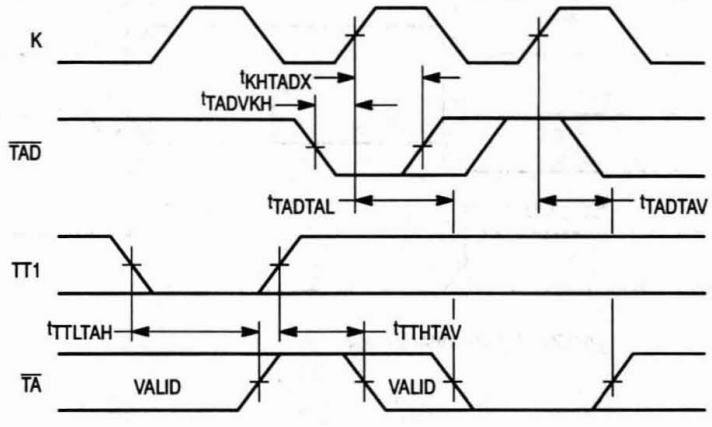
$\overline{\text{RESET}}$ FUNCTION



* Transition is measured plus or minus 200 mV from steady state.

$\overline{\text{TA}}$ AND TT1 SIGNAL

(SFUNC = low)



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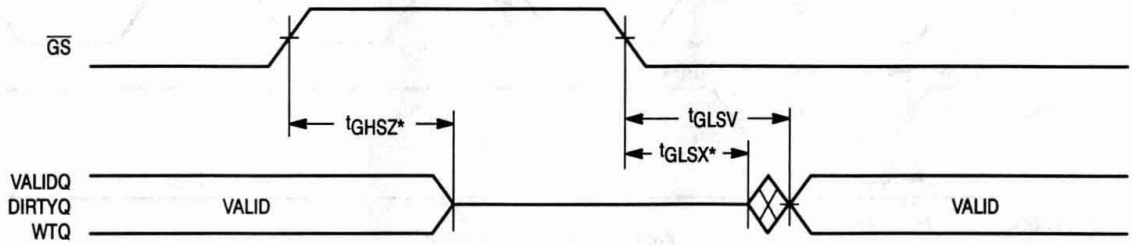
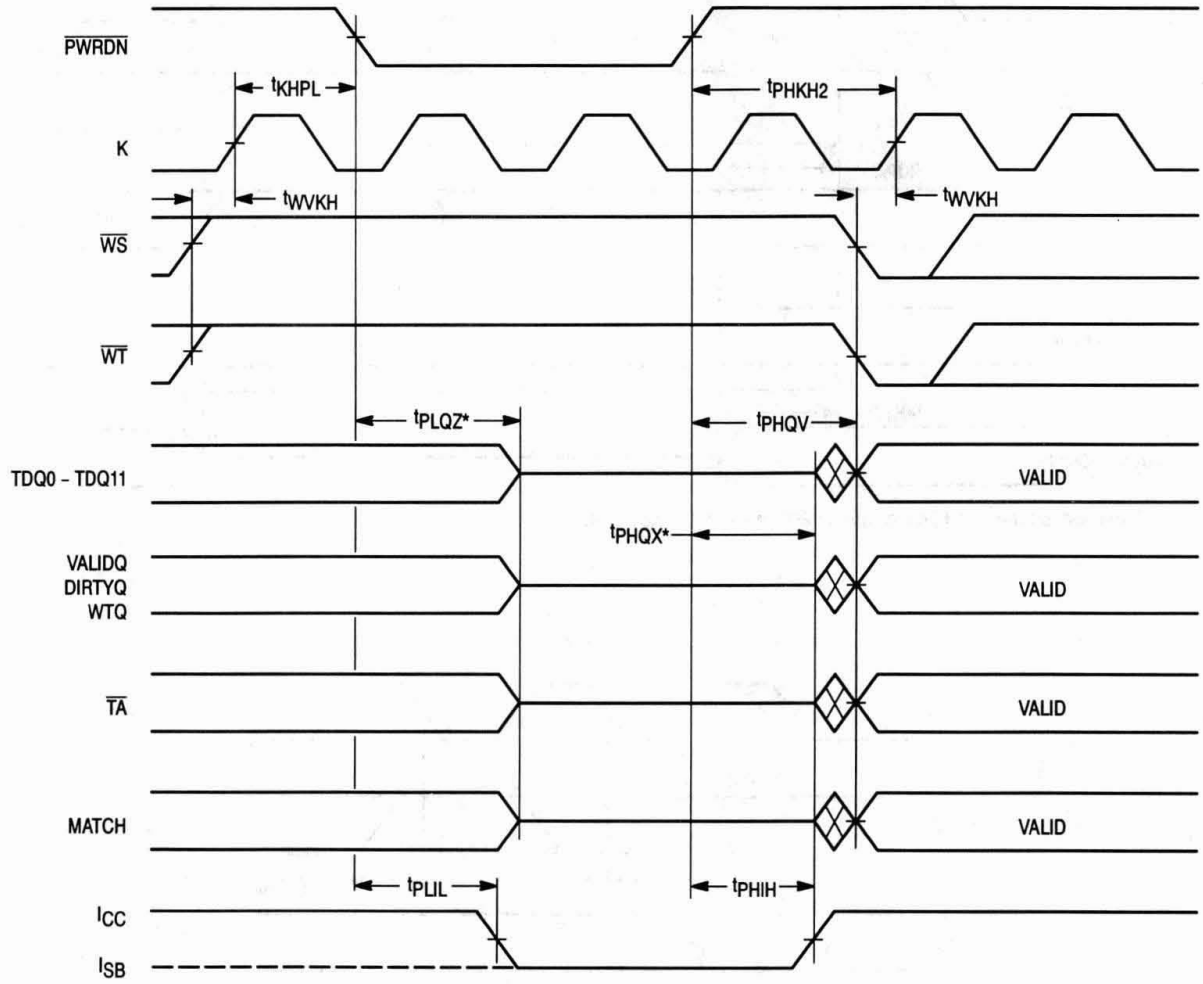
$\overline{GS}$ FUNCTION



* Transition is measured plus or minus 200 mV from steady state.

POWER DOWN FUNCTION



* Transition is measured plus or minus 200 mV from steady state.

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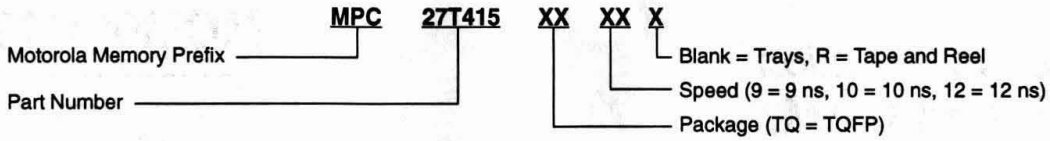
ORDERING INFORMATION
(Order by Full Part Number)


MPC 27T415 XX XX X
Motorola Memory Prefix
Part Number
Blank = Trays, R = Tape and Reel
Speed (9 = 9 ns, 10 = 10 ns, 12 = 12 ns)
Package (TQ = TQFP)

Full Part Numbers — MPC27T415TQ9 MPC27T415TQ10 MPC27T415TQ12
MPC27T415TQ9R MPC27T415TQ10R MPC27T415TQ12R

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MCM69C432

Advance Information

16,383 x 64 CAM

TQ PACKAGE
TQFP
CASE 983A–01

The MCM69C432 is a flexible content–addressable memory (CAM) that can contain 16,383 entries of 64 bits each. The widths of the match field and the output field are programmable, and the match time is designed to be 180 ns. As a result, the MCM69C432 is well suited for datacom applications such as Virtual Path Identifier/Virtual Circuit Identifier (VPI/VCI) translation in ATM switches up to OC12 (622 Mbps) data rates and Media Access Control (MAC) address lookup in Ethernet/Fast Ethernet bridges. The match duty cycle of the MCM69C432 is user defined, with a trade–off between the time between matches and the number of new entries added to the CAM per second.

- 16,383 Entries
- 180 ns Match Time
- Mask Register to "Don't Care" Selected Bits
- Depth Expansion by Cascading Multiple Devices
- 50 MHz Maximum Clock Rate
- Programmable Match and Output Field Widths
- Concurrent Matching of Virtual Path Circuits and Virtual Connection Circuits in ATM Mode
- Separate Ports for Control and Match Operations
- 300 ns Insertion Time if One of Fourteen Entry Queue Locations is Empty
- 80 ms Initialization Time After Fast Insertion (at Power–Up Only)
- Single 3.3 V ± 5% Supply
- 100 Pin TQFP Package
- IEEE Standard 1149.1 Test Port (JTAG)

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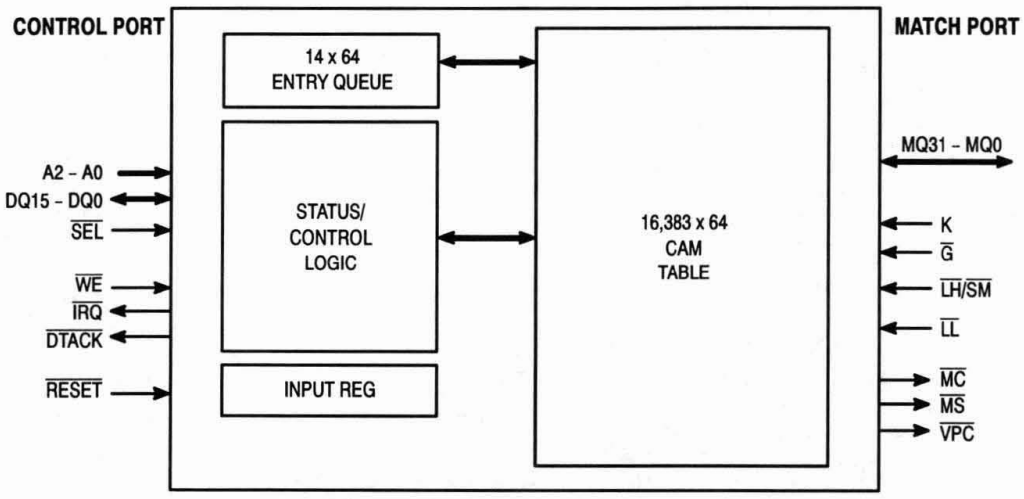
Related Products

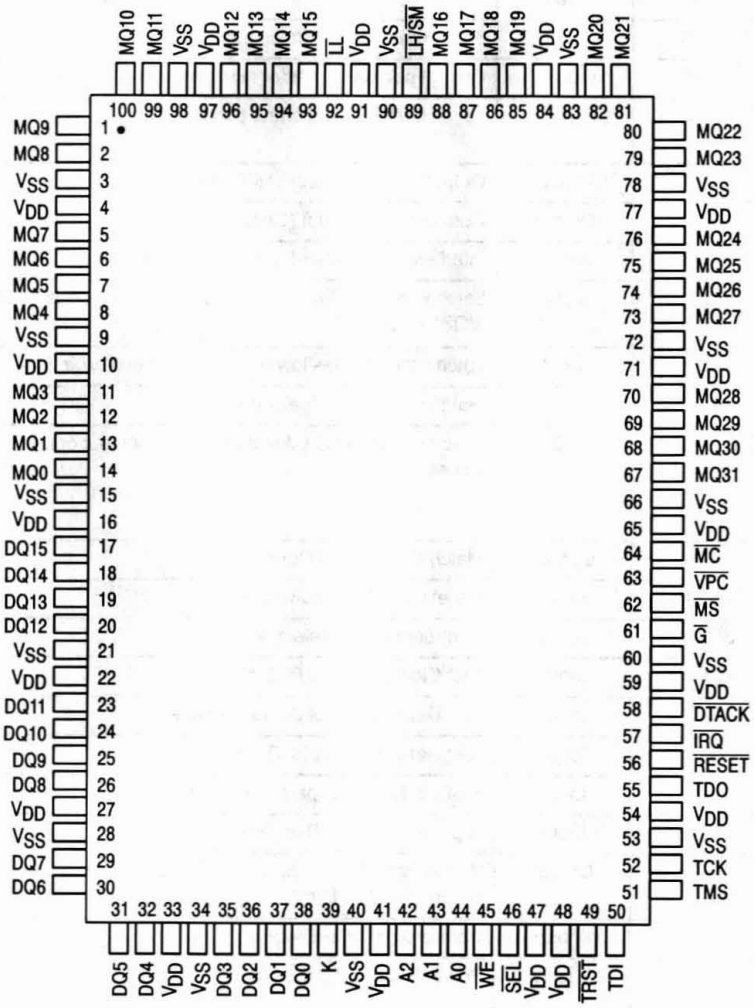
— MCM69Q536, MCM69Q618 (Separate I/O, Dual Address RAMs)
— MCM69D536, MCM69D618 (Dual I/O, Dual Address RAMs)
— MCM67Q709, MCM67Q804, MCM67Q909 (Separate I/O RAMs)
— MCM69C232 (CAM)



This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 1
4/7//97

PIN ASSIGNMENT



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PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
42 – 44	A2 – A0	Input	3–bit control port address bus.
58	$\overline{\text{DTACK}}$	Output	Control port data transfer acknowledge (Open Drain).
17 – 20, 23 – 26, 29 – 32, 35 – 38	DQ15 – DQ0	I/O	16–bit bidirectional control port data bus.
61	$\overline{\text{G}}$	Input	Output Enable control of MQ31 – MQ0.
57	$\overline{\text{IRQ}}$	Output	Control port interrupt (Open Drain).
39	K	Input	Interface Clock, max frequency of 50 MHz.
89	$\overline{\text{LH/SM}}$	Input	Latch High/Start Match. Initiates match sequence on match data present on MQ31 – MQ0.
92	$\overline{\text{LL}}$	Input	Latch Low. Latches low order bits if match width is > 32 bits.
64	$\overline{\text{MC}}$	Output	Match Complete (Open Drain).
1, 2, 5 – 8, 11 – 14, 67 – 70, 73 – 76, 79 – 82, 85 – 88, 93 – 96, 99, 100	MQ31 – MQ0	I/O	32–bit common I/O CAM data. Used for input of match RAM and data RAM values.
62	$\overline{\text{MS}}$	Output	Match Successful (Open Drain).
56	$\overline{\text{RESET}}$	Input	Resets chip to a known state.
46	$\overline{\text{SEL}}$	Input	Control port chip select, active low.
52	TCK	Input	Test Clock, part of JTAG interface.
50	TDI	Input	Test Data In, part of JTAG interface.
55	TDO	Output	Test Data Out, part of JTAG interface.
51	TMS	Input	Test Mode Select, part of JTAG interface.
49	$\overline{\text{TRST}}$	Input	Tap Reset part of JTAG interface.
63	$\overline{\text{VPC}}$	Output	Virtual Path Circuit. Used in ATM mode to indicate a virtual path circuit match has occurred (Open Drain).
45	$\overline{\text{WE}}$	Input	Control port Write Enable.
4, 10, 16, 22, 27, 33, 41, 47, 48, 54, 59, 65, 71, 77, 84, 91, 97	V_{DD}	Supply	Power Supply: 3.3 V ± 5%.
3, 9, 15, 21, 28, 34, 40, 53, 60, 66, 72, 78, 83, 90, 98	V_{SS}	Supply	Ground.

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ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Supply Voltage (see Note 2)	V_{DD}	4.6	V
Voltage Relative to V_{SS} (see Note 2)	V_{in}	– 0.5 to V_{DD} + 0.5 V	V
Output Current per Pin	I_{out}	± 20	mA
Package Power Dissipation (see Note 3)	P_D	—	W
Temperature Under Bias (see Note 3)	T_{bias}	– 10 to 85	°C
Operating Temperature	T_A	0 to 70	°C
Storage Temperature	T_{stg}	– 55 to 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. All voltages are referenced to V_{SS}.
3. Power dissipation capability will be dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V ± 5%, T_J = 20 to 120°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	3.1	3.3	3.5	V
Operating Temperature (Junction)	T_J	20	—	120	°C
Input Low Voltage	V_{IL}	– 0.5*	0	0.8	V
Input High Voltage	V_{IH}	2.2	3	5.5	V

* V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Active Power Supply Current @ 20°C T_J	I_{DD1}	—	TBD	mA
Active Power Supply Current @ 120°C T_J	I_{DD2}	—	TBD	mA
Input Leakage Current (0 V ≤ V_{in} ≤ V_{DD})	$I_{lkg}(I)$	—	TBD	µA
Output Leakage Current (0 V ≤ V_{in} ≤ V_{DD})	$I_{lkg}(O)$	—	TBD	µA
Output Low Voltage (I_{OL} = 8 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4 mA)	V_{OH}	2.4	—	V

PACKAGE THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit
Thermal Resistance Junction to Ambient (200 lfpm, 4 Layer Board) (see Note 2)	$R_{\theta JA}$	TBD	°C/W
Thermal Resistance Junction to Board (Bottom) (see Note 3)	$R_{\theta JB}$	TBD	°C/W
Thermal Resistance Junction to Case (Top) (see Note 4)	$R_{\theta JC}$	TBD	°C/W

NOTES:
1. RAM junction temperature is a function of on–chip power dissipation, package thermal impedance, mounting site temperature, and mounting site thermal impedance.
2. Per SEMI G38–87.
3. Indicates the average thermal impedance between the die and the mounting surface.
4. Indicates the average thermal impedance between the die and the case top surface. Measured via the cold plate method (MIL SPEC–883 Method 1012.1).

CAPACITANCE (Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Max	Unit
Input Capacitance	C_{in}	—	5	pF
I/O Capacitance	$C_{I/O}$	—	8	pF

JUNCTION TO AMBIENT THERMAL CHARACTERISTICS

Board	Air (LFPM)	θ_{JA} (°C/W)	Maximum Ambient Temperature (°C)
1 Layer	0	TBD	TBD
1 Layer	200	TBD	TBD
1 Layer	400	TBD	TBD
4 Layer	0	TBD	TBD
4 Layer	200	TBD	TBD
4 Layer	400	TBD	TBD

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V ± 5%, T_J = 20 to 120°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... Figure 1 Unless Otherwise Noted

CONTROL PORT AND MATCH PORT TIMINGS

(Voltages Referenced to V_{SS} = 0 V, Max's are t_{KHKH} Dependent and Listed Values are for t_{KHKH} = 20 ns)

Parameter	Symbol	Min	Max	Unit	Notes
CONTROL PORT TIMING					
Address Valid to $\overline{SEL}$ Low	t_{AVSL}	0	—	ns	
$\overline{DTACK}$ Low to Address Invalid	t_{DTLAX}	0	—	ns	
Data Valid to Select Low	t_{DVSL}	0	—	ns	
$\overline{DTACK}$ Low to Data Invalid	t_{DTLDX}	0	—	ns	
Output Valid to $\overline{DTACK}$ Low	t_{QVDTL}	2	—	ns	
$\overline{WE}$ Valid to Select Low	t_{WVSL}	0	—	ns	
$\overline{DTACK}$ Low to $\overline{WE}$ High	t_{DTLWH}	0	—	ns	
$\overline{WE}$ High to Output Active	t_{WHQX}	TBD	—	ns	
Select Low to $\overline{DTACK}$ Low	t_{SLDTL}	10	—	ns	1
Select High to $\overline{DTACK}$ High	t_{SHDTH}	10	—	ns	
$\overline{DTACK}$ Low to $\overline{IRQ}$ Low	t_{DTLIL}	TBD	—	ns	
$\overline{IRQ}$ Low to $\overline{IRQ}$ High	t_{ILIH}	20	—	ns	
$\overline{DTACK}$ Low to Select High	t_{DTLSH}	0	—	ns	
$\overline{DTACK}$ High to Select Low	t_{DTHSL}	0	—	ns	
Address Valid to Output Valid	t_{AVQV}	—	8	ns	
Select High to Output Three–State	t_{SHQZ}	—	8	ns	

NOTE:
1. $\overline{DTACK}$ is delayed when a write is attempted during certain operations. See Functional Description.

CONTROL PORT AND MATCH PORT TIMINGS

(Voltages Referenced to V_{SS} = 0 V, Max's are t_{KHKH} Dependent and Listed Values are for t_{KHKH} = 20 ns)

Parameter	Symbol	Min	Max	Unit	Notes
MATCH PORT TIMING					
Clock Cycle Time	t_{KHKH}	20	250	ns	
Clock High Time	t_{KHKL}	8	242	ns	
Clock Low Time	t_{KLKH}	8	242	ns	
Clock High to $\overline{LHSM}$ or $\overline{LL}$ Low	t_{KHLL}	—	7	ns	
Clock High to $\overline{LHSM}$ or $\overline{LL}$ High	t_{KHLH}	—	7	ns	
MQ Input Data Valid to Clock High	t_{MQVKH}	8	—	ns	
Clock High to Match Data Invalid	t_{KHMQX}	2	—	ns	
Clock High to MQ Valid	t_{KHMQV}	—	12	ns	
Clock High to $\overline{MC}$ High	t_{KHMCH}	—	5	ns	
Clock High to $\overline{MC}$ Low	t_{KHMCL}	—	5	ns	
Clock High to $\overline{MS}$ Low	t_{KHMSL}	—	5	ns	
Clock High to $\overline{MS}$ High	t_{KHMSH}	—	5	ns	
Clock High to $\overline{VPC}$ Low	t_{KHVPL}	—	5	ns	
Clock High to $\overline{VPC}$ High	t_{KHVPH}	—	5	ns	
$\overline{G}$ Low to MQ Active	t_{GLMQX}	3.8	—	ns	
$\overline{G}$ High to MQ Three–State	t_{GHMQZ}	—	4	ns	
$\overline{LH/SM}$ Low to $\overline{LH/SM}$ Low	t_{SMSM}	11	—	cycles	

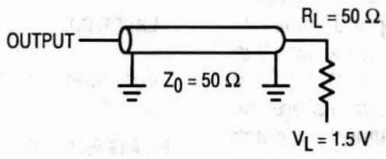
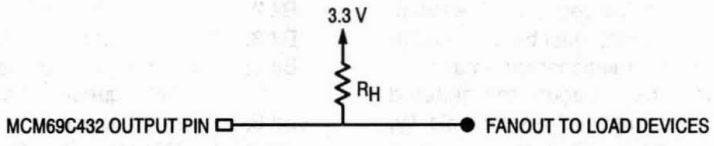


Figure 1. AC Test Load



NOTES:
1. For $\overline{IRQ}$, $\overline{DTACK}$, $\overline{MS}$, $\overline{MC}$ and $\overline{VPC}$, R_H = 200 Ω.
2. If multiple MCM69C432s are used, R_H should be placed as close to the load devices as possible.

Figure 2. Pullup for Open Drain Outputs

FUNCTIONAL DESCRIPTION

The MCM69C432 is a flexible content–addressable memory (CAM) that can contain 16,383 entries of 64 bits each. The widths of the match field and the output field are programmable, and the match time is designed to be 180 ns. As a result, the MCM69C432 is well suited for datacom applications such as Virtual Path Identifier/Virtual Circuit Identifier (VPI/VCI) translation in ATM switches up to OC12 (622 Mbps) data rates and Media Access Control (MAC) address lookup in Ethernet/Fast Ethernet bridges. The match duty cycle of the MCM69C432 is determined by the user, with a trade–off between the match cycle time and the number of entries added to/deleted from the CAM. With the minimum required 40 ns of idle time between matches, a typical value of 555 insertions or deletions per second can be made. See Figure 2 for a graph of the relationship between insertion/deletion pairs and match cycle time.

In its basic operating mode, the MCM69C432 reads a data input word and compares it to all the entries in its CAM table. Whether a match is found or not, the $\overline{MC}$ pin is asserted after the comparisons have been made. If a match is found, the $\overline{MS}$ pin is asserted, and the data associated with the matching entry is output on the MQ bus. If no match is found, the MQ bus remains in a high impedance state to facilitate depth expansion via the cascading of multiple CAMs.

Before the basic operating mode can be entered, however, several start–up functions must be performed. First, the output width and match width must be designated by setting the global–mask register. Second, a choice must be made between buffered entry mode and fast entry mode. Next, the match/output data pairs must be loaded into the table. Depending on the entry mode of choice, the table may have to be initialized. Optionally, the "almost full" point may be set to provide warning of impending table overflow.

The input bits to be compared are defined by the global–mask register. The mask bits that are 0 correspond to the bits that are used in the match operation.Typically, the bits that are used in matching are the high order bits in the 64 bit CAM table entries, and the bits that are used as outputs are the low order bits. While any of the bits can be defined as match bits, the low order 32 bits of an entry are always driven on the MQ bus as output data.

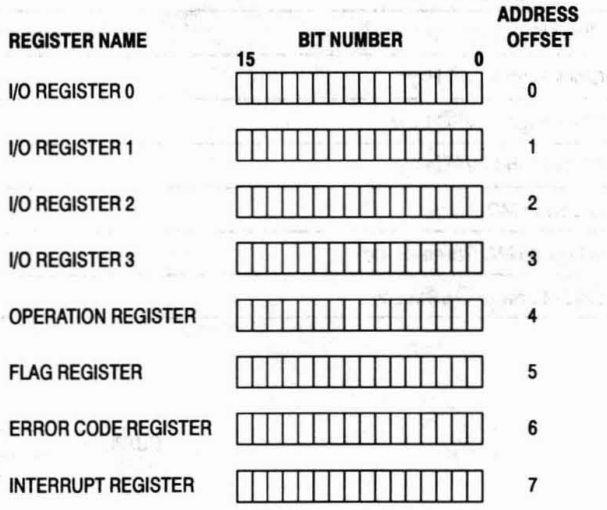
The choice of entry mode is a trade–off between speed of entry and latency before matching operations can begin. In a typical application, the fast entry mode will be used to load the initial values into the CAM table. Subsequently, the initialize–table operation, which takes 80 ms, must be executed to establish the required linkages and relationships among the entries. After match operations have begun, the buffered entry mode should be used to enter new values dynamically; even one addition in fast entry mode will disable matching until the table is reinitialized. Table insertions using the buffered entry mode and the fast entry mode actually take the same amount of time unless the entry queue is full. The capacity of the queue is 14 entries.

After the entry mode choice is made, the table can be loaded. Each 64 bit entry is constructed by writing a 16 bit value to each of the four I/O registers in the MCM69C432. The insertion can then be processed. After all the start–up entries have been loaded into the CAM table, the initialization operation is run if required. Normal matching operations can then begin. A delete operation is provided to remove stale data from the CAM table.

Several error codes are defined in the details of the instruction set. When an error occurs, its corresponding code is written into the error register and the error bit in the flag register is set. The error bit is cleared and the error register is set to $FFFF_{16}$ by the next write to the operation register.

PROGRAMMING MODEL

Three types of registers are accessible through the MCM69C432's control port: I/O registers, an operation register, and result/condition code registers. Each register is sixteen bits in length.



FLAG BIT DEFINITIONS

Bit 0: 1 = At least one interrupt enabled,
0 = No interrupts generated
Bit 1: 1 = Last control port match successful,
0 = Last match unsuccessful
Bit 2: 1 = Table initialized, 0 = Table not initialized
Bit 3: 1 = Buffered entry mode, 0 = Fast entry mode
Bit 4: 1 = Entry queue empty,
0 = Entry queue not empty
Bit 5: 1 = Entry queue full, 0 = Entry queue not full
Bit 6: 1 = CAM table full, 0 = CAM table not full
Bit 7: 1 = Error condition set, 0 = No error
Bit 8: 1 = Table almost full, 0 = Table not almost full
Bit 9: 1 = ATM mode, 0 = Standard mode
Bit 10: 1 = Last operation complete, 0 = Not yet complete

INTERRUPT BIT DEFINITIONS

Bit 0: 1 = Enable interrupt on insert with full entry queue
Bit 1: 1 = Enable interrupt on insert with full table
Bit 2: 1 = Enable interrupt on completion of CHECK–FOR–VALUE instruction
Bit 3: 1 = Enable interrupt on completion of INITIALIZE–TABLE instruction
Bit 4: 1 = Enable interrupt on failed attempt to enter fast entry mode
Bit 5: 1 = Enable interrupt on CAM table reaching almost–full point
Bit 6: 1 = Enable interrupt on fast read with non–empty queue
Bit 7: 1 = Enable interrupt on illegal instruction

INSTRUCTION SET DETAILS

The MCM69C432 is prepared for match operations by writing to data and instruction registers via the control port. In the general case, required data is loaded into I/O registers 0 – 3, then an instruction is issued by writing an operation code to the instruction register. As a result of running an instruction, the CAM table can be modified, bit(s) can be set in the flag register, error codes can be returned in the error code register, and an interrupt can be generated if enabled. For a particular condition to generate an interrupt, the interrupt register bit specific to that condition must be set. The user should verify that the operation–complete bit of the flag register is set before executing the next instruction, if the instruction just executed is one that modifies I/O registers.

Table 1. MCM69C432 Operation Summary

Operation	Description	OP Code (Base 16)
INSERT VALUE	Loads a new entry into the CAM table	0000 or 000F
DELETE VALUE	Removes an entry from the CAM table	0001 or 000E
CHECK FOR VALUE	Runs a match cycle via the control port	0006
INITIALIZE TABLE	Prepares CAM table for matching	000B
FAST ENTRY MODE	Selects entry mode suited for initial CAM table load	0004
BUFFERED ENTRY MODE	Selects entry mode suited for simultaneous loading and matching	0005
SET ATM MODE	Enter mode that provides concurrent VPC/VCC search	0008
RETURN ENTRY COUNT	Determines number of entries in CAM	0003
SET GLOBAL MASK REGISTER	Determines match bits to be checked in a match operation	0002 or 000D
SET ALMOST FULL POINT	Defines CAM almost full condition	0007
SET FAST–READ REGISTER	Defines table entry that is output by the fast read operation	0009
FAST READ	Outputs one CAM table entry	000A

5

INSERT VALUE

This instruction is used to load a new match/output value into the CAM. The contents of I/O registers 0 – 3 are concatenated, with bit 15 of register 3 as the most significant bit, and bit 0 of register 0 as the least significant bit.

If the MCM69C432 is running in buffered entry mode, the resulting 64 bit value is written to the first available location in the entry queue, and is immediately available for matching. If a buffered insert–value instruction is attempted when the entry queue is full (indicated by bit 5 of the flag register = 1), no value is written, an error code of $FFF8_{16}$ is returned in the error code register, and the error–condition flag (bit 7) is set in the flag register. An interrupt is generated, if enabled by bit 0 of the interrupt register being set.

If the MCM69C432 is running in fast entry mode, the concatenated 64 bit value is written directly to the CAM array. If an insert–value instruction is attempted when in fast entry mode and the table is full, no value is written, an error code of $FFF9_{16}$ is returned in the error code register, and the error–condition flag (bit 7) is set in the flag register. (The table–full condition is indicated by bit 6 of the flag register being set.) An interrupt is generated, if enabled by bit 1 of the interrupt register being set.

Only one entry is allowed for a given match pattern. If an entry is made in the table that duplicates an existing match pattern, it will overwrite the entry already in the CAM table, if the CAM is in buffered entry mode. The user must ensure that no entries with the same match pattern are inserted in fast entry mode.

DELETE VALUE

This instruction is used to remove a match/output value from the CAM. The contents of I/O registers 0 – 3 are concatenated, with bit 15 of register 3 as the most significant bit, and bit 0 of register 0 as the least significant bit. The bits that have a 0 in the corresponding bit of the global–mask register are used to find a matching entry in the CAM table. If such an entry is found, it is invalidated. Note that any bit that is not a

match bit as defined by the mask register is ignored for this operation. The operation of the MCM69C432 guarantees that no more than one matching entry can exist in the table, unless they were accidently loaded using fast entry mode. This must be avoided by the user, as the results of subsequent matches and deletes will be undefined.

Example: I/O Register 0 = 3020_{16}
I/O Register 1 = 0000_{16}
I/O Register 2 = $543A_{16}$
I/O Register 3 = $FE55_{16}$
Concatenated value = $FE55543A0000302_{16}$
Global Mask Register = $C0000000FFFFFFFF_{16}$

Of the high–order 32 bits, the rightmost 30 bits are cared by the global–mask register. Therefore, the MCM69C432 will delete an entry, if it exists, which has a value of $3E55543A_{16}$ in bits 61 – 32.

CHECK FOR VALUE

This instruction checks for a matching value in the CAM table. The contents of I/O registers 0 – 3 are concatenated, with bit 15 of register 3 as the most significant bit, and bit 0 of register 0 as the least significant bit. The bits that have a 0 in the corresponding bit of the global–mask register are used to find a matching entry in the CAM table. If such an entry is found, the last–match–successful bit of the flag register is set. In addition, the matching entry is written to I/O registers 0 – 3, with bit 15 of register 3 as the most significant bit, and bit 0 of register 0 as the least significant bit

If no match is found, the last–match–successful bit is cleared. An interrupt is generated regardless of the result, if enabled by bit 2 of the interrupt register, when the operation has been completed. The operation of the MCM69C432 guarantees that no more than one matching entry can exist in the table. If uninterrupted by match port activity, the check for value instruction will finish in 8 clock cycles.

INITIALIZE TABLE

If fast entry mode has been used to load the CAM table, the initialize–table operation must be used to establish the needed relationships and linkages between the entries in the table before matching can proceed. Upon completion, this operation sets the table–initialized bit in the flag register, and generates an interrupt if enabled by bit 3 of the interrupt register. It also sets the buffered entry mode bit in the flag register. This operation makes the programming model's registers read–only for up to 80 ms after the acknowledgment of the op code write cycle.

FAST ENTRY MODE

This instruction is used to enter the fast–entry mode. When the MCM69C432 is in this mode, insert–value operations bypass the entry queue and write new table entries directly to the CAM table. The fast–entry mode can only be entered while the entry queue is empty, as reflected by the queue–empty flag being set (bit 4 of the flag register.) If this operation is attempted while the entry queue is not empty, the value $FFFA_{16}$ is written to the error code register, the error–condition flag (bit 7) is set in the flag register, and an interrupt is generated if enabled by bit 4 of the interrupt register.

If this mode is used to enter data, the initialize–table operation must be executed before matching operations can begin. The entry–mode bit and the table–initialized bit of the flag register are cleared by this operation.

BUFFERED ENTRY MODE

This instruction is used to enter the buffered–entry mode. When the MCM69C432 is in this mode, insert–value and delete–value operations utilize the entry queue. This mode can be entered at any time. Table entries are available for match operations immediately, without running the initialize–table operation, if all entries are made in this mode. Note that if both modes have been used to input data, none of the entries are available for matching until the initialize–table operation is executed. Conflicting table and queue values are resolved in favor of the latest entry in the queue. For example, if there is an entry in the CAM, a corresponding delete–entry in the queue, and a later insert–entry in the queue (all with the same match data), the queued insert–entry will return a match value.

RETURN ENTRY COUNT

This operation is used to determine the number of valid entries in the MCM69C432. The value is returned in I/O register 0, and reflects the sum of the number of valid entries in the CAM table and the inserts in the entry queue.

SET GLOBAL MASK REGISTER

This operation is used to indicate the bits to be used in performing matches. A 1 indicates that a bit should be ignored in the match operation, while a 0 indicates that a bit should be used in the match operation.

When this operation is executed, the contents of I/O registers 0 – 3 are concatenated, with bit 15 of register 3 as the most significant bit, and bit 0 of register 0 as the least significant bit. The resulting 64 bit value is written to the global–mask register.

This operation should be executed before entering required values into the CAM table. Otherwise, the initialize–table instruction must be executed if the global mask register is changed after data is loaded into the CAM.

SET ALMOST–FULL POINT

This operation is used to define the "almost–full" condition in the CAM table. The 14 low–order bits of I/O register 0 are copied to the almost–full–point register. If an entry is added to the MCM69C432 (via the insert–value operation) that causes the valid–entry count to equal the almost–full–point, then bit 8 of the flag register is set, and an interrupt is generated if enabled by bit 5 of the interrupt register. The value of the almost–full register can be changed dynamically during match operations. For example, it could first be set to 2048 to generate an interrupt when the table is half full. When that point is reached, the register could be reprogrammed to 3072 to provide warning that the table has become three–quarters full. The almost–full interrupt is generated, if enabled, based on the number of entries in the CAM table. Entries in the queue are not included in the count.

SET FAST–READ REGISTER VALUE

This operation defines the table address that is output by the fast read operation. The least significant 14 bits of I/O register 0 are copied to the register. The queue must be empty when this instruction is executed.

FAST READ

This operation is used to output the contents of one entry in the CAM table. The fast–read register is used to specify the appropriate entry, and is then auto–incremented. As a result, successive execution of multiple fast–read operations will provide access to contiguous entries in the CAM table.

The CAM entry is copied to I/O registers 0 – 3, with bit 15 of register 3 as the most significant bit, and bit 0 of register 0 as the least significant bit.

The fast–read instruction can only be executed while the entry queue is empty, as reflected by the queue–empty flag being set (bit 4 of the flag register.) If this operation is attempted while the entry queue is not empty, the value $FFFC_{16}$ is written to the error code register, the error–condition flag (bit 7) is set in the flag register, and an interrupt is generated if enabled by bit 7 of the interrupt register.

SET ATM MODE

When the MCM69C432 is placed in ATM mode, it provides simultaneous searching for virtual path circuits (VPCs) and virtual connection circuits (VCCs). A VCC is detected when both the virtual path identifier (VPI) and the virtual circuit identifier (VCI) of an incoming cell match an entry in the CAM. A VPC match occurs when the VPI of an incoming cell matches the VPI field of a CAM entry that has all 1s as its VCI. A VPC match is signalled by the assertion of the $\overline{VPC}$ pin along with the $\overline{MS}$ pin. At 50 MHz, a match is completed in 180 ns, whether the applied VPI/VCI belongs to a VCC or a VPC.

The VCI match field must be defined as bits 32 – 47 of each entry. The VPI match data must occupy bits 48 – 59. The VPI can be limited to bits 48 – 55, if the switch handles only User–Network Interface (UNI) protocols. The mask register should be used to "don't care" any unused bits beyond the VPI field. Entering ATM mode will set bit 9 of the flag register.

To load a VPC into the CAM table, the desired VPI value is written (right justified) to I/O register 3, $FFFF_{16}$ is written to I/O register 2 as the VCI field, the upper half of the desired output word is written to I/O register 1, and the lower half of the desired output word is written to I/O register 0. Then, the "INSERT VALUE" instruction is written to the operation register.

When performing a match operation, the VCI must be placed in bits 0 – 15 of the MQ port. The VPI is expected on bits 16 – 27, or bits 16 – 23 in the UNI case.

Buffered entry mode insertions and deletions are modified in the following way when the MCM69C432 is in ATM mode. If you try to add a VCC with the same VPI as an existing VPC, you overwrite the VPC. If you try to delete a VCC when the VCC is not in the table, but a VPC with that VPI is in the table, the VPC will be deleted.

MATCH CYCLE TIME

At 50 MHz, the MCM69C432 completes a match 180 ns after assertion of the $\overline{SM}$ signal. If minimal entries need to be added to or deleted from the CAM, the part can be cycled at 220 ns. In other words, $\overline{SM}$ can be asserted again immediately after the completion of a match operation and data output.

However, idle time is required between matches to allow insertions or deletions. The worst case occurs if an entry with a match data value smaller than any other entry in the CAM is continually added and dropped from the table. The number of insertion/deletion pairs per second in this scenario is shown versus match cycle time as the curve labeled "Worst Case" in Figure 3. As shown, a match cycle time of 220 ns allows for 139 insertion/deletion pairs per second. Note that this analysis is based on a 50 MHz input clock. Values should be derated in proportion to any decrease in clock speed. For example, at 25 MHz, twice as much idle time is required to achieve the same number of insertion/deletion pairs per second.

A more typical case would consist of either randomly placed insertions and deletions in the CAM table (as determined by the magnitude of the match field), or when insertions occur at one end of the table and deletions occur at the other end. The number of insertion/deletion pairs per second in this scenario is shown versus match cycle time as the curve labeled "Typical" in Figure 3. As shown, a match cycle time of 220 ns allows for 277 insertion/deletion pairs per second.

For any match cycle time ≥ 220 ns and evenly divisible by 20 ns (220 ns, 240 ns, ...), the time to perform a worst–case insertion *or* deletion is equal to 327,680* MCT/(MCT – 200) ns at 50 MHz, where MCT is the match cycle time in nanoseconds. In general, the time for an insertion or deletion is proportional to its distance from the end of the CAM table. That is, entries with the largest match values take the least time to insert or delete, while entries with the smallest values take the most time.

Therefore, the effective rate of insertion and deletion is maximized if the longest–lived entries are placed near the beginning of the table and the shortest–lived entries are placed near the end of the table. For an ATM application, this would correspond to the assignment of small VPI values to permanent virtual circuits and large VPI values to switched virtual circuits.

Note that at start–up, when entries are loaded into the CAM via the fast–entry mode, the process is dominated by the time it takes to execute the initialization instruction that follows. The resulting effective rate of loading the CAM at start–up is approximately 240,000 entries per second.

$\overline{RESET}$

Asserting $\overline{RESET}$ removes all entries from the CAM table and entry queue. The flag register is set to $1C_{16}$ (setting the queue empty, buffered entry mode, and table initialized bits). The error register is set to $FFFF_{16}$, indicating no errors. Finally, the almost full register is set to $3FFF_{16}$.

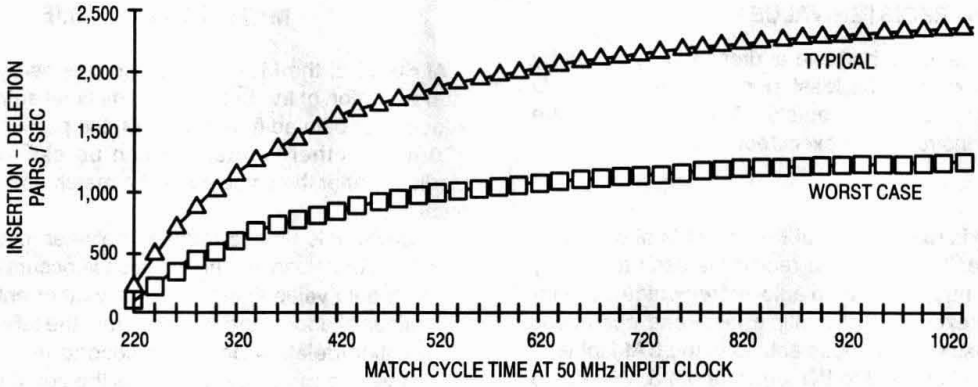


Figure 3. Connections per Second vs Match Cycle Time

TIMING OVERVIEW

CONTROL PORT

The control port of the MCM69C432 is asynchronous. Data transfers, both read and write, are initiated by the assertion of the $\overline{SEL}$ signal. Address values should be valid, and $\overline{WE}$ should be high, when $\overline{SEL}$ is asserted to begin a read cycle. All values (address, $\overline{WE}$, and $\overline{SEL}$) should be held until the MCM69C432 asserts $\overline{DTACK}$ to signal the end of the read cycle.

Address and data values should be valid, and $\overline{WE}$ should be low, when $\overline{SEL}$ is asserted to begin a write cycle. Address, data, $\overline{WE}$, and $\overline{SEL}$ values should be held until the MCM69C432 asserts $\overline{DTACK}$ to signal the end of the write cycle.

MATCH PORT

The MCM69C432's match port is synchronous in operation. When the match width is ≤ 32 bits, a match cycle can be initiated by presenting the match data on MQ31 – MQ0 and asserting the $\overline{LH}/\overline{SM}$ signal with the appropriate setup time relative to the rising edge of the clock. The assertion of the $\overline{MC}$ output signifies the completion of the match cycle. If a match has been found, the $\overline{MS}$ output is also asserted. If the match is a virtual path circuit match in ATM mode, the $\overline{VPC}$ output will be asserted with the $\overline{MS}$ output. Output data, if any, is enabled by the assertion of the $\overline{G}$ input.

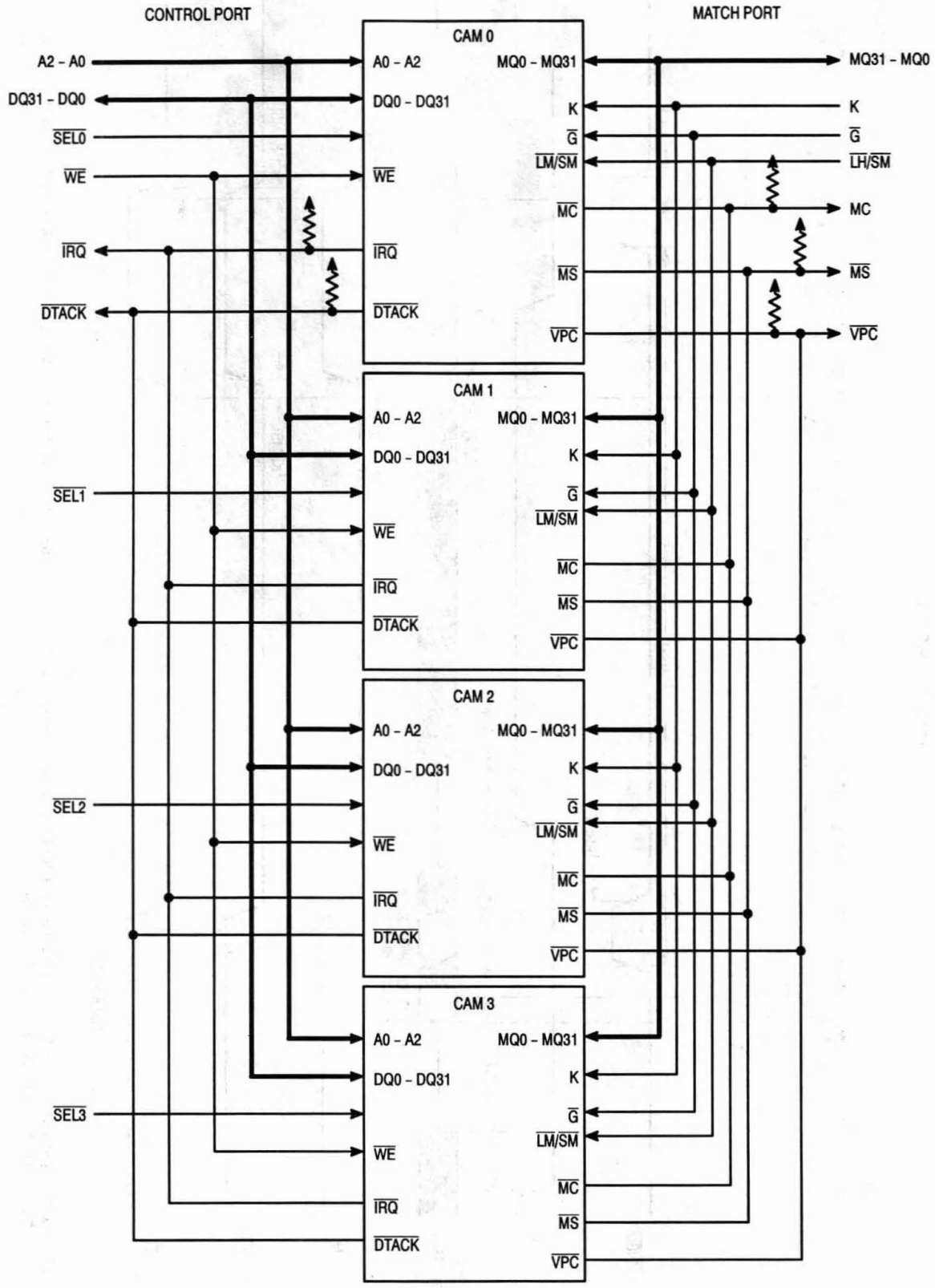
If the match width is greater than 32 bits, the lower bits are first latched into the MCM69C432 by the $\overline{LL}$ input. The match cycle is then initiated as specified in the previous paragraph.

DEPTH EXPANSION

Multiple CAMs can be cascaded to increase the depth of the match table. The hardware requirements are very straightforward, as the following pins on each device are simply wired in parallel: A2 – A0, DQ15 – DQ0, $\overline{WE}$, $\overline{IRQ}$, $\overline{DTACK}$, MQ31 – MQ0, K, $\overline{G}$, $\overline{LH}/\overline{SM}$, $\overline{MC}$, $\overline{MS}$, and $\overline{VPC}$. Four CAMs can be easily cascaded. Simulations show that eight devices can be cascaded if care is taken to minimize the length of the PC board traces connecting the CAMs.

The buffered entry mode prevents multiple matching entries in a single CAM. The check for value instruction should be used to verify that multiple matching entries will not result from a potential new entry. If a match is found in CAM 1, for example, the new value should be placed in CAM 1, where it will replace the existing entry.

DEPTH EXPANSION EXAMPLE
CASCADING FOUR MCM69C432s FOR A 64K WORD TABLE



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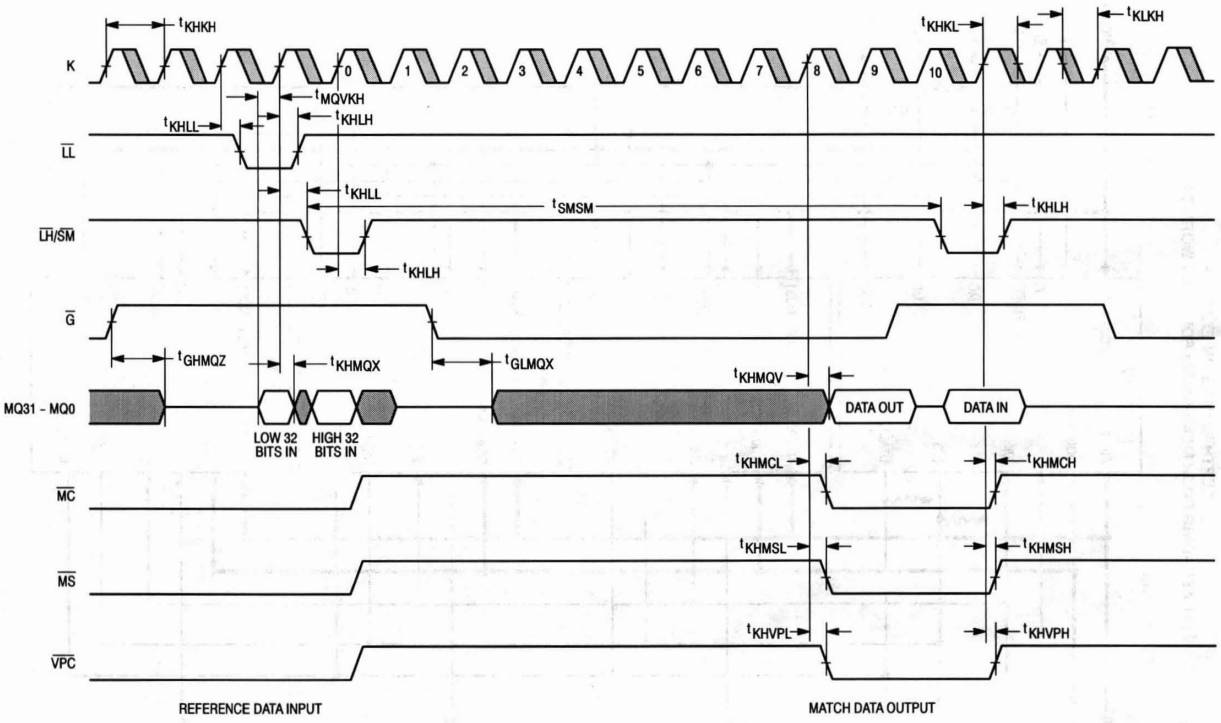
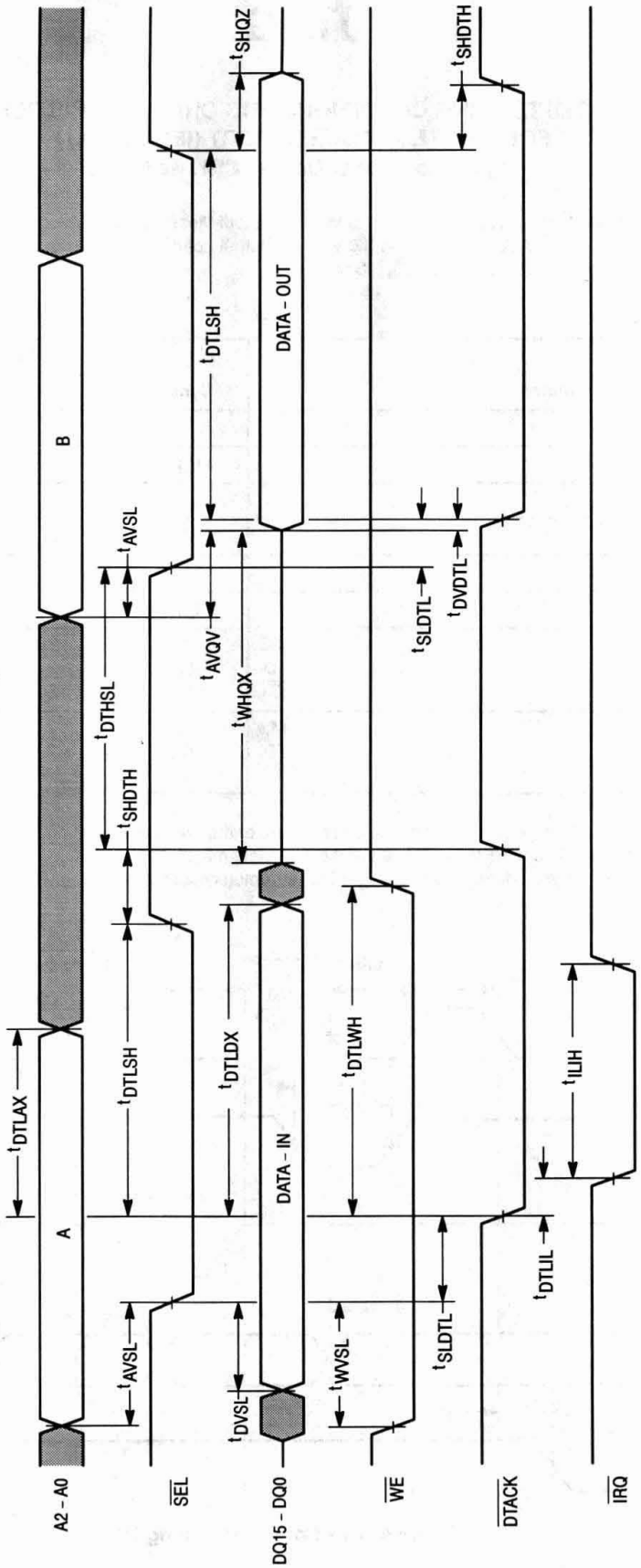
MATCH PORT TIMING



NOTE: In normal operation, all matches would be the same size, i.e., $\overline{LL}$ would either be used in every match cycle or in none. This diagram shows a 64 bit match followed by a 32 bit match in order to illustrate all the key specs.

CONTROL PORT TIMING



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JTAG

AC OPERATING CONDITIONS AND CHARACTERISTICS FOR THE TEST ACCESS PORT (IEEE 1149.1)

(T_J = 20 to + 120°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Measurement Timing Level ..... 1.5 V
Output Load ..... 50 Ω Termination to 1.5 V

TAP CONTROLLER TIMING

Parameter		Symbol	MCM69C432 Min	MCM69C432 Max	Unit	Notes
Cycle Time		t_{CK}	30	—	ns	
Clock High Time		t_{CKH}	12	—	ns	
Clock Low Time		t_{CKL}	12	—	ns	
Clock Low to Output Valid		t_A	5	9	ns	
Clock Low to Output High–Z		t_{CKZ}	0	9	ns	1
Clock Low to Output Active		t_{CKX}	0	9	ns	2, 3
Setup Times:	TMS TDI $\overline{TRST}$	t_S t_{SD} t_{SR}	2 2 2	—	ns	
Hold Times:	TMS TDI $\overline{TRST}$	t_H t_{HD} t_{HR}	2 2 10	—	ns	

NOTES:
1. TDO will High–Z from a clock low edge depending on the current state of the TAP state machine.
2. TDO is active only in the SHIFT–IR and SHIFT–DR state of the TAP state machine.
3. Transition is measured ± 500 mV from steady–state voltage. This parameter is sampled and not 100% tested.

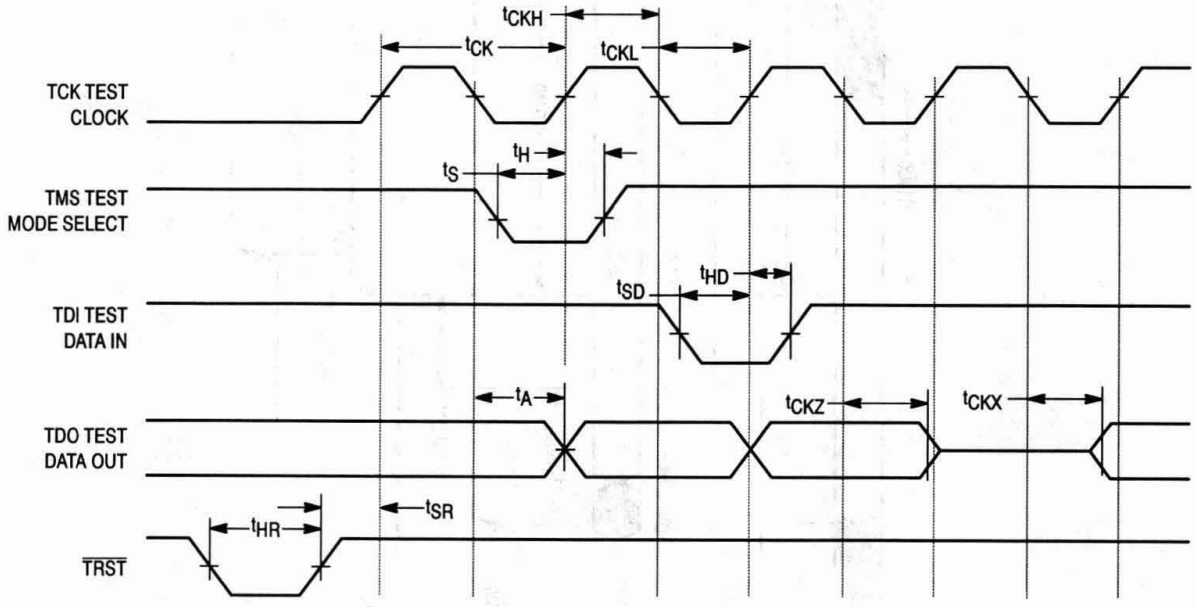

Figure 4. TAP Controller Timing

INSTRUCTION SET

A five pin IEEE Standard 1149.1 Test Port (JTAG) is included on this device. When the TAP (Test Access Port) controller is in the SHIFT–IR state, the instruction register is placed between TDI and TDO. In this state, the desired instruction would be serially loaded through the TDI input. TRST resets the TAP controller to the test–logic reset state. The TAP instruction set for this device are as follows.

STANDARD INSTRUCTIONS

Instruction	Code (Binary)	Description
BYPASS	1111*	Bypass instruction
SAMPLE/PRELOAD	0010	Sample and/or preload instruction
EXTEST	0000	Extest instruction
HIGHZ	1001	High–Z all output pins while bypass register is between TDI and TDO
CLAMP	1100	Clamp output pins while bypass register is between TDI and TDO

* Default state at power–up.

SAMPLE/PRELOAD TAP INSTRUCTION

The SAMPLE/PRELOAD TAP instruction is used to allow scanning of the boundary–scan register without causing interference to the normal operation of the chip logic. The 62–bit boundary–scan register contains bits for all device signal and clock pins and associated control signals. This register is accessible when the SAMPLE/PRELOAD TAP instruction is loaded into the TAP instruction register in the SHIFT–IR state. When the TAP controller is then moved to the SHIFT–DR state, the boundary–scan register is placed between TDI and TDO. This scan register can then be used prior to the EXTEST instruction to preload the output pins with desired values so that these pins will drive the desired state when the EXTEST instruction is loaded. As data is written into TDI, data also streams out TDO which can be used to pre–sample the inputs and outputs.

SAMPLE/PRELOAD would also be used prior to the CLAMP instruction to preload the values on the output pins that will be driven out when the CLAMP instruction is loaded.

EXTEST TAP INSTRUCTION

The EXTEST instruction is intended to be used in conjunction with the SAMPLE/PRELOAD instruction to assist in testing board level connectivity. Normally, the SAMPLE/PRELOAD instruction would be used to preload all output pins. The EXTEST instruction would then be loaded. During EXTEST, the boundary–scan register is placed between TDI and TDO in the SHIFT–DR state of the TAP controller. Once the EXTEST instruction is loaded, the TAP controller would then be moved to the run–test/idle state. In this state, one cycle of TCK would cause the preloaded data on the output pins to be driven while the values on the input pins would be sampled. Note the TCK, not the clock pin (CLK), is used as the clock input while CLK is only sampled during EXTEST. After one clock cycle of TCK, the TAP controller would then be moved to the SHIFT–DR state where the sampled values would be shifted out of TDO (and new values would be shifted in TDI). These values would normally be compared to expected values to test for board connectivity.

Table 2. Sample/Preload Boundary Scan Register Bit Definitions

Bit Number	Bit Pin Name	Bit Pin Number	Pin Type	Bit Number	Bit Pin Name	Bit Pin Number	Pin Type
1	$\overline{G}$	61	Input	32	MQ6	6	I/O
2	$\overline{MS}$	62	Output	33	MQ5	7	I/O
3	$\overline{VPC}$	63	Output	34	MQ4	8	I/O
4	$\overline{MC}$	64	Output	35	MQ3	11	I/O
5	MQ31	67	I/O	36	MQ2	12	I/O
6	MQ30	68	I/O	37	MQ1	13	I/O
7	MQ29	69	I/O	38	MQ0	14	I/O
8	MQ28	70	I/O	39	DQ15	17	I/O
9	MQ27	73	I/O	40	DQ14	18	I/O
10	MQ26	74	I/O	41	DQ13	19	I/O
11	MQ25	75	I/O	42	DQ12	20	I/O
12	MQ24	76	I/O	43	DQ11	23	I/O
13	MQ23	79	I/O	44	DQ10	24	I/O
14	MQ22	80	I/O	45	DQ9	25	I/O
15	MQ21	81	I/O	46	DQ8	26	I/O
16	MQ20	82	I/O	47	DQ7	29	I/O
17	MQ19	85	I/O	48	DQ6	30	I/O
18	MQ18	86	I/O	49	DQ5	31	I/O
19	MQ17	87	I/O	50	DQ4	32	I/O
20	MQ16	88	I/O	51	DQ3	35	I/O
21	$\overline{LH/SM}$	89	Input	52	DQ2	36	I/O
22	$\overline{LL}$	92	Input	53	DQ1	37	I/O
23	MQ15	93	I/O	54	DQ0	38	I/O
24	MQ14	94	I/O	55	A2	42	Input
25	MQ13	95	I/O	56	A1	43	Input
26	MQ12	96	I/O	57	A0	44	Input
27	MQ11	99	I/O	58	$\overline{WE}$	45	Input
28	MQ10	100	I/O	59	$\overline{SEL}$	46	Input
29	MQ9	1	I/O	60	$\overline{RESET}$	56	Input
30	MQ8	2	I/O	61	$\overline{IRQ}$	57	Output
31	MQ7	5	I/O	62	$\overline{DTACK}$	58	Output

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TEST ACCESS PORT PINS

TCK — TEST CLOCK (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

TMS — TEST MODE SELECT (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.

TDI — TEST DATA IN (INPUT)

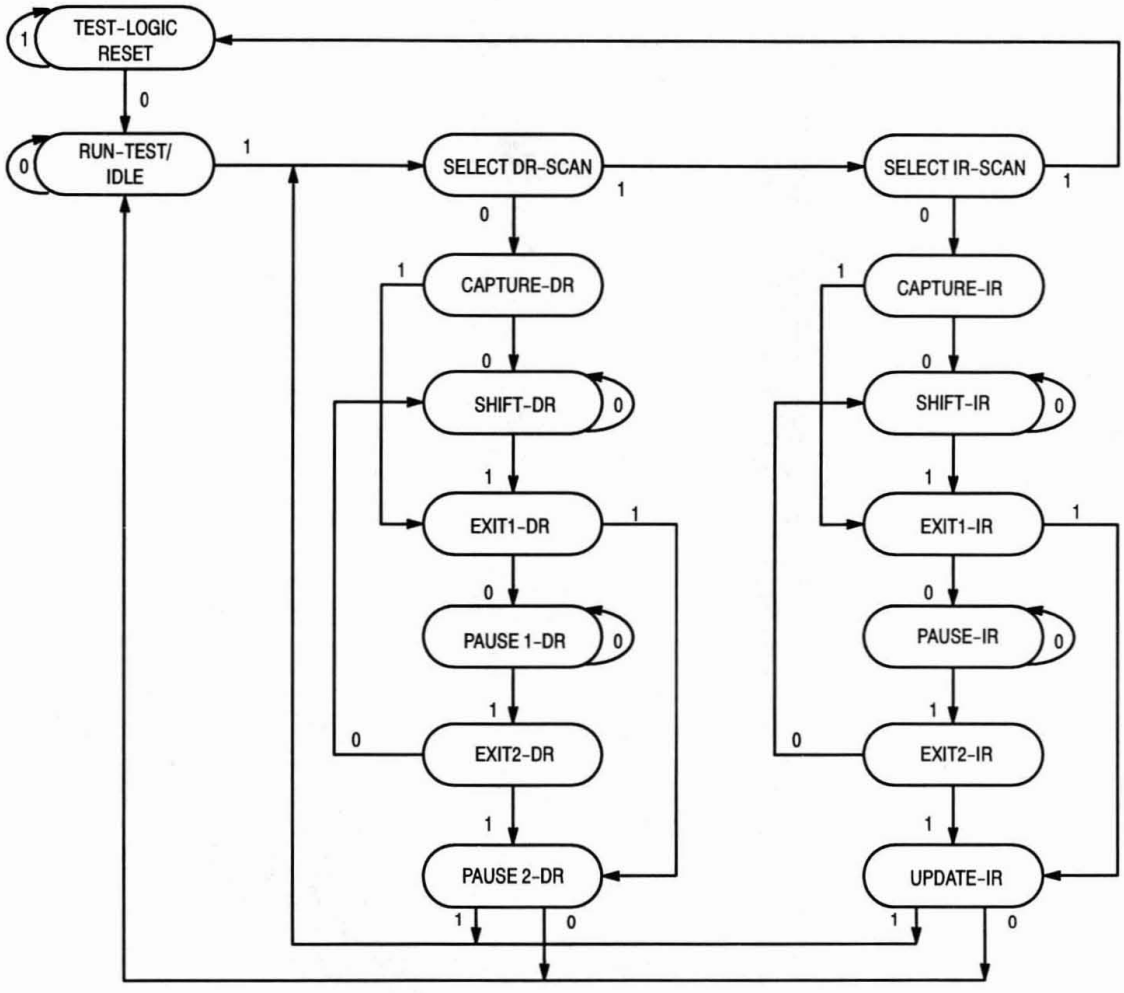
The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (see Figure 5). An undriven TDI pin will produce the same result as a logic one input level.

TDO — TEST DATA OUT (OUTPUT)

Output that is active depending on the state of the TAP state machine (see Figure 5). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

$\overline{\text{TRST}}$ — TAP RESET

This device has a $\overline{\text{TRST}}$ pin. $\overline{\text{TRST}}$ is optional in IEEE 1149.1. Asserting the asynchronous $\overline{\text{TRST}}$ places the TAP controller in test–logic reset state. Test–logic reset state can also be entered by holding TMS high for five rising edges of TCK. This type of reset does not affect the operation of the system logic.



NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 5. TAP Controller State Diagram

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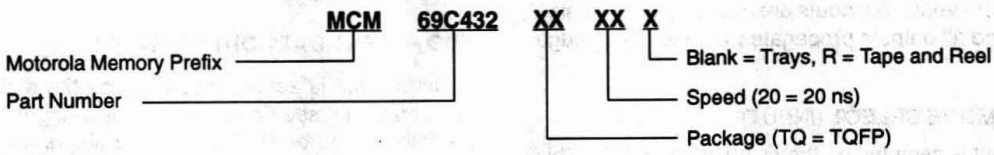
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM69C432TQ20 MCM69C432TQ20R

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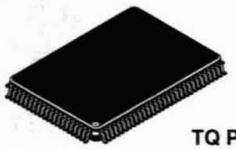
MCM69C232

Advance Information

4K x 64 CAM



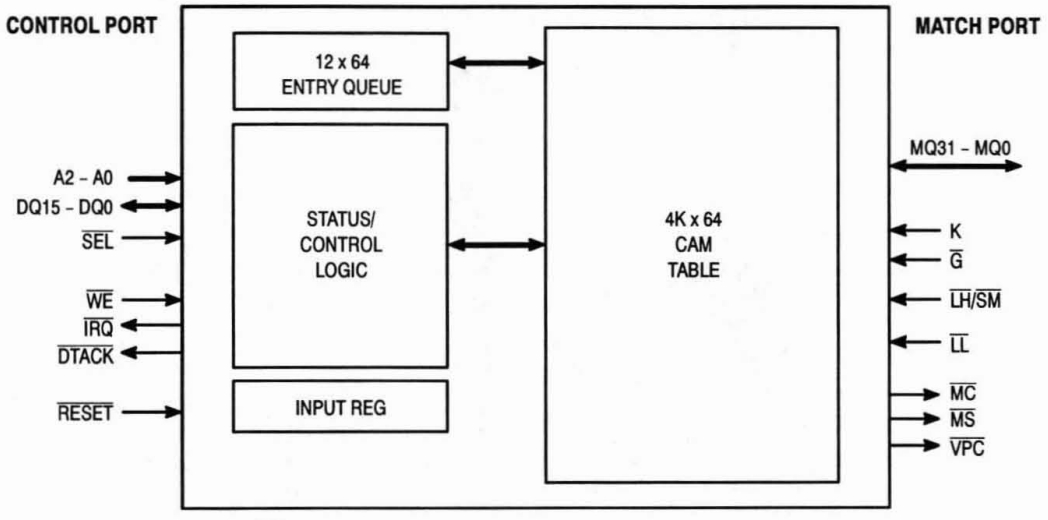
TQ PACKAGE
TQFP
CASE 983A–01

The MCM69C232 is a flexible content–addressable memory (CAM) that can contain 4096 entries of 64 bits each. The widths of the match field and the output field are programmable, and the match time is designed to be 160 ns. As a result, the MCM69C232 is well suited for datacom applications such as Virtual Path Identifier/Virtual Circuit Identifier (VPI/VCI) translation in ATM switches up to OC12 (622 Mbps) data rates and Media Access Control (MAC) address lookup in Ethernet/Fast Ethernet bridges. The match duty cycle of the MCM69C232 is user defined, with a trade–off between the time between matches and the number of new entries added to the CAM per second.

- 4096 Entries
- 160 ns Match Time
- Mask Register to "Don't Care" Selected Bits
- Depth Expansion by Cascading Multiple Devices
- 50 MHz Maximum Clock Rate
- Programmable Match and Output Field Widths
- Concurrent Matching of Virtual Path Circuits and Virtual Connection Circuits in ATM Mode
- Separate Ports for Control and Match Operations
- 200 ns Insertion Time if One of Twelve Entry Queue Locations is Empty
- 12 ms Initialization Time After Fast Insertion (at Power–Up Only)
- Single 3.3 V ± 5% Supply
- 100 Pin TQFP Package
- IEEE Standard 1149.1 Test Port (JTAG)

Related Products

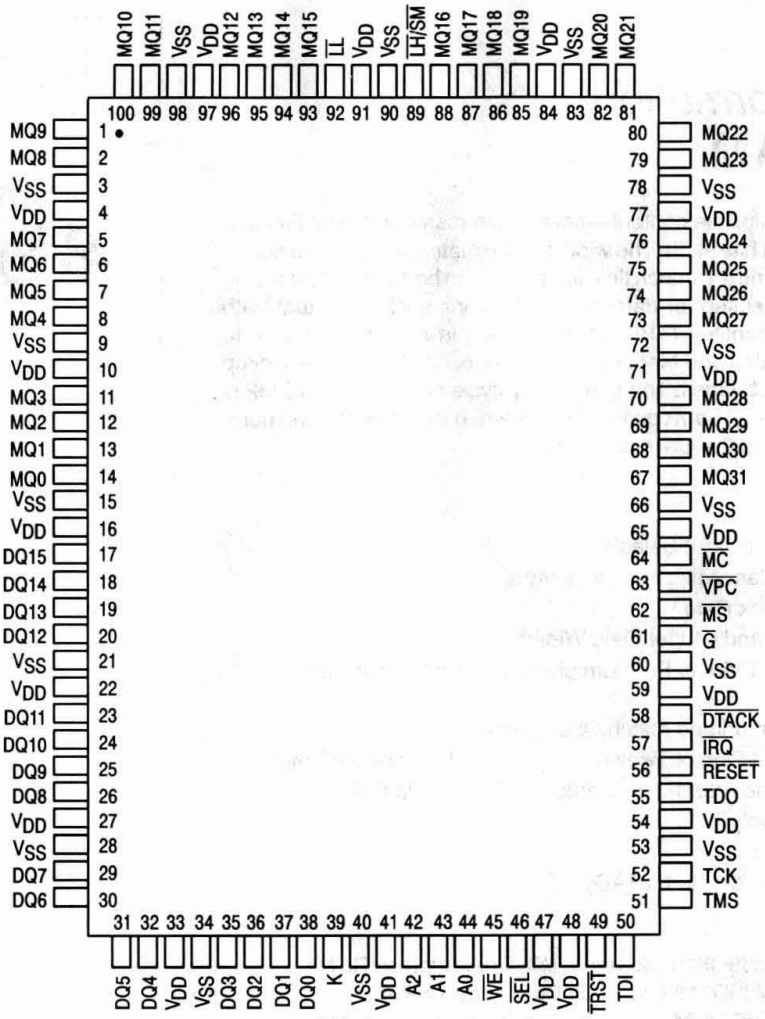
— MCM69Q536, MCM69Q618 (Separate I/O, Dual Address RAMs)
— MCM69D536, MCM69D618 (Dual I/O, Dual Address RAMs)
— MCM67Q709, MCM67Q804, MCM67Q909 (Separate I/O RAMs)
— MCM69C432 (CAM)



This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 2
4/8/97

PIN ASSIGNMENT



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PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
42 – 44	A2 – A0	Input	3–bit control port address bus.
58	$\overline{\text{DTACK}}$	Output	Control port data transfer acknowledge (Open Drain).
17 – 20, 23 – 26, 29 – 32, 35 – 38	DQ15 – DQ0	I/O	16–bit bidirectional control port data bus.
61	$\overline{\text{G}}$	Input	Asynchronous Output Enable control of MQ31 – MQ0.
57	$\overline{\text{IRQ}}$	Output	Control port interrupt (Open Drain).
39	K	Input	Interface Clock, max frequency of 50 MHz.
89	$\overline{\text{LH/SM}}$	Input	Latch High/Start Match. Initiates match sequence on match data present on MQ31 – MQ0.
92	$\overline{\text{LL}}$	Input	Latch Low. Latches low order bits if match width is > 32 bits.
64	$\overline{\text{MC}}$	Output	Match Complete (Open Drain).
62	$\overline{\text{MS}}$	Output	Match Successful (Open Drain).
1, 2, 5 – 8, 11 – 14, 67 – 70, 73 – 76, 79 – 82, 85 – 88, 93 – 96, 99, 100	MQ31 – MQ0	I/O	32–bit common I/O CAM data. Used for input of match RAM and data RAM values.
56	$\overline{\text{RESET}}$	Input	Resets chip to a known state.
46	$\overline{\text{SEL}}$	Input	Control port chip select, active low.
52	TCK	Input	Test Clock, part of JTAG interface.
50	TDI	Input	Test Data In, part of JTAG interface.
55	TDO	Output	Test Data Out, part of JTAG interface.
51	TMS	Input	Test Mode Select, part of JTAG interface.
49	$\overline{\text{TRST}}$	Input	TAP Reset part of JTAG interface.
63	$\overline{\text{VPC}}$	Output	Virtual Path Circuit. Used in ATM mode to indicate a virtual path circuit match has occurred (Open Drain).
45	$\overline{\text{WE}}$	Input	Control port Write Enable.
4, 10, 16, 22, 27, 33, 41, 47, 48, 54, 59, 65, 71, 77, 84, 91, 97	V_{DD}	Supply	Power Supply: 3.3 V ± 5%.
3, 9, 15, 21, 28, 34, 40, 53, 60, 66, 72, 78, 83, 90, 98	V_{SS}	Supply	Ground.

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Supply Voltage (see Note 2)	V_{DD}	4.6	V
Voltage Relative to V_{SS} (see Note 2)	V_{in}	– 0.5 to V_{DD} + 0.5 V	V
Output Current per Pin	I_{out}	± 20	mA
Package Power Dissipation (see Note 3)	P_D	—	W
Temperature Under Bias (see Note 3)	T_{bias}	– 10 to 85	°C
Operating Temperature (see Note 4)	T_A	0 to 70	°C
Storage Temperature	T_{stg}	– 55 to 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. All voltages are referenced to V_{SS}.
3. Power dissipation capability will be dependent upon package characteristics and use environment. See Package Thermal Characteristics.
4. Consult Junction to Ambient Thermal Characteristics table for details and conditions.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V ± 5%, T_J = 20 to 120°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	3.1	3.3	3.5	V
Operating Temperature (Junction)	T_J	20	—	120	°C
Input Low Voltage	V_{IL}	– 0.5*	0	0.8	V
Input High Voltage	V_{IH}	2.0	3	5.5	V

* V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Active Power Supply Current @ 20°C T_J	I_{DD1}	—	575	mA
Active Power Supply Current @ 120°C T_J	I_{DD2}	—	460	mA
Input Leakage Current (0 V ≤ V_{in} ≤ V_{DD})	$I_{lkg}(I)$	—	TBD	µA
Output Leakage Current (0 V ≤ V_{in} ≤ V_{DD})	$I_{lkg}(O)$	—	TBD	µA
Output Low Voltage (I_{OL} = 8 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4 mA)	V_{OH}	2.4	—	V

PACKAGE THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit
Thermal Resistance Junction to Ambient (200 lfpm, 4 Layer Board) (Note 2)	$R_{\theta JA}$	27.1	°C/W
Thermal Resistance Junction to Board (Bottom) (Note 3)	$R_{\theta JB}$	17	°C/W
Thermal Resistance Junction to Case (Top) (Note 4)	$R_{\theta JC}$	9	°C/W

NOTES:
1. RAM junction temperature is a function of on–chip power dissipation, package thermal impedance, mounting site temperature, and mounting site thermal impedance.
2. Per SEMI G38–87.
3. Indicates the average thermal impedance between the die and the mounting surface.
4. Indicates the average thermal impedance between the die and the case top surface. Measured via the cold plate method (MIL SPEC–883 Method 1012.1).

CAPACITANCE (Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Max	Unit
Input Capacitance	C_{in}	—	5	pF
I/O Capacitance	$C_{I/O}$	—	8	pF

JUNCTION TO AMBIENT THERMAL CHARACTERISTICS

Board	Air (LFPM)	θ_{JA} (°C/W)	Maximum Ambient Temperature (°C)
1 Layer	0	40.1	55.8
1 Layer	200	34.7	64.4
1 Layer	400	32.1	68.7
4 Layer	0	30.5	71.1
4 Layer	200	27.1	76.6
4 Layer	400	25.6	79.0

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V ± 5%, T_J = 20 to 120°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... Figure 1 Unless Otherwise Noted

CONTROL PORT AND MATCH PORT TIMINGS

(Voltages Referenced to V_{SS} = 0 V, Max's are t_{KHKH} Dependent and Listed Values are for t_{KHKH} = 20 ns)

Parameter	Symbol	Min	Max	Unit
CONTROL PORT TIMING				
Address Valid to $\overline{SEL}$ Low	t_{AVSL}	0	—	ns
$\overline{DTACK}$ Low to Address Invalid	t_{DTLAX}	0	—	ns
Data Valid to Select Low	t_{DVSL}	0	—	ns
$\overline{DTACK}$ Low to Data Invalid	t_{DTLDX}	0	—	ns
Output Valid to $\overline{DTACK}$ Low	t_{QVDTL}	2	—	ns
$\overline{WE}$ Valid to Select Low	t_{WVSL}	0	—	ns
$\overline{DTACK}$ Low to $\overline{WE}$ High	t_{DTLWH}	0	—	ns
$\overline{WE}$ High to Output Active	t_{WHQX}	TBD	—	ns
Select Low to $\overline{DTACK}$ Low*	t_{SLDTL}	10	—	ns
Select High to $\overline{DTACK}$ High	t_{SHDTH}	10	30	ns
$\overline{DTACK}$ Low to $\overline{IRQ}$ Low	t_{DTLIL}	TBD	—	ns
$\overline{IRQ}$ Low to $\overline{IRQ}$ High	t_{ILIH}	20	—	ns
$\overline{DTACK}$ Low to Select High	t_{DTLSH}	0	—	ns
$\overline{DTACK}$ High to Select Low	t_{DTHSL}	0	—	ns
Address Valid to Output Valid	t_{AVQV}	—	8	ns
Select High to Output Three–State	t_{SHQZ}	—	8	ns

* $\overline{DTACK}$ is delayed when a write is attempted during certain operations. See Functional Description.

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CONTROL PORT AND MATCH PORT TIMINGS

(Voltages Referenced to V_{SS} = 0 V, Max's are t_{KHKH} Dependent and Listed Values are for t_{KHKH} = 20 ns)

Parameter	Symbol	Min	Max	Unit
MATCH PORT TIMING				
Clock Cycle Time	t_{KHKH}	20	250	ns
Clock High Time	t_{KHKL}	8	242	ns
Clock Low Time	t_{KLKH}	8	242	ns
Clock High to $\overline{LHSM}$ or $\overline{LL}$ Low	t_{KHLL}	—	7	ns
Clock High to $\overline{LHSM}$ or $\overline{LL}$ High	t_{KHLH}	—	7	ns
MQ Input Data Setup Time to Clock High	t_{MQVKH}	8	—	ns
Clock High to Match Data Hold Time	t_{KHMQX}	2	—	ns
Clock High to MQ Valid	t_{KHMQV}	—	12	ns
Clock High to $\overline{MC}$ High	t_{KHMCH}	—	5	ns
Clock High to $\overline{MC}$ Low	t_{KHMCL}	—	5	ns
Clock High to $\overline{MS}$ Low	t_{KHMSL}	—	12	ns
Clock High to $\overline{MS}$ High	t_{KHMSH}	—	5	ns
Clock High to $\overline{VPC}$ Low	t_{KHVPL}	—	12	ns
Clock High to $\overline{VPC}$ High	t_{KHVPH}	—	5	ns
$\overline{G}$ Low to MQ Active	t_{GLMQX}	3.8	—	ns
$\overline{G}$ High to MQ High–Z	t_{GHMQZ}	—	4	ns
$\overline{LH/SM}$ Low to $\overline{LH/SM}$ Low	t_{SMSM}	10	—	cycles

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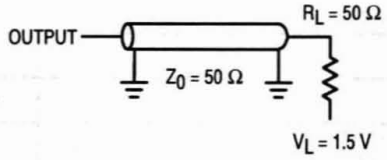
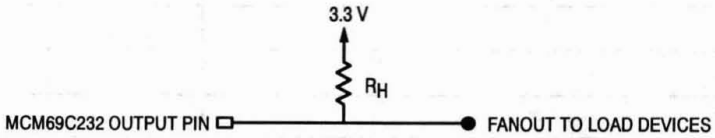


Figure 1. AC Test Loads



NOTES:
1. For $\overline{IRQ}$, $\overline{DTACK}$, $\overline{MS}$, $\overline{MC}$, and $\overline{VPC}$, R_H = 200 Ω.
2. If multiple MCM69C232s are used, R_H should be placed as close to the load devices as possible.

Figure 2. Pullup for Open Drain Outputs

FUNCTIONAL DESCRIPTION

The MCM69C232 is a flexible content–addressable memory (CAM) that can contain 4096 entries of 64 bits each. The widths of the match field and the output field are programmable, and the match time is designed to be 160 ns. As a result, the MCM69C232 is well suited for datacom applications such as Virtual Path Identifier/Virtual Circuit Identifier (VPI/VCI) translation in ATM switches up to OC12 (622 Mbps) data rates and Media Access Control (MAC) address lookup in Ethernet/Fast Ethernet bridges. The match duty cycle of the MCM69C232 is determined by the user, with a trade–off between the match cycle time and the number of entries added to/deleted from the CAM. With the minimum required 40 ns of idle time between matches, a typical value of 2440 insertions or deletions per second can be made. See Figure 3 for a graph of the relationship between insertion/deletion pairs and match cycle time.

In its basic operating mode, the MCM69C232 reads a data input word and compares it to all the entries in its CAM table. Whether a match is found or not, the $\overline{MC}$ pin is asserted after the comparisons have been made. If a match is found, the $\overline{MS}$ pin is asserted, and the data associated with the matching entry is output on the MQ bus. If no match is found, the MQ bus remains in a high impedance state to facilitate depth expansion via the cascading of multiple CAMs.

Before the basic operating mode can be entered, however, several start–up functions must be performed. First, the output width and match width must be designated by setting the global–mask register. Second, a choice must be made between buffered entry mode and fast entry mode. Next, the match/output data pairs must be loaded into the table. Depending on the entry mode of choice, the table may have to be initialized. Optionally, the "almost full" point may be set to provide warning of impending table overflow.

The input bits to be compared are defined by the global–mask register. The mask bits that are 0 correspond to the bits that are used in the match operation.Typically, the bits that are used in matching are the high order bits in the 64 bit CAM table entries, and the bits that are used as outputs are the low order bits. While any of the bits can be defined as match bits, the low order 32 bits of an entry are always driven on the MQ bus as output data.

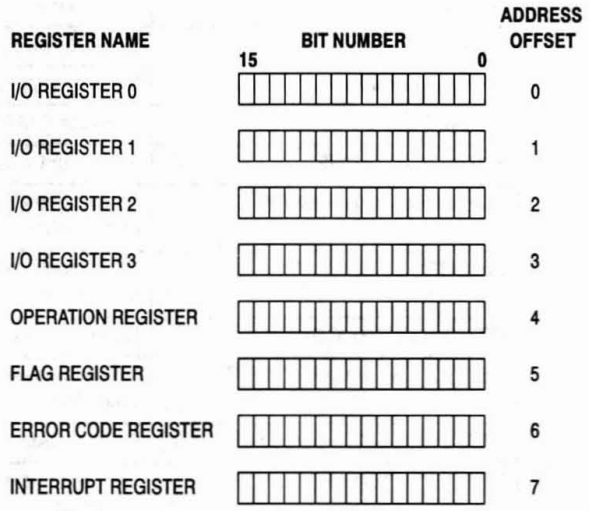
The choice of entry mode is a trade–off between speed of entry and latency before matching operations can begin. In a typical application, the fast entry mode will be used to load the initial values into the CAM table. Subsequently, the initialize–table operation, which takes 12 ms, must be executed to establish the required linkages and relationships among the entries. After match operations have begun, the buffered entry mode should be used to enter new values dynamically; even one addition in fast entry mode will disable matching until the table is reinitialized. Table insertions using the buffered entry mode and the fast entry mode actually take the same amount of time unless the entry queue is full. The capacity of the queue is 12 entries.

After the entry mode choice is made, the table can be loaded. Each 64 bit entry is constructed by writing a 16 bit value to each of the four I/O registers in the MCM69C232. The insertion can then be processed. After all the start–up entries have been loaded into the CAM table, the initialization operation is run if required. Normal matching operations can then begin. A delete operation is provided to remove stale data from the CAM table.

Several error codes are defined in the details of the instruction set. When an error occurs, its corresponding code is written into the error register and the error bit in the flag register is set. The error bit is cleared and the error register is set to $FFFF_{16}$ by the next write to the operation register.

PROGRAMMING MODEL

Three types of registers are accessible through the MCM69C232's control port: I/O registers, an operation register, and result/condition code registers. Each register is sixteen bits in length.



FLAG BIT DEFINITIONS

Bit 0: 1 = At least one Interrupt enabled,
0 = No interrupts generated
Bit 1: 1 = Last control port match successful,
0 = Last match unsuccessful
Bit 2: 1 = Table initialized, 0 = Table not initialized
Bit 3: 1 = Buffered entry mode, 0 = Fast entry mode
Bit 4: 1 = Entry queue empty,
0 = Entry queue not empty
Bit 5: 1 = Entry queue full, 0 = Entry queue not full
Bit 6: 1 = CAM table full, 0 = CAM table not full
Bit 7: 1 = Error condition set, 0 = No error
Bit 8: 1 = Table almost full, 0 = Table not almost full
Bit 9: 1 = ATM mode, 0 = Standard mode
Bit 10: 1 = Last operation complete, 0 = Not yet complete

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INTERRUPT BIT DEFINITIONS

Bit 0: 1 = Enable interrupt on insert with full entry queue
Bit 1: 1 = Enable interrupt on insert with full table
Bit 2: 1 = Enable interrupt on completion of CHECK–FOR–VALUE instruction
Bit 3: 1 = Enable interrupt on completion of INITIALIZE–TABLE instruction
Bit 4: 1 = Enable interrupt on failed attempt to enter fast entry mode
Bit 5: 1 = Enable interrupt on CAM table reaching almost–full point
Bit 6: 1 = Enable interrupt on fast read with non–empty queue
Bit 7: 1 = Enable interrupt on illegal instruction

INSTRUCTION SET DETAILS

The MCM69C232 is prepared for match operations by writing to data and instruction registers via the control port. In the general case, required data is loaded into I/O registers 0 – 3, then an instruction is issued by writing an operation code to the instruction register. As a result of running an instruction, the CAM table can be modified, bit(s) can be set in the flag register, error codes can be returned in the error code register, and an interrupt can be generated if enabled. For a particular condition to generate an interrupt, the interrupt register bit specific to that condition must be set. The user should verify that the operation–complete bit of the flag register is set before executing the next instruction, if the instruction just executed is one that modifies I/O registers.

Table 1. MCM69C232 Operation Summary

Operation	Description	OP Code (Base 16)
INSERT VALUE	Loads a new entry into the CAM table	0000 or 000F
DELETE VALUE	Removes an entry from the CAM table	0001 or 000E
CHECK FOR VALUE	Runs a match cycle via the control port	0006
INITIALIZE TABLE	Prepares CAM table for matching	000B
FAST ENTRY MODE	Selects entry mode suited for initial CAM table load	0004
BUFFERED ENTRY MODE	Selects entry mode suited for simultaneous loading and matching	0005
SET ATM MODE	Enter mode that provides concurrent VPC/VCC search	0008
RETURN ENTRY COUNT	Determines number of entries in CAM	0003
SET GLOBAL MASK REGISTER	Determines match bits to be checked in a match operation	0002 or 000D
SET ALMOST–FULL POINT	Defines CAM almost full condition	0007
SET FAST–READ REGISTER	Defines table entry that is output by the fast read operation	0009
FAST READ	Outputs one CAM table entry	000A

INSERT VALUE

This instruction is used to load a new match/output value into the CAM. The contents of I/O registers 0 – 3 are concatenated, with bit 15 of register 3 as the most significant bit, and bit 0 of register 0 as the least significant bit.

If the MCM69C232 is running in buffered entry mode, the resulting 64 bit value is written to the first available location in the entry queue, and is immediately available for matching. If a buffered insert–value instruction is attempted when the entry queue is full (indicated by bit 5 of the flag register = 1), no value is written, an error code of $FFF8_{16}$ is returned in the error code register, and the error–condition flag (bit 7) is set in the flag register. An interrupt is generated, if enabled by bit 0 of the interrupt register being set.

If the MCM69C232 is running in fast entry mode, the concatenated 64 bit value is written directly to the CAM array. If an insert–value instruction is attempted when in fast entry mode and the table is full, no value is written, an error code of $FFF9_{16}$ is returned in the error code register, and the error–condition flag (bit 7) is set in the flag register. (The table–full condition is indicated by bit 6 of the flag register being set.) An interrupt is generated, if enabled by bit 1 of the interrupt register being set.

Only one entry is allowed for a given match pattern. If an entry is made in the table that duplicates an existing match pattern, it will overwrite the entry already in the CAM table, if the CAM is in buffered entry mode. The user must ensure that no entries with the same match pattern are inserted in fast entry mode.

DELETE VALUE

This instruction is used to remove a match/output value from the CAM. The contents of I/O registers 0 – 3 are concatenated, with bit 15 of register 3 as the most significant bit, and bit 0 of register 0 as the least significant bit. The bits that have a 0 in the corresponding bit of the global–mask register are used to find a matching entry in the CAM table. If such an entry is found, it is invalidated. Note that any bit that is not a match bit as defined by the mask register is ignored for this operation. The operation of the MCM69C232 guarantees that no more than one matching entry can exist in the table,

unless they were accidently loaded using fast entry mode. This must be avoided by the user, as the results of subsequent matches and deletes will be undefined.

Example: I/O Register 0 = 3020_{16}
I/O Register 1 = 0000_{16}
I/O Register 2 = $543A_{16}$
I/O Register 3 = $FE55_{16}$
Concatenated value = $FE55543A00003020_{16}$
Global Mask Register = $C0000000FFFFFFFF_{16}$

Of the high–order 32 bits, the rightmost 30 bits are cared by the global–mask register. Therefore, the MCM69C232 will delete an entry, if it exists, which has a value of $3E55543A_{16}$ in bits 61 – 32.

CHECK FOR VALUE

This instruction checks for a matching value in the CAM table. The contents of I/O registers 0 – 3 are concatenated, with bit 15 of register 3 as the most significant bit, and bit 0 of register 0 as the least significant bit. The bits that have a 0 in the corresponding bit of the global–mask register are used to find a matching entry in the CAM table. If such an entry is found, the last–match–successful bit of the flag register is set. In addition, the matching entry is written to I/O registers 0 – 3, with bit 15 of register 3 as the most significant bit, and bit 0 of register 0 as the least significant bit

If no match is found, the last–match–successful bit is cleared. An interrupt is generated regardless of the result, if enabled by bit 2 of the interrupt register, when the operation has been completed. The operation of the MCM69C232 guarantees that no more than one matching entry can exist in the table. If uninterrupted by match port activity, the check for value instruction will finish in 8 clock cycles.

INITIALIZE TABLE

If fast entry mode has been used to load the CAM table, the initialize–table operation must be used to establish the needed relationships and linkages between the entries in the table before matching can proceed. Upon completion, this operation sets the table–initialized bit in the flag register, and generates an interrupt if enabled by bit 3 of the interrupt register. It also sets the buffered entry mode bit in the flag register. This operation makes the programming model's registers read–only for up to 12 ms after the acknowledgment of the op code write cycle.

FAST ENTRY MODE

This instruction is used to enter the fast–entry mode. When the MCM69C232 is in this mode, insert–value operations bypass the entry queue and write new table entries directly to the CAM table. The fast–entry mode can only be entered while the entry queue is empty, as reflected by the queue–empty flag being set (bit 4 of the flag register.) If this operation is attempted while the entry queue is not empty, the value $FFFA_{16}$ is written to the error code register, the error–condition flag (bit 7) is set in the flag register, and an interrupt is generated if enabled by bit 4 of the interrupt register.

If this mode is used to enter data, the initialize–table operation must be executed before matching operations can begin. The entry–mode bit and the table–initialized bit of the flag register (bit 3) are cleared by this operation.

BUFFERED ENTRY MODE

This instruction is used to enter the buffered–entry mode. When the MCM69C232 is in this mode, insert–value and delete–value operations utilize the entry queue. This mode can be entered at any time. Table entries are available for match operations immediately, without running the initialize–table operation, if all entries are made in this mode. Note that if both modes have been used to input data, none of the entries are available for matching until the initialize–table operation is executed. Conflicting table and queue values are resolved in favor of the latest entry in the queue. For example, if there is an entry in the CAM, a corresponding delete–entry in the queue, and a later insert–entry in the queue (all with the same match data), the queued insert–entry will return a match value.

RETURN ENTRY COUNT

This operation is used to determine the number of valid entries in the MCM69C232. The value is returned in I/O register 0, and reflects the sum of the number of valid entries in the CAM table and the inserts in the entry queue.

SET GLOBAL MASK REGISTER

This operation is used to indicate the bits to be used in performing matches. A 1 indicates that a bit should be ignored in the match operation, while a 0 indicates that a bit should be used in the match operation.

When this operation is executed, the contents of I/O registers 0 – 3 are concatenated, with bit 15 of register 3 as the most significant bit, and bit 0 of register 0 as the least significant bit. The resulting 64 bit value is written to the global–mask register.

This operation should be executed before entering required values into the CAM table. Otherwise, the initialize–table instruction must be executed if the global mask register is changed after data is loaded into the CAM.

SET ALMOST–FULL POINT

This operation is used to define the "almost–full" condition in the CAM table. The 12 low–order bits of I/O register 0 are copied to the almost–full–point register. If an entry is added to the MCM69C232 (via the insert–value operation) that causes the valid–entry count to equal the almost–full–point, then bit 8 of the flag register is set, and an interrupt is generated if enabled by bit 5 of the interrupt register. The value of the almost–full register can be changed dynamically during match operations. For example, it could first be set to 2048 to generate an interrupt when the table is half full. When that point is reached, the register could be reprogrammed to 3072 to provide warning that the table has become three–quarters full. The almost–full interrupt is generated, if enabled, based on the number of entries in the CAM table. Entries in the queue are not included in the count.

SET FAST–READ REGISTER VALUE

This operation defines the table address that is output by the fast read operation. The least significant 12 bits of I/O register 0 are copied to the register. The queue must be empty when this instruction is executed.

FAST READ

This operation is used to output the contents of one entry in the CAM table. The fast–read register is used to specify the appropriate entry, and is then auto–incremented. As a result, successive execution of multiple fast–read operations will provide access to contiguous entries in the CAM table.

The CAM entry is copied to I/O registers 0 – 3, with bit 15 of register 3 as the most significant bit, and bit 0 of register 0 as the least significant bit.

The fast–read instruction can only be executed while the entry queue is empty, as reflected by the queue–empty flag being set (bit 4 of the flag register.) If this operation is attempted while the entry queue is not empty, the value $FFFC_{16}$ is written to the error code register, the error–condition flag (bit 7) is set in the flag register, and an interrupt is generated if enabled by bit 7 of the interrupt register.

SET ATM MODE

When the MCM69C232 is placed in ATM mode, it provides simultaneous searching for virtual path circuits (VPCs) and virtual connection circuits (VCCs). A VCC is detected when both the virtual path identifier (VPI) and the virtual circuit identifier (VCI) of an incoming cell match an entry in the CAM. A VPC match occurs when the VPI of an incoming cell matches the VPI field of a CAM entry that has all 1s as its VCI. A VPC match is signalled by the assertion of the $\overline{VPC}$ pin along with the $\overline{MS}$ pin. At 50 MHz, a match is completed in 160 ns, whether the applied VPI/VCI belongs to a VCC or a VPC.

The VCI match field must be defined as bits 32 – 47 of each entry, and the VPI match data must occupy bits 48 – 59. The VPI can be limited to bits 48 – 55, if the switch handles only User–Network Interface (UNI) protocols. The mask register should be used to "don't care" any unused bits beyond the VPI field. Entering ATM mode will set bit 9 of the flag register.

To load a VPC into the CAM table, the desired VPI value is written (right justified) to I/O register 3, $FFFF_{16}$ is written to I/O register 2 as the VCI field, the upper half of the desired output word is written to I/O register 1, and the lower half of the desired output word is written to I/O register 0. Then, the "INSERT VALUE" instruction is written to the operation register.

When performing a match operation, the VCI must be placed in bits 0 – 15 of the MQ port. The VPI is expected on bits 16 – 27, or bits 16 – 23 in the UNI case.

Buffered entry mode insertions and deletions are modified in the following way when the MCM69C232 is in ATM mode. If you try to add a VCC with the same VPI as an existing VPC, you overwrite the VPC. If you try to delete a VCC when the VCC is not in the table, but a VPC with that VPI is in the table, the VPC will be deleted.

MATCH CYCLE TIME

At 50 MHz, the MCM69C232 completes a match 160 ns after assertion of the $\overline{SM}$ signal. If minimal entries need to be added to or deleted from the CAM, the part can be cycled at 200 ns. In other words, $\overline{SM}$ can be asserted again immediately after the completion of a match operation and data output.

However, idle time is required between matches to allow insertions or deletions. The worst case occurs if an entry with a match data value smaller than any other entry in the CAM is continually added and dropped from the table. The number of insertion/deletion pairs per second in this scenario is shown versus match cycle time as the curve labeled "Worst Case" in Figure 3. As shown, a match cycle time of 200 ns allows for 610 insertion/deletion pairs per second. Note that this analysis is based on a 50 MHz input clock. Values should be derated in proportion to any decrease in clock speed. For example, at 25 MHz, twice as much idle time is required to achieve the same number of insertion/deletion pairs per second.

A more typical case would consist of either randomly placed insertions and deletions in the CAM table (as determined by the magnitude of the match field), or when insertions occur at one end of the table and deletions occur at the other end. The number of insertion/deletion pairs per second in this scenario is shown versus match cycle time as the curve labeled "Typical" in Figure 3. As shown, a match cycle time of 200 ns allows for 1220 insertion/deletion pairs per second.

For any match cycle time ≥ 200 ns and evenly divisible by 20 ns (200 ns, 220 ns, 240 ns, ...), the time to perform a worst–case insertion *or* deletion is equal to 81,920*MCT /(MCT–180) ns at 50 MHz, where MCT is the match cycle time in nanoseconds. In general, the time for an insertion or deletion is proportional to its distance from the end of the CAM table. That is, entries with the largest match values take the least time to insert or delete, while entries with the smallest values take the most time.

Therefore, the effective rate of insertion and deletion is maximized if the longest–lived entries are placed near the beginning of the table and the shortest–lived entries are placed near the end of the table. For an ATM application, this would correspond to the assignment of small VPI values to permanent virtual circuits and large VPI values to switched virtual circuits.

Note that at start–up, when entries are loaded into the CAM via the fast–entry mode, the process is dominated by the time it takes to execute the initialization instruction that follows. The resulting effective rate of loading the CAM at start–up is approximately 270,000 entries per second.

$\overline{RESET}$

Asserting $\overline{RESET}$ removes all entries from the CAM table and entry queue. The flag register is set to $1C_{16}$ (setting the queue empty, buffered entry mode, and table initialized bits). The error register is set to $FFFF_{16}$, indicating no errors. Finally, the almost full register is set to FFF_{16}.

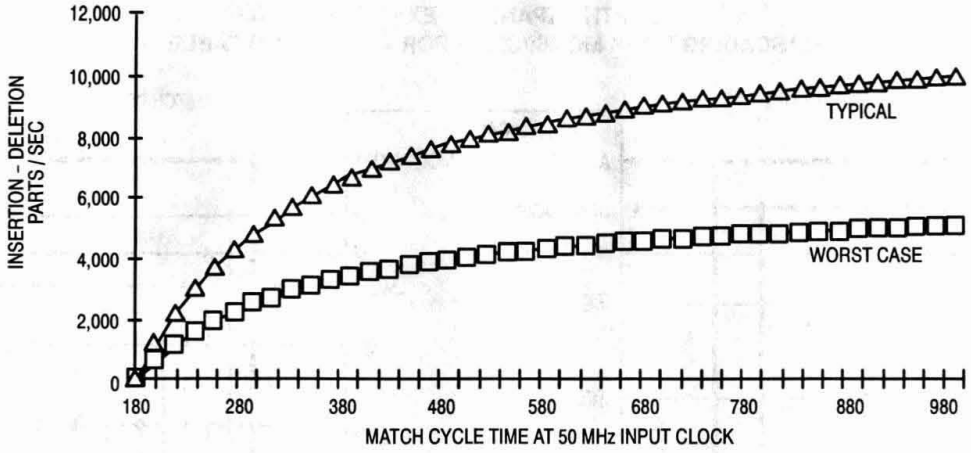

Figure 3. Connections per Second vs Match Cycle Time

TIMING OVERVIEW

CONTROL PORT

The control port of the MCM69C232 is asynchronous. Data transfers, both read and write, are initiated by the assertion of the $\overline{SEL}$ signal. Address values should be valid, and $\overline{WE}$ should be high, when $\overline{SEL}$ is asserted to begin a read cycle. All values (address, $\overline{WE}$, and $\overline{SEL}$) should be held until the MCM69C232 asserts $\overline{DTACK}$ to signal the end of the read cycle.

Address and data values should be valid, and $\overline{WE}$ should be low, when $\overline{SEL}$ is asserted to begin a write cycle. Address, data, $\overline{WE}$, and $\overline{SEL}$ values should be held until the MCM69C232 asserts $\overline{DTACK}$ to signal the end of the write cycle.

MATCH PORT

The MCM69C232's match port is synchronous in operation. When the match width is ≤ 32 bits, a match cycle can be initiated by presenting the match data on MQ31 – MQ0 and asserting the $\overline{LH/SM}$ signal with the appropriate setup time relative to the rising edge of the clock. The assertion of the $\overline{MC}$ output signifies the completion of the match cycle. If a match has been found, the $\overline{MS}$ output is also asserted. If the match is a virtual path circuit match in ATM mode, the $\overline{VPC}$ output will be asserted with the $\overline{MS}$ output. Output data, if any, is enabled by the assertion of the $\overline{G}$ input.

If the match width is greater than 32 bits, the lower bits are first latched into the MCM69C232 by the $\overline{LL}$ input. The match cycle is then initiated as specified in the previous paragraph.

DEPTH EXPANSION

Multiple CAMs can be cascaded to increase the depth of the match table. The hardware requirements are very straightforward, as the following pins on each device are simply wired in parallel: A2 – A0, DQ15 – DQ0, $\overline{WE}$, $\overline{IRQ}$, $\overline{DTACK}$, MQ31 – MQ0, K, $\overline{G}$, $\overline{LH/SM}$, $\overline{MC}$, $\overline{MS}$, and $\overline{VPC}$. Four CAMs can be easily cascaded. Simulations show that eight devices can be cascaded if care is taken to minimize the length of the PC board traces connecting the CAMs.

The buffered entry mode prevents multiple matching entries in a single CAM. The check for value instruction should be used to verify that multiple matching entries will not result from a potential new entry. If a match is found in CAM 1, for example, the new value should be placed in CAM 1, where it will replace the existing entry.

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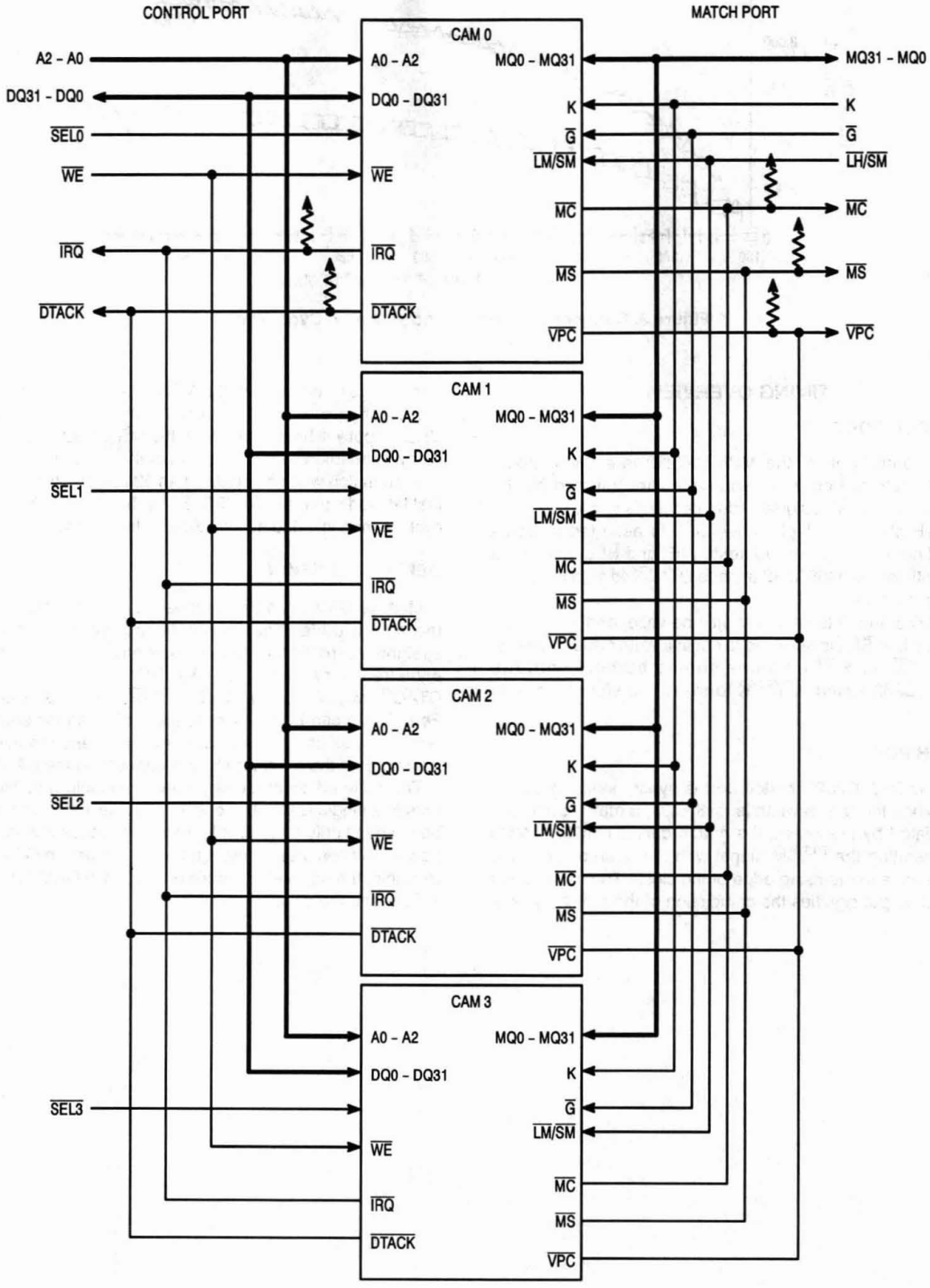
DEPTH EXPANSION EXAMPLE
CASCADING FOUR MCM69C232s FOR A 16K WORD TABLE



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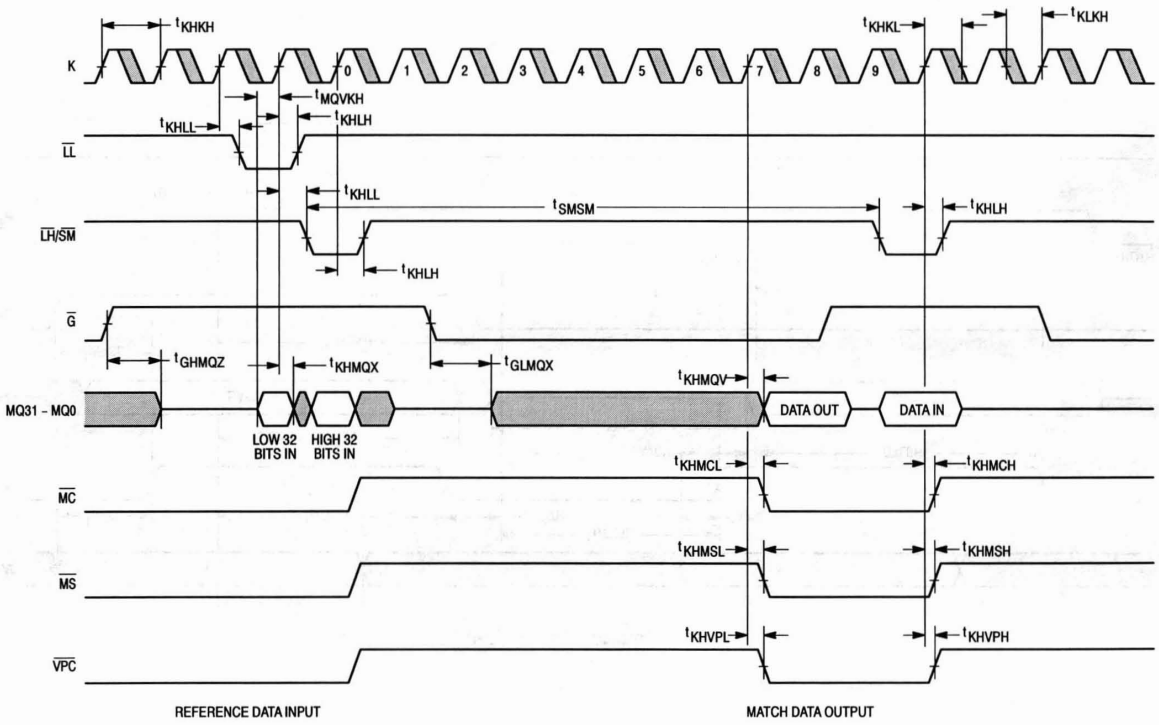
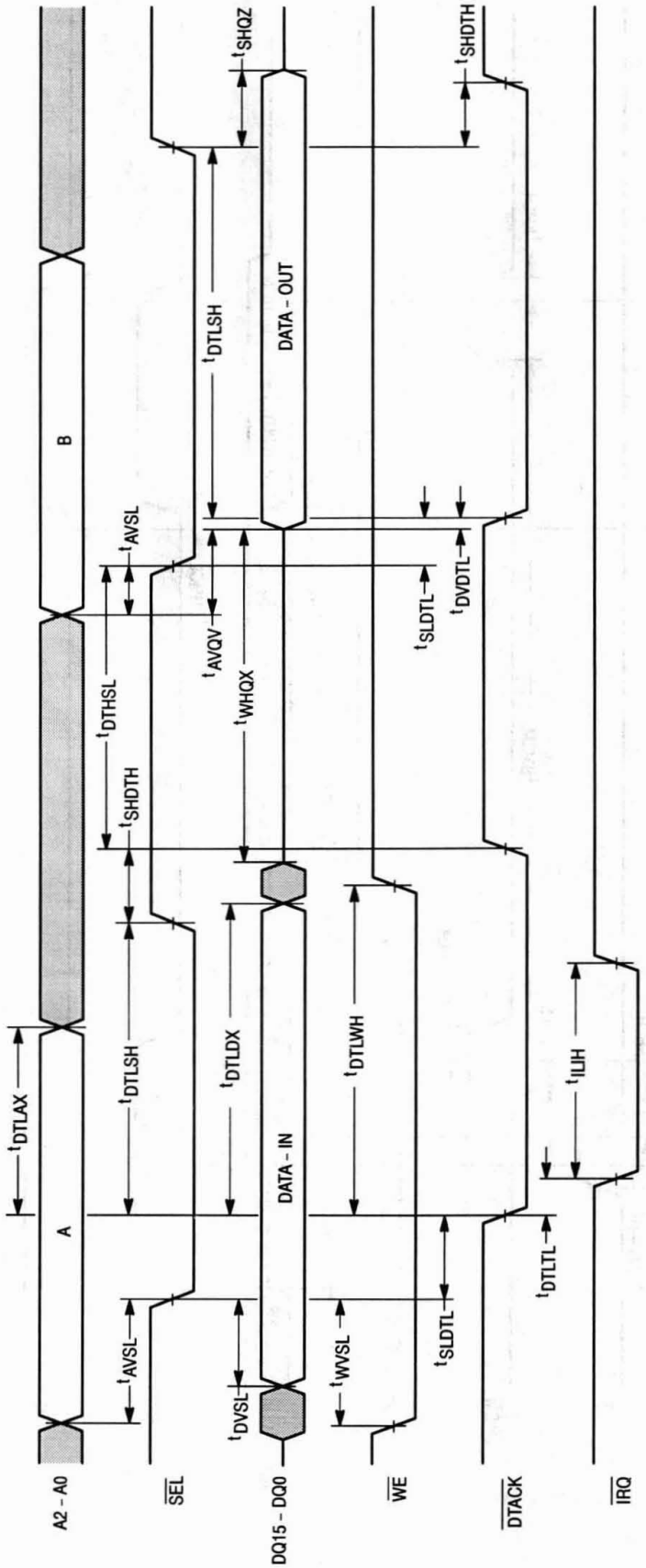
MATCH PORT TIMING



NOTE: In normal operation, all matches would be the same size, i.e., $\overline{LL}$ would either be used in every match cycle or in none. This diagram shows a 64 bit match followed by a 32 bit match in order to illustrate all the key specs.

CONTROL PORT TIMING



JTAG

AC OPERATING CONDITIONS AND CHARACTERISTICS FOR THE TEST ACCESS PORT (IEEE 1149.1)

(T_J = 20 to + 120°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Measurement Timing Level ..... 1.5 V
Output Load ..... 50 Ω Termination to 1.5 V

TAP CONTROLLER TIMING

Parameter		Symbol	MCM69C232 Min	MCM69C232 Max	Unit	Notes
Cycle Time		t_{CK}	30	—	ns	
Clock High Time		t_{CKH}	12	—	ns	
Clock Low Time		t_{CKL}	12	—	ns	
Clock Low to Output Valid		t_A	5	9	ns	
Clock Low to Output High–Z		t_{CKZ}	0	9	ns	1
Clock Low to Output Active		t_{CKX}	0	9	ns	2, 3
Setup Times:	TMS TDI $\overline{TRST}$	t_S t_{SD} t_{SR}	2 2 2	—	ns	
Hold Times:	TMS TDI $\overline{TRST}$	t_H t_{HD} t_{HR}	2 2 10	—	ns	

NOTES:
1. TDO will High–Z from a clock low edge depending on the current state of the TAP state machine.
2. TDO is active only in the SHIFT–IR and SHIFT–DR state of the TAP state machine.
3. Transition is measured ± 500 mV from steady–state voltage. This parameter is sampled and not 100% tested.

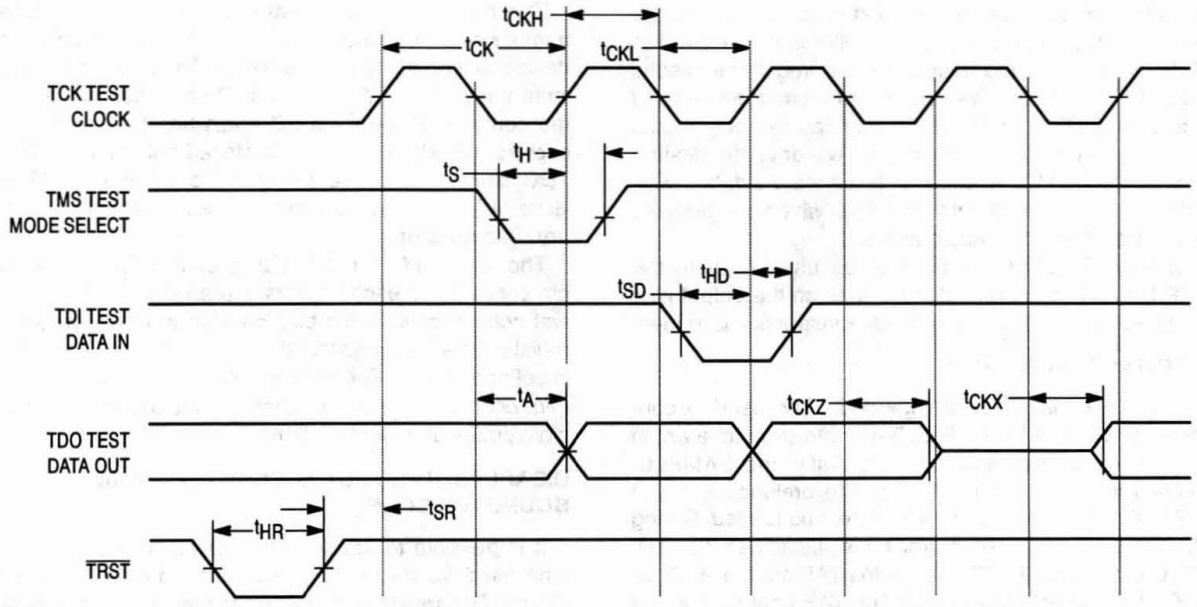


Figure 4. TAP Controller Timing

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INSTRUCTION SET

A five pin IEEE Standard 1149.1 Test Port (JTAG) is included on this device. When the TAP (Test Access Port) controller is in the SHIFT–IR state, the instruction register is placed between TDI and TDO. In this state, the desired instruction would be serially loaded through the TDI input. $\overline{TRST}$ resets the TAP controller to the test–logic reset state. The TAP instruction set for this device are as follows.

STANDARD INSTRUCTIONS

Instruction	Code (Binary)	Description
BYPASS	1111*	Bypass instruction
SAMPLE/PRELOAD	0010	Sample and/or preload instruction
EXTEST	0000	Extest instruction
HIGHZ	1001	High–Z all output pins while bypass register is between TDI and TDO
CLAMP	1100	Clamp output pins while bypass register is between TDI and TDO

* Default state at power–up.

SAMPLE/PRELOAD TAP INSTRUCTION

The SAMPLE/PRELOAD TAP instruction is used to allow scanning of the boundary–scan register without causing interference to the normal operation of the chip logic. The 62–bit boundary–scan register contains bits for all device signal and clock pins and associated control signals. This register is accessible when the SAMPLE/PRELOAD TAP instruction is loaded into the TAP instruction register in the SHIFT–IR state. When the TAP controller is then moved to the SHIFT–DR state, the boundary–scan register is placed between TDI and TDO. This scan register can then be used prior to the EXTEST instruction to preload the output pins with desired values so that these pins will drive the desired state when the EXTEST instruction is loaded. As data is written into TDI, data also streams out TDO which can be used to pre–sample the inputs and outputs.

SAMPLE/PRELOAD would also be used prior to the CLAMP instruction to preload the values on the output pins that will be driven out when the CLAMP instruction is loaded.

EXTEST TAP INSTRUCTION

The EXTEST instruction is intended to be used in conjunction with the SAMPLE/PRELOAD instruction to assist in testing board level connectivity. Normally, the SAMPLE/PRELOAD instruction would be used to preload all output pins. The EXTEST instruction would then be loaded. During EXTEST, the boundary–scan register is placed between TDI and TDO in the SHIFT–DR state of the TAP controller. Once the EXTEST instruction is loaded, the TAP controller would then be moved to the run–test/idle state. In this state, one cycle of TCK would cause the preloaded data on the output pins to be driven while the values on the input pins would be sampled. Note the TCK, not the clock pin (CLK), is used as the clock input while CLK is only sampled during EXTEST. After one clock cycle of TCK, the TAP controller would then be moved to the SHIFT–DR state where the sampled values would be shifted out of TDO (and new values would be shifted in TDI). These values would normally be compared to expected values to test for board connectivity.

CLAMP TAP INSTRUCTION

The CLAMP instruction is provided to allow the state of the signals driven from the output pins to be determined from the boundary–scan register while the bypass register is selected as the serial path between TDI and TDO. The signals driven from the output pins will not change while the CLAMP instruction is selected. EXTEST could also be used for this purpose, but CLAMP shortens the board scan path by inserting only the bypass register between TDI and TDO. To use CLAMP, the SAMPLE/PRELOAD instruction would be used first to scan in the values that will be driven on the output pins when the CLAMP instruction is active.

HIGHZ TAP INSTRUCTION

The HIGH–Z instruction is provided to allow all the outputs to be placed in an inactive drive state (high–Z). During the HIGH–Z instruction the bypass register is connected between TDI and TDO.

BYPASS TAP INSTRUCTION

The BYPASS instruction is the default instruction loaded at power up. This instruction will place a single shift register between TDI and TDO during the SHIFT–DR state of the TAP controller. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

BOUNDARY SCAN REGISTER

The boundary scan register is identical in length to the number of active input, output, and I/O connections on the device (not counting the TAP pins). The boundary scan register, under the control of the TAP controller, is loaded with the contents of the RAM I/O ring when the controller is in capture_DR state and then is placed between the TDI and TDO pins when the controller is moved to shift_DR state. Several TAP instructions can be used to activate the boundary scan register.

The Bit Scan Order table (Table 2) describes which device pin connects to each boundary scan register location. The first column defines the bit's position in the boundary scan register. The shift register bit at $\overline{G}$ (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the pin, third column is the pin number and the fourth column is the pin type (input, output, or I/O).

DISABLING THE TEST ACCESS PORT AND BOUNDARY SCAN

It is possible to use this device without utilizing the four pins used for the test access port. To circuit disable the device, TCK must be tied to V_{SS} to preclude mid level inputs. Although TDI and TMS are designed in such a way that an undriven input will produce a response equivalent to the application of a logic 1, it is still advisable to tie these inputs to V_{DD} through a 1K resistor. TDO should remain unconnected.

Table 2. Sample/Preload Boundary Scan Register Bit Definitions

Bit Number	Bit Pin Name	Bit Pin Number	Pin Type	Bit Number	Bit Pin Name	Bit Pin Number	Pin Type
1	$\overline{G}$	61	Input	32	MQ6	6	I/O
2	$\overline{MS}$	62	Output	33	MQ5	7	I/O
3	$\overline{VPC}$	63	Output	34	MQ4	8	I/O
4	$\overline{MC}$	64	Output	35	MQ3	11	I/O
5	MQ31	67	I/O	36	MQ2	12	I/O
6	MQ30	68	I/O	37	MQ1	13	I/O
7	MQ29	69	I/O	38	MQ0	14	I/O
8	MQ28	70	I/O	39	DQ15	17	I/O
9	MQ27	73	I/O	40	DQ14	18	I/O
10	MQ26	74	I/O	41	DQ13	19	I/O
11	MQ25	75	I/O	42	DQ12	20	I/O
12	MQ24	76	I/O	43	DQ11	23	I/O
13	MQ23	79	I/O	44	DQ10	24	I/O
14	MQ22	80	I/O	45	DQ9	25	I/O
15	MQ21	81	I/O	46	DQ8	26	I/O
16	MQ20	82	I/O	47	DQ7	29	I/O
17	MQ19	85	I/O	48	DQ6	30	I/O
18	MQ18	86	I/O	49	DQ5	31	I/O
19	MQ17	87	I/O	50	DQ4	32	I/O
20	MQ16	88	I/O	51	DQ3	35	I/O
21	$\overline{LH/SM}$	89	Input	52	DQ2	36	I/O
22	$\overline{LL}$	92	Input	53	DQ1	37	I/O
23	MQ15	93	I/O	54	DQ0	38	I/O
24	MQ14	94	I/O	55	A2	42	Input
25	MQ13	95	I/O	56	A1	43	Input
26	MQ12	96	I/O	57	A0	44	Input
27	MQ11	99	I/O	58	$\overline{WE}$	45	Input
28	MQ10	100	I/O	59	$\overline{SEL}$	46	Input
29	MQ9	1	I/O	60	$\overline{RESET}$	56	Input
30	MQ8	2	I/O	61	$\overline{IRQ}$	57	Output
31	MQ7	5	I/O	62	$\overline{DTACK}$	58	Output

TEST ACCESS PORT PINS

TCK — TEST CLOCK (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

TMS — TEST MODE SELECT (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.

TDI — TEST DATA IN (INPUT)

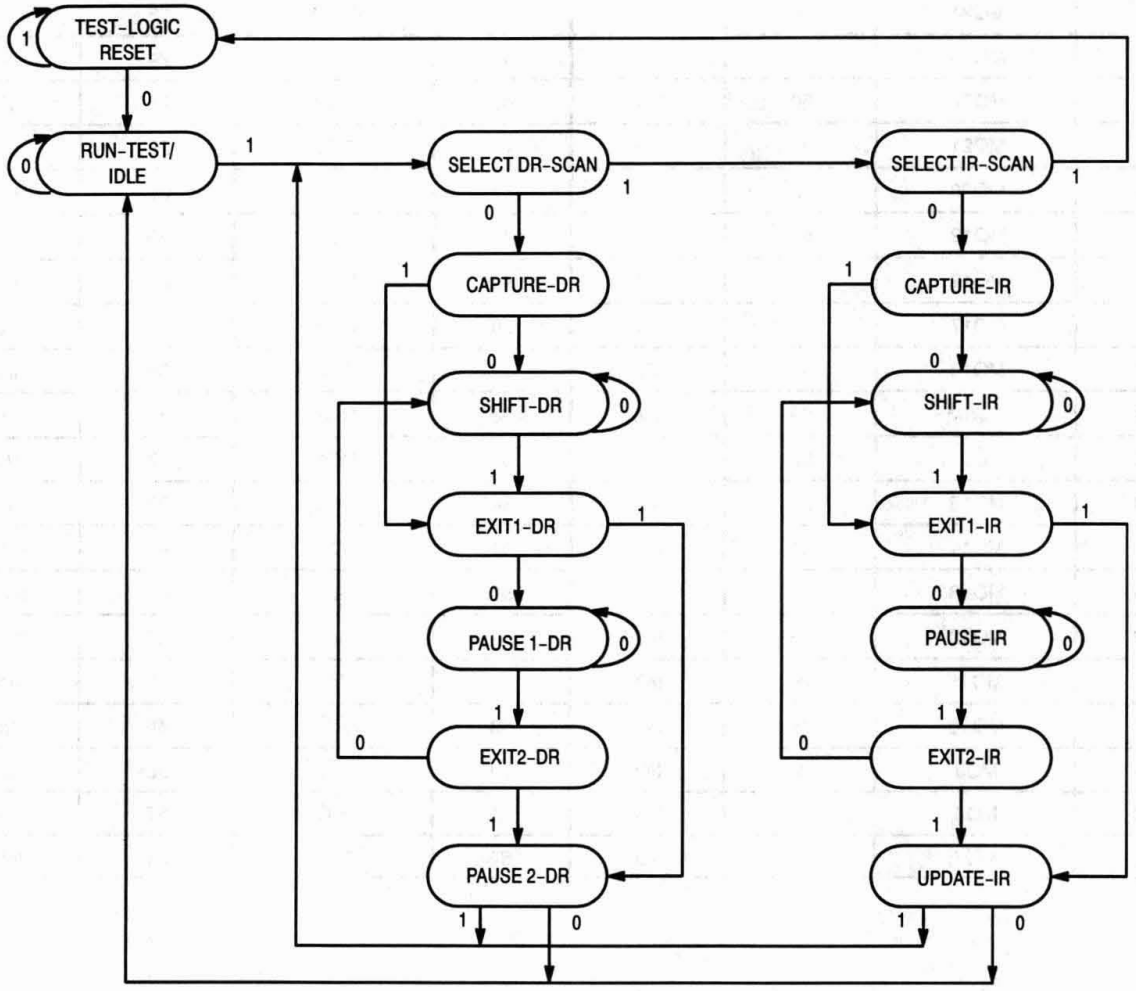
The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (see Figure 5). An undriven TDI pin will produce the same result as a logic one input level.

TDO — TEST DATA OUT (OUTPUT)

Output that is active depending on the state of the TAP state machine (see Figure 5). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

$\overline{\text{TRST}}$ — TAP RESET

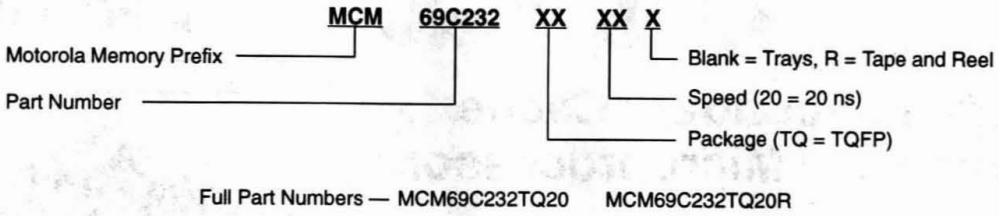
This device has a $\overline{\text{TRST}}$ pin. $\overline{\text{TRST}}$ is optional in IEEE 1149.1. Asserting the asynchronous $\overline{\text{TRST}}$ places the TAP controller in test–logic reset state. Test–logic reset state can also be entered by holding TMS high for five rising edges of TCK. This type of reset does not affect the operation of the system logic.



NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 5. TAP Controller State Diagram

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM69C232TQ20 MCM69C232TQ20R

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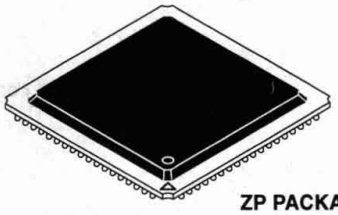
MPC2605

Product Preview

Integrated Secondary Cache for PowerPC™ Microprocessors



ZP PACKAGE
PBGA
CASE 1138–01

The MPC2605 is a single chip, 256KB integrated look–aside cache with copy–back capability designed for PowerPC applications (MPC603 and MPC604). Using 0.38 µm technology along with standard cell logic technology, the MPC2605 integrates data, tag, host interface, and least recently used (LRU) memory with a cache controller to provide a 256KB, 512KB, or 1 MB Level 2 cache with one, two, or four chips on a 64–bit PowerPC bus.

- Single Chip L2 Cache for PowerPC
- 66 MHz Zero Wait State Performance (2–1–1–1 Burst)
- Four–Way Set Associative Cache Design
- 32K x 72 Data Memory Array
- 8K x 18 Tag Array
- Address Parity Support
- LRU Cache Control Logic
- Copy–Back or Write–Through Modes of Operation
- Copy–Back Buffer for Improved Performance
- Single 3.3 V Power Supply
- 5 V Tolerant I/O
- One, Two, or Four Chip Cache Solution (256KB, 512KB, or 1MB)
- Single Clock Operation
- Compliant with IEEE Standard 1149.1 Test Access Port (JTAG)
- Supports up to Four Processors in a Shared Cache Configuration
- High Board Density 25 mm 241 PBGA Package

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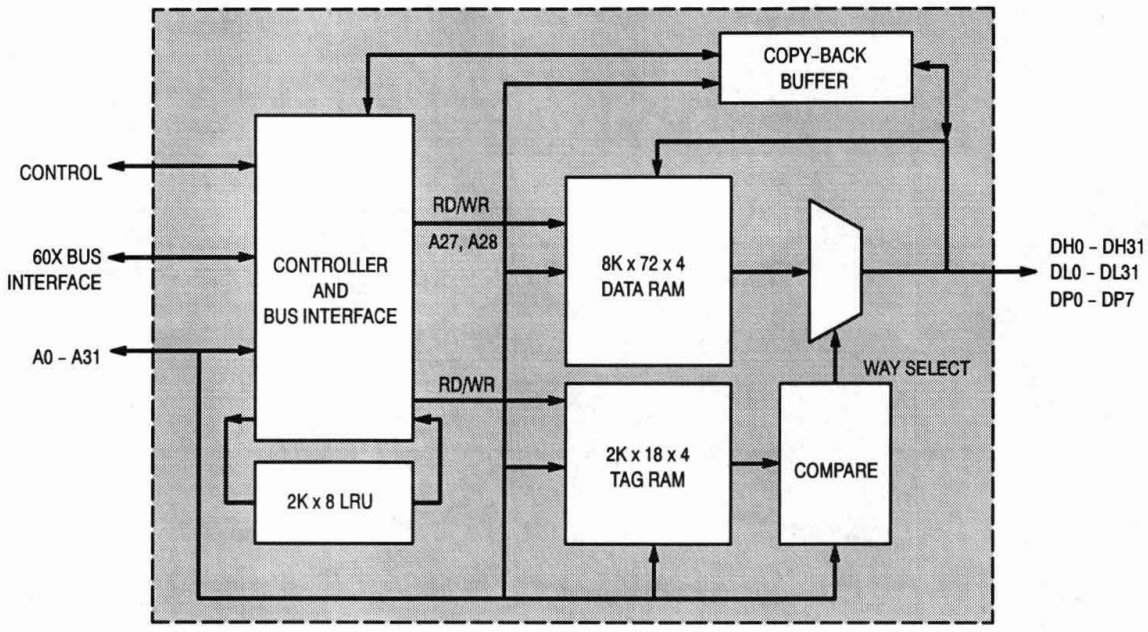
BLOCK DIAGRAM



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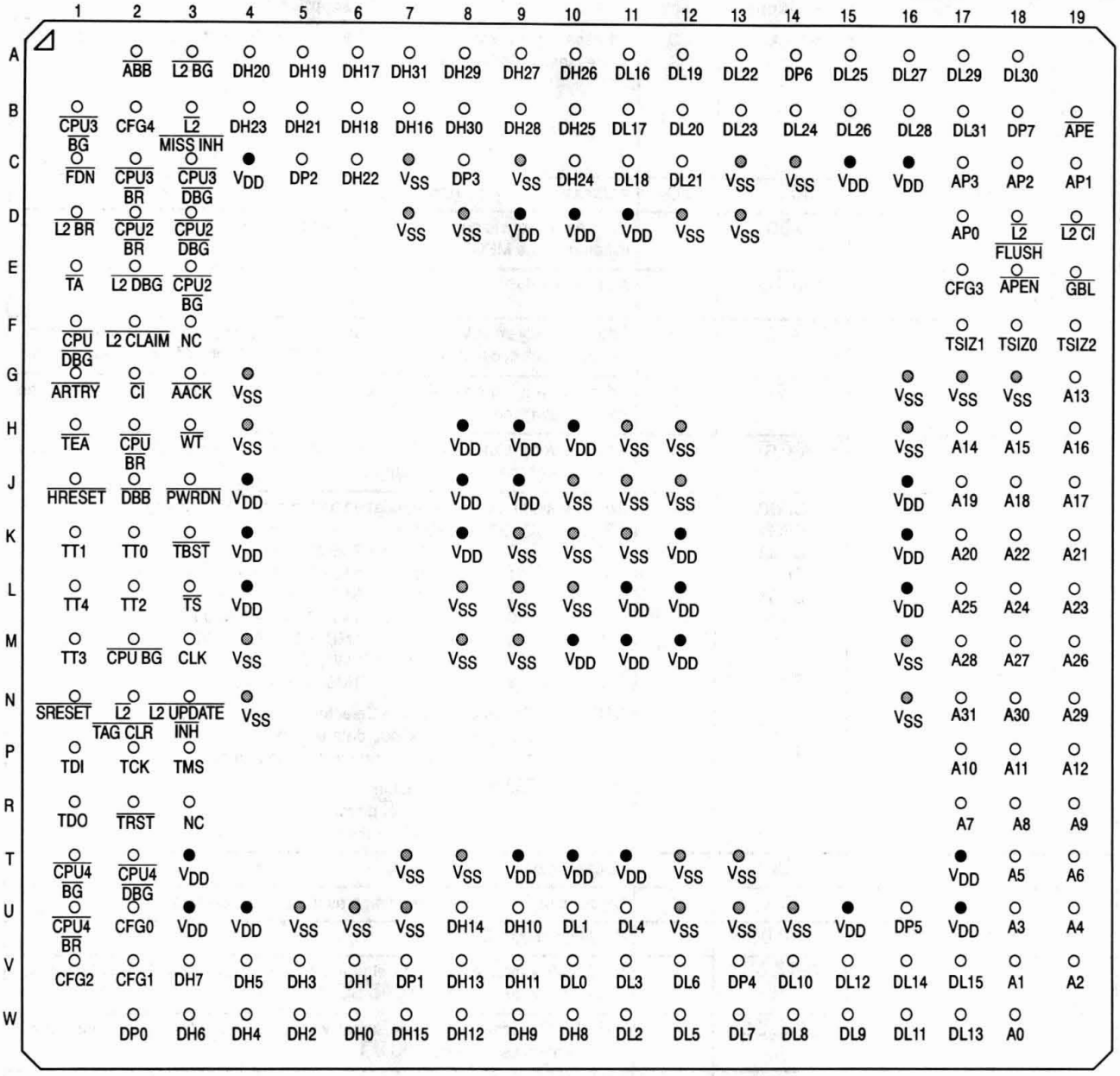
PIN ASSIGNMENT


1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
A: ABB | L2 BG | DH20 | DH19 | DH17 | DH31 | DH29 | DH27 | DH26 | DL16 | DL19 | DL22 | DP6 | DL25 | DL27 | DL29 | DL30
B: CPU3 BG | CFG4 | L2 MISS INH | DH23 | DH21 | DH18 | DH16 | DH30 | DH28 | DH25 | DL17 | DL20 | DL23 | DL24 | DL26 | DL28 | DL31 | DP7 | APE
C: FDN | CPU3 BR | CPU3 DBG | VDD | DP2 | DH22 | VSS | DP3 | VSS | DH24 | DL18 | DL21 | VSS | VSS | VDD | VDD | AP3 | AP2 | AP1
D: L2 BR | CPU2 BR | CPU2 DBG | VSS | VSS | VDD | VDD | VDD | VSS | VSS | AP0 | L2 FLUSH | L2 CI
E: TA | L2 DBG | CPU2 BG | CFG3 | APEN | GBL
F: CPU DBG | L2 CLAIM | NC | TSIZ1 | TSIZ0 | TSIZ2
G: ARTRY | CI | AACK | VSS | VSS | VSS | VSS | A13
H: TEA | CPU BR | WT | VSS | VDD | VDD | VDD | VSS | VSS | VSS | A14 | A15 | A16
J: HRESET | DBB | PWRDN | VDD | VDD | VDD | VSS | VSS | VSS | VDD | A19 | A18 | A17
K: TT1 | TT0 | TBST | VDD | VDD | VSS | VSS | VSS | VSS | VDD | A20 | A22 | A21
L: TT4 | TT2 | TS | VDD | VSS | VSS | VSS | VDD | VDD | VDD | A25 | A24 | A23
M: TT3 | CPU BG | CLK | VSS | VSS | VSS | VDD | VDD | VDD | VSS | A28 | A27 | A26
N: SRESET | L2 TAG CLR | L2 UPDATE INH | VSS | VSS | A31 | A30 | A29
P: TDI | TCK | TMS | A10 | A11 | A12
R: TDO | TRST | NC | A7 | A8 | A9
T: CPU4 BG | CPU4 DBG | VDD | VSS | VSS | VDD | VDD | VDD | VSS | VSS | VDD | A5 | A6
U: CPU4 BR | CFG0 | VDD | VDD | VSS | VSS | VSS | DH14 | DH10 | DL1 | DL4 | VSS | VSS | VSS | VDD | DP5 | VDD | A3 | A4
V: CFG2 | CFG1 | DH7 | DH5 | DH3 | DH1 | DP1 | DH13 | DH11 | DL0 | DL3 | DL6 | DP4 | DL10 | DL12 | DL14 | DL15 | A1 | A2
W: DP0 | DH6 | DH4 | DH2 | DH0 | DH15 | DH12 | DH9 | DH8 | DL2 | DL5 | DL7 | DL8 | DL9 | DL11 | DL13 | A0

TOP VIEW (X–RAY VIEW)

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PIN DESCRIPTIONS

Pin Locations	Pin Name	Type	Description
19G, 17H – 19H, 17J – 19J, 17K – 19K, 17L – 19L, 17M – 19M, 17N – 19N, 17P – 19P, 17R – 19R, 18T, 19T, 18U, 19U, 18V, 19V, 18W *	A0 – A31	I/O	Address inputs from processor. Can also be outputs for processor snoop addresses. A0 is the MSB. A31 is the LSB.
3G	$\overline{\text{AACK}}$	I/O	Address acknowledge input/output.
2A	$\overline{\text{ABB}}$	I/O	Used as an input to qualify bus grants. Driven as an output during address tenure initiated by the MPC2605.
17C – 19C, 17D *	AP0 – AP3	I/O	Address parity.
19B	$\overline{\text{APE}}$	O	Address parity error. When an address parity error is detected, $\overline{\text{APE}}$ will be driven low one clock cycle after the assertion of $\overline{\text{TS}}$ then High–Z following clock cycle.
18E	$\overline{\text{APEN}}$	I	Address parity enable. When tied low, enables address parity bits and the address parity error bit.
1G	$\overline{\text{ARTRY}}$	I/O	Address retry status I/O. Generated when a read or write snoop to a dirty processor cache line has occurred.
2U 2V 1V 17E 2B	CFG0 CFG1 CFG2 CFG3 CFG4	I	Configuration inputs. These must be tied to either V_{DD} or V_{SS}. CFG0 CFG1 CFG2 0 0 0 256KB 0 1 0 512KB; A26 = 0 0 1 1 512KB; A26 = 1 1 0 0 1MB; A25 – A26 = 00 1 0 1 1MB; A25 – A26 = 01 1 1 0 1MB; A25 – A26 = 10 1 1 1 1MB; A25 – A26 = 11 CFG3 Snoop Data Tenure Selector 0 Supports snoop data tenure 1 Does not support snoop data tenure CFG4 $\overline{\text{AACK}}$ Driver Enable 0 Disable $\overline{\text{AACK}}$ driver 1 Enable $\overline{\text{AACK}}$ driver
2G	$\overline{\text{CI}}$	I/O	Cache inhibit I/O.
3M	CLK	I	Clock input. This must be the same as the processor clock input.
2M	$\overline{\text{CPU BG}}$	I	CPU bus grant input.
3E	$\overline{\text{CPU2 BG}}$	I	MPC2605 logically ORs this signal with $\overline{\text{CPU BG}}$. Used in multiprocessor configuration as the second $\overline{\text{CPU BG}}$.
1B	$\overline{\text{CPU3 BG}}$	I	MPC2605 logically ORs this signal with $\overline{\text{CPU BG}}$. Used in multiprocessor configuration as the third $\overline{\text{CPU BG}}$.
1T	$\overline{\text{CPU4 BG}}$	I	MPC2605 logically ORs this signal with $\overline{\text{CPU BG}}$. Used in multiprocessor configuration as the fourth $\overline{\text{CPU BG}}$.
2H	$\overline{\text{CPU BR}}$	I	CPU bus request input.
2D	$\overline{\text{CPU2 BR}}$	I	MPC2605 logically ORs this signal with $\overline{\text{CPU BR}}$. Used in multiprocessor configuration as the second $\overline{\text{CPU BR}}$.
2C	$\overline{\text{CPU3 BR}}$	I	MPC2605 logically ORs this signal with $\overline{\text{CPU BR}}$. Used in multiprocessor configuration as the third $\overline{\text{CPU BR}}$.
1U	$\overline{\text{CPU4 BR}}$	I	MPC2605 logically ORs this signal with $\overline{\text{CPU BR}}$. Used in multiprocessor configuration as the fourth $\overline{\text{CPU BR}}$.
1F	$\overline{\text{CPU DBG}}$	I	CPU data bus grant input from arbiter.
3D	$\overline{\text{CPU2 DBG}}$	I	MPC2605 logically ORs this signal with $\overline{\text{CPU DBG}}$. Used in multiprocessor configuration as the second $\overline{\text{CPU DBG}}$.
3C	$\overline{\text{CPU3 DBG}}$	I	MPC2605 logically ORs this signal with $\overline{\text{CPU DBG}}$. Used in multiprocessor configuration as the third $\overline{\text{CPU DBG}}$.

* See pin diagram (page 2) for specific pin assignment of these bus signals.

Pin Locations	Pin Name	Type	Description
2T	$\overline{\text{CPU4 DBG}}$	I	MPC2605 logically ORs this signal with $\overline{\text{CPU DBG}}$. Used in multiprocessor configuration as the fourth $\overline{\text{CPU DBG}}$.
11A – 13A, 15A – 18A, 11B – 17B, 11C, 12C, 10U, 11U, 10V – 12V, 14V – 17V, 11W – 17W *	DL0 – DL31	I/O	Data bus low input and output. DL0 is the MSB. DL31 is the LSB.
4A – 10A, 4B – 10B, 6C, 10C, 8U, 9U, 3V – 6V, 8V, 9V, 3W –10W *	DH0 – DH31	I/O	Data bus high input and output. DH0 is the MSB. DH31 is the LSB.
2J	$\overline{\text{DBB}}$	I/O	Data bus busy. Used as input when processor is master, driven as an output after a qualified $\overline{\text{L2 DBG}}$ when MPC2605 is the bus master. Note: To operate in Fast L2 mode, this pin must be tied high.
14A, 18B, 5C, 8C, 16U, 7V, 13V, 2W *	DP0 – DP7	I/O	Data bus parity input and output.
1C	$\overline{\text{FDN}}$	I/O	Flush done I/O used for communication between other MPC2605 devices. Must be tied together between all MPC2605 parts along with a pullup resistor.
19E	$\overline{\text{GBL}}$	O	Global transaction. Always negated when MPC2604 is bus master.
1J	$\overline{\text{HRESET}}$	I	Hard reset input from processor bus. This is an asynchronous input that must be low for at least 16 clock cycles to ensure the MPC2605 is properly reset.
3A	$\overline{\text{L2 BG}}$	I	Bus grant input from arbiter.
1D	$\overline{\text{L2 BR}}$	I/O	Bus request I/O. Normally used as an output.
19D	$\overline{\text{L2 CI}}$	I	Secondary cache inhibit sampled, after assertion of $\overline{\text{TS}}$. Assertion prevents linefill.
2F	$\overline{\text{L2 CLAIM}}$	O	L2 cache claim output. Used to claim the bus for processor initiated memory operations that hit the L2 cache. $\overline{\text{L2 CLAIM}}$ goes true (low) before the rising edge of CLK following $\overline{\text{TS}}$ true. Because this output is not always driven, a pullup resistor may be necessary to ensure proper system functioning.
2E	$\overline{\text{L2 DBG}}$	I	Data bus grant input. Comes from system arbiter, used to start data tenure for bus operations where MPC2605 is the bus master.
18D	$\overline{\text{L2 FLUSH}}$	I	Causes cache to write back dirty lines and clears all tag valid bits.
3B	$\overline{\text{L2 MISS INH}}$	I	Prevents line fills on misses when asserted.
2N	$\overline{\text{L2 TAG CLR}}$	I	Invalidates all tags and holds cache in a reset condition.
3N	$\overline{\text{L2 UPDATE INH}}$	I	Cache disable. When asserted, the MPC2605 will not respond to signals on the local bus and internal states do not change.
3J	$\overline{\text{PWRDN}}$	I	Provides low power mode. Disables internal clock tree and prevents address and data transitions into the RAM array. MPC2605 becomes active 4 µs after deassertion.
1N	$\overline{\text{SRESET}}$	I	Soft reset input from processor bus.
1E	$\overline{\text{TA}}$	I/O	Transfer acknowledge status I/O from processor bus.
3K	$\overline{\text{TBST}}$	I/O	Transfer burst status I/O from processor bus. Used to distinguish between burstable and non–burstable memory operations.
2P	TCK	I	Test clock input for IEEE 1149.1 boundary scan (JTAG).
1P	TDI	I	Test data input for IEEE 1149.1 boundary scan (JTAG).
1R	TDO	O	Test data output for IEEE 1149.1 boundary scan (JTAG).
1H	$\overline{\text{TEA}}$	I	Transfer error acknowledge status input from processor bus.
3P	TMS	I	Test mode select for IEEE 1149.1 boundary scan (JTAG).
2R	$\overline{\text{TRST}}$	I	Test reset input for IEEE 1149.1 boundary scan (JTAG).
3L	$\overline{\text{TS}}$	I/O	Transfer start I/O from processor bus (can also come from any bus master on the processor bus). Signals the start of either a processor or bus master cycle.

* See pin diagram (page 2) for specific pin assignment of these bus signals.

Pin Locations	Pin Name	Type	Description
17F – 19F *	TSIZ0–TSIZ2	I/O	Transfer size I/O from processor bus.
1K, 2K, 1L, 2L, 1M *	TT0–TT4	I/O	Transfer type I/O from processor bus.
3H	$\overline{WT}$	I/O	Write through status input from processor bus. When tied to ground, the MPC2605 will operate in write–through mode only (no copy–back).
4C, 15C, 16C, 9D – 11D, 8H – 10H, 4J, 8J, 9J, 16J, 4K, 8K, 12K, 16K, 4L, 11L, 12L, 16L, 10M – 12M, 3T, 9T – 11T, 17T, 3U, 4U, 15U, 17U	V_{DD}	Supply	Power supply: 3.3 V ± 5%.
7C, 9C, 13C, 14C, 7D, 8D, 12D, 13D, 4G, 16G – 18G, 4H, 11H, 12H, 16H, 10J – 12J, 9K – 11K, 8L – 10L, 4M, 8M, 9M, 16M, 4N, 16N, 7T, 8T, 12T, 13T, 5U – 7U, 12U – 14U	V_{SS}	Supply	Ground.
3F, 3R	NC	—	No connection: There is no connection to the chip.

* See pin diagram (page 2) for specific pin assignment of these bus signals.

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation (Note 2)	P_D	—	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_J	20 to + 110	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(T_J = 20 to + 110°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{DD}	3.135	3.3	3.465	V
Input High Voltage	V_{IH}	2.0	—	5.5	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL}(min) = – 2.0 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{DD})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current (High–Z State, V_{out} = 0 to V_{DD})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current (I_{out} = 0 mA, All inputs = V_{IL} or V_{IH}, V_{IL} = 0 V, and V_{IH} ≥ 3.0 V, Cycle Time = 15 ns, max value assumes a constant burst read hit, with 100% bus utilization, and 100% hit rate)	I_{CCA}	—	720	mA
AC Quiescent Current (I_{out} = 0 mA, All inputs = V_{IL} or V_{IH}, V_{IL} = 0 V and V_{IH} ≥ 3.0 V, Cycle Time = 15 ns, All Other Inputs DC)	I_Q	—	195	mA
Power Down Current	I_{PD}	—	2	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance	C_{out}	6	8	pF
Input/Output Capacitance	$C_{I/O}$	8	10	pF

PACKAGE THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit
Thermal Resistance Junction to Ambient (Still Air, 4 Layer Board)	$R_{\theta JA}$	19	°C/W
Thermal Resistance Junction to Ambient (200 lfpm, 4 Layer Board)	$R_{\theta JA}$	15	°C/W
Thermal Resistance Junction to Board (Bottom)	$R_{\theta JB}$	7.3	°C/W
Thermal Resistance Junction to Case (Top)	$R_{\theta JC}$	8	°C/W

AC OPERATING CONDITIONS AND CHARACTERISTICS

(T_J = 20 to + 110°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

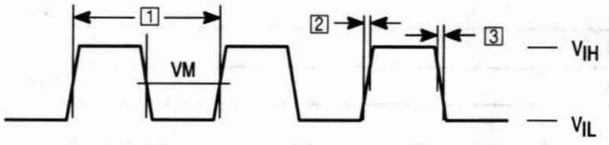
Output Measurement Timing Level ..... 1.5 V
Output Load ..... 50 Ω Termination to 1.5 V

AC CLOCK SPECIFICATIONS

Parameter	Timing Reference	MPC2605–66		Unit	Notes
		Min	Max		
Frequency of Operation		—	66.67	MHz	
Clock Cycle Time	[1]	15	—	ns	1
Clock Rise and Fall Time	[2], [3]	1.0	2.0	ns	2
Clock Duty Cycle Measured at 1.5 V		40	60	%	
Clock Short–Term Jitter (Cycle to Cycle)		—	± 150	ps	1

NOTES:
1. This parameter is sampled and not 100% tested.
2. Rise and fall times for the clock input are measured from 0.4 to 2.4 V.

CLOCK INPUT TIMING DIAGRAM



VM = Midpoint Voltage (1.5 V)

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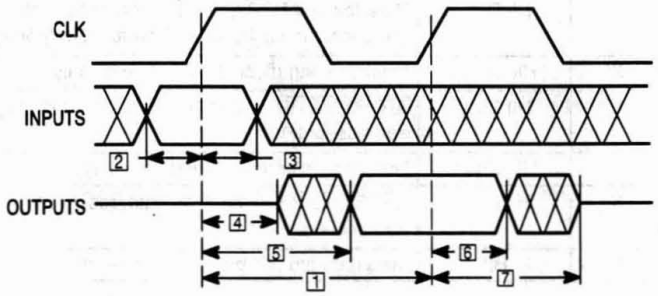
AC SPECIFICATIONS

Parameter	Timing Reference	MPC2605–66		Unit	Notes
		Min	Max		
Clock Cycle Time	1	15	—	ns	
Input Setup Time	2	4.5	—	ns	1
Clock to Input Invalid (Input Hold)	3	1	—	ns	1
Clock to Output Driven	4	2	9	ns	2
Clock to Output Valid	5	2	9	ns	
Clock to Output Invalid	6	2	—	ns	2
Clock to Output High–Z	7	2	12	ns	2
PWRDN Disable to Recovery		—	4	µs	

NOTES:
1. All input specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the 1.4 V level of the rising edge of the input clock. Both input and output timings are measured at the pin.
2. This parameter is sampled and not 100% tested.



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MPC2605 RESPONSE TO 60X TRANSFER ATTRIBUTES

TT0 – TT4	$\overline{TBST}$	$\overline{CI}$	$\overline{WT}$	Tag Status	MPC2605 Response	Notes
X1X10	0	1	X	Miss	Line–fill (processor read miss)	1, 2, 3
X1X10	0	1	X	Hit	$\overline{L2\ CLAIM}$, $\overline{AACK}$, $\overline{TA}$ (processor read hit)	4
X1010	1	0	X	Hit Clean	Paradox — Invalidate the line (processor n–cacheable read hit clean line)	
X1010	1	0	X	Hit Dirty	Paradox — $\overline{ARTRY}$, $\overline{L2\ BR}$, then write back data, invalidate the line (processor n–cacheable read hit dirty line)	
00110	0	1	X	Miss	Line–fill except right after a snoop hit to processor (processor write miss)	1, 3, 5, 6
00110	0	1	1	Hit	$\overline{L2\ CLAIM}$, $\overline{AACK}$, $\overline{TA}$ except after a snoop hit to processor (processor write hit)	5, 6
00X10	X	1	0	Hit Clean	Cache update (processor write through $\overline{WT}$ hit clean)	
00110	0	1	0	Hit Dirty	Cache update, clear dirty bit	
00010	1	1	0	Hit Dirty	Paradox — $\overline{ARTRY}$, $\overline{L2\ BR}$, write back data, keep valid, clear dirty bit	
X0010	1	0	X	Hit Clean	Paradox — Invalidate the line (processor n–cacheable write hit clean line)	
X0010	1	0	X	Hit Dirty	Paradox — $\overline{ARTRY}$, $\overline{L2\ BR}$, then write back data, invalidate the line (processor n–cacheable SB write hit dirty line)	
00100	X	X	X	Hit Clean	Invalidate tag (flush block address–only)	
00100	X	X	X	Hit Dirty	$\overline{ARTRY}$, $\overline{L2\ BR}$, write back data, invalidate tag (flush block address–only)	
00000	X	X	X	Hit Clean	No action (clean block address–only)	
00000	X	X	X	Hit Dirty	$\overline{ARTRY}$, $\overline{L2\ BR}$, write back data, reset dirty bit (clean block address–only)	
01100	X	X	X	Hit	Invalidate tag (kill block address–only)	

NOTES:

1. If a line fill is going to replace a dirty line and the cast out buffer (COB) is full, the line fill will be cancelled. (Unless the line fill is a write which hits in the COB. In this case, the line fill will occur.)
2. If a burst read misses the cache but hits the COB, the MPC2605 will supply the data from the COB, but not perform a line fill.
3. If $\overline{ARTRY}$ is asserted during a line fill to replace a dirty line, the line fill will be cancelled, the to–be–replaced line will recover its old tag (valid, dirty, tag field), and the COB goes back to an invalid condition, even if the line fill is a burst write to the line in the COB.
4. If $\overline{ARTRY}$ is asserted during a read hit, the MPC2605 will abort the process.
5. If a processor burst write occurs right after a snoop write that was a cache hit, the MPC2605 will invalidate the line. If the snoop was a cache miss, the MPC2605 will not perform a write allocate.
6. If a processor burst write occurs right after a snoop read that was a cache hit, the MPC2605 will update the cache and clear the dirty bit. If the snoop was a cache miss, the MPC2605 will perform a write allocate.

MPC2605 RESPONSE TO CHIPSET TRANSFER ATTRIBUTES

TT0 – TT4	Tag Status	MPC2605 Response
00100 X0010 X1110	Hit Clean	Invalidate line
00100 X0010 X1110	Hit Dirty	$\overline{ARTRY}$ and $\overline{L2\ BR}$ write back data, invalidate line (see Note)
00000 X1010	Hit Clean	No action
00000 X1010	Hit Dirty	$\overline{ARTRY}$ and $\overline{L2\ BR}$, write back data, reset dirty bit (see Note)
0110X 00110	Hit	Invalidate (kill block)

NOTE: In all snoop push cases, $\overline{BR}$ is sampled the cycle after the ARTRY window. If $\overline{BR}$ is asserted in this cycle, $\overline{L2\ BR}$ will be immediately negated and an assertion of $\overline{L2\ BG}$ will be ignored.

TRANSFER ATTRIBUTES GENERATED FOR L2 COPYBACK

TT0 – TT4	$\overline{TBST}$	$\overline{CI}$	$\overline{WT}$
00010	0	1	1

SYSTEM USAGE AND REQUIREMENTS

The MPC2605 is a high–performance look–aside cache for PowerPC systems. A look–aside cache is defined as a cache that resides on the same bus as the processor, the memory controller, the DMA bridge, and the arbiter. The advantage of a look–aside cache is that, when the processor makes a memory request, the cache adds no delay to the memory controller's response time in the event that the request cannot be satisfied by the cache. However, there are certain system requirements that must be met before a look–aside cache can be used.

Comprehension of $\overline{\text{L2 CLAIM}}$

Because the memory controller sees every memory request that is issued by the processor, there must be a mechanism for the cache to inform the memory controller that it has detected a cache hit and that it will satisfy the processor's request. The MPC2605 has a signal called $\overline{\text{L2 CLAIM}}$ that is asserted whenever a cache hit is detected. Any memory controller with which the MPC2605 is to be used must have the ability to monitor this signal.

Pipeline Depth

The 60X bus allows pipelining of transactions such that a new transaction can be initiated before a previous transaction has fully completed. The level of pipelining that exists on the bus is defined by how many new data transactions have been initiated while the original transaction is still being processed. By this definition the MPC2605 can only work in a one level deep pipeline. In the presence of transactions for which it has asserted $\overline{\text{L2 CLAIM}}$, the MPC2605 can control the level of pipelining by delaying its assertion of $\overline{\text{AACK}}$. However, for transactions that it cannot control, the MPC2605 is dependent upon the memory controller to control pipeline depth. Thus, another system requirement for the use of the MPC2605 is the use of a memory controller that only allows one level deep of pipelining on the 60X bus.

Bus Mastering

Bus mastering is a requirement only for systems which seek to use the MPC2605 as a copyback, as opposed to a write–through, cache. The requirement is that the system arbiter must have the ability to allow the MPC2605 to become a bus master. Specifically, the system arbiter must be able to recognize assertions of $\overline{\text{L2 BR}}$ and must have the ability to assert $\overline{\text{L2 BG}}$ and $\overline{\text{L2 DBG}}$.

These are the only requirements above and beyond what should already exist in a PowerPC system. All other necessary control signals are signals that are required for the processor to communicate with the memory controller, the DMA bridge, and the arbiter.

CONFIGURATION PINS

The MPC2605 has five configuration pins: CFG0, CFG1, CFG2, CFG3, and CFG4.

CFG0 – CFG2

These three configuration pins are used to implement the different cache sizes supported by the MPC2605.

256KB: For a single chip implementation, CFG0, CFG1, and CFG2 should all be tied low.

512KB: This two chip configuration requires both parts to have CFG0 tied low and CFG1 tied high. CFG2 is used as a chip select when it matches the value of A26. Therefore, one device must have CFG2 tied low and the other device must have CFG2 tied high.

1MB: The four chip configuration requires all four devices to have CFG0 tied high. The CFG1, CFG2 vector becomes the chip select when it matches the A25, A26 vector. Therefore, each of the four parts must have a unique value of the CFG[1:2] vector.

CFG3

Many core logic chipsets are designed such that the DMA bridge and the memory controller are resident in the same device. In such systems there is internal communication between these two functional units. Bus transactions generated by the DMA bridge are solely for the purpose of keeping the system coherent. They are not explicit requests from memory that have data tenures associated with them. However, some chipsets are designed with the memory controller and the DMA bridge partitioned into different devices. In systems such as these, transactions generated by the DMA bridge are true memory requests that have data tenures associated with them. These are called snoop data tenures. Because these two types of systems are fundamentally different, the MPC2605 must know in which type of system it is resident in order to respond properly to the different types of transactions. For systems that do not have snoop data tenures, CFG3 must be tied high. For systems that do use snoop data tenures, CFG3 must be tied low.

CFG4

When the MPC2605 asserts $\overline{\text{L2 CLAIM}}$ to signal to the memory controller that a cache hit has been detected, it is taking control of the address and data tenures of the transaction (see **60X Bus Operation** and **Memory Coherence**). This means that the MPC2605 will assert $\overline{\text{AACK}}$ to end the address tenure, and it will assert $\overline{\text{TA}}$ as needed for the data tenure. If the data bus is idle when a processor request is initiated, the MPC2605 will assert $\overline{\text{AACK}}$ the cycle after $\overline{\text{TS}}$ was asserted. If the data bus is busy when the request is made, the MPC2605 will wait until the outstanding data tenure has completed before asserting $\overline{\text{AACK}}$. By holding off on the assertion of $\overline{\text{AACK}}$, the MPC2605 enforces the policy of, at most, two outstanding data transactions at any one time. Tying CFG4 low prevents the MPC2605 from asserting $\overline{\text{AACK}}$ to end transactions for which it has asserted $\overline{\text{L2 CLAIM}}$. In systems that tie CFG4 low it is necessary for the memory controller to assert $\overline{\text{AACK}}$ for all transactions. This allows the DMA bridge to initiate snoop transactions (as defined later) even when there are two outstanding data transactions. If this type of system is implemented, the arbiter must ensure

that the processor's bus grant is negated once there are two outstanding data transactions. It is expected that most systems will tie CFG4 high.

RESET/INITIALIZATION

To ensure proper initialization and system functionality, the HRESET pin of the MPC2605 should be connected to the same signal that is used to reset the processor. When HRESET is negated, the MPC2605 commences an internal initialization sequence to clear all of the valid bits in the cache. The sequence takes approximately 4000 clock cycles. During this time the MPC2605 will not participate in any bus transaction that occurs. All transactions are, however, monitored so that, regardless of when the initialization sequence completes, the MPC2605 is prepared to take action on the next transaction initiated by the processor.

At some point after this 4000 cycle sequence, the MPC2605 will detect its first cache hit. At this time the system will experience its first assertion of L2 CLAIM. If the memory controller must be configured via software to comprehend assertions of L2 CLAIM, this configuration operation must have completed by this time. For systems that cannot guarantee that this requirement is met, it is necessary to disable the MPC2605 until such time as this configuration can be guaranteed. Disabling the MPC2605 can be accomplished by asserting L2 UPDATE INH sometime during reset and negating it when it is deemed safe for caching to commence.

60X BUS OPERATION

5

All transactions have what is called an address tenure. An address tenure is a set number of bus cycles during which the address bus and its associated control signals are being used for the transaction at hand. In general, there are two types of transactions. Those that only have address tenures, called address–only transactions. And those that require the use of the data bus and therefore will have a data tenure. These transactions are called data transactions. This section describes how address and data tenures are defined as viewed by the MPC2605.

Address Tenures

Address tenures on the 60X bus are fairly well defined. They start with an assertion of TS by a device that has been granted the bus by the system arbiter. This device is called the bus master for this transaction. At the same time that TS is asserted, the bus master also drives the address and all other relevant control signals that define the transaction. TS is only asserted for one cycle but all other signals are held valid by the bus master until some other device asserts AACK. The device that asserts AACK becomes the slave to this transaction. Typically, the slave is the memory controller, although for transactions that are cache hits the MPC2605 becomes the slave by driving L2 CLAIM.

Transactions can be aborted by any device on the bus by asserting ARTRY. ARTRY may be asserted at any time after TS is asserted, but must be held through the cycle after AACK is asserted. This cycle is referred to as the ARTRY window, since it is the cycle in which all devices sample ARTRY to determine if the address tenure has completed successfully.

If an address tenure is not aborted by an assertion of ARTRY, then the next bus master is free to assert TS, the cycle after the ARTRY window to start a new address tenure. If ARTRY is asserted in the ARTRY window, all devices that are not asserting ARTRY must negate their bus request in the following cycle. This next cycle is called the BR window. The purpose of this protocol is to give immediate bus mastership to the device that asserted ARTRY with the expectation that that device will take this opportunity to clean up whatever circumstances caused it to assert ARTRY. Typically, this involves writing data back to memory to maintain coherence in the system.

Data Tenures

Data tenures are more complicated to define than address tenures. They require two conditions to start: an assertion of TS that initiates a data transaction and a qualified assertion of the bus master's data bus grant. For a data bus grant to be considered qualified, no device on the bus may be asserting DBB in the cycle that the data bus grant is asserted.

Data transactions come in two types: single–beat transactions and burst transactions. The type is determined by the state of TBST during the address tenure of the transaction. If the bus master asserts TBST, the transaction is a burst transaction and will require four assertions of TA in order to complete normally. If TBST is negated during the address tenure, the transaction only requires one assertion of TA, thus the name single–beat.

Which device drives the data bus during a data transaction depends upon whether the transaction is a read or a write. For a read transaction, the slave device drives the data bus. For a write transaction, the master drives the data bus. In all data transactions, the slave device asserts TA to indicate that either valid data is present on the bus, in the case of a read; or that it is reading data off the data bus, in the case of a write. The master device asserts DBB the cycle after it has been granted the data bus and keeps it asserted until the data tenure has completed.

A data tenure can be aborted in two different ways. The address tenure for the transaction can be aborted by an assertion of ARTRY. Or, the slave device may assert TEA to indicate that some error condition has been detected. Either event will prematurely terminate the data tenure.

Data Streaming

For the majority of data transactions there must be a wait state between the completion of one data tenure and the start of the next. This turnaround cycle avoids the contention on the data bus that would occur if one device starts driving data before another device has had a chance to turn off its data bus drivers. When a cache read hit is pipelined on top of another cache read hit, there is no need for this turnaround cycle since the same device will be driving the data bus for both data tenures. The 60X bus has the ability to remove this unnecessary wait state and allow back–to–back cache read hits to stream together. This ability is only enabled if the system is put into Fast L2 mode. Note that not all PowerPC processors support Fast L2 mode.

One of the requirements for taking advantage of this data streaming capability is that the system arbiter must be sophisticated enough to identify situations in which streaming may occur. Upon recognizing these situations, it must assert the processor's data bus grant in the cycle coincident with the fourth assertion of TA of the first cache read, so that

the data tenure for the second cache read may commence in the next cycle.

Because it only recognizes qualified assertions of $\overline{\text{CPU DBG}}$, the MPC2605 must not be aware of the processor's assertions of $\overline{\text{DBB}}$. This means that the $\overline{\text{DBB}}$ pin of the MPC2605 must be tied to a pullup resistor rather than connected to the system $\overline{\text{DBB}}$ to which all other devices are connected. This forces the system arbiter to a level of sophistication such that it only supplies qualified data bus grants and thus the $\overline{\text{DBB}}$ signal is unnecessary to the whole system.

Note: In a multi–chip configuration each MPC2605 device acts as an independent cache. Zero wait state data streaming can only occur if the back to back read hits occur in a given device. If the second read hit is not in the device as the first read hit, a wait state will occur between the two data tenures (2–1–1–1–2–1–1–1 timing).

Data Bus Parking

The MPC2605 has the ability to respond to a processor read or write hit starting in the cycle after the processor has asserted $\overline{\text{TS}}$. This is referred to as a 2–1–1–1 response. However, even though the MPC2605 has this ability, it is dependent upon the system to allow this quick of a response to occur. As discussed above, a data tenure cannot start until the master has been given a qualified bus grant. In order for the data tenure to start the cycle after $\overline{\text{TS}}$ is asserted, the data bus must be granted in the cycle coincident with the assertion of $\overline{\text{TS}}$. At bus speeds of 66 MHz it is extremely difficult for an arbiter to detect an assertion of $\overline{\text{TS}}$ and itself assert $\overline{\text{CPU DBG}}$ in the same cycle. In order to realistically allow this situation to occur, $\overline{\text{CPU DBG}}$ must be asserted independent of the processor's assertion of $\overline{\text{TS}}$.

Data bus parking is a system feature whereby the processor always has a qualified data bus grant when the data bus is idle. It is also a requirement for systems which seek to take advantage of the 2–1–1–1 response time capabilities of the MPC2605. This feature is typically present in arbiters that have the level of sophistication necessary to support data streaming. But it is also a feature of systems that do not even have a data bus arbiter. In these systems the data bus grant of every device in the system is tied to ground. The assertion of $\overline{\text{DBB}}$ by the current data bus master effectively removes the qualified data bus grant of all devices in the system, including its own. Note that in systems that have no data bus arbiter that it is impossible to take advantage of data streaming.

There is another caveat associated with data bus parking. Care must be taken when using data bus parking along with Fast L2 mode. In normal bus mode when the processor reads data off the bus, it will wait one cycle before passing the data on to internal functional units. The purpose of this one cycle waiting period is to check for an assertion of $\overline{\text{DRTRY}}$, which invalidates the data that has been already read. One of the advantages of running the processor in Fast L2 mode is that this internal processor wait state is removed.

A problem will arise, however, if the processor is given data the cycle after $\overline{\text{TS}}$ is asserted, as is possible with the MPC2605, and the transaction is aborted by some other device asserting $\overline{\text{ARTRY}}$. Because the processor will not sample $\overline{\text{ARTRY}}$ until two cycles after the assertion of $\overline{\text{TS}}$, the data read off the bus will have already been forwarded to the internal functional units. Thus, incorrect results may occur in the system.

To avoid this situation in a system that seeks to run Fast L2 mode with the data bus parked, there must be a guarantee that $\overline{\text{ARTRY}}$ will never be asserted for cache read hits. This is a further requirement to be imposed upon the DMA bridge and the memory controller. If this guarantee cannot be made, the data bus cannot be parked when running in Fast L2 mode.

Processor Reads

When the processor issues a read transaction, the MPC2605 does a tag lookup to determine if this data is in the cache. If there is a cache hit and $\overline{\text{CI}}$ is not asserted, the MPC2605 will assert $\overline{\text{L2 CLAIM}}$ and supply the data to the processor when the data tenure starts.

If the processor issues a cache–inhibited read ($\overline{\text{CI}}$ asserted) and the MPC2605 detects a cache hit to a non–dirty, or clean, cache line, the line will be marked invalid. If the cache–inhibited read hits a dirty line, the MPC2605 will assert $\overline{\text{ARTRY}}$ and write the dirty line back to memory.

If the read misses in the cache, the MPC2605 will perform a linefill only if it is a burst read and it is not marked cache–inhibited. During a linefill, the MPC2605 stores the data present on the bus as it is supplied by the memory controller.

Processor Writes

The conditions for asserting $\overline{\text{L2 CLAIM}}$ for processor writes are almost the same as for processor reads. There must be a cache hit and $\overline{\text{CI}}$ must not be asserted. In addition, however, $\overline{\text{WT}}$ must not be asserted. Single beat writes that are marked either write–through or cache–inhibited that hit in the cache cause the MPC2605 to assert $\overline{\text{ARTRY}}$ and write the dirty line back to memory.

Transaction Pipelining

As explained in **Pipeline Depth**, the MPC2605 can only handle one level of pipelining on the bus. Since the assertion of $\overline{\text{L2 CLAIM}}$ gives it the ability to assert $\overline{\text{AACK}}$, the MPC2605 has the ability to control this pipeline depth for transactions that are cache hits by delaying its assertion of $\overline{\text{AACK}}$.

Pipelined cache hits are transactions that hit in the cache but occur while there is still an outstanding data transaction on the bus. The timing of the assertion of $\overline{\text{AACK}}$ for a pipelined cache hit is dependent upon the completion of the previous transaction. For explanation purposes, the previous transaction will be referred to as transaction one. The pipelined cache hit will be referred to as transaction two.

If transaction one is a cache hit, the MPC2605 will be the slave device for the transaction. Since, for burst operations, the MPC2605 always asserts $\overline{\text{TA}}$ for four consecutive clock cycles, the end of the data tenure for transaction one will be at a deterministic clock cycle. In this case, $\overline{\text{AACK}}$ for transaction two can be asserted coincident with the last assertion of $\overline{\text{TA}}$ for transaction one. If transaction one is not a cache hit, the MPC2605 will wait until after the data tenure for transaction one has completed before asserting $\overline{\text{AACK}}$ to complete the address tenure of transaction two.

MEMORY COHERENCE

When a processor brings data into its on–chip cache and modifies it, a situation has arisen in which the main memory

now contains irrelevant, or stale, data. Given that most systems support some form of DMA there must exist a means by which the processor is forced to write this modified, or dirty, data back to main memory. The DMA bridge is responsible for generating bus transactions to ensure that main memory locations accessed by DMA operations do not contain stale data. These transactions, called snoops, come in three different categories, each of which will be discussed below.

Snoops cause the processor and the MPC2605 to check to see if they have dirty copies of the memory location specified in the snoop transaction. If either device does have a dirty copy it will assert $\overline{\text{ARTRY}}$ and make use of the opportunity presented in the BR window to write this data back to main memory.

Situations can arise where a cache line is dirty in both the processor's L1 cache and in the MPC2605. In cases such as these, snoop transactions should cause the processor to write its data back to memory since it is by definition more recent than the data in the MPC2605. Since $\overline{\text{ARTRY}}$ is a shared signal and it cannot be determined which devices are driving it, the MPC2605 samples $\overline{\text{CPU BR}}$ in the BR window to determine if the snoop hit a dirty line in the L1 cache. If $\overline{\text{CPU BR}}$ is asserted during this window, the MPC2605 will defer to the processor.

Snoop Reads

A snoop read causes dirty data to be written back to memory but allows both the L1 and L2 to keep a valid copy. In cases where the snoop hits a dirty cache line in the processor, the MPC2605 will update its contents as the processor writes the data back to main memory.

Snoop reads can be implemented in two ways. One is that the DMA bridge can issue a clean transaction (TT[0:4] = 00000). The other is that the DMA bridge can do a read transaction (TT[0:4] = x1010). If the DMA bridge does a read transaction, the MPC2605 determines that it is a snoop read rather than a processor read by the state of $\overline{\text{CPU BG}}$ the cycle before $\overline{\text{TS}}$ was asserted. If the processor was not granted the bus then the transaction had to have been issued by the DMA bridge and is therefore a snoop read.

Snoop Writes

Snoop writes also cause dirty data to be written back to main memory. The difference from a snoop read is that the cache line must then be invalidated in both the processor's cache and in the L2 cache. When the processor writes data back to memory in response to a snoop write, the MPC2605 will not cache the data as it appears on the bus. If a valid copy resides in the cache, the MPC2605 will invalidate it.

Again there are multiple transactions that can be used by the DMA bridge to implement a snoop write. It can issue a flush transaction (TT[0:4] = 00100), a read with intent to modify (TT[0:4] = x1110), or a write with flush (TT[0:4] = 00010). As with snoop reads, the MPC2605 distinguishes between processor issued data transactions and snoop transactions by the state of $\overline{\text{CPU BG}}$ in the cycle previous to the assertion of $\overline{\text{TS}}$.

Snoop Kills

Kills are snoops that cause cache entries to be immediately invalidated, regardless of whether they are dirty. This saves time if the DMA operation is going to modify all the data in the cache line. To implement a snoop kill the DMA bridge can issue a kill transaction (TT[0:4] = 01100) or a write with kill (TT[0:4] = 00110).

TWO/FOUR CHIP IMPLEMENTATION

Multiple Castouts

Because each MPC2605 has its own castout buffer (COB), it is possible for situations to arise in which more than one device needs to do a copyback operation. Under normal circumstances each device will enter castout conditions at different times. In these cases, when a device determines that it needs to do a castout, the $\overline{\text{L2 BR}}$ signal is first sampled. If $\overline{\text{L2 BR}}$ is already asserted then it is clear that another device is also in a castout situation. The late device will wait until $\overline{\text{L2 BR}}$ is negated before continuing in its attempt to perform its castout.

Because of the BR window protocol associated with assertions of $\overline{\text{ARTRY}}$, it is possible for a situation to arise where device two is waiting for device one to do its castout before asserting $\overline{\text{L2 BR}}$. If there is an assertion of $\overline{\text{ARTRY}}$ by a device other than device one, device one is required to negate $\overline{\text{L2 BR}}$ in the BR window. In order to prevent device two from interpreting device one's negation of $\overline{\text{L2 BR}}$ as an indication that device one has completed its castout, a simple arbitration mechanism is used. All devices have a simple two–bit counter that is synchronized such that all counters always have the same value. For the purposes of performing a castout operation, a given pair can only assert $\overline{\text{L2 BR}}$ if the counter is equal to its value of CFG[1:2]. This simple mechanism prevents more than one device from asserting $\overline{\text{L2 BR}}$ in the same cycle and therefore not being cognizant of the another device's need to perform a castout.

Snoop Hit Before Castout

The other situation that can cause problems with a shared bus request occurs when a snoop hits a dirty line in one of the MPC2605 devices. If device one has a cache line in its COB, it will assert $\overline{\text{L2 BR}}$ so that it may perform a castout operation. If a snoop hits a dirty line in device two, it will assert both $\overline{\text{ARTRY}}$ and $\overline{\text{L2 BR}}$ so that it can write the snoop data back to main memory. When device one detects that $\overline{\text{ARTRY}}$ has been asserted, it needs to be made aware that device two needs to request the bus. Otherwise, at the same time that device two is asserting $\overline{\text{L2 BR}}$, device one will attempt to conform to the BR window protocol and negate $\overline{\text{L2 BR}}$. This situation is avoided by device one sampling $\overline{\text{FDN}}$ when it detects that $\overline{\text{ARTRY}}$ has been asserted. If $\overline{\text{FDN}}$ is asserted at the same time as $\overline{\text{ARTRY}}$ is asserted, device one will recognize that device two is asserting $\overline{\text{ARTRY}}$. device one will then high–Z $\overline{\text{L2 BR}}$ so that there will not be contention when device two is asserting $\overline{\text{L2 BR}}$.

MULTIPROCESSING

The MPC2605 can be used as a common cache for up to four processors. For each processor there is a bus request, bus grant, and data bus grant signal pin on the MPC2605. Each of these pins needs to be connected to the respective processor's arbitration signals in the system.

The MPC2605 treats multiple processors as one processor. Thus, the same restrictions on pipelining depth are true with regard to how many processor transactions can be outstanding at any one time. There can only be one data

transaction from ANY processor pipelined on top of a current data transaction that was issued by ANY processor.

The data tenures for all processors must be performed in the same order as the address tenures on a system–wide basis. If processor one makes a request and then processor two makes a request, processor one's data tenure must precede processor two's data tenure. Note that this is not a 60X bus restriction, but rather a restriction necessary for proper operation of the MPC2605.

The MPC2605 keeps coherent with the L1 caches of multiple processors as defined by the MESI (modified–exclusive–shared–invalid) protocol without actually implementing the protocol. This is possible for two reasons. Since the MPC2605 is a look–aside cache, all transactions are monitored by all devices on the bus. Also, the MPC2605 cannot, on its own, modify data. Thus, if one processor requests exclusive access to a cache line, it is not necessary for the MPC2605 to invalidate its copy of the data, as would be required under the MESI protocol. If a second processor requests the same data, the transaction will cause the first processor to assert $\overline{\text{ARTRY}}$. This will prevent the MPC2605 from supplying stale data to the second processor.

As discussed in **Data Bus Parking**, care must be taken when parking the data bus in Fast L2 mode. By the nature of MP systems running under the MESI protocol there will be assertions of $\overline{\text{ARTRY}}$ to abort cache read hits. Thus, in an MP system, the data bus cannot be parked to any processor if the system is to be run in Fast L2 mode.

$\overline{\text{PWRDN}}$

An assertion of $\overline{\text{PWRDN}}$ will cause the MPC2605 to go into a low–power sleep state. This state is entered after $\overline{\text{PWRDN}}$ is synchronized and both the address and data buses are idle. All data is retained while in the sleep state.

The behavior of the MPC2605 upon negation of $\overline{\text{PWRDN}}$ is dependent upon the state of $\overline{\text{WT}}$ at the rising edge of $\overline{\text{HRESET}}$. If $\overline{\text{WT}}$ is asserted at reset, the MPC2605 will invalidate all cache entries when $\overline{\text{PWRDN}}$ is negated. If $\overline{\text{WT}}$ is negated at reset, the MPC2605 will leave all cache entries as they were prior to the assertion of $\overline{\text{PWRDN}}$. However, in this situation, the system designer must insure that no bus activity occur within two microseconds of the negation of $\overline{\text{PWRDN}}$.

Note: While in the sleep state the MPC2605 does not disable its internal clock network. The low power state current stated in this specification assumes that the system clock is not toggling.

ASYNCHRONOUS SIGNALS

The MPC2605 supports four asynchronous control signals. These signals were originally defined in the PowerPC reference platform (PReP) specification. Because these signals are defined to be asynchronous, the MPC2605 must synchronize them internally. This process takes eight clock cycles. Thus, to guarantee recognition by the MPC2605, assertions of any one of these signals must last a minimum of eight clock cycles.

$\overline{\text{L2 FLUSH}}$

When $\overline{\text{L2 FLUSH}}$ is asserted, the MPC2605 initiates an internal sequence that steps through every cache line present. Valid lines that are clean are immediately marked invalid. Valid lines that are dirty must be written back to main memory.

To keep memory up to date, the MPC2605 must still monitor all transactions on the bus. Any transaction that is not a processor burst write will cause the MPC2605 to assert $\overline{\text{ARTRY}}$. Burst writes cause the MPC2605 to do a lookup on the affected address and mark the line invalid if it is present.

Because the MPC2605 must still monitor all transactions, it cannot use the tag RAM for the flush sequence unless there is a guarantee that no new transaction will be initiated on the bus. The only way to ensure that no new transactions will occur is for the MPC2605 to be granted the bus. Thus, upon entering the sequence initiated by the assertion of $\overline{\text{L2 FLUSH}}$, the MPC2605 will assert $\overline{\text{L2 BR}}$. As soon as $\overline{\text{L2 BG}}$ is asserted, the MPC2605 can start stepping through the tag RAM entries.

$\overline{\text{L2 FLUSH}}$ need not be held asserted for the flush sequence to complete. Once started the sequence will run to completion unless overridden by an assertion of $\overline{\text{HRESET}}$.

$\overline{\text{L2 MISS INH}}$

When $\overline{\text{L2 MISS INH}}$ is asserted, the MPC2605 will not load any new data into the cache. The data already present will remain valid and the MPC2605 will respond to cache hits. This condition only lasts as long as $\overline{\text{L2 MISS INH}}$ is asserted. When $\overline{\text{L2 MISS INH}}$ is negated, the MPC2605 will start to bring new data into the cache when there are cache misses.

$\overline{\text{L2 TAG CLR}}$

When $\overline{\text{L2 TAG CLR}}$ is asserted, the MPC2605 will invalidate all entries in the cache. This internal sequence is the same as the one initiated by an assertion of $\overline{\text{HRESET}}$. During this sequence, the MPC2605 will not participate in any bus transaction. However, it will keep track of all bus transactions so that when the sequence is finished, the MPC2605 can immediately participate in the next bus transaction.

As is the case with assertions of $\overline{\text{L2 FLUSH}}$, an assertion of $\overline{\text{L2 TAG CLR}}$ need not be held for the duration of the sequence. Once asserted the sequence will run to completion regardless of the state of $\overline{\text{L2 TAG CLR}}$.

$\overline{\text{L2 UPDATE INH}}$

When $\overline{\text{L2 UPDATE INH}}$ is asserted, the MPC2605 is disabled from responding to cacheable transactions. Bus transactions continue to be monitored so that as soon as $\overline{\text{L2 UPDATE INH}}$ is negated, the MPC204GA can participate in the next transaction.

READ HIT/WRITE HIT

Figure 1 shows a read hit from an idle bus state. The MPC2605 asserts $\overline{\text{L2 CLAIM}}$ the cycle after $\overline{\text{TS}}$ to inform the memory controller that there is a cache hit and the cache will control the rest of the transaction. $\overline{\text{L2 CLAIM}}$ is held through the cycle after $\overline{\text{AACK}}$ is asserted. Since there are no active data tenures from previous transactions, the MPC2605 asserts $\overline{\text{AACK}}$ the cycle after $\overline{\text{TS}}$ is asserted. Note there must be a qualified assertion of $\overline{\text{CPU DBG}}$ in the same cycle as the assertion of $\overline{\text{TS}}$ for the MPC2605 to respond with $\overline{\text{TA}}$ in the next cycle. $\overline{\text{CPU DBG}}$ does not affect the timing of $\overline{\text{L2 CLAIM}}$ or $\overline{\text{AACK}}$.

The write hit timing is virtually the same. The only difference is the processor drives the data instead of the MPC2605.

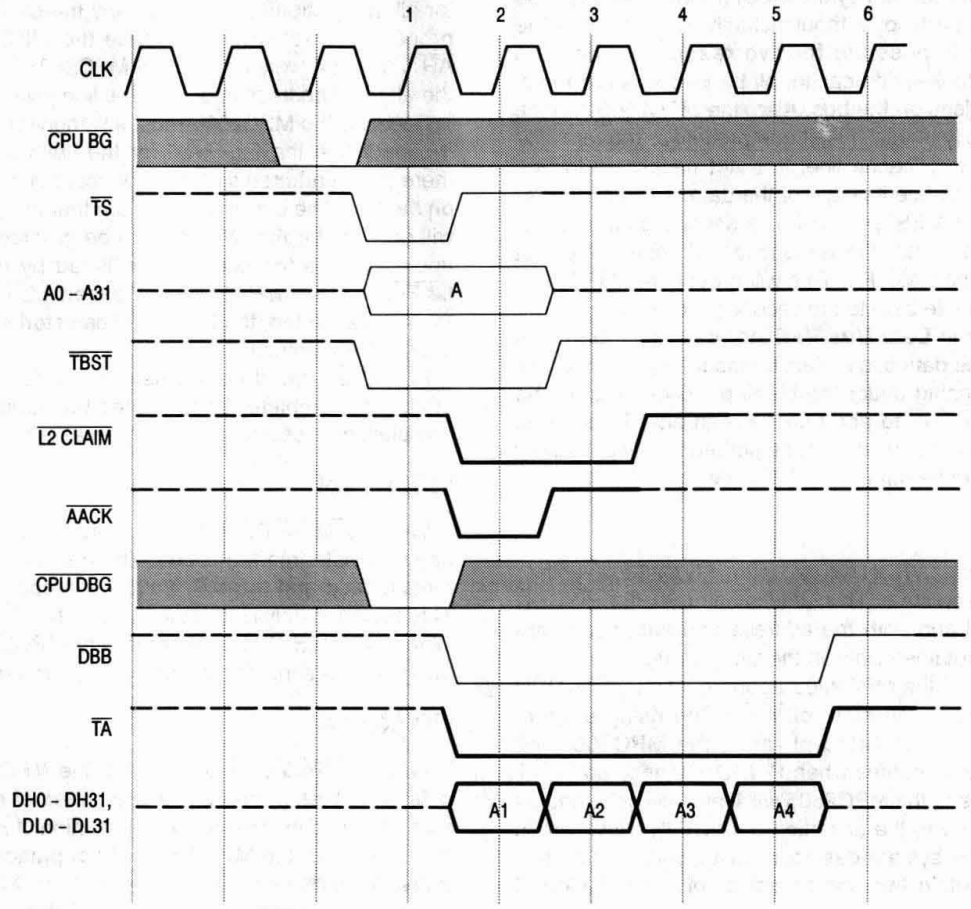
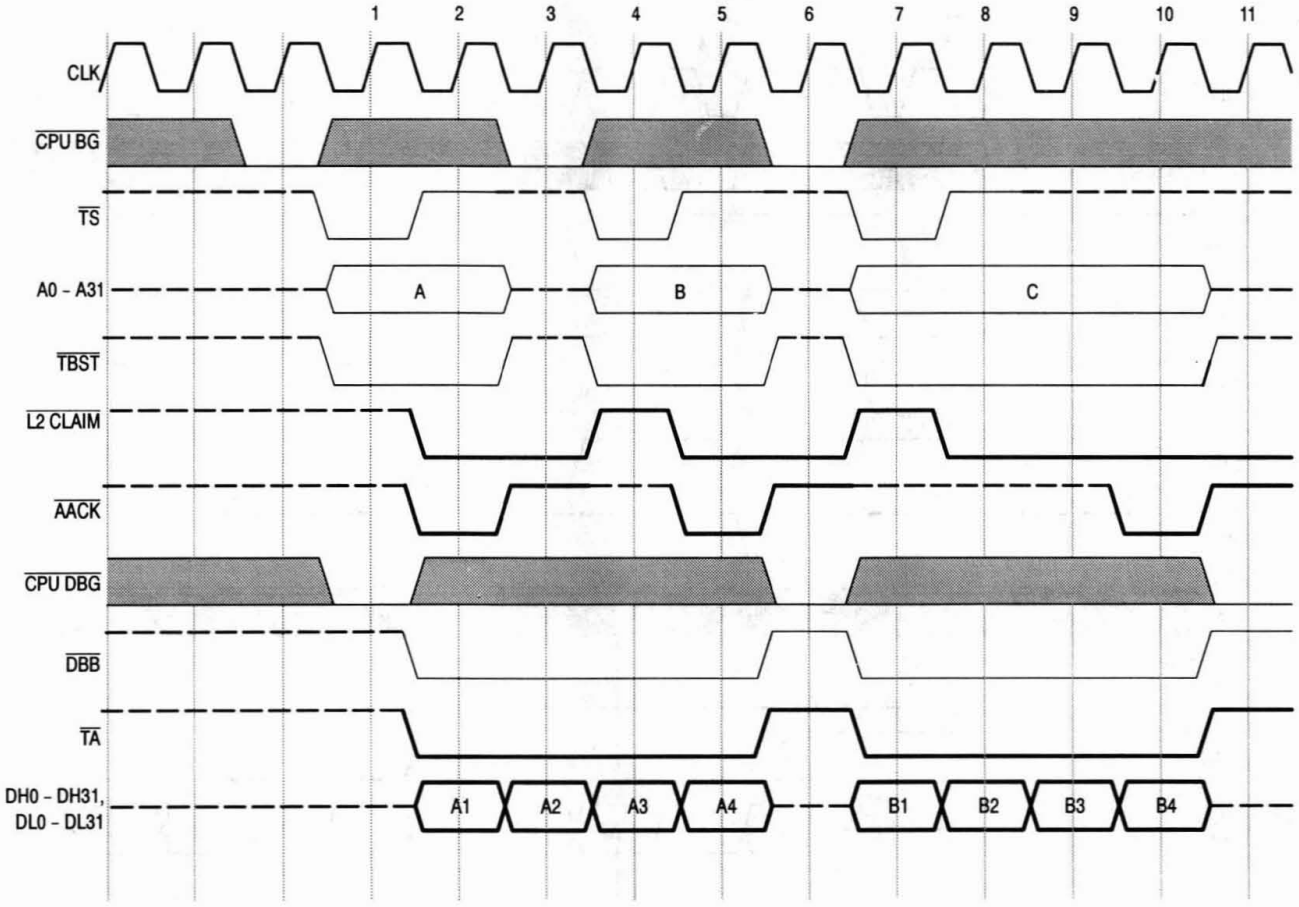


Figure 1. Burst Read (or Write) Hit

MULTIPLE READ/WRITE HITS (NORMAL BUS MODE)

Figure 2 is an illustration of MPC2605 pipeline depth limit with multiple read hits. The MPC2605 supports only one level of address pipelining for data transfer. Therefore, it must hold off on its assertion of $\overline{\text{AACK}}$ for a pipelined $\overline{\text{TS}}$ until the data tenure for the first $\overline{\text{TS}}$ is done. The MPC2605 asserts $\overline{\text{AACK}}$ at the same time as the fourth $\overline{\text{TA}}$ for data tenures that it controls.



LEGEND

——— Signal driven to the MPC2605

——— Signal driven by the MPC2605

– – – High–Z

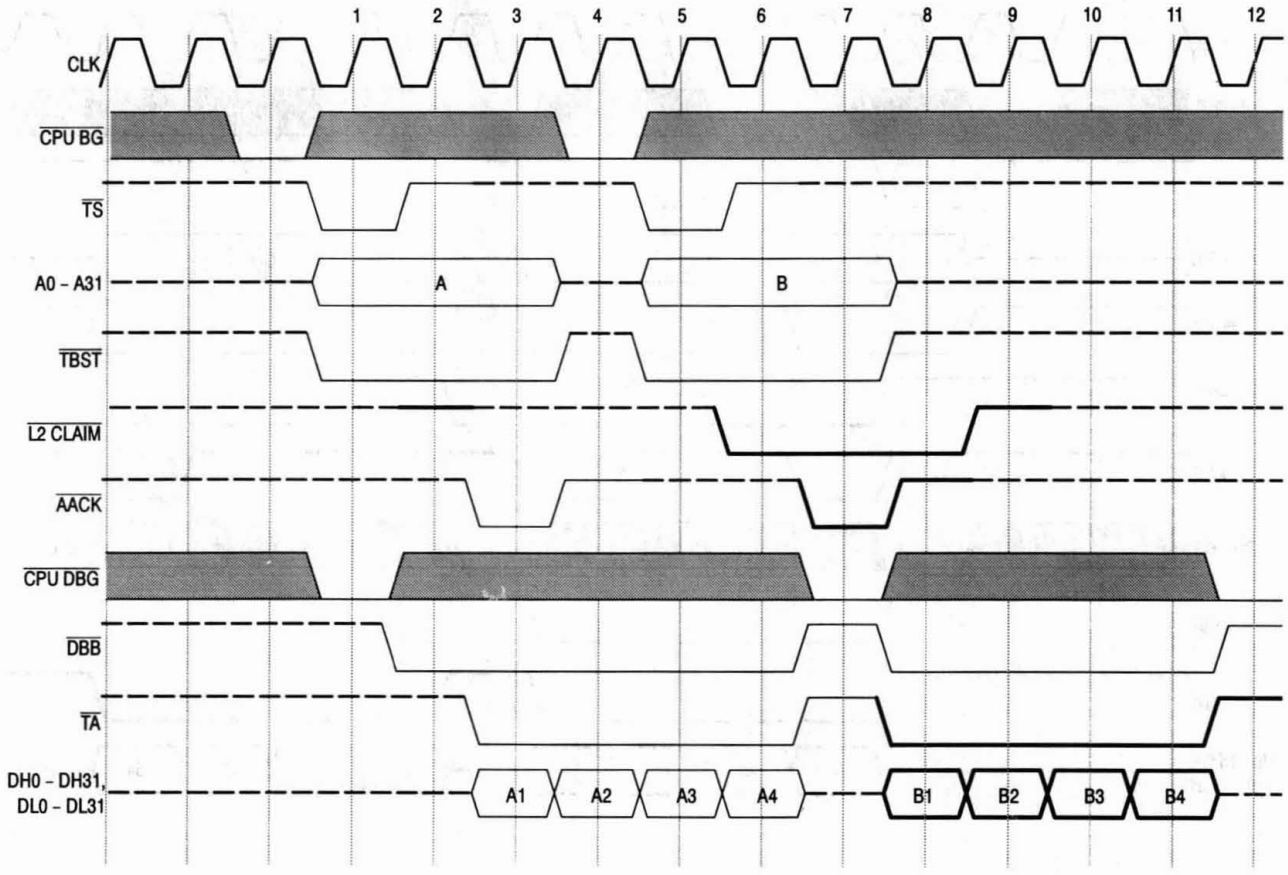
Figure 2. Multiple Burst Read (or Write) Hits

5

READ MISS (NORMAL BUS MODE)

Figure 3 is an illustration of MPC2605 pipeline depth with a read miss followed by a read hit.

For illustration purposes the read miss is shown as a 3–1–1–1 response from memory. $\overline{AACK}$ for the second access is not driven true until the cycle after the fourth $\overline{TA}$ of the read miss. This is because the MPC2605 is not in control of $\overline{TA}$ for the first access and must, therefore, wait until the first access' data tenure is complete before it can drive $\overline{AACK}$ true for the read hit.



LEGEND

Signal driven to the MPC2605

Signal driven by the MPC2605

High–Z

Figure 3. Read Miss Followed by a Burst Read Hit for MPC603/604

MULTIPLE READ HITS (FAST L2 MODE)

Back to back pipelined burst read hits for the MPC604 in Fast L2 mode, also called data streaming mode, are shown in Figure 4. Note that $\overline{\text{CPU DBG}}$ is negated except for the cycles coincident with the fourth $\overline{\text{TA}}$ of each data tenure. This is a requirement for data streaming. Note also that $\overline{\text{DBB}}$ is not shown. For proper operation in Fast L2 mode the $\overline{\text{DBB}}$ pin of the MPC2605 must be tied to a pull–up resistor.

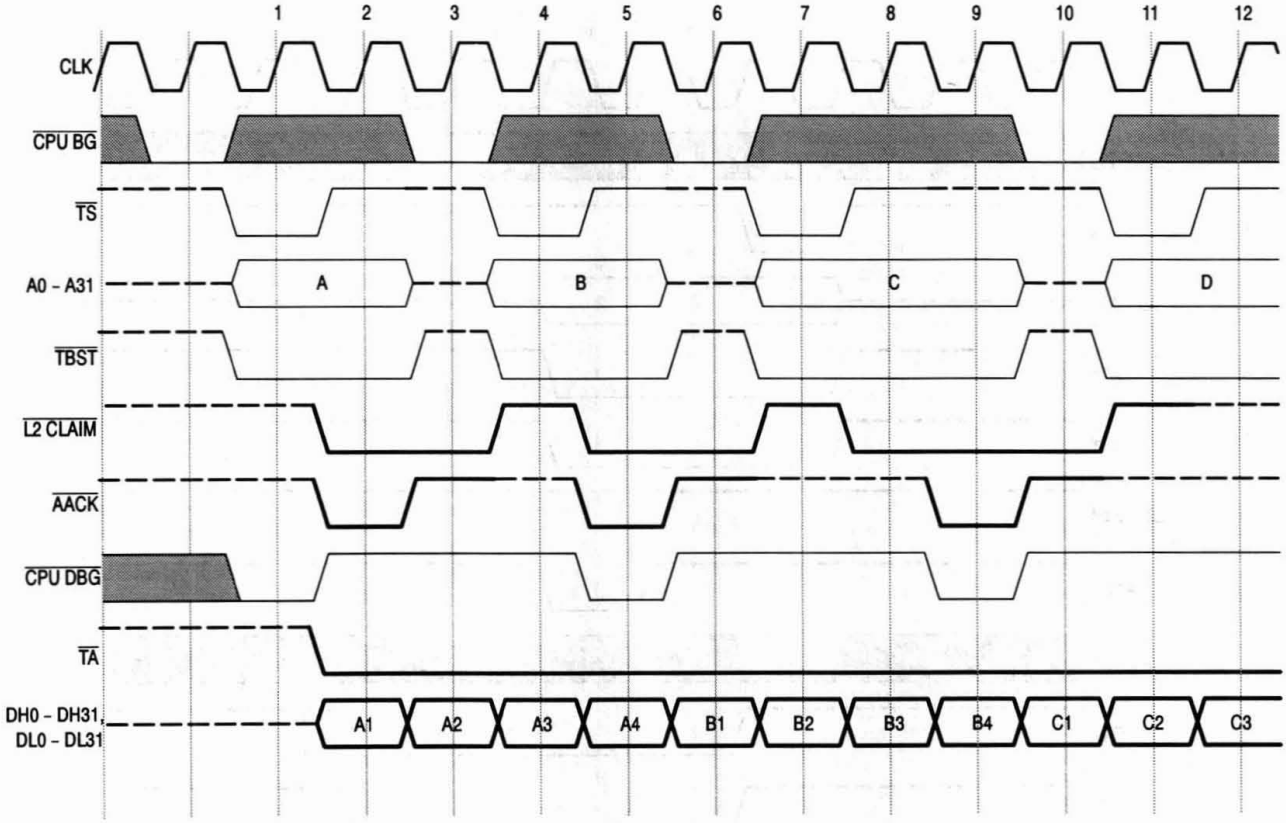


Figure 4. Multiple Burst Read Hits in Fast L2 Mode

5

WRITE THROUGH BURST WRITE HIT

Figure 5 shows the fastest possible burst write hit to a write–through mode L2 cache line, read miss or write miss processing that replaces a clean line. For these operations MPC2605 will not assert any signals on the 60X bus. A cache line is considered write through if $\overline{WT}$ is asserted by the processor when it asserts $\overline{TS}$.

The speed at which a write–through operation completes is solely dependent on the memory controller. The timing shown here assumes that the memory controller has a write buffer that can accept data this quickly.

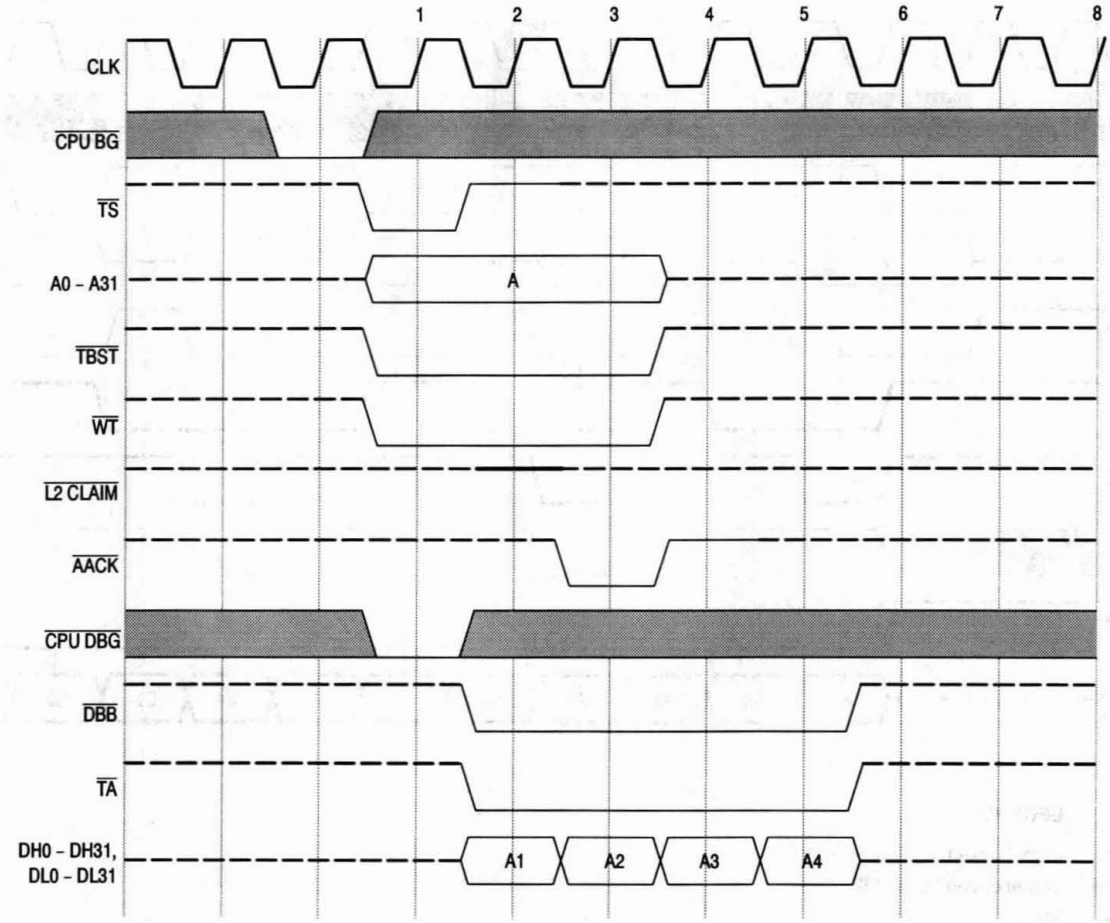
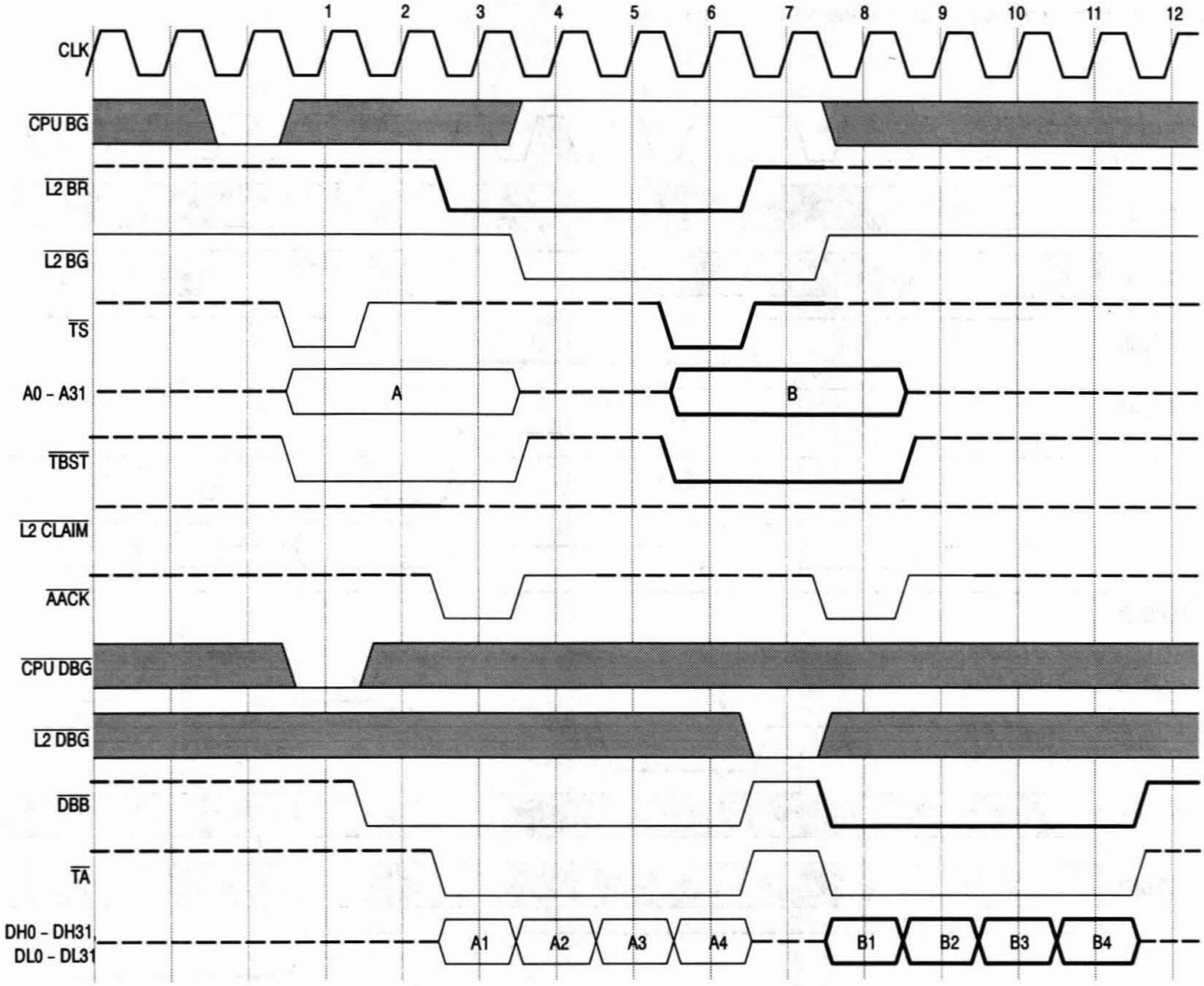


Figure 5. Fastest Possible Write Through Burst Write Hit for MPC603/604

READ/WRITE MISS

Figure 6 is an illustration of a processor read or write miss that causes the MPC2605 to replace a dirty line. $\overline{\text{L2 BR}}$ is asserted two clocks after $\overline{\text{TS}}$. The dirty data to be replaced is moved into the internal cast out buffer (COB) at the same time the new data is written into the cache. Note that the copyback operation occurs after the processor request is satisfied. In addition, no delay is added to the processor transaction. It proceeds as fast as the memory controller will allow.



LEGEND

- Signal driven to the MPC2605
- Signal driven by the MPC2605
- High–Z

Figure 6. Read or Write Miss Followed by Castout

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READ/WRITE SNOOP HIT (DIRTY L2 LINE)

Figure 7 is an illustration of a read or write snoop to a cache line that is dirty in the L2, but is not dirty in the processor's cache. When a snoop hits a dirty line, the MPC2605 will assert $\overline{\text{ARTRY}}$ through the cycle following the assertion of $\overline{\text{AACK}}$. This cycle is called the ARTRY window. Note that the MPC2605 also asserts $\overline{\text{L2 BR}}$ at the same time it asserts $\overline{\text{ARTRY}}$. Because the snoop could also have hit a dirty line in the processor's cache, the MPC2605 samples the processor's $\overline{\text{BR}}$ signal the cycle following the ARTRY window. This cycle is called the BR window. If the processor's $\overline{\text{BR}}$ signal is not asserted, the MPC2605 will start sampling $\overline{\text{L2 BG}}$, the cycle after the BR window.

Note that the MPC2605 cannot do a 2–1–1–1 copy back burst. The earliest that it can handle the first assertion of $\overline{\text{TA}}$ is two cycles after its assertion of $\overline{\text{TS}}$.

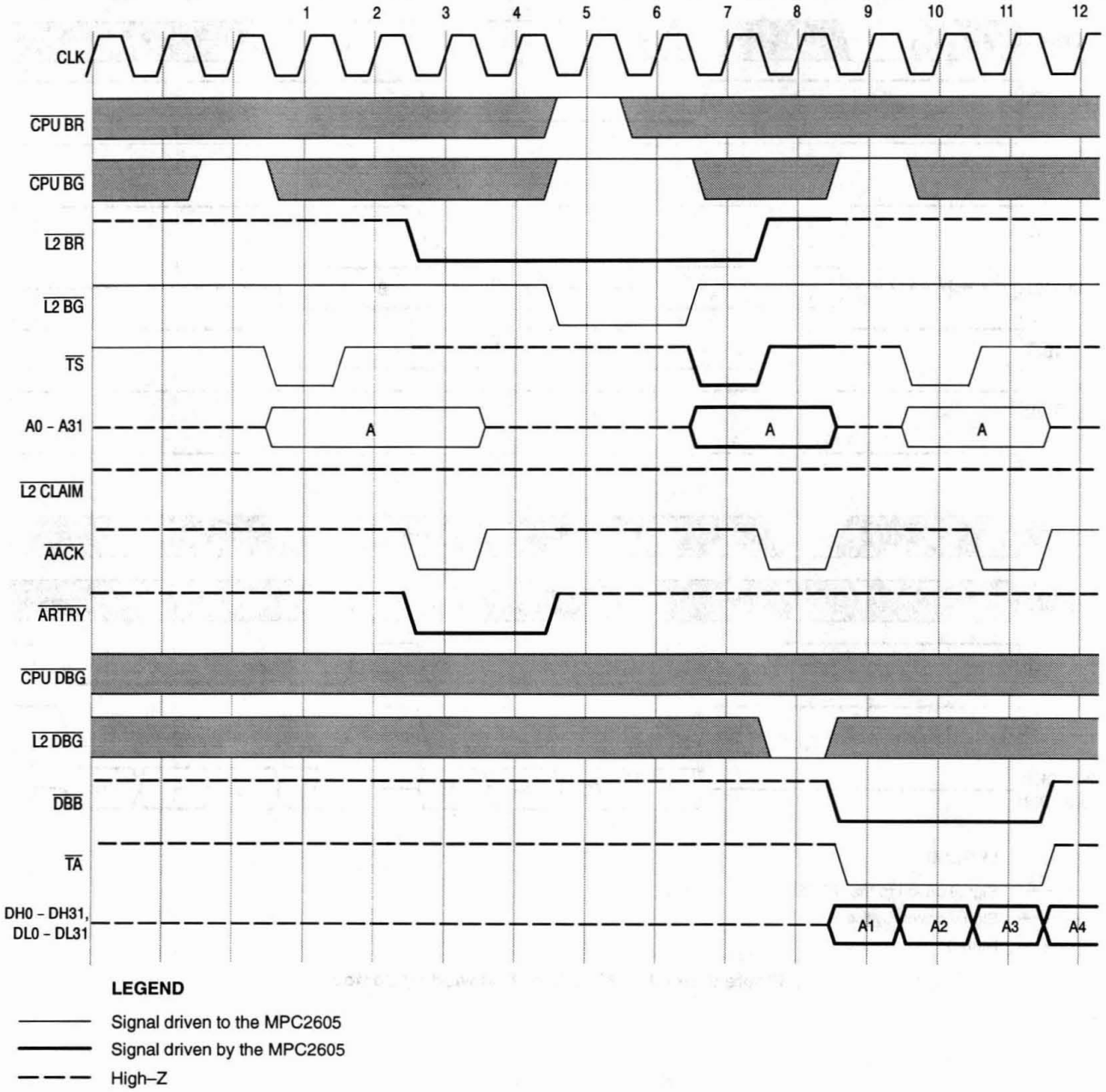
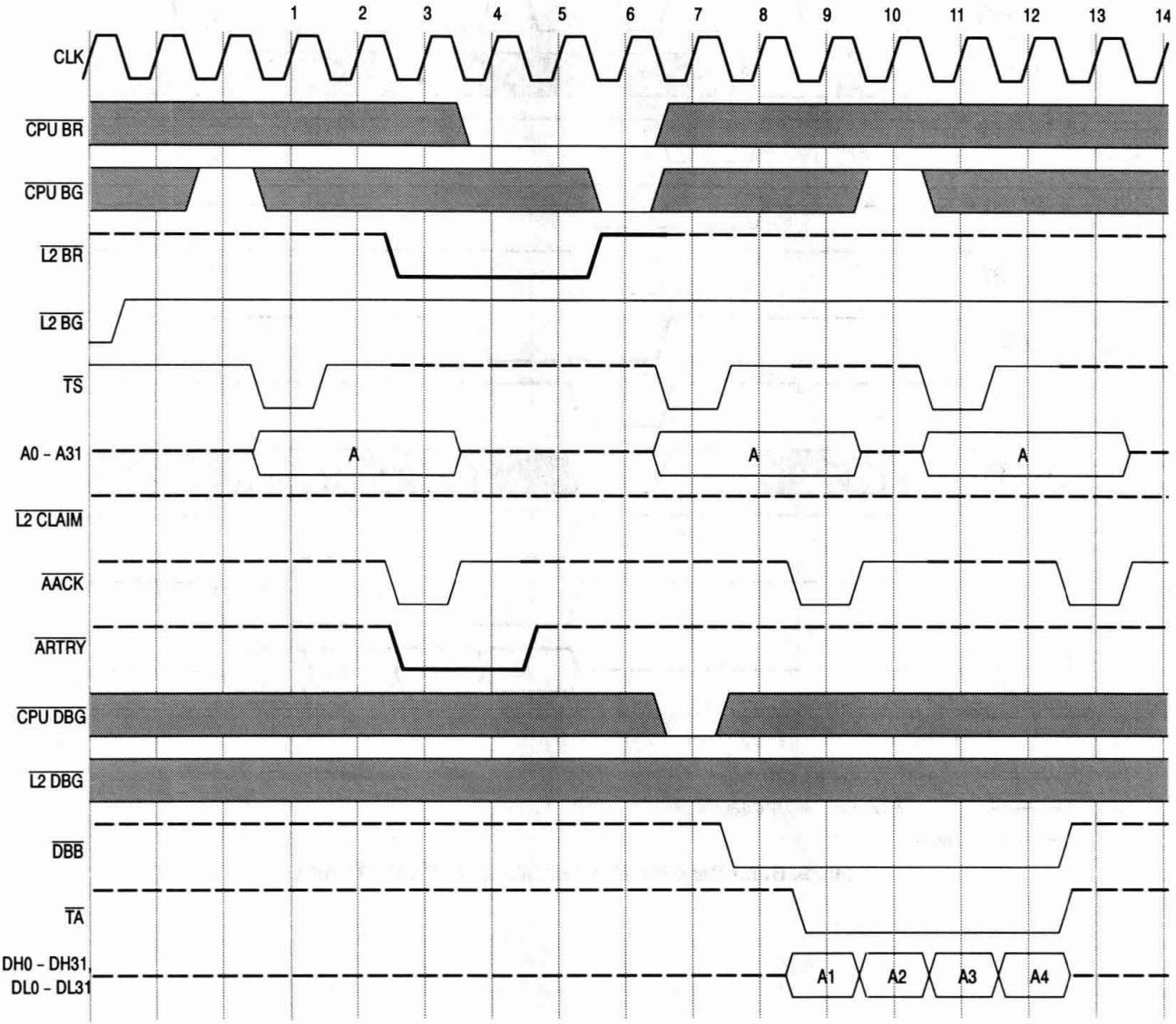


Figure 7. Read or Write Snoop Hit to Dirty L2 Cache Line and Clean Processor Cache Line

READ/WRITE SNOOP HIT (DIRTY L2 AND PROCESSOR LINE)

An illustration of PowerPC read or write snoop hit to a dirty L2 cache line is shown in Figure 8. The processor has a dirty copy of the cache line. In this case, both the processor and the MPC2605 assert $\overline{\text{ARTRY}}$. This situation is detected by sampling $\overline{\text{CPU BR}}$ in the $\overline{\text{BR}}$ window, as described in the previous example. If $\overline{\text{CPU BR}}$ is asserted in the $\overline{\text{BR}}$ window, the MPC2605 will negate $\overline{\text{L2 BR}}$. It will also ignore assertions of $\overline{\text{L2 BG}}$. This allows the processor to write back its dirty cache line, at which time the MPC2605 will either update or invalidate its copy depending on whether it is a snoop read or snoop write.



LEGEND

- Signal driven to the MPC2605
- Signal driven by the MPC2605
- High–Z

Figure 8. Read or Write Snoop Hit to Dirty L2 Cache Line and Dirty Processor Cache Line

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READ HIT/WRITE HIT (WITHOUT $\overline{\text{CPU DBG}}$ PARKED)

Most of the previous examples have assumed $\overline{\text{CPU DBG}}$ is asserted in the same cycle that the processor asserts $\overline{\text{TS}}$. This implies $\overline{\text{CPU DBG}}$ is parked. In some systems it may not be desirable or possible to park $\overline{\text{CPU DBG}}$. Figure 9 shows the response for a read hit from the MPC2605 is gated by the assertion of $\overline{\text{CPU DBG}}$. The fastest response possible in a system that does not park $\overline{\text{CPU DBG}}$ is 3–1–1–1.

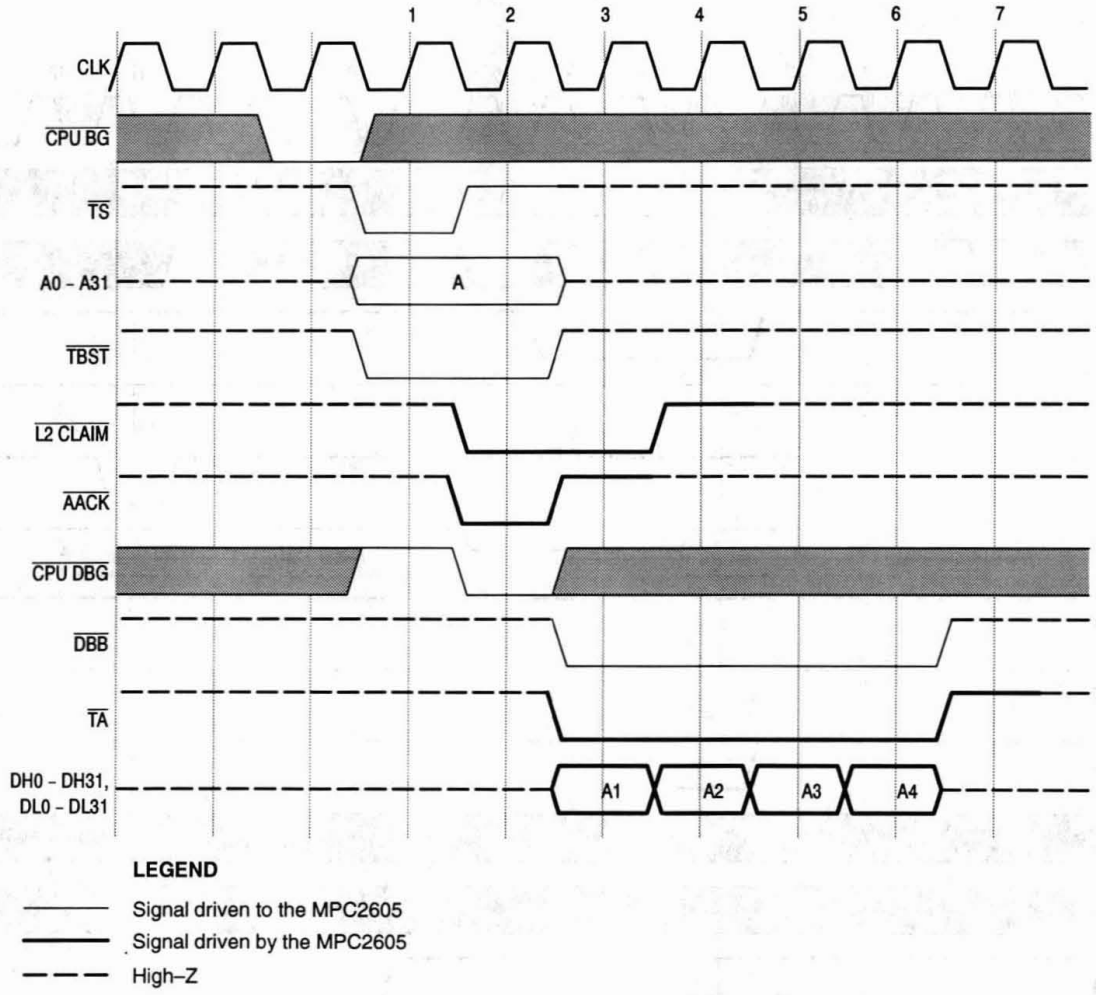

Figure 9. Burst Read (or Write) Hit Without $\overline{\text{CPU DBG}}$ Parked

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AC OPERATING CONDITIONS AND CHARACTERISTICS FOR THE TEST ACCESS PORT (IEEE 1149.1)

(T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Measurement Timing Level ..... 1.5 V
Output Load ..... 50 Ω Termination to 1.5 V

TAP CONTROLLER TIMING

Parameter	Symbol	MPC2605–66 Min	MPC2605–66 Max	Unit	Notes
Cycle Time	t_{CK}	30	—	ns	
Clock High Time	t_{CKH}	12	—	ns	
Clock Low Time	t_{CKL}	12	—	ns	
Clock Low to Output Valid	t_A	5	9	ns	
Clock Low to Output High–Z	t_{CKZ}	0	9	ns	1
Clock Low to Output Active	t_{CKX}	0	9	ns	2, 3
Setup Times: TMS TDI	t_s t_{sd}	2	—	ns	
Hold Times: TMS TDI	t_h t_{hd}	2	—	ns	

NOTES:
1. TDO will High–Z from a clock low edge depending on the current state of the TAP state machine.
2. TDO is active only in the SHIFT–IR and SHIFT–DR state of the TAP state machine.
3. Transition is measured ± 500 mV from steady–state voltage. This parameter is sampled and not 100% tested.

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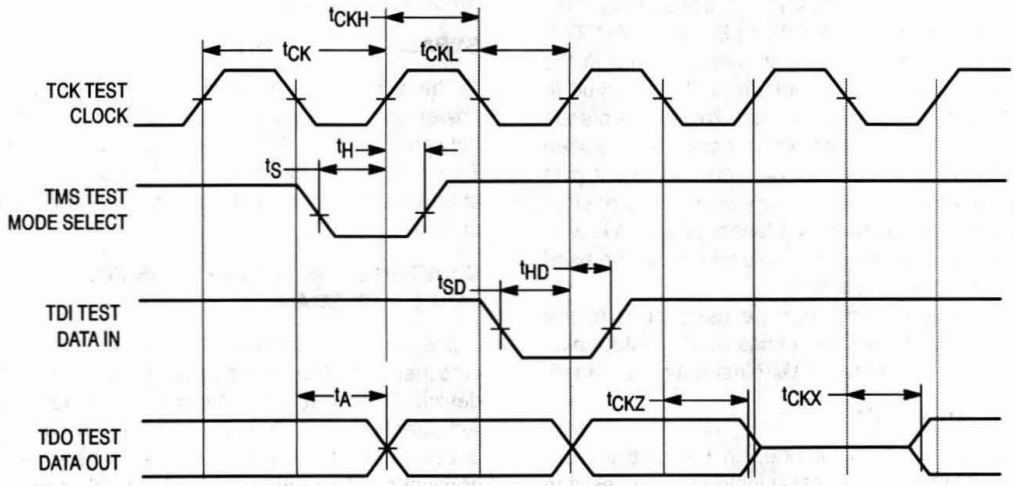

Figure 10. TAP Controller Timing

INSTRUCTION SET

A five pin IEEE Standard 1149.1 Test Port (JTAG) is included on this device. When the TAP (Test Access Port) controller is in the SHIFT–IR state, the instruction register is placed between TDI and TDO. In this state, the desired instruction would be serially loaded through the TDI input. TRST resets the TAP controller to the test–logic reset state. The TAP instruction set for this device are as follows.

STANDARD INSTRUCTIONS

Instruction	Code (Binary)	Description
BYPASS	1111*	Bypass instruction
SAMPLE/PRELOAD	0010	Sample and/or preload instruction
EXTEST	0000	Extest instruction
HIGHZ	1001	High–Z all output pins while bypass register is between TDI and TDO
CLAMP	1100	Clamp output pins while bypass register is between TDI and TDO

* Default state at power–up.

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SAMPLE/PRELOAD TAP INSTRUCTION

The SAMPLE/PRELOAD TAP instruction is used to allow scanning of the boundary–scan register without causing interference to the normal operation of the chip logic. The 168–bit boundary–scan register contains bits for all device signal and clock pins and associated control signals. This register is accessible when the SAMPLE/PRELOAD TAP instruction is loaded into the TAP instruction register in the SHIFT–IR state. When the TAP controller is then moved to the SHIFT–DR state, the boundary–scan register is placed between TDI and TDO. This scan register can then be used prior to the EXTEST instruction to preload the output pins with desired values so that these pins will drive the desired state when the EXTEST instruction is loaded. As data is written into TDI, data also streams out TDO which can be used to pre–sample the inputs and outputs.

SAMPLE/PRELOAD would also be used prior to the CLAMP instruction to preload the values on the output pins that will be driven out when the CLAMP instruction is loaded.

EXTEST TAP INSTRUCTION

The EXTEST instruction is intended to be used in conjunction with the SAMPLE/PRELOAD instruction to assist in testing board level connectivity. Normally, the SAMPLE/PRELOAD instruction would be used to preload all output pins. The EXTEST instruction would then be loaded. During EXTEST, the boundary–scan register is placed between TDI and TDO in the SHIFT–DR state of the TAP controller. Once the EXTEST instruction is loaded, the TAP controller would then be moved to the run–test/idle state. In this state, one cycle of TCK would cause the preloaded data on the output pins to be driven while the values on the input pins would be sampled. Note the TCK, not the clock pin (CLK), is used as the clock input while CLK is only sampled during EXTEST. After one clock cycle of TCK, the TAP controller would then be moved to the SHIFT–DR state where the sampled values would be shifted out of TDO (and new values would be shifted in TDI). These values would normally be compared to expected values to test for board connectivity.

CLAMP TAP INSTRUCTION

The CLAMP instruction is provided to allow the state of the signals driven from the output pins to be determined from the boundary–scan register while the bypass register is selected as the serial path between TDI and TDO. The signals driven from the output pins will not change while the CLAMP instruction is selected. EXTEST could also be used for this purpose, but CLAMP shortens the board scan path by inserting only the bypass register between TDI and TDO. To use CLAMP, the SAMPLE/PRELOAD instruction would be used first to scan in the values that will be driven on the output pins when the CLAMP instruction is active.

HIGHZ TAP INSTRUCTION

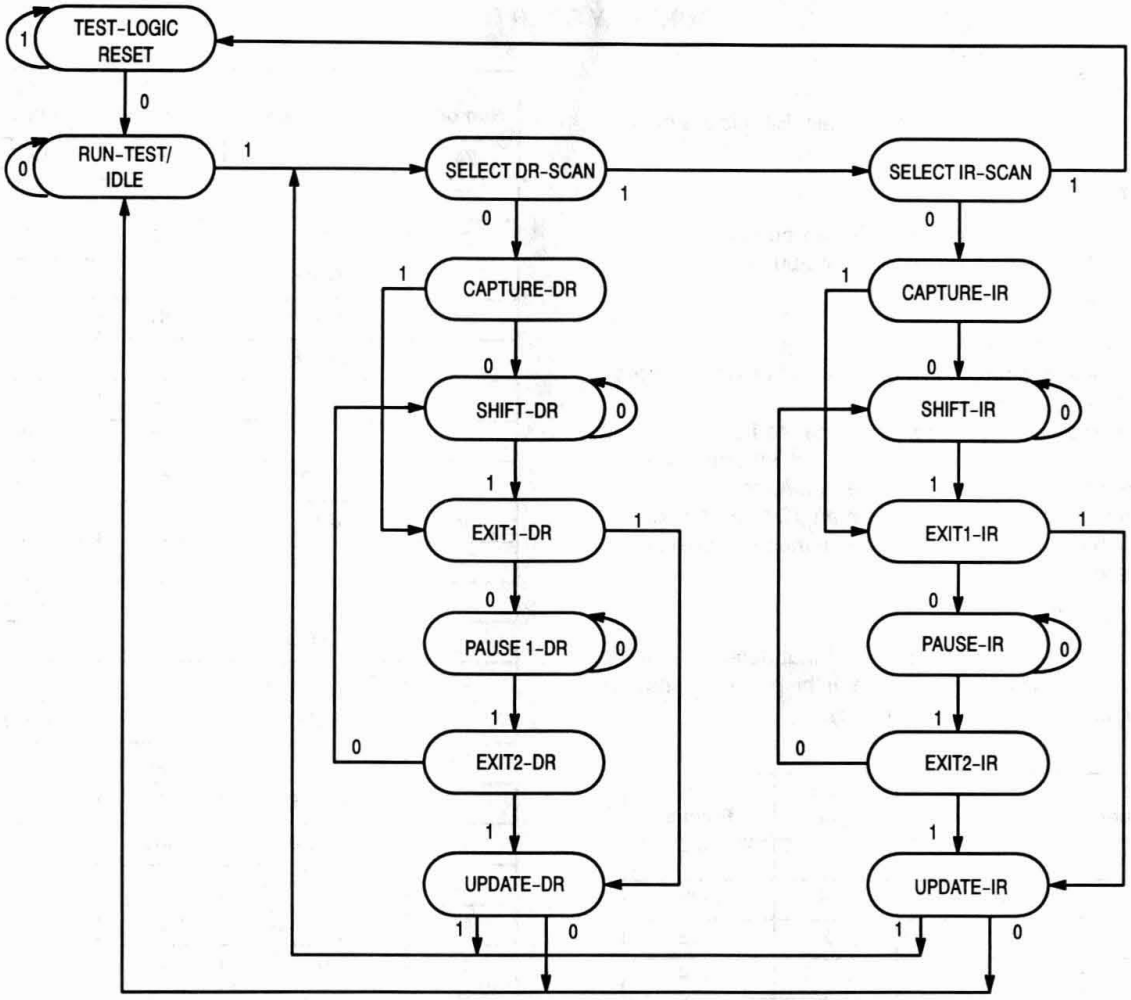
The HIGH–Z instruction is provided to allow all the outputs to be placed in an inactive drive state (high–Z). During the HIGH–Z instruction the bypass register is connected between TDI and TDO.

BYPASS TAP INSTRUCTION

The BYPASS instruction is the default instruction loaded at power up. This instruction will place a single shift register between TDI and TDO during the SHIFT–DR state of the TAP controller. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

DISABLING THE TEST ACCESS PORT AND BOUNDARY SCAN

It is possible to use this device without utilizing the four pins used for the test access port. To circuit disable the device, TCK must be tied to V_{SS} to preclude mid level inputs. Although TDI and TMS are designed in such a way that an undriven input will produce a response equivalent to the application of a logic 1, it is still advisable to tie these inputs to V_{DD} through a 1K resistor. TDO should remain unconnected.



NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 11. TAP Controller State Diagram

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BOUNDARY SCAN ORDER

BIT NUMBER

The order of the boundary scan chain. Bit 0 is the closest to TDO.

BIT/PIN NAME

The name of the physical pin. For an output enable cell, this is the name of the corresponding output enable.

BIT/PIN TYPE

Input — Input only pin.
I/O — Bi–directional pin that can be put into high–Z state.
Output — Output only pin.
Output Enable — Boundary scan cell to hold the output enable state of other I/O pads. Output enable does not correspond to a physical pin. To set an I/O to an input, the output enable must have a 1. To set an I/O to an output, the output enable must have a 0. Note that these internal output enables are active low.

OUTPUT ENABLE

The name of the output enable cell that determines if the cell is enabled or in the high–Z state. If the pin type is input or output enable, this entry will be empty.

Bit Number	Bit/Pin Name	Bit/Pin Type	Output Enable
0	DL16	I/O	DOE
1	DL17	I/O	DOE
2	DL18	I/O	DOE
3	DL19	I/O	DOE
4	DL20	I/O	DOE
5	DL21	I/O	DOE
6	DL22	I/O	DOE
7	DL23	I/O	DOE
8	DP6	I/O	DOE
9	DL24	I/O	DOE
10	DL25	I/O	DOE
11	DL26	I/O	DOE
12	DL27	I/O	DOE
13	DL28	I/O	DOE
14	DL29	I/O	DOE
15	DL30	I/O	DOE
16	DL31	I/O	DOE
17	DP7	I/O	DOE
18	DH24	I/O	DOE
19	DH25	I/O	DOE
20	DH26	I/O	DOE
21	DH27	I/O	DOE
22	DH28	I/O	DOE
23	DH29	I/O	DOE
24	DH30	I/O	DOE
25	DH31	I/O	DOE
26	DP3	I/O	DOE
27	DH16	I/O	DOE
28	DH17	I/O	DOE
29	DH18	I/O	DOE
30	DH19	I/O	DOE
31	DH20	I/O	DOE
32	DH21	I/O	DOE
33	DH22	I/O	DOE
34	DH23	I/O	DOE
35	DP2	I/O	DOE
36	$\overline{\text{L2 BG}}$	Input	
37	$\overline{\text{L2 MISS INH}}$	Input	
38	$\overline{\text{ABB}}$	I/O	ABBOE
39	$\overline{\text{CPU3 DBG}}$	Input	
40	$\overline{\text{CPU3 BG}}$	Input	
41	$\overline{\text{CPU3 BR}}$	Input	
42	$\overline{\text{CPU2 DBG}}$	Input	
43	$\overline{\text{CPU2 BG}}$	Input	
44	$\overline{\text{CPU2 BR}}$	Input	
45	$\overline{\text{FDN}}$	I/O	FDNOE
46	$\overline{\text{L2 DBG}}$	Input	
47	$\overline{\text{L2 BR}}$	I/O	L2BROE
48	$\overline{\text{TA}}$	I/O	TAOE
49	$\overline{\text{L2 CLAIM}}$	Output	L2CLAIMOE
50	$\overline{\text{CPU DBG}}$	Input	
51	$\overline{\text{AACK}}$	I/O	AACKOE
52	$\overline{\text{CI}}$	I/O	AOE
53	$\overline{\text{ARTRY}}$	I/O	ARTRYOE
54	$\overline{\text{WT}}$	I/O	AOE
55	$\overline{\text{CPU BR}}$	Input	
56	$\overline{\text{TEA}}$	Input	
57	PWRDN	Input	
58	$\overline{\text{DBB}}$	I/O	DBBOE
59	$\overline{\text{HRESET}}$	Input	
60	$\overline{\text{TBST}}$	I/O	AOE
61	TT0	I/O	AOE
62	$\overline{\text{TS}}$	I/O	AOE
63	TT1	I/O	AOE
64	TT2	I/O	AOE

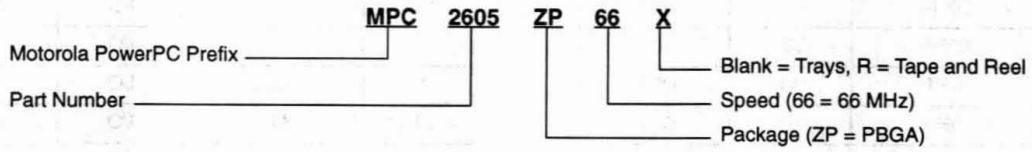
Bit Number	Bit/Pin Name	Bit/Pin Type	Output Enable
65	TT4	I/O	AOE
66	TT3	I/O	AOE
67	$\overline{\text{CPU BG}}$	Input	
68	$\overline{\text{SRESET}}$	Input	
69	$\overline{\text{L2 TAG CLR}}$	Input	
70	$\overline{\text{L2 UPDATE INH}}$	Input	
71	$\overline{\text{CPU4 BG}}$	Input	
72	$\overline{\text{CPU4 DBG}}$	Input	
73	$\overline{\text{CPU4 BR}}$	Input	
74	CFG0	Input	
75	CFG2	Input	
76	CFG1	Input	
77	DH8	I/O	DOE
78	DH9	I/O	DOE
79	DH10	I/O	DOE
80	DH11	I/O	DOE
81	DH12	I/O	DOE
82	DH13	I/O	DOE
83	DH14	I/O	DOE
84	DH15	I/O	DOE
85	DP1	I/O	DOE
86	DH0	I/O	DOE
87	DH1	I/O	DOE
88	DH2	I/O	DOE
89	Dh3	I/O	DOE
90	DH4	I/O	DOE
91	DH5	I/O	DOE
92	DH6	I/O	DOE
93	DH7	I/O	DOE
94	DP0	I/O	DOE
95	DL0	I/O	DOE
96	DL1	I/O	DOE
97	DL2	I/O	DOE
98	DL3	I/O	DOE
99	DL4	I/O	DOE
100	DL5	I/O	DOE
101	DL6	I/O	DOE
102	DL7	I/O	DOE
103	DP4	I/O	DOE
104	DL8	I/O	DOE
105	DL9	I/O	DOE
106	DL10	I/O	DOE
107	DL11	I/O	DOE

Bit Number	Bit/Pin Name	Bit/Pin Type	Output Enable
108	DL12	I/O	DOE
109	DL13	I/O	DOE
110	DL14	I/O	DOE
111	DL15	I/O	DOE
112	DP5	I/O	DOE
113	A0	I/O	AOE
114	A1	I/O	AOE
115	A2	I/O	AOE
116	A3	I/O	AOE
117	A4	I/O	AOE
118	A5	I/O	AOE
119	A6	I/O	AOE
120	A7	I/O	AOE
121	A8	I/O	AOE
122	A9	I/O	AOE
123	A10	I/O	AOE
124	A11	I/O	AOE
125	A12	I/O	AOE
126	A31	I/O	AOE
127	A30	I/O	AOE
128	A29	I/O	AOE
129	A28	I/O	AOE
130	A27	I/O	AOE
131	A26	I/O	AOE
132	A25	I/O	AOE
133	A24	I/O	AOE
134	A23	I/O	AOE
135	A22	I/O	AOE
136	A21	I/O	AOE
137	A20	I/O	AOE
138	A19	I/O	AOE
139	A18	I/O	AOE
140	A17	I/O	AOE
141	A16	I/O	AOE
142	A15	I/O	AOE
143	A14	I/O	AOE
144	A13	I/O	AOE
145	TSIZ2	I/O	AOE
146	TSIZ0	I/O	AOE
147	TSIZ1	I/O	AOE
148	$\overline{\text{GBL}}$	Output	AOE
149	CFG3	Input	
150	$\overline{\text{L2 CI}}$	Input	

Bit Number	Bit/Pin Name	Bit/Pin Type	Output Enable
151	$\overline{\text{L2 FLUSH}}$	Input	
152	AP3	I/O	AOE
153	AP2	I/O	AOE
154	AP1	I/O	AOE
155	AP0	I/O	AOE
156	$\overline{\text{APE}}$	Output	APEOE
157	TAOE	Output Enable	
158	L2CLAIMOE	Output Enable	
159	L2BROE	Output Enable	
160	FDNOE	Output Enable	

Bit Number	Bit/Pin Name	Bit/Pin Type	Output Enable
161	DBBOE	Output Enable	
162	DOE	Output Enable	
163	ARTRYOE	Output Enable	
164	APEOE	Output Enable	
165	ABBOE	Output Enable	
166	AACKOE	Output Enable	
167	AOE	Output Enable	

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Number — MPC2605ZP66
MPC2605ZP66R

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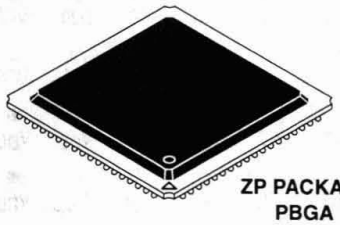
MPC2604GA

Integrated Secondary Cache for PowerPC™ Microprocessors



ZP PACKAGE
PBGA
CASE 1103–01

The MPC2604GA is an integrated look–aside cache with copy–back or write–through capability designed for all PowerPC 60X applications. Using 0.5 µm technology along with standard cell logic technology, the MPC2604GA integrates data, tag, host interface, and least recently used (LRU) memory with a cache controller to provide the highest performance Level 2 cache solution available for the 64–bit PowerPC bus.

- 66 MHz Zero Wait State Performance (2–1–1–1 Burst)
- 4–Way Set Associative Cache Design
- 32K x 36 Data Memory Array
- 8K x 19 Tag Array
- LRU Cache Control Logic
- Copy–Back or Write–Through Modes of Operation
- Copy–Back Buffer for Improved Performance
- Single 5 V Power Supply with 3.3 V Compatible I/O
- Two or Four Chip Cache Solution (Two Chips = 256K, Four Chips = 512K Bytes)
- Single Clock Operation
- Compliant with Proposed IEEE Standard 1149.2 Test Access Port (JTAG)
- Supports Four–Processor Multiprocessor Systems in a Shared Cache Configuration
- High Board Density 25 mm PBGA Package

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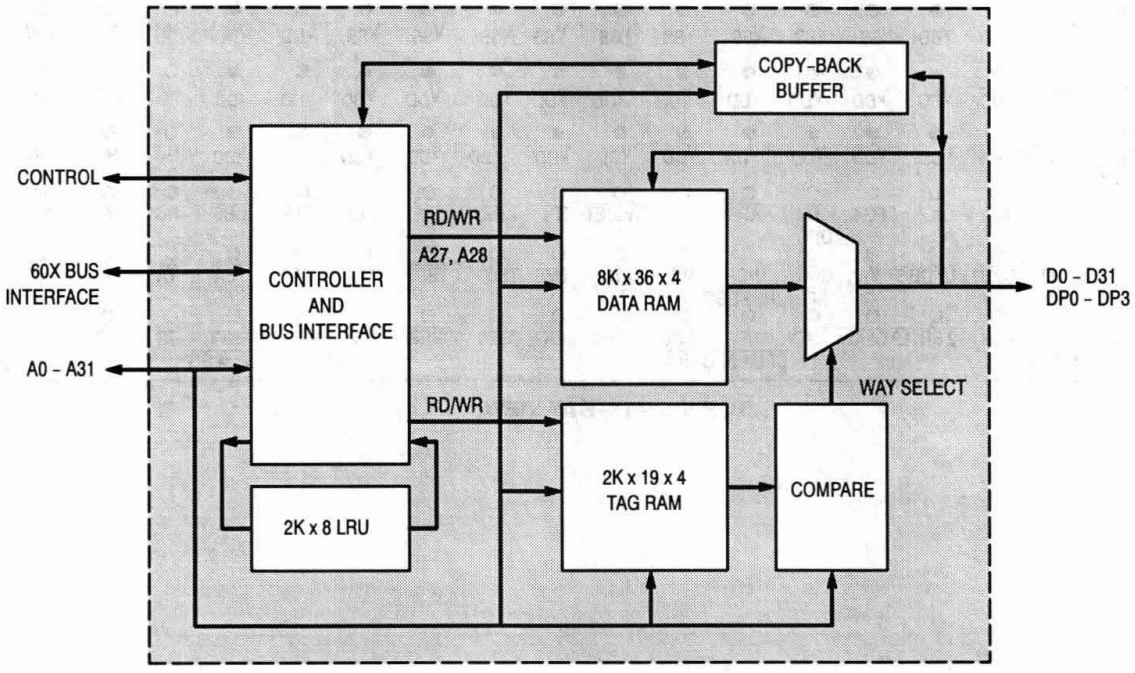
BLOCK DIAGRAM



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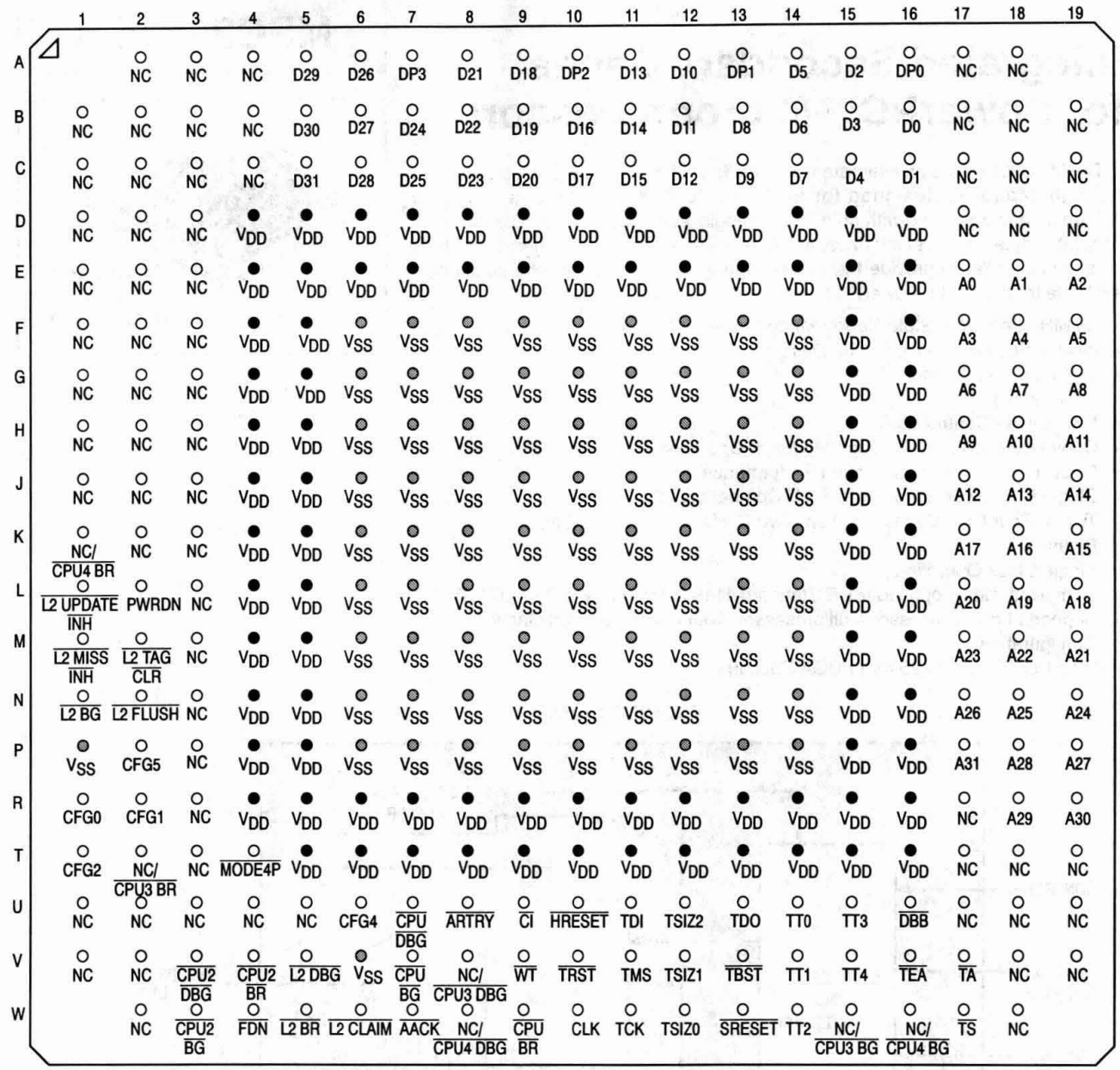
REV 6
5/7/97 This data sheet describes the MPC2604GA revision 2.1



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A		NC	NC	NC	D29	D26	DP3	D21	D18	DP2	D13	D10	DP1	D5	D2	DP0	NC	NC	
B	NC	NC	NC	NC	D30	D27	D24	D22	D19	D16	D14	D11	D8	D6	D3	D0	NC	NC	NC
C	NC	NC	NC	NC	D31	D28	D25	D23	D20	D17	D15	D12	D9	D7	D4	D1	NC	NC	NC
D	NC	NC	NC	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	NC	NC	NC
E	NC	NC	NC	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	A0	A1	A2
F	NC	NC	NC	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	A3	A4	A5
G	NC	NC	NC	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	A6	A7	A8
H	NC	NC	NC	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	A9	A10	A11
J	NC	NC	NC	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	A12	A13	A14
K	NC/ $\overline{\text{CPU4 BR}}$	NC	NC	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	A17	A16	A15
L	$\overline{\text{L2 UPDATE INH}}$	PWRDN	NC	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	A20	A19	A18
M	$\overline{\text{L2 MISS INH}}$	$\overline{\text{L2 TAG CLR}}$	NC	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	A23	A22	A21
N	$\overline{\text{L2 BG}}$	$\overline{\text{L2 FLUSH}}$	NC	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	A26	A25	A24
P	V_{SS}	CFG5	NC	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	A31	A28	A27
R	CFG0	CFG1	NC	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	NC	A29	A30
T	CFG2	NC/ $\overline{\text{CPU3 BR}}$	NC	$\overline{\text{MODE4P}}$	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	NC	NC	NC
U	NC	NC	NC	NC	NC	CFG4	$\overline{\text{CPU DBG}}$	$\overline{\text{ARTRY}}$	$\overline{\text{CI}}$	$\overline{\text{HRESET}}$	TDI	TSIZ2	TDO	TT0	TT3	$\overline{\text{DBB}}$	NC	NC	NC
V	NC	NC	$\overline{\text{CPU2 DBG}}$	$\overline{\text{CPU2 BR}}$	$\overline{\text{L2 DBG}}$	V_{SS}	$\overline{\text{CPU BG}}$	NC/ $\overline{\text{CPU3 DBG}}$	$\overline{\text{WT}}$	$\overline{\text{TRST}}$	TMS	TSIZ1	$\overline{\text{TBST}}$	TT1	TT4	$\overline{\text{TEA}}$	$\overline{\text{TA}}$	NC	NC
W		NC	$\overline{\text{CPU2 BG}}$	$\overline{\text{FDN}}$	$\overline{\text{L2 BR}}$	$\overline{\text{L2 CLAIM}}$	$\overline{\text{AACK}}$	NC/ $\overline{\text{CPU4 DBG}}$	$\overline{\text{CPU BR}}$	CLK	TCK	TSIZ0	$\overline{\text{SRESET}}$	TT2	NC/ $\overline{\text{CPU3 BG}}$	NC/ $\overline{\text{CPU4 BG}}$	$\overline{\text{TS}}$	NC	

TOP VIEW (X–RAY VIEW)

PIN DESCRIPTIONS

Pin Locations	Pin Name	Type	Description
17E – 17P, 18E – 18R, 19E – 19R *	A0 – A31	I/O	Address inputs from processor. Can also be outputs for processor snoop addresses. A0 is the MSB. A31 is the LSB.
7W	$\overline{\text{AACK}}$	I/O	Address acknowledge input/output.
8U	$\overline{\text{ARTRY}}$	I/O	Address retry status I/O. Generated when a read or write snoop to a dirty processor cache line has occurred.
1R, 2R, 1T, 6U, 2P	CFG0 CFG1 CFG2 CFG4 CFG5	I	Configuration inputs. These must be tied to either V_{DD} or V_{SS}. CFG0 Defines data bus side 0 Data bus low 1 Data bus high CFG1 Defines cache size 0 256K 1 512K CFG2 Cache line selector for 512K cache size 0 Even cache lines 1 Odd cache lines CFG4 $\overline{\text{AACK}}$ driver enable 0 Disable $\overline{\text{AACK}}$ driver 1 Enable $\overline{\text{AACK}}$ driver CFG5 Snoop data tenure selector 0 Supports snoop data tenure 1 Does not support snoop data tenure
9U	$\overline{\text{CI}}$	I/O	Cache inhibit I/O.
10W	CLK	I	Clock input. This must be the same as the processor clock input.
7V	$\overline{\text{CPU BG}}$	I	CPU bus grant input.
3W	$\overline{\text{CPU2 BG}}$	I	MPC2604GA logically ORs this signal with $\overline{\text{CPU BG}}$. Used in multiprocessor configuration as the second $\overline{\text{CPU BG}}$.
15W	NC/$\overline{\text{CPU3 BG}}$	I	MPC2604GA logically ORs this signal with $\overline{\text{CPU BG}}$. Used in multiprocessor configuration as the third $\overline{\text{CPU BG}}$. This pin is a no connect when $\overline{\text{MODE4P}}$ is high.
16W	NC/$\overline{\text{CPU4 BG}}$	I	MPC2604GA logically ORs this signal with $\overline{\text{CPU BG}}$. Used in multiprocessor configuration as the fourth $\overline{\text{CPU BG}}$. This pin is a no connect when $\overline{\text{MODE4P}}$ is high.
9W	$\overline{\text{CPU BR}}$	I	CPU bus request input.
4V	$\overline{\text{CPU2 BR}}$	I	MPC2604GA logically ORs this signal with $\overline{\text{CPU BR}}$. Used in multiprocessor configuration as the second $\overline{\text{CPU BR}}$.
2T	NC/$\overline{\text{CPU3 BR}}$	I	MPC2604GA logically ORs this signal with $\overline{\text{CPU BR}}$. Used in multiprocessor configuration as the third $\overline{\text{CPU BR}}$. This pin is a no connect when $\overline{\text{MODE4P}}$ is high.
1K	NC/$\overline{\text{CPU4 BR}}$	I	MPC2604GA logically ORs this signal with $\overline{\text{CPU BR}}$. Used in multiprocessor configuration as the fourth $\overline{\text{CPU BR}}$. This pin is a no connect when $\overline{\text{MODE4P}}$ is high.
7U	$\overline{\text{CPU DBG}}$	I	CPU data bus grant input from arbiter.
3V	$\overline{\text{CPU2 DBG}}$	I	MPC2604GA logically ORs this signal with $\overline{\text{CPU DBG}}$. Used in multiprocessor configuration as the second $\overline{\text{CPU DBG}}$.
8V	NC/$\overline{\text{CPU3 DBG}}$	I	MPC2604GA logically ORs this signal with $\overline{\text{CPU DBG}}$. Used in multiprocessor configuration as the third $\overline{\text{CPU DBG}}$. This pin is a no connect when $\overline{\text{MODE4P}}$ is high.
8W	NC/$\overline{\text{CPU4 DBG}}$	I	MPC2604GA logically ORs this signal with $\overline{\text{CPU DBG}}$. Used in multiprocessor configuration as the fourth $\overline{\text{CPU DBG}}$. This pin is a no connect when $\overline{\text{MODE4P}}$ is high.
5A, 6A, 8A, 9A, 11A, 12A, 14A, 15A, 5B – 16B, 5C – 16C *	D0 – D31	I/O	Data bus input and output. D0 is the MSB. D31 is the LSB.
16U	$\overline{\text{DBB}}$	I/O	Data bus busy. Used as input when processor is master, driven as an output after a qualified $\overline{\text{L2 DBG}}$ when MPC2604GA is the bus master. Note: To operate in Fast L2 mode, this pin must be tied high.
7A, 10A, 13A, 16A *	DP0 – DP3	I/O	Data bus parity input and output.

* See pin diagram (page 2) for specific pin assignment of these bus signals.

Pin Locations	Pin Name	Type	Description
4W	$\overline{\text{FDN}}$	I/O	Flush done I/O used for communication between other MPC2604GA devices. Must be tied together between all MPC2604GA parts along with a pullup resistor.
10U	$\overline{\text{HRESET}}$	I	Hard reset input from processor bus. This is an asynchronous input that must be low for at least 16 clock cycles to ensure the MPC2604GA is properly reset.
1N	$\overline{\text{L2 BG}}$	I	Bus grant input from arbiter.
5W	$\overline{\text{L2 BR}}$	I/O	Bus request I/O. Normally used as an output.
6W	$\overline{\text{L2 CLAIM}}$	O	L2 Cache Claim output. Used to claim the bus for processor initiated memory operations that hit the L2 cache. $\overline{\text{L2 CLAIM}}$ goes true (low) before the rising edge of CLK following $\overline{\text{TS}}$ true. Because the output is not always driven, a pullup resistor may be necessary to ensure proper system functioning.
5V	$\overline{\text{L2 DBG}}$	I	Data bus grant input. Comes from system arbiter, used to start data tenure for bus operations where MPC2604GA is the bus master.
2N	$\overline{\text{L2 FLUSH}}$	I	Causes cache to write back dirty lines and clears all tag valid bits.
1M	$\overline{\text{L2 MISS INH}}$	I	Prevents line fills on misses when asserted.
2M	$\overline{\text{L2 TAG CLR}}$	I	Invalidates all tags and holds cache in a reset condition.
1L	$\overline{\text{L2 UPDATE INH}}$	I	Cache disable. When asserted, the MPC2604GA will not respond to signals on the local bus and internal states do not change.
4T	$\overline{\text{MODE4P}}$	I	When tied low, enables arbitration pins for four–processor configuration.
2L	PWRDN	I	Provides low power mode. Not fully implemented.
13W	$\overline{\text{SRESET}}$	I	Soft reset input from processor bus.
17V	$\overline{\text{TA}}$	I/O	Transfer acknowledge status I/O from processor bus.
13V	$\overline{\text{TBST}}$	I/O	Transfer burst status I/O from processor bus. Used to distinguish between burstable and non–burstable memory operations.
11W	TCK	I	Test clock input for IEEE 1149.2 boundary scan (JTAG).
11U	TDI	I	Test data input for IEEE 1149.2 boundary scan (JTAG).
13U	TDO	O	Test data output for IEEE 1149.2 boundary scan (JTAG).
16V	$\overline{\text{TEA}}$	I	Transfer error acknowledge status input from processor bus.
11V	TMS	I	Test mode select for IEEE 1149.2 boundary scan (JTAG).
10V	$\overline{\text{TRST}}$	I	Test reset input for IEEE 1149.2 boundary scan (JTAG).
17W	$\overline{\text{TS}}$	I/O	Transfer start I/O from processor bus (can also come from any bus master on the processor bus). Signals the start of either a processor or bus master cycle.
12U, 12V, 12W *	TSIZ0–TSIZ2	I/O	Transfer size I/O from processor bus.
14U, 15U, 14V, 15V, 14W *	TT0–TT4	I/O	Transfer type I/O from processor bus.
9V	$\overline{\text{WT}}$	I/O	Write through status input from processor bus. When tied to ground, the MPC2604GA will operate in write–through mode only (no copy–back).
2A – 4A, 17A, 18A, 1B – 4B, 17B – 19B, 1C – 4C, 17C – 19C, 1D – 3D, 17D – 19D, 1E – 3E, 1F – 3F, 1G – 3G, 1H – 3H, 1J – 3J, 2K, 3K, 3L, 3M, 3N, 3P, 3R, 17R, 3T, 17T – 19T, 1U – 5U, 17U – 19U, 1V, 2V, 18V, 19V, 2W, 18W	NC	—	No connection: There is no connection to the chip.

* See pin diagram (page 2) for specific pin assignment of these bus signals.

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Pin Locations	Pin Name	Type	Description
4D – 16D, 4E – 16E, 4F, 5F, 15F, 16F, 4G, 5G, 15G, 16G, 4H, 5H, 15H, 16H, 4J, 5J, 15J, 16J, 4K, 5K, 15K 16K, 4L, 5L, 15L, 16L, 4M, 5M, 15M, 16M, 4N, 5N, 15N, 16N, 4P, 5P, 15P, 16P, 4R – 16R, 5T – 16T	V_{DD}	Supply	Power supply: 5.0 V ± 5%.
6F – 14F, 6G – 14G, 6H – 14H, 6J – 14J, 6K – 14K, 6L – 14L, 6M – 14M, 6N – 14N, 1P, 6P – 14P, 6V	V_{SS}	Supply	Ground.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V, See Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Package Power Dissipation (See Note 2)	P_D	—	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_J	20 to + 110	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability will be dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(T_J = 20 to + 110°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{DD}	4.75	5.0	5.25	V
Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL}(min) = – 2.0 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{DD})	$I_{lkg(I)}$	—	—	± 1.0	µA
Output Leakage Current (High–Z State, V_{out} = 0 to V_{DD})	$I_{lkg(O)}$	—	—	± 1.0	µA
AC Supply Current (I_{out} = 0 mA, All inputs = V_{IL} or V_{IH}, V_{IL} = 0 V, and V_{IH} ≥ 3.0 V, Cycle Time = 15 ns, max value assumes a constant burst read hit, with 100% bus utilization, and 100% hit rate; typ value, 50% bus utilization, 90% hit rate)	I_{CCA}	—	—	720	mA
AC Quiescent Current (I_{out} = 0 mA, All inputs = V_{IL} or V_{IH}, V_{IL} = 0 V and V_{IH} ≥ 3.0 V, Cycle Time = 15 ns, All Other Inputs DC)	I_Q	—	—	195	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V
Output High Voltage (I_{OH} = – 20 µA)	V_{OH}	—	—	3.3	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance	C_{out}	6	8	pF
Input/Output Capacitance	$C_{I/O}$	8	10	pF

PACKAGE THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit
Thermal Resistance Junction to Ambient (Still Air, 4 Layer Board)	$R_{\theta JA}$	19	°C/W
Thermal Resistance Junction to Ambient (200 lfpm, 4 Layer Board)	$R_{\theta JA}$	15	°C/W
Thermal Resistance Junction to Board (Bottom)	$R_{\theta JB}$	7.3	°C/W
Thermal Resistance Junction to Case (Top)	$R_{\theta JC}$	8	°C/W

AC OPERATING CONDITIONS AND CHARACTERISTICS

(T_J = 20 to + 110°C, Unless Otherwise Noted)

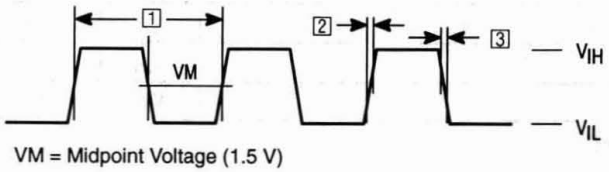
Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Output Measurement Timing Level ..... 1.5 V
Output Load ..... 50 Ω Termination to 1.5 V

AC CLOCK SPECIFICATIONS

Parameter	Timing Reference	MPC2604GA–66		Unit	Notes
		Min	Max		
Frequency of Operation		—	66.67	MHz	
Clock Cycle Time	[1]	15	—	ns	1
Clock Rise and Fall Time	[2], [3]	1.0	2.0	ns	2
Clock Duty Cycle Measured at 1.5 V		40	60	%	
Clock Short–Term Jitter (Cycle to Cycle)		—	± 150	ps	1

NOTES:
1. This parameter is sampled and not 100% tested.
2. Rise and fall times for the clock input are measured from 0.4 to 2.4 V.

CLOCK INPUT TIMING DIAGRAM



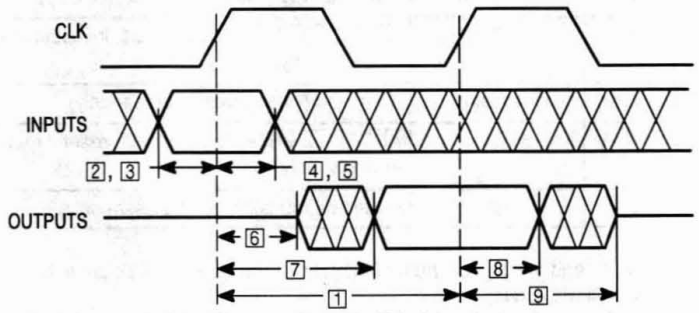
VM = Midpoint Voltage (1.5 V)

AC SPECIFICATIONS

Parameter	Timing Reference	MPC2604GA–66		Unit	Notes
		Min	Max		
Clock Cycle Time	1	15	—	ns	
Address/Transfer Start Setup	2	4.5	—	ns	1
Setup Time for All Other Inputs	3	4.5	—	ns	1, 2
Clock to Address/Transfer Start Inputs Invalid (Input Hold)	4	1	—	ns	1, 3
Clock to All Other Inputs Invalid (Input Hold)	5	1	—	ns	1, 2
Clock to Output Driven	6	2	9	ns	4
Clock to $\overline{TA}$, $\overline{L2\ CLAIM}$, D0 – D31, DP0 – DP3, A0 – A31 Valid	7	2	10	ns	
Clock to All Other Outputs Valid	7	2	9	ns	
Clock to Output Invalid	8	2	—	ns	4
Clock to all Outputs High–Z	9	2	12	ns	4

NOTES:

1. All input specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the 1.4 V level of the rising edge of the input clock. Both input and output timings are measured at the pin.
2. All other input signals are composed of the following: $\overline{AACK}$, $\overline{ARTRY}$, $\overline{CPU\ BG}$, $\overline{CPU2\ BG}$, $\overline{CPU\ BR}$, $\overline{CPU2\ BR}$, $\overline{CI}$, $\overline{DBB}$, $\overline{CPU\ DBG}$, $\overline{CPU2\ DBG}$, D0 – D31, DP0 – DP3, $\overline{L2\ BG}$, $\overline{L2\ DBG}$, $\overline{TA}$, $\overline{TBST}$, $\overline{TEA}$, $\overline{TS}$, TSIZ0 – TSIZ2, TT0 – TT4, $\overline{WT}$.
3. Address/transfer start input signals are composed of the following: A0 – A31, $\overline{TS}$.
4. This parameter is sampled and not 100% tested.



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MPC2604GA RESPONSE TO 60X TRANSFER ATTRIBUTES

TT0 – TT4	$\overline{TBST}$	$\overline{CI}$	$\overline{WT}$	Tag Status	MPC2604GA Response	Notes
X1X10	0	1	X	Miss	Line–fill (processor read miss)	1, 2, 3
X1X10	0	1	X	Hit	$\overline{L2\ CLAIM}$, $\overline{AACK}$, $\overline{TA}$ (processor read hit)	4
X1010	1	0	X	Hit Clean	Paradox — Invalidate the line (processor n–cacheable read hit clean line)	
X1010	1	0	X	Hit Dirty	Paradox — $\overline{ARTRY}$, $\overline{L2\ BR}$, then write back data, invalidate the line (processor n–cacheable read hit dirty line)	
00110	0	1	X	Miss	Line–fill except right after a snoop hit to processor (processor write miss)	1, 3, 5, 6
00110	0	1	1	Hit	$\overline{L2\ CLAIM}$, $\overline{AACK}$, $\overline{TA}$ except after a snoop hit to processor (processor write hit)	5, 6
00X10	X	1	0	Hit Clean	Cache update (processor write through $\overline{WT}$ hit clean)	
00110	0	1	0	Hit Dirty	Cache update, clear dirty bit	
00010	1	1	0	Hit Dirty	Paradox — $\overline{ARTRY}$, $\overline{L2\ BR}$, write back data, keep valid, clear dirty bit	
X0010	1	0	X	Hit Clean	Paradox — Invalidate the line (processor n–cacheable write hit clean line)	
X0010	1	0	X	Hit Dirty	Paradox — $\overline{ARTRY}$, $\overline{L2\ BR}$, then write back data, invalidate the line (processor n–cacheable SB write hit dirty line)	
00100	X	X	X	Hit Clean	Invalidate tag (flush block address–only)	
00100	X	X	X	Hit Dirty	$\overline{ARTRY}$, $\overline{L2\ BR}$, write back data, invalidate tag (flush block address–only)	
00000	X	X	X	Hit Clean	No action (clean block address–only)	
00000	X	X	X	Hit Dirty	$\overline{ARTRY}$, $\overline{L2\ BR}$, write back data, reset dirty bit (clean block address–only)	
01100	X	X	X	Hit	Invalidate tag (kill block address–only)	

NOTES:

1. If a line fill is going to replace a dirty line and the cast out buffer (COB) is full, the line fill will be cancelled, (unless the line fill is a write which hits in the COB. In this case, the line fill will occur.)
2. If a burst read misses the cache but hits the COB, the MPC2604GA will supply the data from the COB, but not perform a line fill.
3. If $\overline{ARTRY}$ is asserted during a line fill to replace a dirty line, the line fill will be cancelled, the to–be–replaced line will recover its old tag (valid, dirty, tag field), and the COB goes back to an invalid condition, even if the line fill is a burst write to the line in the COB.
4. If $\overline{ARTRY}$ is asserted during a read hit, the MPC2604GA will abort the process.
5. If a processor burst write occurs right after a snoop write that was a cache hit, the MPC2604GA will invalidate the line. If the snoop was a cache miss, the MPC2604GA will not perform a write allocate.
6. If a processor burst write occurs right after a snoop read that was a cache hit, the MPC2604GA will update the cache and clear the dirty bit. If the snoop was a cache miss, the MPC2604GA will perform a write allocate.

MPC2604GA RESPONSE TO CHIPSET TRANSFER ATTRIBUTES

TT0 – TT4	Tag Status	MPC2604GA Response
00100 X0010 X1110	Hit Clean	Invalidate line
00100 X0010 X1110	Hit Dirty	$\overline{\text{ARTRY}}$ and $\overline{\text{L2 BR}}$ write back data, invalidate line (See Note)
00000 X1010	Hit Clean	No action
00000 X1010	Hit Dirty	$\overline{\text{ARTRY}}$ and $\overline{\text{L2 BR}}$, write back data, reset dirty bit (See Note)
0110X 00110	Hit	Invalidate (kill block)

NOTE: In all snoop push cases, $\overline{\text{BR}}$ is sampled the cycle after the ARTRY window. If $\overline{\text{BR}}$ is asserted in this cycle, $\overline{\text{L2 BR}}$ will be immediately negated and an assertion of $\overline{\text{L2 BG}}$ will be ignored.

TRANSFER ATTRIBUTES GENERATED FOR L2 COPYBACK

TT0 – TT4	$\overline{\text{TBST}}$	$\overline{\text{CI}}$	$\overline{\text{WT}}$
00010	0	1	1

FUNCTIONAL OPERATION

SYSTEM USAGE AND REQUIREMENTS

The MPC2604GA is a high–performance look–aside cache for PowerPC systems. A look–aside cache is defined as a cache that resides on the same bus as the processor, the memory controller, the DMA bridge, and the arbiter. The advantage of a look–aside cache is that, when the processor makes a memory request, the cache adds no delay to the memory controller's response time in the event that the request cannot be satisfied by the cache. However, there are certain system requirements that must be met before a look–aside cache can be used.

Comprehension of $\overline{\text{L2 CLAIM}}$

Because the memory controller sees every memory request that is issued by the processor, there must be a mechanism for the cache to inform the memory controller that it has detected a cache hit and that it will satisfy the processor's request. The MPC2604GA has a signal called $\overline{\text{L2 CLAIM}}$ that is asserted whenever a cache hit is detected. Any memory controller with which the MPC2604GA is to be used must have the ability to monitor this signal.

Pipeline Depth

The 60X bus allows pipelining of transactions such that a new transaction can be initiated before a previous transaction has fully completed. The level of pipelining that exists on the bus is defined by how many new data transactions have been initiated while the original transaction is still being processed. By this definition the MPC2604GA can only work in a one level deep pipeline. In the presence of transactions for which it has asserted $\overline{\text{L2 CLAIM}}$, the MPC2604GA can control the level of pipelining by delaying its assertion of $\overline{\text{AACK}}$. However, for transactions that it cannot control, the MPC2604GA is dependent upon the memory controller to control pipeline depth. Thus, another system requirement for the use of the MPC2604GA is the use of a memory controller that only allows one level deep of pipelining on the 60X bus.

Bus Mastering

Bus mastering is a requirement only for systems which seek to use the MPC2604GA as a copyback, as opposed to a write–through, cache. The requirement is that the system arbiter must have the ability to allow the MPC2604GA to become a bus master. Specifically, the system arbiter must be able to recognize assertions of $\overline{\text{L2 BR}}$ and must have the ability to assert $\overline{\text{L2 BG}}$ and $\overline{\text{L2 DBG}}$.

Note: The MPC2604GA does not have a $\overline{\text{GBL}}$ pin and therefore cannot drive $\overline{\text{GBL}}$ high during a copyback operation. If $\overline{\text{GBL}}$ is low during a copyback, it is possible for the processor to assert $\overline{\text{ARTRY}}$ under certain conditions. If the system memory controller cannot support an assertion of $\overline{\text{ARTRY}}$ during an L2 copyback, then it is necessary to have an active or passive pullup on $\overline{\text{GBL}}$ to facilitate correct copyback operation.

These are the only requirements above and beyond what should already exist in a PowerPC system. All other necessary control signals are signals that are required for the processor to communicate with the memory controller, the DMA bridge, and the arbiter.

CONFIGURATION PINS

The MPC2604GA has five configuration pins: CFG0, CFG1, CFG2, CFG4, and CFG5.

CFG0

A given MPC2604GA device only has 32 data pins, plus parity. Because the PowerPC 60X bus is defined to be a 64–bit bus, it is necessary to use two MPC2604GA devices to create a cache. Since the processor can write quantities of

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less than 8 bytes (64 bits) in a transaction, and because each MPC2604GA device is exactly the same, there must be a mechanism to indicate which device is connected to the high half of the data bus (D0 – D31) and which device is connected to the low half of the data bus (D32 – D63). CFG0 is the means to this end. CFG0 should be tied high on the device that is connected to the high half of the data bus, and CFG0 should be tied low on the device that is connected to the low half of the data bus.

CFG1, CFG2

When used as a two chip solution, the MPC2604GA implements a 256KB cache. It has the ability to be used in a four chip solution to create a 512KB cache. In this configuration, two independent pairs are created that each cache different addresses. Specifically, one pair, the even pair, will only cache addresses with A26 = 0. The odd pair will only cache addresses with A26 = 1. CFG1 defines whether a 256KB cache is being used (CFG1 = 0) or a 512KB cache is being used (CFG1 = 1). In the case where CFG1 = 1, CFG2 defines whether a given device is a member of the even pair or the odd pair. Thus, when implementing a four chip configuration, each of the devices should have CFG1 tied high, and each device should have a different combination of CFG0 and CFG2:

- The even high device should have CFG0 = 1 and CFG2 = 0.
- The even low device should have CFG0 = 0 and CFG2 = 0.
- The odd high device should have CFG0 = 1 and CFG2 = 1.
- The odd low device should have CFG0 = 0 and CFG2 = 1.

When CFG1 = 0, CFG2 is not used by the MPC2604GA.

CFG4

When the MPC2604GA asserts $\overline{\text{L2 CLAIM}}$ to signal to the memory controller that a cache hit has been detected, it is taking control of the address and data tenures of the transaction (see **60X Bus Operation** and **Memory Coherence**). This means that the MPC2604GA will assert $\overline{\text{AACK}}$ to end the address tenure, and it will assert $\overline{\text{TA}}$ as needed for the data tenure. Tying CFG4 low implements a custom feature that prevents the MPC2604GA from asserting $\overline{\text{AACK}}$ to end transactions for which it has asserted $\overline{\text{L2 CLAIM}}$. In systems that tie CFG4 low it is necessary for the memory controller to assert $\overline{\text{AACK}}$ for all transactions. It is expected that most systems will tie CFG4 high.

CFG5

Many core logic chipsets are designed such that the DMA bridge and the memory controller are resident in the same device. In such systems there is internal communication between these two functional units. Bus transactions generated by the DMA bridge are solely for the purpose of keeping the system coherent. They are not explicit requests from memory that have data tenures associated with them. However, some chipsets are designed with the memory controller and the DMA bridge partitioned into different devices. In systems such as these, transactions generated by the DMA bridge are true memory requests that have data tenures associated with them. These are called snoop data tenures. Because these two types of systems are fundamentally different, the MPC2604GA must know in which type of system it is resident in order to respond properly to the different types of transactions. For systems that do not have snoop data tenures, CFG5 must be tied high. For systems that do use snoop data tenures, CFG5 must be tied low.

RESET/INITIALIZATION

To ensure proper initialization and system functionality, the $\overline{\text{HRESET}}$ pin of the MPC2604GA should be connected to the same signal that is used to reset the processor. When $\overline{\text{HRESET}}$ is negated, the MPC2604GA commences an internal initialization sequence to clear all of the valid bits in the cache. The sequence takes approximately 4000 clock cycles. During this time the MPC2604GA will not participate in any bus transaction that occurs. All transactions are, however, monitored so that, regardless of when the initialization sequence completes, the MPC2604GA is prepared to take action on the next transaction initiated by the processor.

At some point after this 4000 cycle sequence, the MPC2604GA will detect its first cache hit. At this time the system will experience its first assertion of $\overline{\text{L2 CLAIM}}$. If the memory controller must be configured via software to comprehend assertions of $\overline{\text{L2 CLAIM}}$, this configuration operation must have completed by this time. For systems that cannot guarantee that this requirement is met, it is necessary to disable the MPC2604GA until such time as this configuration can be guaranteed. Disabling the MPC2604GA can be accomplished by asserting $\overline{\text{L2 UPDATE INH}}$ sometime during reset and negating it when it is deemed safe for caching to commence.

60X BUS OPERATION

All transactions have what is called an address tenure. An address tenure is a set number of bus cycles during which the address bus and its associated control signals are being used for the transaction at hand. In general, there are two types of transactions. Those that only have address tenures, called address–only transactions. And those that require the use of the data bus and therefore will have a data tenure. These transactions are called data transactions. This section describes how address and data tenures are defined as viewed by the MPC2604GA.

Address Tenures

Address tenures on the 60X bus are fairly well defined. They start with an assertion of $\overline{\text{TS}}$ by a device that has been granted the bus by the system arbiter. This device is called the bus master for this transaction. At the same time that $\overline{\text{TS}}$ is asserted, the bus master also drives the address and all other relevant control signals that define the transaction. $\overline{\text{TS}}$ is only asserted for one cycle but all other signals are held valid by the bus master until some other device asserts $\overline{\text{AACK}}$. The device that asserts $\overline{\text{AACK}}$ becomes the slave to this transaction. Typically, the slave is the memory controller, although for transactions that are cache hits the MPC2604GA becomes the slave by driving $\overline{\text{L2 CLAIM}}$.

Transactions can be aborted by any device on the bus by asserting $\overline{\text{ARTRY}}$. $\overline{\text{ARTRY}}$ may be asserted at any time after $\overline{\text{TS}}$ is asserted, but must be held through the cycle after $\overline{\text{AACK}}$ is asserted. This cycle is referred to as the ARTRY window, since it is the cycle in which all devices sample

$\overline{\text{ARTRY}}$ to determine if the address tenure has completed successfully.

If an address tenure is not aborted by an assertion of $\overline{\text{ARTRY}}$, then the next bus master is free to assert $\overline{\text{TS}}$, the cycle after the ARTRY window to start a new address tenure. If $\overline{\text{ARTRY}}$ is asserted in the ARTRY window, all devices that are not asserting $\overline{\text{ARTRY}}$ must negate their bus request in the following cycle. This next cycle is called the BR window. The purpose of this protocol is to give immediate bus mastership to the device that asserted $\overline{\text{ARTRY}}$ with the expectation that that device will take this opportunity to clean up whatever circumstances caused it to assert $\overline{\text{ARTRY}}$. Typically, this involves writing data back to memory to maintain coherence in the system.

Data Tenures

Data tenures are more complicated to define than address tenures. They require two conditions to start: an assertion of $\overline{\text{TS}}$ that initiates a data transaction and a qualified assertion of the bus master's data bus grant. For a data bus grant to be considered qualified, no device on the bus may be asserting $\overline{\text{DBB}}$ in the cycle that the data bus grant is asserted.

Data transactions come in two types: single–beat transactions and burst transactions. The type is determined by the state of $\overline{\text{TBST}}$ during the address tenure of the transaction. If the bus master asserts $\overline{\text{TBST}}$, the transaction is a burst transaction and will require four assertions of $\overline{\text{TA}}$ in order to complete normally. If $\overline{\text{TBST}}$ is negated during the address tenure, the transaction only requires one assertion of $\overline{\text{TA}}$, thus the name single–beat.

Which device drives the data bus during a data transaction depends upon whether the transaction is a read or a write. For a read transaction, the slave device drives the data bus. For a write transaction, the master drives the data bus. In all data transactions, the slave device asserts $\overline{\text{TA}}$ to indicate that either valid data is present on the bus, in the case of a read; or that it is reading data off the data bus, in the case of a write. The master device asserts $\overline{\text{DBB}}$ the cycle after it has been granted the data bus and keeps it asserted until the data tenure has completed.

A data tenure can be aborted in two different ways. The address tenure for the transaction can be aborted by an assertion of $\overline{\text{ARTRY}}$. Or, the slave device may assert $\overline{\text{TEA}}$ to indicate that some error condition has been detected. Either event will prematurely terminate the data tenure.

Data Streaming

For the majority of data transactions there must be a wait state between the completion of one data tenure and the start of the next. This turnaround cycle avoids the contention on the data bus that would occur if one device starts driving data before another device has had a chance to turn off its data bus drivers. When a cache read hit is pipelined on top of another cache read hit, there is no need for this turnaround cycle since the same device will be driving the data bus for both data tenures. The 60X bus has the ability to remove this unnecessary wait state and allow back–to–back cache read hits to stream together. This ability is only enabled if the system is put into Fast L2 mode. Note that not all PowerPC processors support Fast L2 mode.

One of the requirements for taking advantage of this data streaming capability is that the system arbiter must be sophisticated enough to identify situations in which streaming may occur. Upon recognizing these situations, it must assert the processor's data bus grant in the cycle coincident with the fourth assertion of $\overline{\text{TA}}$ of the first cache read, so that the data tenure for the second cache read may commence in the next cycle.

Because it only recognizes qualified assertions of $\overline{\text{CPU DBG}}$, the MPC2604GA must not be aware of the processor's assertions of $\overline{\text{DBB}}$. This means that the $\overline{\text{DBB}}$ pin of the MPC2604GA must be tied to a pullup resistor rather than connected to the system $\overline{\text{DBB}}$ to which all other devices are connected. This forces the system arbiter to a level of sophistication such that it only supplies qualified data bus grants and thus the $\overline{\text{DBB}}$ signal is unnecessary to the whole system.

Note: In a 512KB configuration, the even and odd pair of MPC2604GA devices act as independent caches. Data streaming can only occur if the back to back read hits occur in the same pair. If the second read hit is not in the same pair as the first read hit, a wait state will occur between the two data tenures (2–1–1–1–2–1–1–1 timing).

Data Bus Parking

The MPC2604GA has the ability to respond to a processor read or write hit starting in the cycle after the processor has asserted $\overline{\text{TS}}$. This is referred to as a 2–1–1–1 response. However, even though the MPC2604GA has this ability, it is dependent upon the system to allow this quick of a response to occur. As discussed above, a data tenure cannot start until the master has been given a qualified bus grant. In order for the data tenure to start the cycle after $\overline{\text{TS}}$ is asserted, the data bus must be granted in the cycle coincident with the assertion of $\overline{\text{TS}}$. At bus speeds of 66 MHz it is extremely difficult for an arbiter to detect an assertion of $\overline{\text{TS}}$ and itself assert $\overline{\text{CPU DBG}}$ in the same cycle. In order to realistically allow this situation to occur, $\overline{\text{CPU DBG}}$ must be asserted independent of the processor's assertion of $\overline{\text{TS}}$.

Data bus parking is a system feature whereby the processor always has a qualified data bus grant when the data bus is idle. It is also a requirement for systems which seek to take advantage of the 2–1–1–1 response time capabilities of the MPC2604GA. This feature is typically present in arbiters that have the level of sophistication necessary to support data streaming. But it is also a feature of systems that do not even have a data bus arbiter. In these systems the data bus grant of every device in the system is tied to ground. The assertion of $\overline{\text{DBB}}$ by the current data bus master effectively removes the qualified data bus grant of all devices in the system, including its own. Note that in systems that have no data bus arbiter that it is impossible to take advantage of data streaming.

There is another caveat associated with data bus parking. Care must be taken when using data bus parking along with Fast L2 mode. In normal bus mode when the processor reads data off the bus, it will wait one cycle before passing the data on to internal functional units. The purpose of this one cycle waiting period is to check for an assertion of $\overline{\text{DRTRY}}$, which invalidates the data that has been already read. One of the advantages of running the processor in Fast L2 mode is that this internal processor wait state is removed.

A problem will arise, however, if the processor is given data the cycle after $\overline{\text{TS}}$ is asserted, as is possible with the MPC2604GA, and the transaction is aborted by some other device asserting $\overline{\text{ARTRY}}$. Because the processor will not

sample ARTRY until two cycles after the assertion of TS, the data read off the bus will have already been forwarded to the internal functional units. Thus, incorrect results may occur in the system.

To avoid this situation in a system that seeks to run Fast L2 mode with the data bus parked, there must be a guarantee that ARTRY will never be asserted for cache read hits. This is a further requirement to be imposed upon the DMA bridge and the memory controller. If this guarantee cannot be made, the data bus cannot be parked when running in Fast L2 mode.

Processor Reads

When the processor issues a read transaction, the MPC2604GA does a tag lookup to determine if this data is in the cache. If there is a cache hit and CI is not asserted, the MPC2604GA will assert L2 CLAIM and supply the data to the processor when the data tenure starts.

If the processor issues a cache–inhibited read (CI asserted) and the MPC2604GA detects a cache hit to a non–dirty, or clean, cache line, the line will be marked invalid. If the cache–inhibited read hits a dirty line, the MPC2604GA will assert ARTRY and write the dirty line back to memory.

If the read misses in the cache, the MPC2604GA will perform a linefill only if it is a burst read and it is not marked cache–inhibited. During a linefill, the MPC2604GA stores the data present on the bus as it is supplied by the memory controller.

Processor Writes

The conditions for asserting L2 CLAIM for processor writes are almost the same as for processor reads. There must be a cache hit and CI must not be asserted. In addition, however, WT must not be asserted. Single beat writes that are marked either write–through or cache–inhibited that hit in the cache cause the MPC2604GA to assert ARTRY and write the dirty line back to memory.

Transaction Pipelining

As explained in **Pipeline Depth**, the MPC2604GA can only handle one level of pipelining on the bus. Since the assertion of L2 CLAIM gives it the ability to assert AACK, the MPC2604GA has the ability to control this pipeline depth for transactions that are cache hits by delaying its assertion of AACK.

Pipelined cache hits are transactions that hit in the cache but occur while there is still an outstanding data transaction on the bus. The timing of the assertion of AACK for a pipelined cache hit is dependent upon the completion of the previous transaction. For explanation purposes, the previous transaction will be referred to as transaction one. The pipelined cache hit will be referred to as transaction two.

If transaction one is a cache hit, the MPC2604GA will be the slave device for the transaction. Since, for burst operations, the MPC2604GA always asserts TA for four consecutive clock cycles, the end of the data tenure for transaction one will be at a deterministic clock cycle. In this case, AACK for transaction two can be asserted coincident with the last assertion of TA for transaction one. If transaction one is not a cache hit, the MPC2604GA will wait until after the data tenure for transaction one has completed before asserting AACK to complete the address tenure of transaction two.

MEMORY COHERENCE

When a processor brings data into its on–chip cache and modifies it, a situation has arisen in which the main memory now contains irrelevant, or stale, data. Given that most systems support some form of DMA there must exist a means by which the processor is forced to write this modified, or dirty, data back to main memory. The DMA bridge is responsible for generating bus transactions to ensure that main memory locations accessed by DMA operations do not contain stale data. These transactions, called snoops, come in three different categories, each of which will be discussed below.

Snoops cause the processor and the MPC2604GA to check to see if they have dirty copies of the memory location specified in the snoop transaction. If either device does have a dirty copy it will assert ARTRY and make use of the opportunity presented in the BR window to write this data back to main memory.

Situations can arise where a cache line is dirty in both the processor's L1 cache and in the MPC2604GA. In cases such as these, snoop transactions should cause the processor to write its data back to memory since it is by definition more recent than the data in the MPC2604GA. Since ARTRY is a shared signal and it cannot be determined which devices are driving it, the MPC2604GA samples CPU BR in the BR window to determine if the snoop hit a dirty line in the L1 cache. If CPU BR is asserted during this window, the MPC2604GA will defer to the processor.

Snoop Reads

A snoop read causes dirty data to be written back to memory but allows both the L1 and L2 to keep a valid copy. In cases where the snoop hits a dirty cache line in the processor, the MPC2604GA will update its contents as the processor writes the data back to main memory.

Snoop reads can be implemented in two ways. One is that the DMA bridge can issue a clean transaction (TT[0:4] = 00000). The other is that the DMA bridge can do a read transaction (TT[0:4] = x1010). If the DMA bridge does a read transaction, the MPC2604GA determines that it is a snoop read rather than a processor read by the state of CPU BG the cycle before TS was asserted. If the processor was not granted the bus then the transaction had to have been issued by the DMA bridge and is therefore a snoop read.

Snoop Writes

Snoop writes also cause dirty data to be written back to main memory. The difference from a snoop read is that the cache line must then be invalidated in both the processor's cache and in the L2 cache. When the processor writes data back to memory in response to a snoop write, the MPC2604GA will not cache the data as it appears on the bus. If a valid copy resides in the cache, the MPC2604GA will invalidate it.

Again there are multiple transactions that can be used by the DMA bridge to implement a snoop write. It can issue a flush transaction (TT[0:4] = 00100), a read with intent to modify (TT[0:4] = x1110), or a write with flush (TT[0:4] = 00010). As with snoop reads, the MPC2604GA distinguishes between processor issued data transactions and snoop transactions by the state of CPU BG in the cycle previous to the assertion of TS.

Snoop Kills

Kills are snoops that cause cache entries to be immediately invalidated, regardless of whether they are dirty. This saves time if the DMA operation is going to modify all the data in the cache line. To implement a snoop kill the DMA bridge can issue a kill transaction (TT[0:4] = 01100) or a write with kill (TT[0:4] = 00110).

FOUR CHIP IMPLEMENTATION

The MPC2604GA has the ability to cascade two pairs of devices together to implement a 512KB cache. The **CFG1, CFG2** section discusses the details of configuring the devices for this type of implementation. The four chip implementation adds a level of complexity to the functionality of a copyback cache. This is due to the fact that in this situation there are essentially two independent caches that are sharing common arbitration signals for bus mastership. This section will discuss situations that can cause contention over these arbitration signals and how the MPC2604GA was designed to avoid these situations.

Multiple Castouts

Because each pair of MPC2604GAs has its own castout buffer (COB), it is possible for situations to arise in which both pairs need to do copyback operations. Under normal circumstances the two pairs will enter castout conditions at different times. In these cases, when a pair determines that it needs to do a castout, the $\overline{\text{L2 BR}}$ signal is first sampled. If $\overline{\text{L2 BR}}$ is already asserted then it is clear that the other pair is also in a castout situation. The late pair will wait until $\overline{\text{L2 BR}}$ is negated before continuing in its attempt to perform its castout.

Because of the BR window protocol associated with assertions of $\overline{\text{ARTRY}}$, it is possible for a situation to arise where pair two is waiting for pair one to do its castout before asserting $\overline{\text{L2 BR}}$. If there is an assertion of $\overline{\text{ARTRY}}$ by a device other than pair one, the pair one is required to negate $\overline{\text{L2 BR}}$ in the BR window. In order to prevent pair two from interpreting pair one's negation of $\overline{\text{L2 BR}}$ as an indication that pair one has completed its castout, a simple arbitration mechanism is used. Both pairs have a simple one–bit counter that is synchronized such that both counters always have the same value. For the purposes of performing a castout operation, the even pair can only assert $\overline{\text{L2 BR}}$ if the counter is zero. The odd pair can only assert $\overline{\text{L2 BR}}$ if the counter is one. This simple mechanism prevents both pairs from asserting $\overline{\text{L2 BR}}$ in the same cycle and therefore not being cognizant of the other pair's need to perform a castout.

Snoop Hit Before Castout

The other situation that can cause problems with a shared bus request occurs when a snoop hits a dirty line in one of the MPC2604GA pairs. If pair one has a cache line in its COB, it will assert $\overline{\text{L2 BR}}$ so that it may perform a castout operation. If a snoop hits a dirty line in pair two, it will assert both $\overline{\text{ARTRY}}$ and $\overline{\text{L2 BR}}$ so that it can write the snoop data back to main memory. When pair one detects that $\overline{\text{ARTRY}}$ has been asserted, it needs to be made aware that pair two needs to request the bus. Otherwise, at the same time that pair two is asserting $\overline{\text{L2 BR}}$, pair one will attempt to conform to the BR window protocol and negate $\overline{\text{L2 BR}}$. This situation is avoided by pair one sampling $\overline{\text{FDN}}$ when it detects that $\overline{\text{ARTRY}}$ has been asserted. If $\overline{\text{FDN}}$ is asserted at the same time as $\overline{\text{ARTRY}}$ is asserted, pair one will recognize that pair two is asserting $\overline{\text{ARTRY}}$. Pair one will then high–Z $\overline{\text{L2 BR}}$ so that there will not be contention when pair two is asserting $\overline{\text{L2 BR}}$.

MULTIPROCESSING

The MPC2604GA can be used as a common cache for up to four processors. For each processor there is a bus request, bus grant, and data bus grant signal pin on the MPC2604GA. Each of these pins needs to be connected to the respective processor's arbitration signals in the system.

The MPC2604GA treats multiple processors as one processor. Thus, the same restrictions on pipelining depth are true with regard to how many processor transactions can be outstanding at any one time. There can only be one data transaction from ANY processor pipelined on top of a current data transaction that was issued by ANY processor.

The data tenures for all processors must be performed in the same order as the address tenures on a system–wide basis. If processor one makes a request and then processor two makes a request, processor one's data tenure must precede processor two's data tenure. Note that this is not a 60X bus restriction, but rather a restriction necessary for proper operation of the MPC2604GA.

The MPC2604GA keeps coherent with the L1 caches of multiple processors as defined by the MESI (Modified–Exclusive–Shared–Invalid) protocol without actually implementing the protocol. This is possible for two reasons. Since the MPC2604GA is a look–aside cache, all transactions are monitored by all devices on the bus. Also, the MPC2604GA cannot, on its own, modify data. Thus, if one processor requests exclusive access to a cache line, it is not necessary for the MPC2604GA to invalidate its copy of the data, as would be required under the MESI protocol. If a second processor requests the same data, the transaction will cause the first processor to assert $\overline{\text{ARTRY}}$. This will prevent the MPC2604GA from supplying stale data to the second processor.

As discussed in **Data Bus Parking**, care must be taken when parking the data bus in Fast L2 mode. By the nature of MP systems running under the MESI protocol there will be assertions of $\overline{\text{ARTRY}}$ to abort cache read hits. Thus, in an MP system, the data bus cannot be parked to any processor if the system is to be run in Fast L2 mode.

ASYNCHRONOUS SIGNALS

The MPC2604GA supports four asynchronous control signals. These signals were originally defined in the PowerPC Reference Platform (PReP) specification. Because these signals are defined to be asynchronous, the MPC2604GA must synchronize them internally. This process takes eight clock cycles. Thus, to guarantee recognition by the MPC2604GA, assertions of any one of these signals must last a minimum of eight clock cycles.

$\overline{\text{L2 FLUSH}}$

When $\overline{\text{L2 FLUSH}}$ is asserted, the MPC2604GA initiates an internal sequence that steps through every cache line present. Valid lines that are clean are immediately marked invalid. Valid lines that are dirty must be written back to main memory.

To keep memory up to date, the MPC2604GA must still monitor all transactions on the bus. Any transaction that is

not a processor burst write will cause the MPC2604GA to assert ARTRY. Burst writes cause the MPC2604GA to do a lookup on the affected address and mark the line invalid if it is present.

Because the MPC2604GA must still monitor all transactions, it cannot use the tag RAM for the flush sequence unless there is a guarantee that no new transaction will be initiated on the bus. The only way to ensure that no new transactions will occur is for the MPC2604GA to be granted the bus. Thus, upon entering the sequence initiated by the assertion of L2 FLUSH, the MPC2604GA will assert L2 BR. As soon as L2 BG is asserted, the MPC2604GA can start stepping through the tag RAM entries.

L2 FLUSH need not be held asserted for the flush sequence to complete. Once started the sequence will run to completion unless overridden by an assertion of HRESET.

L2 MISS INH

When L2 MISS INH is asserted, the MPC2604GA will not load any new data into the cache. The data already present will remain valid and the MPC2604GA will respond to cache hits. This condition only lasts as long as L2 MISS INH is asserted. When L2 MISS INH is negated, the MPC2604GA will start to bring new data into the cache when there are cache misses.

L2 TAG CLR

When L2 TAG CLR is asserted, the MPC2604GA will invalidate all entries in the cache. This internal sequence is the same as the one initiated by an assertion of HRESET. During this sequence, the MPC2604GA will not participate in any bus transaction. However, it will keep track of all bus transactions so that when the sequence is finished, the MPC2604GA can immediately participate in the next bus transaction.

As is the case with assertions of L2 FLUSH, an assertion of L2 TAG CLR need not be held for the duration of the sequence. Once asserted the sequence will run to completion regardless of the state of L2 TAG CLR.

L2 UPDATE INH

When L2 UPDATE INH is asserted, the MPC2604GA is disabled from all activity. Bus transactions continue to be monitored so that as soon as L2 UPDATE INH is negated, the MPC204GA can participate in the next transaction.

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Reference Application Note AN1265, "Configuring the MPC2604GA Integrated L2 Cache with the MPC106."

READ HIT/WRITE HIT

Figure 1 shows a read hit from an idle bus state. The MPC2604GA asserts $\overline{\text{L2 CLAIM}}$ the cycle after $\overline{\text{TS}}$ to inform the memory controller that there is a cache hit and the cache will control the rest of the transaction. $\overline{\text{L2 CLAIM}}$ is held through the cycle after $\overline{\text{AACK}}$ is asserted. Since there are no active data tenures from previous transactions, the MPC2604GA asserts $\overline{\text{AACK}}$ the cycle after $\overline{\text{TS}}$ is asserted.

Note there must be a qualified assertion of $\overline{\text{CPU DBG}}$ in the same cycle as the assertion of $\overline{\text{TS}}$ for the MPC2604GA to respond with $\overline{\text{TA}}$ in the next cycle. $\overline{\text{CPU DBG}}$ does not affect the timing of $\overline{\text{L2 CLAIM}}$ or $\overline{\text{AACK}}$.

The write hit timing is virtually the same. The only difference is the processor drives the data instead of the MPC2604GA.

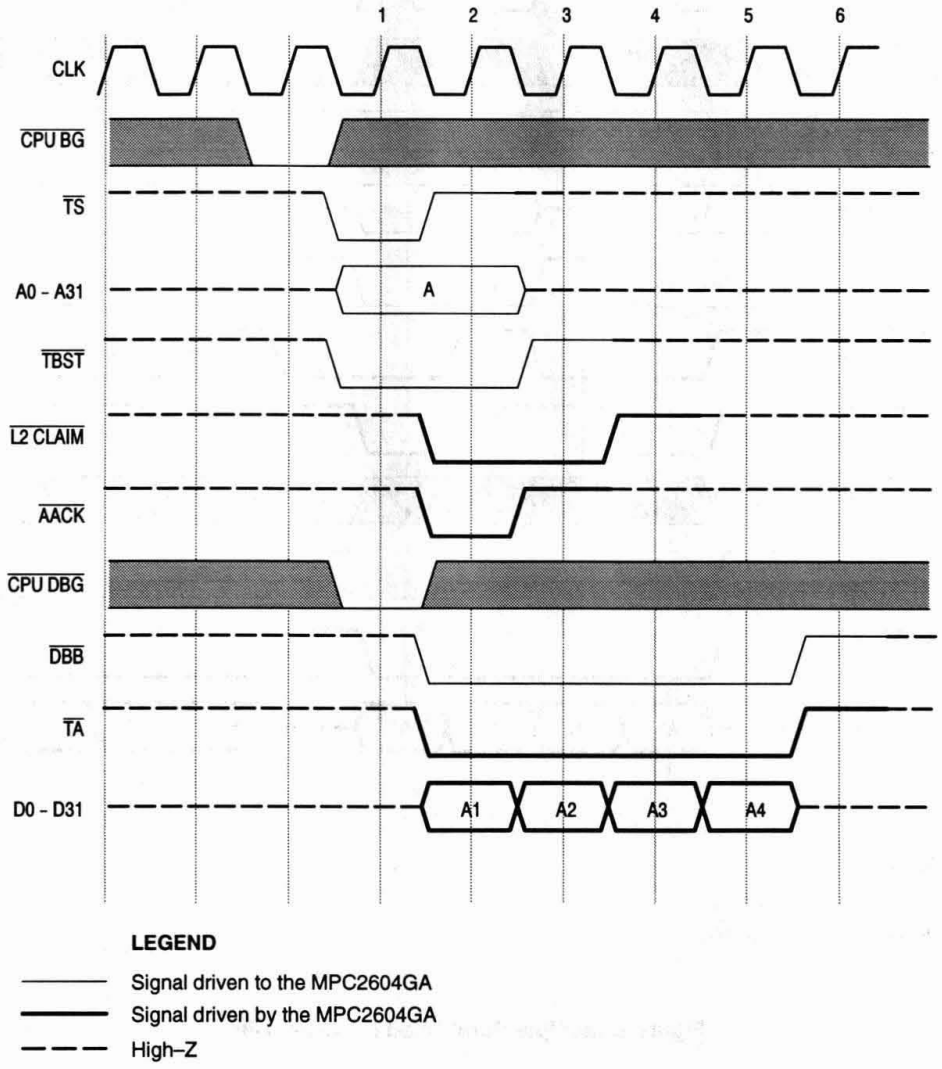

Figure 1. Burst Read (or Write) Hit

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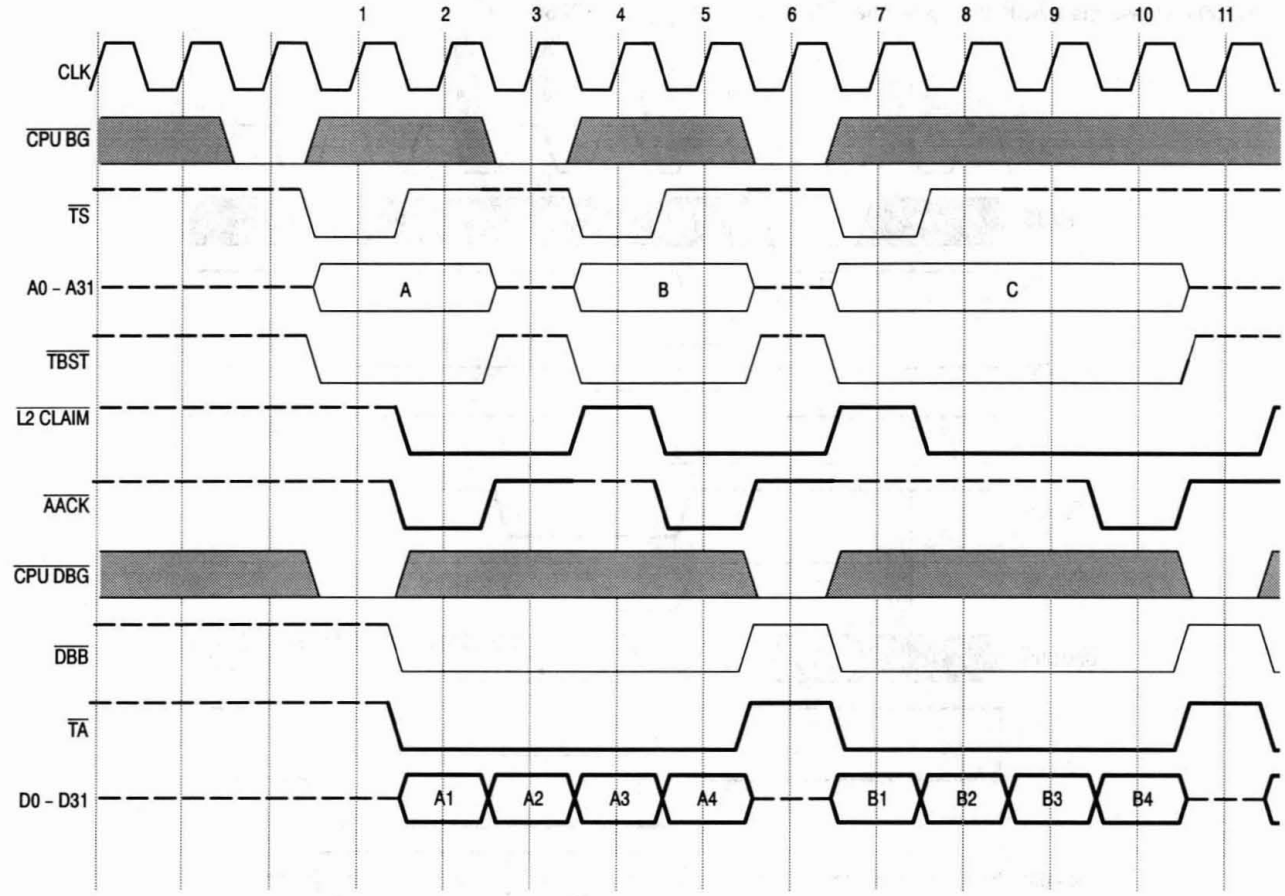
MULTIPLE READ/WRITE HITS (NORMAL BUS MODE)

Figure 2 is an illustration of MPC2604GA pipeline depth limit with multiple read hits. The MPC2604GA supports only one level of address pipelining for data transfer. Therefore, it must hold off on its assertion of $\overline{AACK}$ for a pipelined $\overline{TS}$ until the data tenure for the first $\overline{TS}$ is done. The MPC2604GA asserts $\overline{AACK}$ at the same time as the fourth $\overline{TA}$ for data tenures that it controls.



LEGEND

Signal driven to the MPC2604GA

Signal driven by the MPC2604GA

High–Z

Figure 2. Multiple Burst Read (or Write) Hits

READ MISS (NORMAL BUS MODE)

Figure 3 is an illustration of MPC2604GA pipeline depth with a read miss followed by a read hit.

For illustration purposes the read miss is shown as a 3–1–1–1 response from memory. $\overline{AACK}$ for the second access is not driven true until the cycle after the fourth $\overline{TA}$ of the read miss. This is because the MPC2604GA is not in control of $\overline{TA}$ for the first access and must, therefore, wait until the first access' data tenure is complete before it can drive $\overline{AACK}$ true for the read hit.

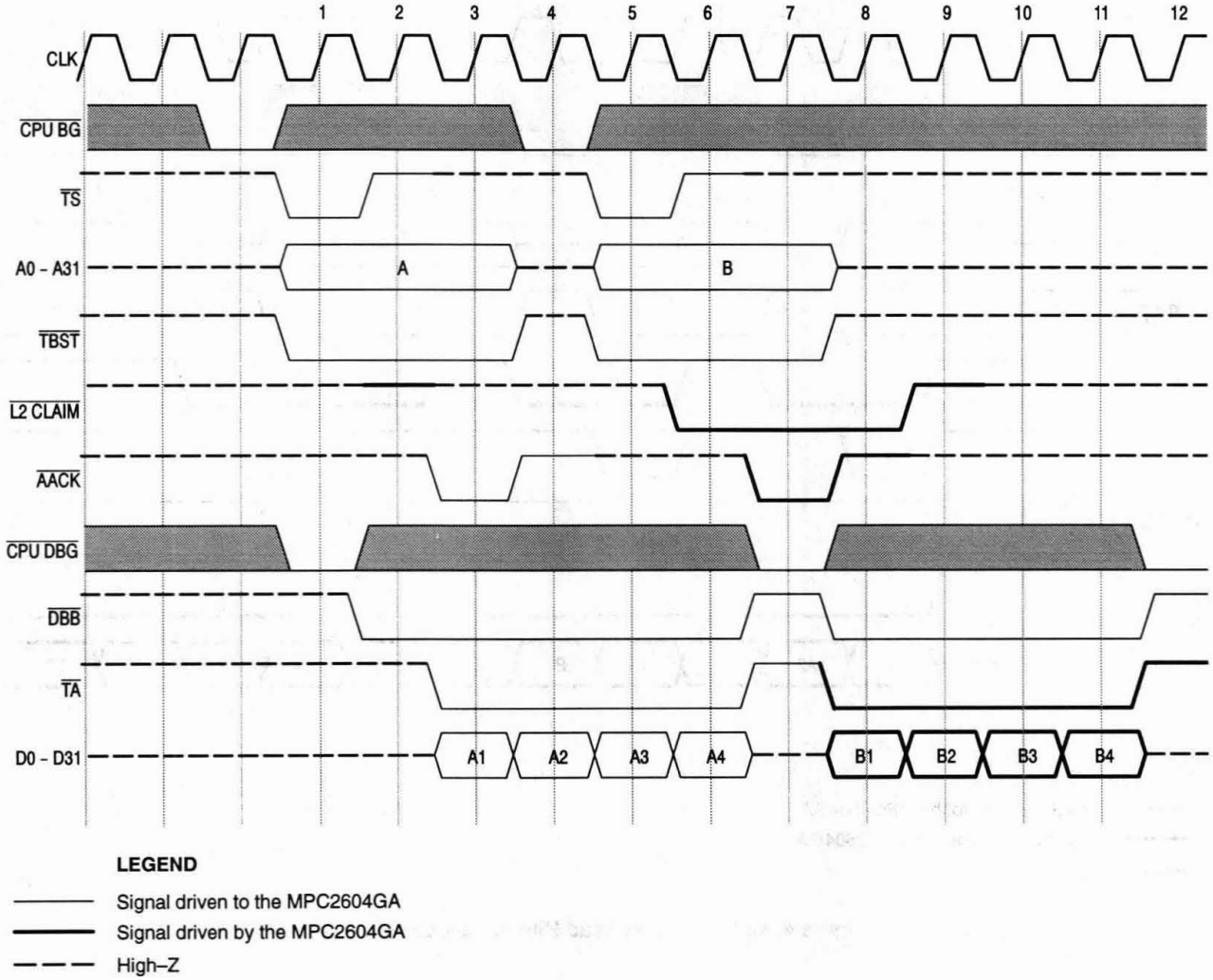


Figure 3. Read Miss Followed by a Burst Read Hit for MPC603/604

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MULTIPLE READ HITS (FAST L2 MODE)

Back to back pipelined burst read hits for the MPC604 in Fast L2 mode, also called data streaming mode, are shown in Figure 4. Note that $\overline{\text{CPU DBG}}$ is negated except for the cycles coincident with the fourth $\overline{\text{TA}}$ of each data tenure. This is a requirement for data streaming. Note also that $\overline{\text{DBB}}$ is not shown. For proper operation in Fast L2 mode the $\overline{\text{DBB}}$ pin of the MPC2604GA must be tied to a pull–up resistor.

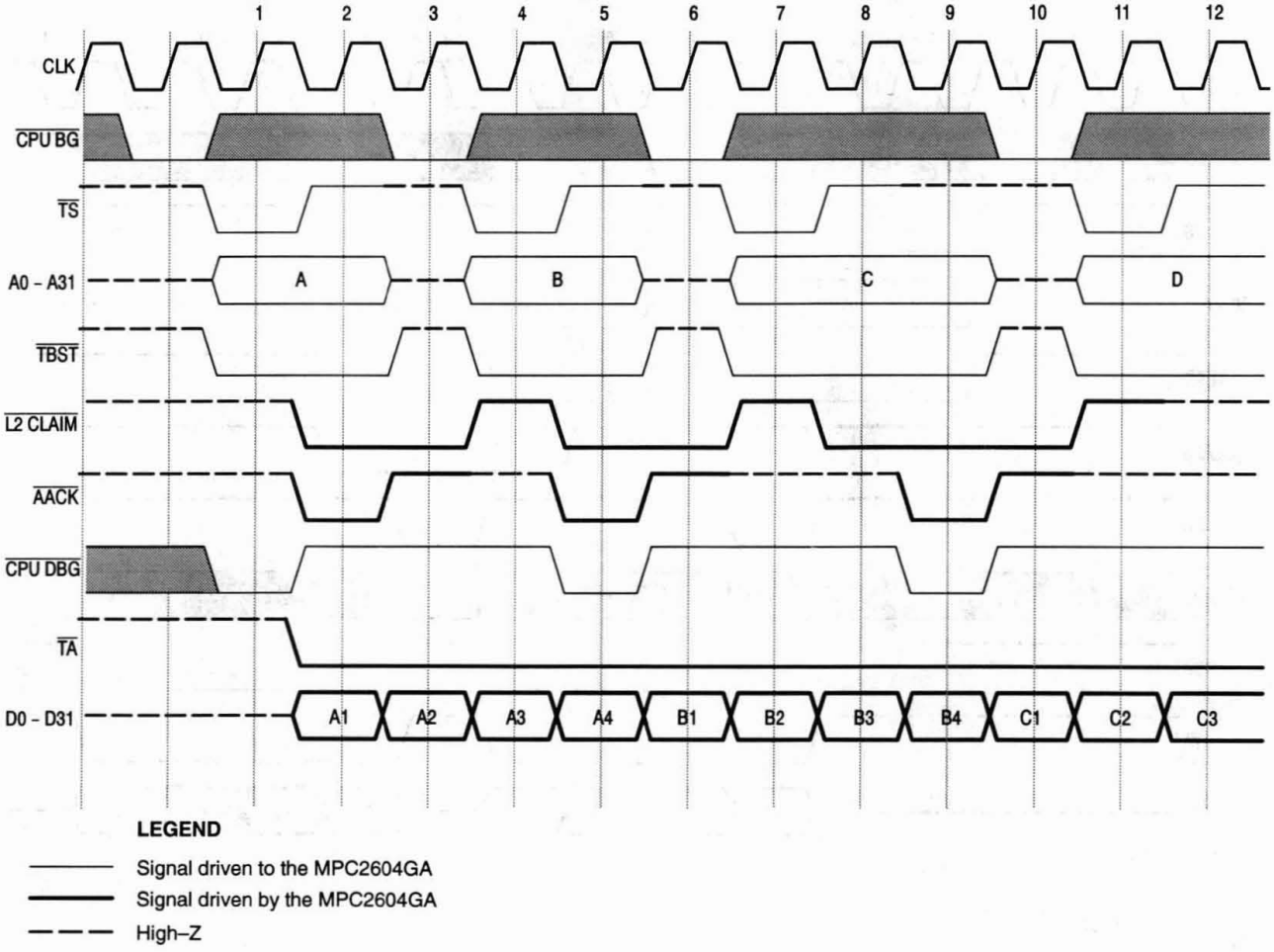


Figure 4. Multiple Burst Read Hits in Fast L2 Mode

5

WRITE THROUGH BURST WRITE HIT

Figure 5 shows the fastest possible burst write hit to a write–through mode L2 cache line, read miss or write miss processing that replaces a clean line. For these operations MPC2604GA will not assert any signals on the 60X bus. A cache line is considered write through if $\overline{WT}$ is asserted by the processor when it asserts $\overline{TS}$.

The speed at which a write–through operation completes is solely dependent on the memory controller. The timing shown here assumes that the memory controller has a write buffer that can accept data this quickly.

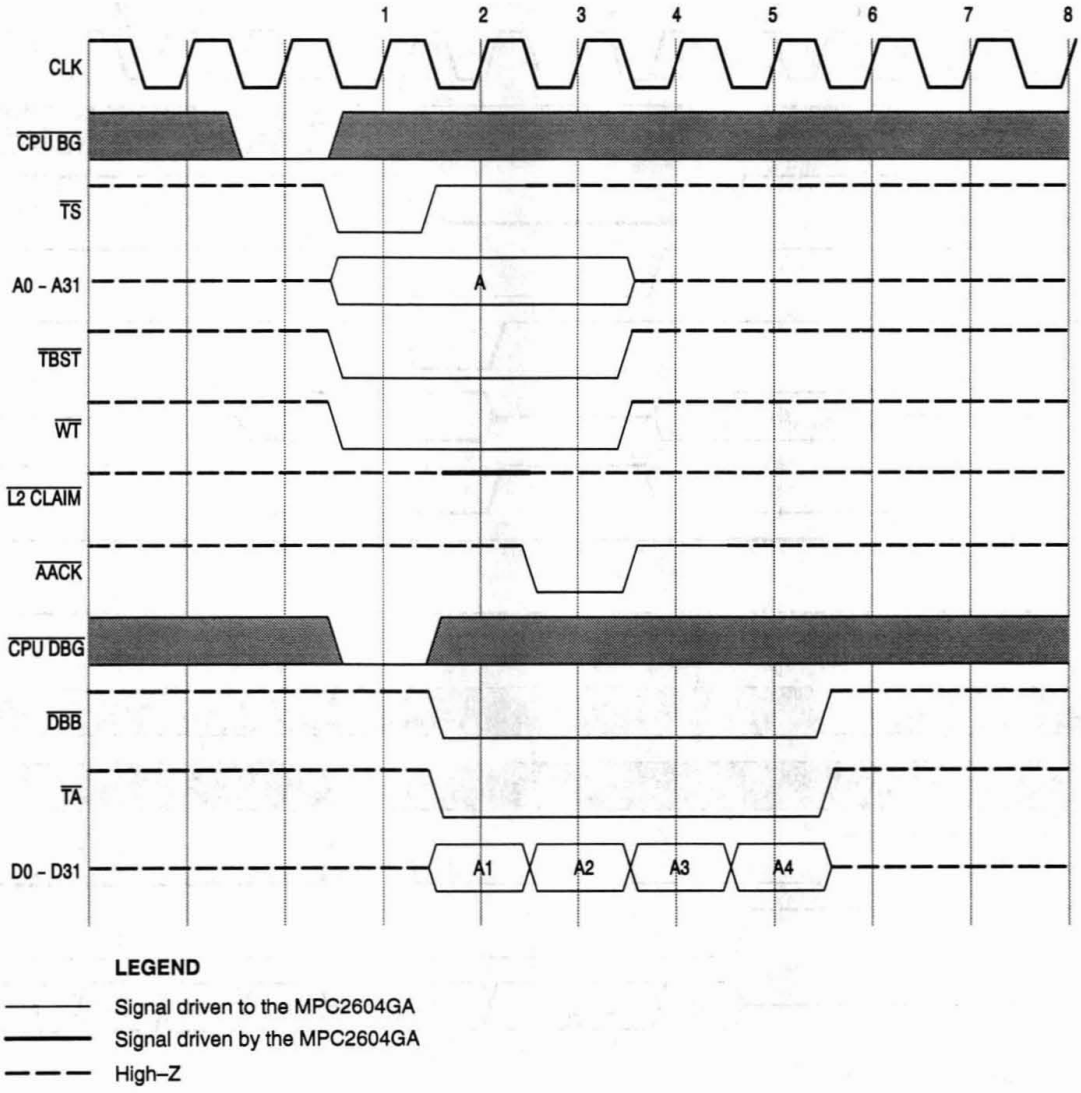
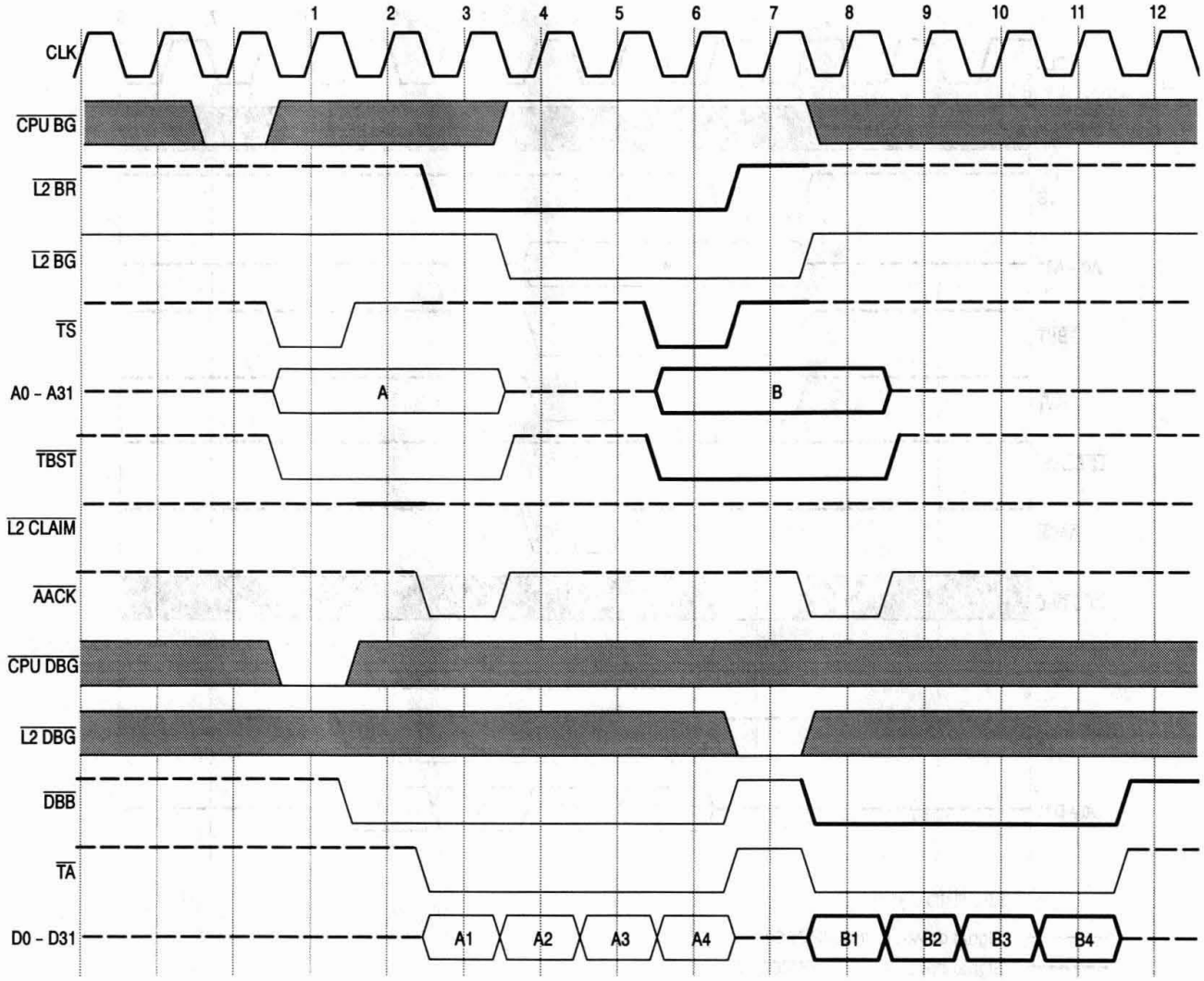


Figure 5. Fastest Possible Write Through Burst Write Hit for MPC603/604

5

READ/WRITE MISS

Figure 6 is an illustration of a processor read or write miss that causes the MPC2604GA to replace a dirty line. $\overline{\text{L2 BR}}$ is asserted two clocks after $\overline{\text{TS}}$. The dirty data to be replaced is moved into the internal Cast Out Buffer (COB) at the same time the new data is written into the cache. Note that the copyback operation occurs after the processor request is satisfied. In addition, no delay is added to the processor transaction. It proceeds as fast as the memory controller will allow.



LEGEND

Signal driven to the MPC2604GA

Signal driven by the MPC2604GA

High–Z

Figure 6. Read or Write Miss Followed by Castout

READ/WRITE SNOOP HIT (DIRTY L2 LINE)

Figure 7 is an illustration of a read or write snoop to a cache line that is dirty in the L2, but is not dirty in the processor's cache. When a snoop hits a dirty line, the MPC2604GA will assert $\overline{\text{ARTRY}}$ through the cycle following the assertion of $\overline{\text{AACK}}$. This cycle is called the ARTRY window. Note that the MPC2604GA also asserts $\overline{\text{L2 BR}}$ at the same time it asserts $\overline{\text{ARTRY}}$. Because the snoop could also have hit a dirty line in the processor's cache, the MPC2604GA samples the processor's $\overline{\text{BR}}$ signal the cycle following the ARTRY window. This cycle is called the BR window. If the processor's $\overline{\text{BR}}$ signal is not asserted, the MPC2604GA will start sampling $\overline{\text{L2 BG}}$, the cycle after the BR window.

Note that the MPC2604GA cannot do a 2–1–1–1 copy back burst. The earliest that it can handle the first assertion of $\overline{\text{TA}}$ is two cycles after its assertion of $\overline{\text{TS}}$.

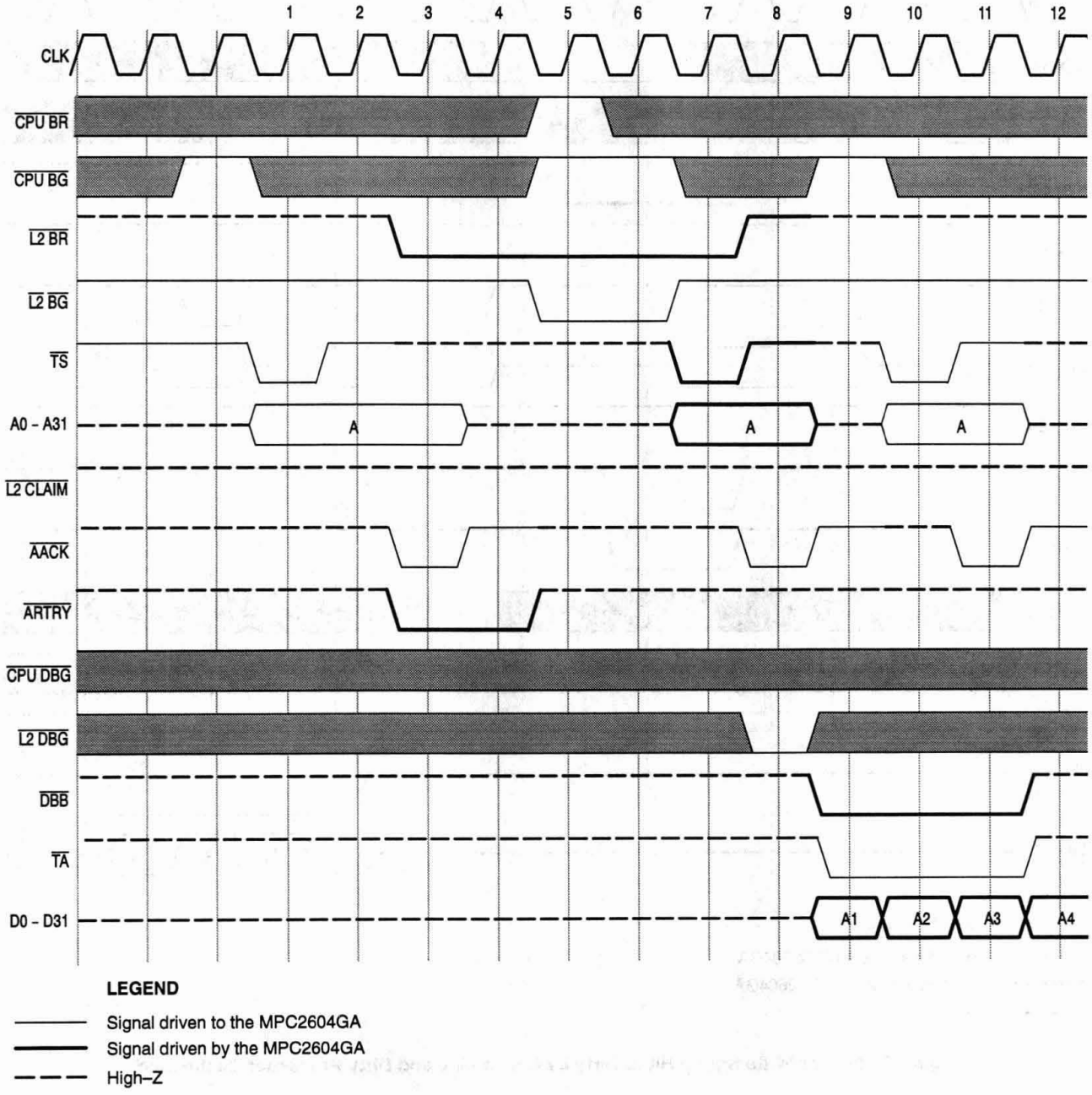


Figure 7. Read or Write Snoop Hit to Dirty L2 Cache Line and Clean Processor Cache Line

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READ/WRITE SNOOP HIT (DIRTY L2 AND PROCESSOR LINE)

An illustration of PowerPC read or write snoop hit to a dirty L2 cache line is shown in Figure 8. The processor has a dirty copy of the cache line. In this case both the processor and the MPC2604GA assert $\overline{\text{ARTRY}}$. This situation is detected by sampling $\overline{\text{CPU BR}}$ in the BR window, as described in the previous example. If $\overline{\text{CPU BR}}$ is asserted in the BR window, the MPC2604GA will negate $\overline{\text{L2 BR}}$. It will also ignore assertions of $\overline{\text{L2 BG}}$. This allows the processor to write back its dirty cache line, at which time the MPC2604GA will either update or invalidate its copy depending on whether it is a snoop read or snoop write.

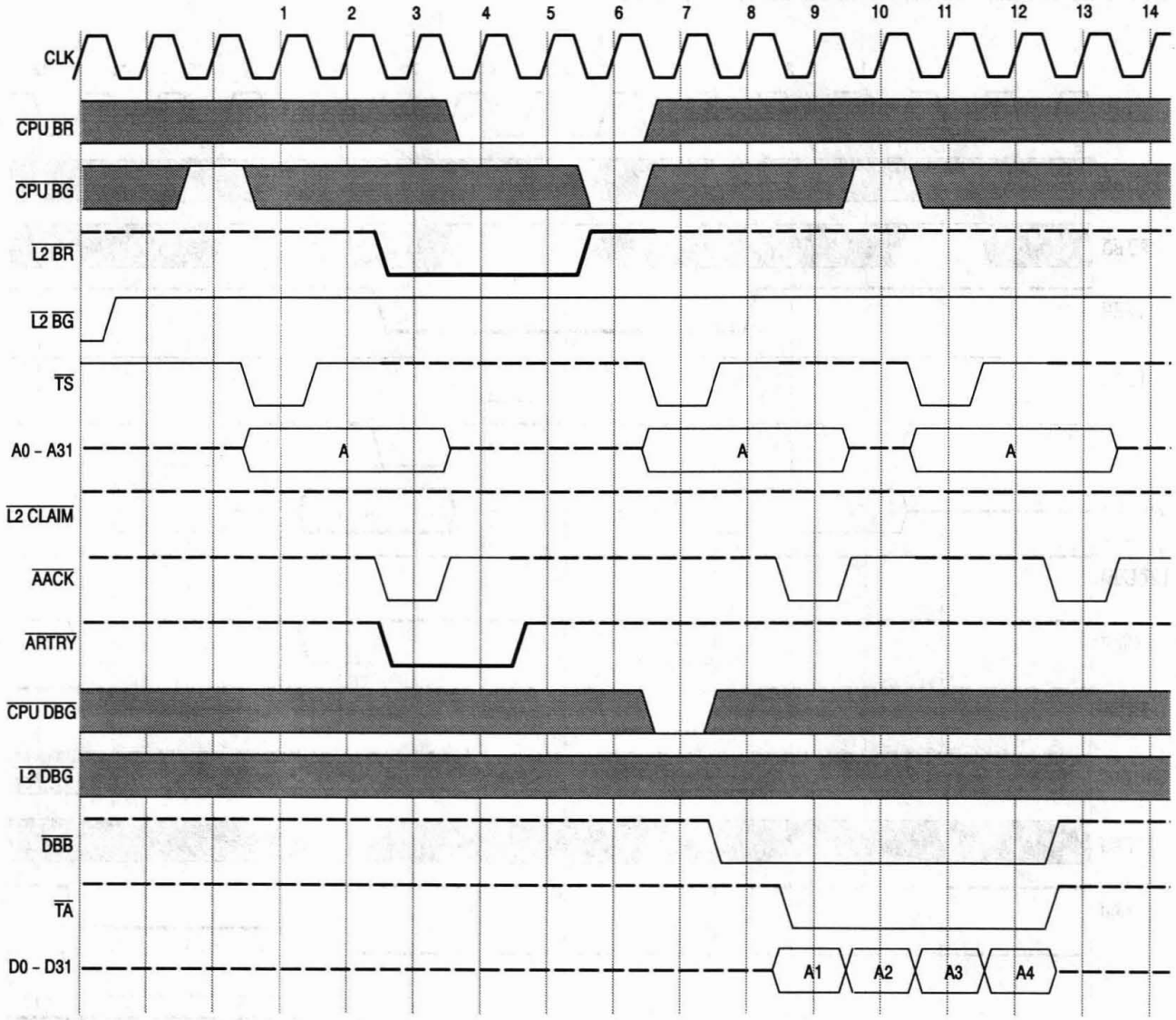

Figure 8. Read or Write Snoop Hit to Dirty L2 Cache Line and Dirty Processor Cache Line

READ HIT/WRITE HIT (WITHOUT $\overline{\text{CPU DBG}}$ PARKED)

Most of the previous examples have assumed $\overline{\text{CPU DBG}}$ is asserted in the same cycle that the processor asserts $\overline{\text{TS}}$. This implies $\overline{\text{CPU DBG}}$ is parked. In some systems it may not be desirable or possible to park $\overline{\text{CPU DBG}}$. Figure 9 shows the response for a read hit from the MPC2604GA is gated by the assertion of $\overline{\text{CPU DBG}}$. The fastest response possible in a system that does not park $\overline{\text{CPU DBG}}$ is 3–1–1–1.

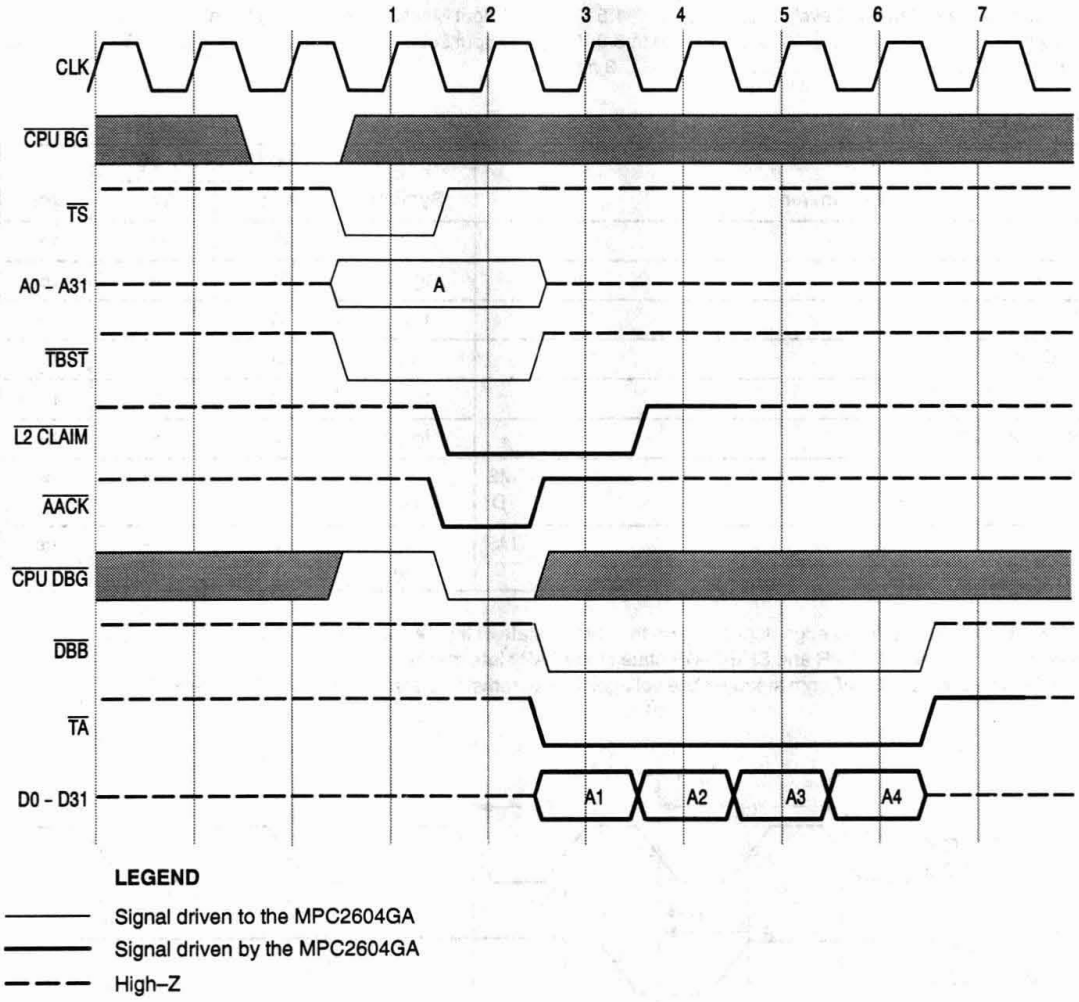

Figure 9. Burst Read (or Write) Hit Without $\overline{\text{CPU DBG}}$ Parked

5

JTAG

AC OPERATING CONDITIONS AND CHARACTERISTICS FOR THE TEST ACCESS PORT (IEEE 1149.2 (Proposed))

(T_J = 20 to + 110°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Measurement Timing Level ..... 1.5 V
Output Load ..... 50 Ω Termination to 1.5 V

TAP CONTROLLER TIMING

Parameter	Symbol	MPC2604GA–66		Unit	Notes
		Min	Max		
Cycle Time	t_{CK}	30	—	ns	
Clock High Time	t_{CKH}	12	—	ns	
Clock Low Time	t_{CKL}	12	—	ns	
Clock Low to Output Valid	t_A	5	9	ns	
Clock Low to Output High–Z	t_{CKZ}	0	9	ns	1
Clock Low to Output Active	t_{CKX}	0	9	ns	2, 3
Setup Times: TMS TDI	t_s t_{sd}	2	—	ns	
Hold Times: TMS TDI	t_h t_{hd}	2	—	ns	

NOTES:
1. TDO will High–Z from a clock low edge depending on the current state of the TAP state machine.
2. TDO is active only in the SHIFT–IR and SHIFT–DR state of the TAP state machine.
3. Transition is measured ± 500 mV from steady–state voltage. This parameter is sampled and not 100% tested.

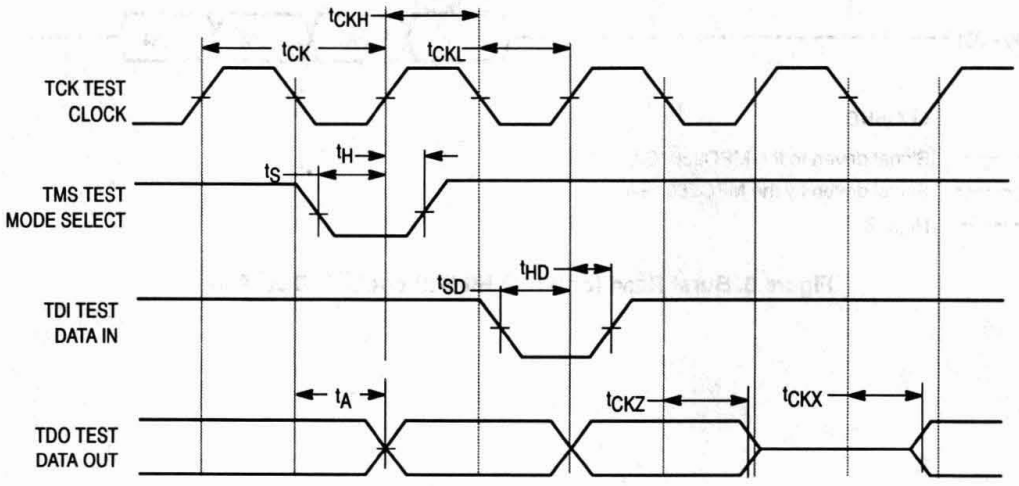

Figure 10. TAP Controller Timing

INSTRUCTION SET

A four pin IEEE Standard 1149.2 Test Port (JTAG) is included on this device. When the TAP (Test Access Port) controller is in the SHIFT–IR state, the instruction register is placed between TDI and TDO. In this state, the desired instruction would be serially loaded through the TDI input. The TAP instruction set for this device are as follows.

STANDARD INSTRUCTIONS

Instruction	Code (Binary)	Description
BYPASS	1111*	Bypass instruction
SAMPLE/PRELOAD	0010	Sample and/or preload instruction
EXTEST	0000	Extest instruction
HIGH–Z	1001	High–Z all output pins while bypass register is between TDI and TDO
CLAMP	1100	Clamp output pins while bypass register is between TDI and TDO

* Default state at power–up.

TAP STANDARD INSTRUCTION SET

NOTE

The descriptions in this section are not intended to be used without the supporting IEEE 1149.1 – 1995 Standard.

SAMPLE/PRELOAD TAP INSTRUCTION

The SAMPLE/PRELOAD TAP instruction is used to allow scanning of the boundary–scan register without causing interference to the normal operation of the chip logic. The 123–bit boundary–scan register contains bits for all device signal and clock pins and associated control signals. This register is accessible when the SAMPLE/PRELOAD TAP instruction is loaded into the TAP instruction register in the SHIFT–IR state. When the TAP controller is then moved to the SHIFT–DR state, the boundary–scan register is placed between TDI and TDO. This scan register can then be used prior to the EXTEST instruction to preload the output pins with desired values so that these pins will drive the desired state when the EXTEST instruction is loaded. As data is written into TDI, data also streams out TDO which can be used to pre–sample the inputs and outputs.

SAMPLE/PRELOAD would also be used prior to the CLAMP instruction to preload the values on the output pins that will be driven out when the CLAMP instruction is loaded.

EXTEST TAP INSTRUCTION

The EXTEST instruction is intended to be used in conjunction with the SAMPLE/PRELOAD instruction to assist in testing board level connectivity. normally, the SAMPLE/PRELOAD instruction would be used to preload all output pins. The EXTEST instruction would then be loaded. During EXTEST, the boundary–scan register is placed between TDI and TDO in the SHIFT–DR state of the TAP controller. Once the EXTEST instruction is loaded, the TAP controller would then be moved to the Run–Test/Idle state. In this state, one cycle of TCK would cause the preloaded data on the output pins to be driven while the values on the input pins would be sampled. Note the TCK, not the clock pin (CLK), is used as the clock input while CLK is only sampled during EXTEST. After one clock cycle of TCK, the TAP controller would then be moved to the SHIFT–DR state where the sampled values would be shifted out of TDO (and new values would be shifted in TDI). These values would normally be compared to expected values to test for board connectivity.

CLAMP TAP INSTRUCTION

The CLAMP instruction is provided to allow the state of the signals driven from the output pins to be determined from the boundary–scan register while the bypass register is selected as the serial path between TDI and TDO. The signals driven from the output pins will not change while the CLAMP instruction is selected. EXTEST could also be used for this purpose, but CLAMP shortens the board scan path by inserting only the bypass register between TDI and TDO. To use CLAMP, the SAMPLE/PRELOAD instruction would be used first to scan in the values that will be driven on the output pins when the CLAMP instruction is active.

HIGH–Z TAP INSTRUCTION

The HIGH–Z instruction is provided to allow all the outputs to be placed in an inactive drive state (high–Z). During the HIGH–Z instruction the bypass register is connected between TDI and TDO.

BYPASS TAP INSTRUCTION

The BYPASS instruction is the default instruction loaded at power up. This instruction will place a single shift register between TDI and TDO during the SHIFT–DR state of the TAP controller. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

DISABLING THE TEST ACCESS PORT AND BOUNDARY SCAN

It is possible to use this device without utilizing the four pins used for the test access port. To circuit disable the device, TCK must be tied to V_{SS} to preclude mid level inputs. Although TDI and TMS are designed in such a way that an undriven input will produce a response equivalent to the application of a logic 1, it is still advisable to tie these inputs to V_{DD} through a 1K resistor. TDO should remain unconnected.

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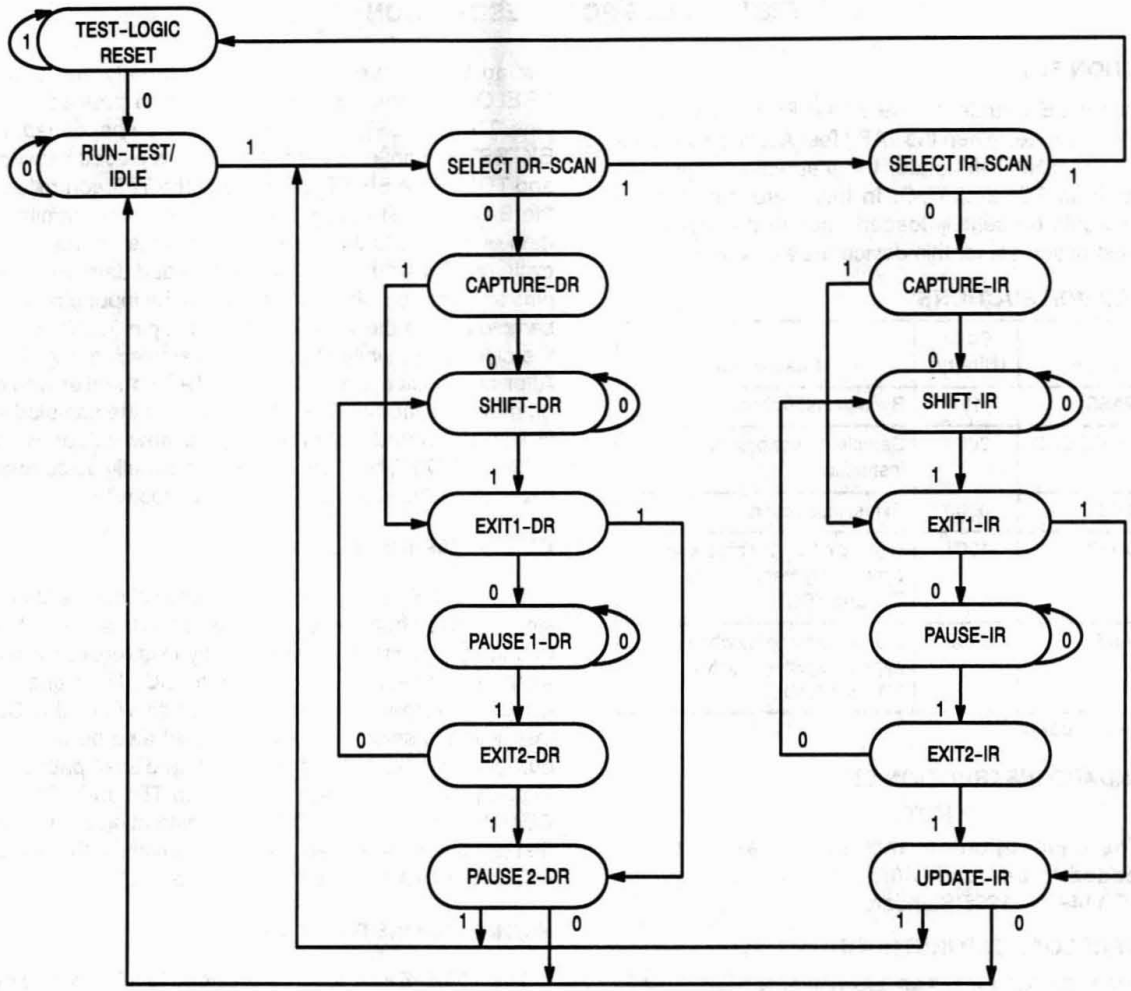

NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 11. TAP Controller State Diagram

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BOUNDARY SCAN ORDER

BIT NUMBER

The order of the boundary scan chain. Bit 0 is the closest to TDO.

BIT/PIN NAME

The name of the physical pin. For an output enable cell, this is the name of the corresponding output enable.

BIT/PIN TYPE

Input — Input only pin.
I/O — Bi–directional pin that can be put into high–Z state.
Output Enable — Boundary scan cell to hold the output enable state of other I/O pads. Output enable does not correspond to a physical pin. To set an I/O to an input, the output enable must have a 1. To set an I/O to an output, the output enable must have a 0. Note that these internal output enables are active low.

OUTPUT ENABLE

The name of the output enable cell that determines if the cell is enabled or in the high–Z state. If the pin type is input or output enable, this entry will be empty.

Bit Number	Bit/Pin Name	Bit/Pin Type	Output Enable
0	D13	I/O	DOE
1	D14	I/O	DOE
2	D15	I/O	DOE
3	D10	I/O	DOE
4	D11	I/O	DOE
5	D12	I/O	DOE
6	DP1	I/O	DOE
7	D8	I/O	DOE
8	D9	I/O	DOE
9	D5	I/O	DOE
10	D6	I/O	DOE
11	D7	I/O	DOE
12	D2	I/O	DOE
13	D3	I/O	DOE
14	D4	I/O	DOE
15	DP0	I/O	DOE
16	D0	I/O	DOE
17	D1	I/O	DOE
18	DP2	I/O	DOE
19	D17	I/O	DOE
20	D16	I/O	DOE
21	D18	I/O	DOE
22	D19	I/O	DOE
23	D20	I/O	DOE
24	D21	I/O	DOE
25	D22	I/O	DOE
26	D23	I/O	DOE
27	DP3	I/O	DOE
28	D24	I/O	DOE
29	D25	I/O	DOE
30	D26	I/O	DOE
31	D27	I/O	DOE
32	D28	I/O	DOE
33	D29	I/O	DOE
34	D30	I/O	DOE
35	D31	I/O	DOE
36	$\overline{\text{CPU4 BR}}$	Input	
37	$\overline{\text{L2 UPDATE INH}}$	Input	
38	PWRDN	Input	
39	$\overline{\text{L2 MISS INH}}$	Input	
40	$\overline{\text{L2 TAG CLR}}$	Input	
41	$\overline{\text{L2 BG}}$	Input	
42	$\overline{\text{L2 FLUSH}}$	Input	
43	CFG5	Input	
44	CFG0	Input	
45	CFG1	Input	
46	CFG2	Input	
47	$\overline{\text{CPU3 BR}}$	Input	
48	$\overline{\text{MODE4P}}$	Input	
49	$\overline{\text{CPU2 DBG}}$	Input	
50	$\overline{\text{CPU2 BG}}$	Input	
51	$\overline{\text{CPU2 BR}}$	Input	
52	$\overline{\text{FDN}}$	I/O	FDNOE
53	$\overline{\text{L2 DBG}}$	Input	
54	$\overline{\text{L2 BR}}$	I/O	L2BROE
55	$\overline{\text{L2 CLAIM}}$	I/O	L2CLAIMOE
56	$\overline{\text{CPU DBG}}$	Input	
57	$\overline{\text{CPU BG}}$	Input	
58	$\overline{\text{AACK}}$	I/O	AACKOE
59	$\overline{\text{ARTRY}}$	I/O	ARTRYOE
60	$\overline{\text{CPU3 DBG}}$	Input	
61	$\overline{\text{CPU4 DBG}}$	Input	
62	$\overline{\text{CI}}$	I/O	AOE
63	$\overline{\text{WT}}$	I/O	AOE
64	$\overline{\text{CPU BR}}$	Input	

Bit Number	Bit/Pin Name	Bit/Pin Type	Output Enable
65	$\overline{\text{HRESET}}$	Input	
66	TSIZ0	I/O	AOE
67	TSIZ1	I/O	AOE
68	TSIZ2	I/O	AOE
69	$\overline{\text{SRESET}}$	Input	
70	$\overline{\text{TBST}}$	I/O	AOE
71	TT2	I/O	AOE
72	TT1	I/O	AOE
73	TT0	I/O	AOE
74	$\overline{\text{CPU3 BG}}$	Input	
75	TT4	I/O	AOE
76	$\overline{\text{TS}}$	I/O	AOE
77	$\overline{\text{TA}}$	I/O	TAOE
78	TT3	I/O	AOE
79	$\overline{\text{CPU4 BG}}$	Input	
80	$\overline{\text{TEA}}$	Input	
81	$\overline{\text{DBB}}$	I/O	DBBOE
82	TAOE	Output Enable	
83	L2CLAIMOE	Output Enable	
84	L2BROE	Output Enable	
85	FDNOE	Output Enable	
86	DBBOE	Output Enable	
87	DOE	Output Enable	
88	ARTRYOE	Output Enable	
89	AACKOE	Output Enable	
90	A0	I/O	AOE

Bit Number	Bit/Pin Name	Bit/Pin Type	Output Enable
91	A1	I/O	AOE
92	A2	I/O	AOE
93	A3	I/O	AOE
94	A4	I/O	AOE
95	A5	I/O	AOE
96	A6	I/O	AOE
97	A7	I/O	AOE
98	A8	I/O	AOE
99	A9	I/O	AOE
100	A10	I/O	AOE
101	A11	I/O	AOE
102	A12	I/O	AOE
103	A13	I/O	AOE
104	A14	I/O	AOE
105	A15	I/O	AOE
106	A16	I/O	AOE
107	A17	I/O	AOE
108	A18	I/O	AOE
109	A19	I/O	AOE
110	A20	I/O	AOE
111	A21	I/O	AOE
112	A22	I/O	AOE
113	A23	I/O	AOE
114	A24	I/O	AOE
115	A25	I/O	AOE
116	A26	I/O	AOE
117	A27	I/O	AOE
118	A28	I/O	AOE
119	A29	I/O	AOE
120	A30	I/O	AOE
121	A31	I/O	AOE
122	AOE	Output Enable	

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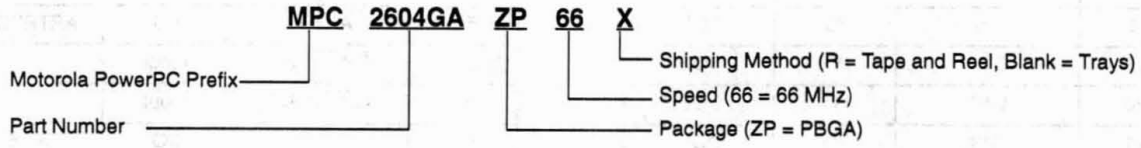
ORDERING INFORMATION
(Order by Full Part Number)

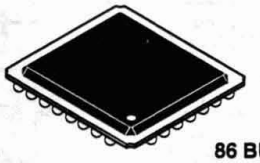

MPC 2604GA ZP 66 X
Motorola PowerPC Prefix
Part Number
Shipping Method (R = Tape and Reel, Blank = Trays)
Speed (66 = 66 MHz)
Package (ZP = PBGA)

Full Part Number — MPC2604GAZP66 MPC2604GAZP66R

MCM67Q909

Advance Information

512K x 9 Bit Separate I/O Synchronous Fast Static RAM



86 BUMP PBGA
CASE 896A–02

The MCM67Q909 is a 4M bit static random access memory, organized as 512K words of 9 bits. It features separate TTL input and output buffers, which drive 3.3 V output levels, and incorporates input and output registers on board with high speed SRAM. It also features transparent–write and data pass–through capabilities.

The synchronous design allows for precise cycle control with the use of an external single clock (K). The addresses (A0 – A18), data input (D0 – D8), data output (Q0 – Q8), write–enable ($\overline{W}$), chip–enable ($\overline{E}$), and output–enable ($\overline{G}$), are registered on the rising edge of clock (K).

The control pins ($\overline{E}$, $\overline{W}$, $\overline{G}$) function differently in comparison to most synchronous SRAMs. This device will not deselect with $\overline{E}$ high. The RAM remains active at all times. If $\overline{E}$ is registered high, the output pins (Q0 – Q8) will be driven if $\overline{G}$ is registered low. The transparent write feature allows the output data to track the input data. $\overline{E}$, $\overline{G}$, and $\overline{W}$ must be asserted to perform a transparent write (write and pass–through). The input data is available at the ouputs on the next rising edge of clock (K).

The pass–through function is always enabled. $\overline{E}$ high disables the write to the array while allowing a pass through cycle to occur on the next rising edge of clock (K). Only a registered $\overline{G}$ high will three–state the outputs.

The MCM67Q909 is available in 86 bump surface mount PBGA (plastic ball grid array) package.

- Single 5 V ± 5% Power Supply
- Fast Cycle Times: 12/15 ns Max
- Single Clock Operation
- TTL Input and Output Levels (Outputs LVTTL Compatible)
- Address, Data Input, $\overline{E}$, $\overline{W}$, and $\overline{G}$ Registers on Chip
- 83 MHz Maximum Clock Cycle Time
- Self Timed Write
- Separate Data Input and Output Pins
- Transparent–Write and Pass–Through
- High Output Drive Capability: 50 pF/Output at Rated Access Time
- Boundary Scan Implementation
- PBGA Package for High Speed Operation

PIN NAMES

A0 – A18	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
D0 – D8	Data Inputs
Q0 – Q8	Data Outputs
K	Clock Input
SCK	Scan Clock Input
SE	Scan Enable
SDI	Scan Data Input
SDO	Scan Data Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

PIN ASSIGNMENT

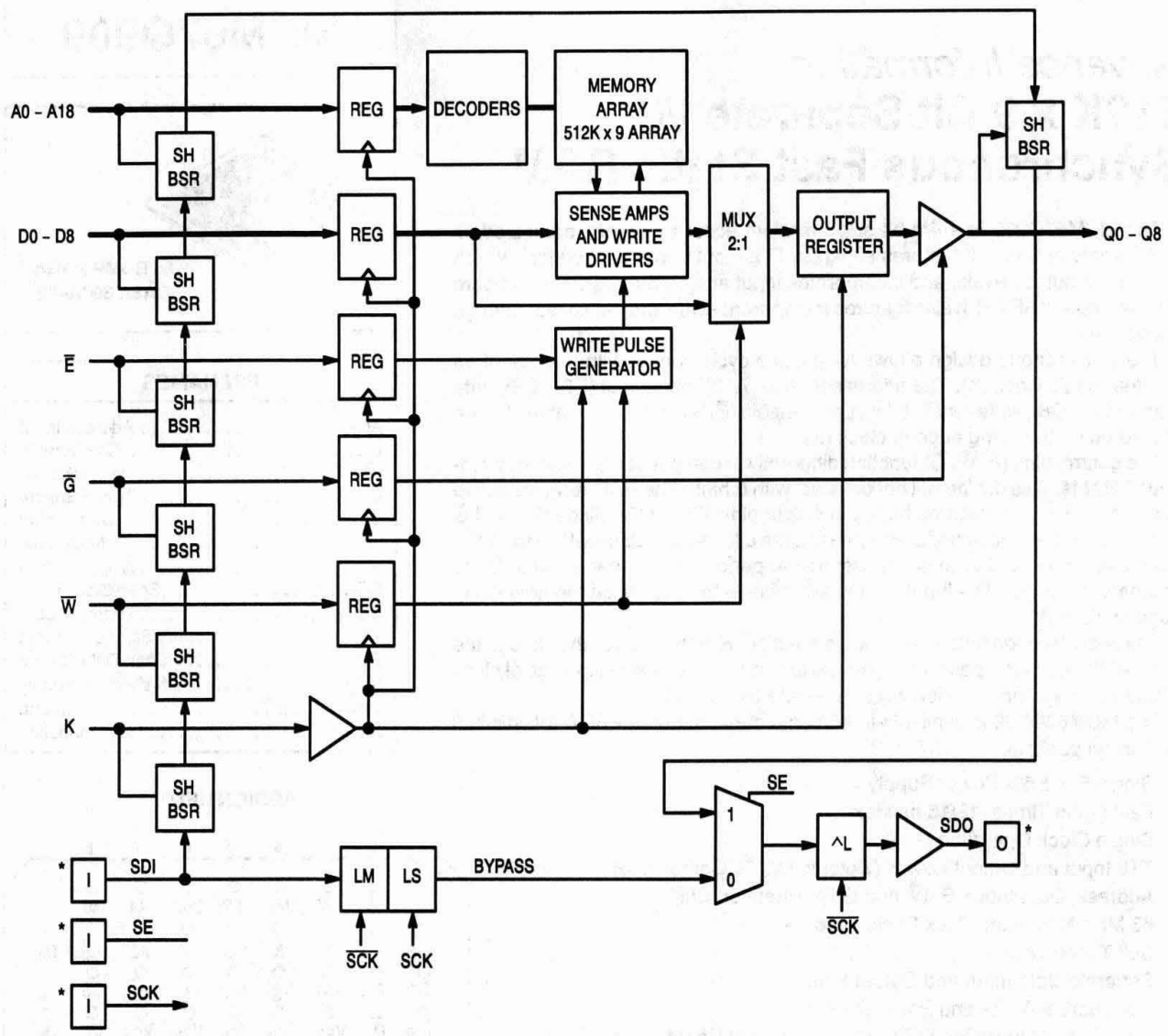
	1	2	3	4	5	6	7	8	9
A		$\overline{E}$	$\overline{W}$	V_{CC}	SDI	SDO	A4	A0	
B	A16	A14	$\overline{G}$	K	V_{SS}	A6	A2	V_{SS}	D8
C	D7	A15	A17	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q8	V_{SS}
D	V_{SS}	Q7	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q6	D6
E	D5	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{CC}
F	V_{CC}	Q5	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D4	Q4
G	D3	Q3	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D2	Q2
H	V_{SS}	D1	A18	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D0	V_{SS}
J	Q1	A12	A10	V_{SS}	A9	A8	A5	A1	Q0
K		A13	A11	SCK	V_{CC}	SE	A7	A3	

TOP VIEW 86 BUMP Not to Scale

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 1
11/6/96

BLOCK DIAGRAM



NOTES:

1. Bypass mode is entered with SE low and SCK cycled.
2. SH BSR = shadow bypass scan register.
3. 41 bumps used in boundary scan. V_{SS}, V_{CC}, NC, SDI, SDO, SE, and SCK not used in scan path.
4. SDO output sequence: A6, A4, A2, A0, D8, Q8, D6, Q6, D4, Q4, D2, Q2, D0, Q0, A18, A1, A3, A5, A7, A8, A9, A10, A11, A12, A13, Q1, D1, Q3, D3, Q5, D5, Q7, D7, A15, A16, A14, A17, $\overline{E}$, $\overline{G}$, $\overline{W}$, K.

* Four added test pins.

TRUTH TABLE

$\overline{E}$ (t_n)	$\overline{W}$ (t_n)	$\overline{G}$ ($t_n + 1$)	Mode	D0 – D8 (t_n)	Q0 – Q8 ($t_n + 1$)	V_{CC} Current
L	L	L	Write and Pass–Through	Valid	D0 – D8 (t_n)	I_{CC}
		H	Write	Valid	High–Z	I_{CC}
H	L	L	Pass–Through	Valid	D0 – D8 (t_n)	I_{CC}
		H	Pass–Through	Don't Care	High–Z	I_{CC}
X	H	L	Read	Don't Care	Q_{out} (t_n)	I_{CC}
		H	Read	Don't Care	High–Z	I_{CC}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	1.7	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This is a synchronous device. All synchronous inputs must meet specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) while the device is selected.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

5

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)		V_{CC}	4.75	5.25	V
Input High Voltage		V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage		V_{IL}	– 0.5*	0.8	V
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	MCM67Q909–12 ns MCM67Q909–15 ns	I_{CCA}	— —	TBD TBD	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	3.3	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address and Data Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance	C_{in}	6	pF
Output Capacitance	C_{out}	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

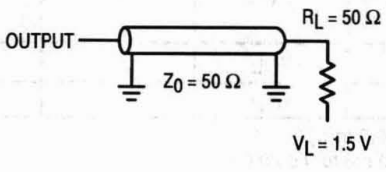
(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns
Output Timing Reference Level ..... 1.5 V
Output Load ..... Figure 1a Unless Otherwise Noted

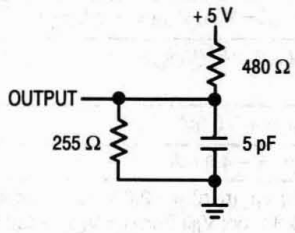
READ/WRITE CYCLE TIMING (See Notes 1, 2, 3 and 4)

Parameter	Symbol	MCM67Q909–12		MCM67Q909–15		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{KHKH}	12	—	15	—	ns	1
Clock Access Time	t_{KHQV}	—	5	—	6	ns	2
Clock Low Pulse Width	t_{KLKH}	4	—	4	—	ns	
Clock High Pulse Width	t_{KHKL}	4	—	4	—	ns	
Clock High to Data Output Invalid	t_{KHQX}	2	—	2	—	ns	
Clock High to Data Output High–Z	t_{KHQZ}	—	5	—	6	ns	3
Setup Times: A	t_{AVKH}	3	—	3	—	ns	4
$\overline{W}$	t_{WVKH}						
$\overline{E}$	t_{EVKH}						
$\overline{G}$	t_{GVKH}						
D0 – D8	t_{DVKH}						
Hold Times: A	t_{KHAX}	2	—	2	—	ns	4
$\overline{W}$	t_{KHWX}						
$\overline{E}$	t_{KHEX}						
$\overline{G}$	t_{KHGX}						
D0 – D8	t_{KHDX}						

NOTES:
1. All read and write cycles are referenced from K.
2. Valid data from clock high will be the data stored at the address or the last valid read cycle.
3. Measured at ± 200 mV from steady state. Tested per High–Z Test Load (See Figure 1b).
4. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) while the device is selected.



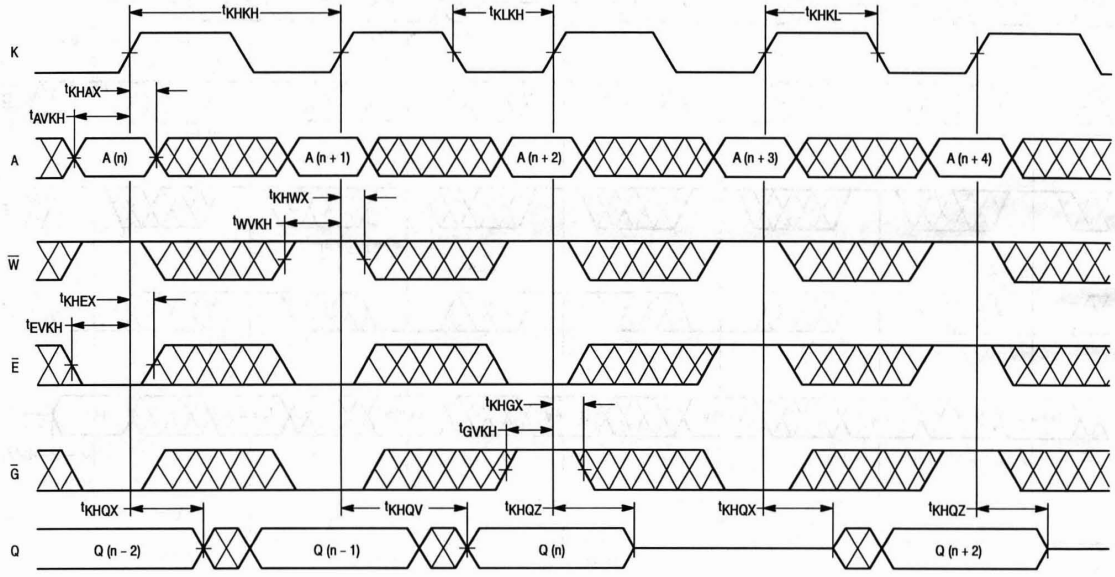
(a)



(b)

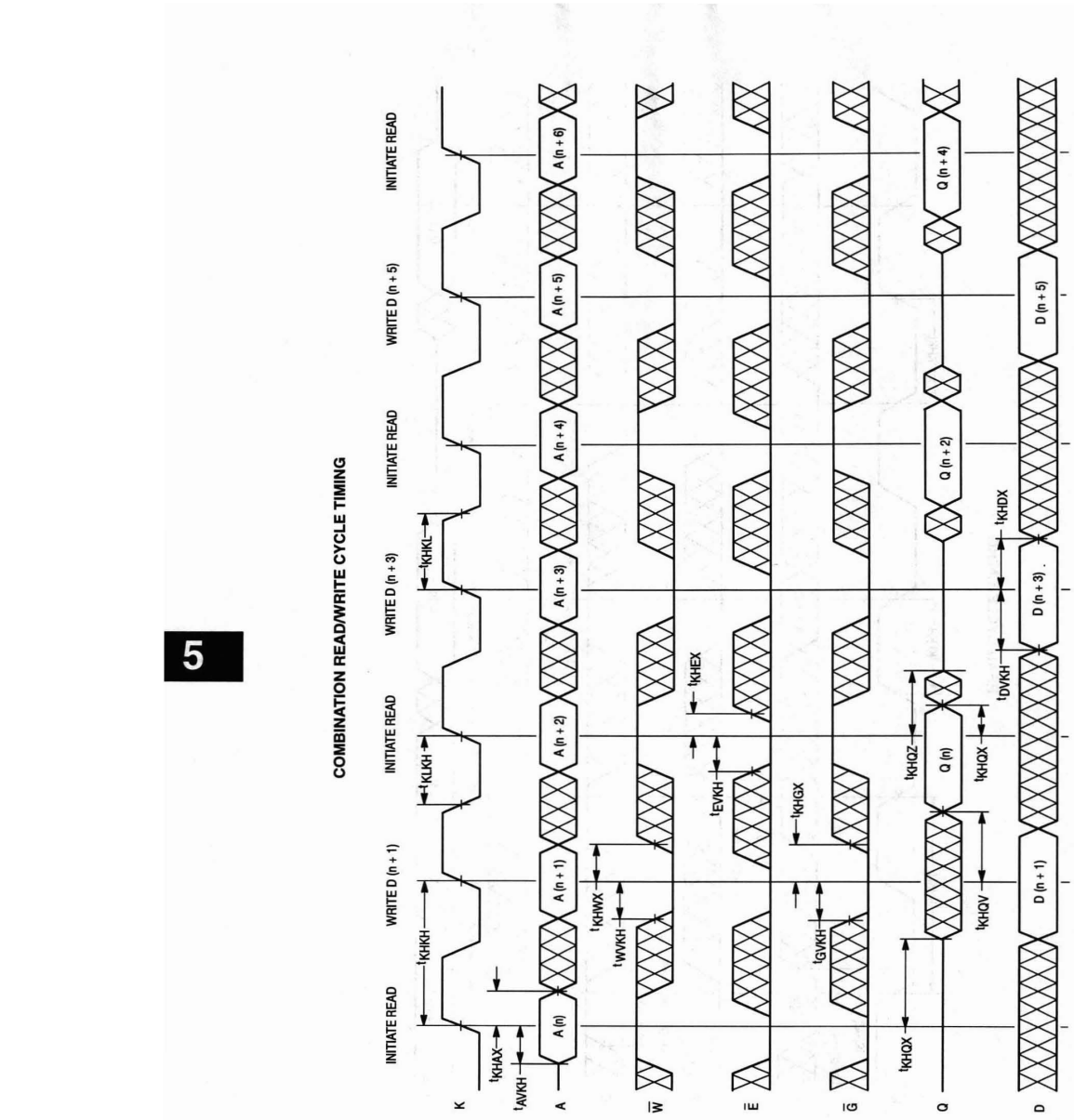
Figure 1. Test Loads

READ CYCLE TIMING

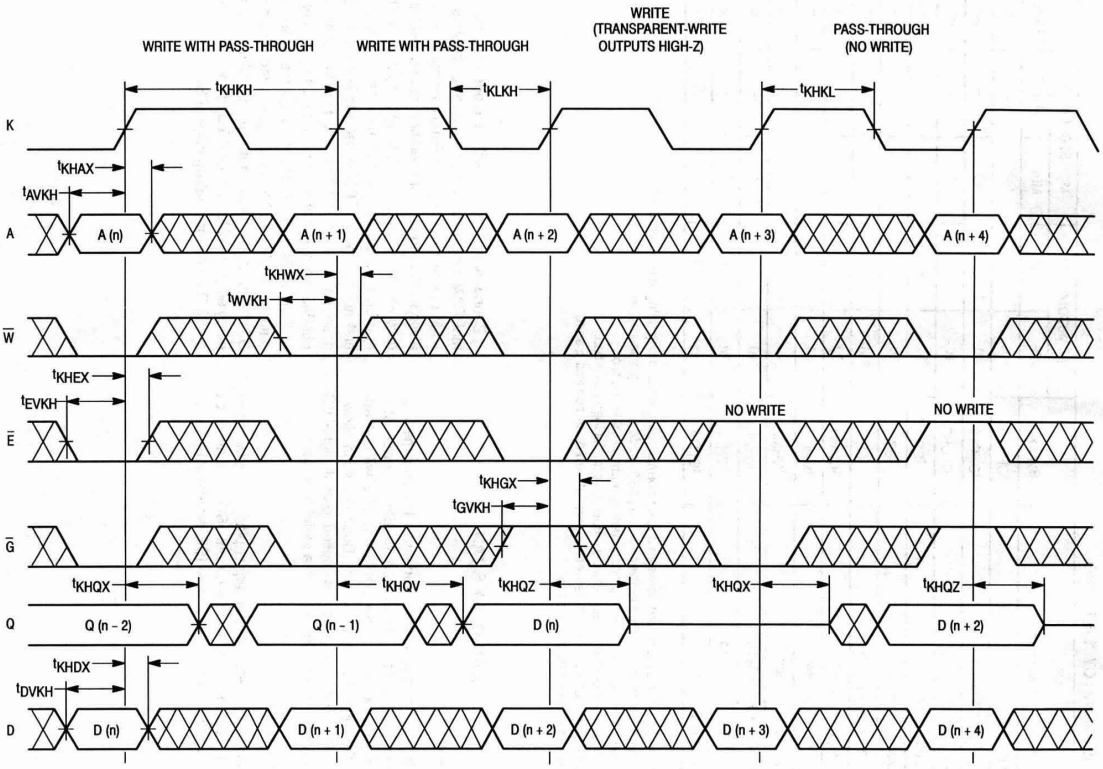


5

COMBINATION READ/WRITE CYCLE TIMING



TRANSPARENT-WRITE AND PASS-THROUGH CYCLE TIMING



BOUNDARY SCAN CYCLE TIMING

Parameter	Symbol	MCM67Q909–12		MCM67Q909–15		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{CHCH2}	100	—	100	—	ns	
Clock High Pulse Width	t_{CHCL2}	40	—	40	—	ns	
Clock Low Pulse Width	t_{CLCH2}	40	—	40	—	ns	
Scan Mode Setup Time	t_{SS}	10	—	10	—	ns	1
Bypass Mode Setup Time	t_{BS}	10	—	10	—	ns	2
Scan Mode Recovery Time	t_{SR}	100	—	100	—	ns	3
SCK Low to SE Hold High	t_{CLMH}	10	—	10	—	ns	4
SE High to SCK High Setup	t_{MHCH}	10	—	10	—	ns	5
SCK High to SE Low Hold Time	t_{CHML}	10	—	10	—	ns	6
SDI Valid to SCK High Setup	t_{IVCH}	10	—	10	—	ns	
SCK High to SDI Don't Care	t_{CHIX}	10	—	10	—	ns	
SCK Low to SDO Valid	t_{CLOV}	—	20	—	20	ns	

NOTES:
1. The minimum delay required between ending normal operation and beginning scan operations.
2. The minimum delay required between ending shift mode and beginning bypass mode.
3. The minimum delay required before restarting normal RAM operation.
4. The minimum delay required before executing a parallel load operation.
5. The minimum delay required between a parallel load operation and a shift.
6. Minimum shift command hold time.

5

BOUNDARY SCAN

OVERVIEW

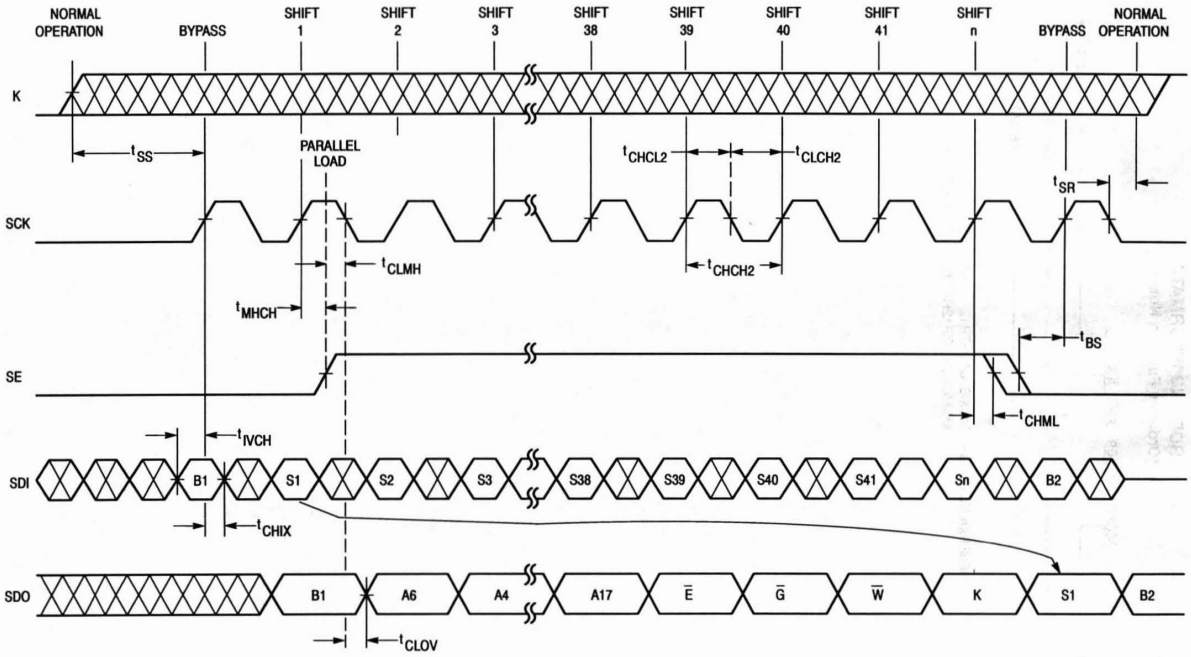
Boundary scan is a simple, non–intrusive scheme that allows verification of electrical continuity for each of a clocked RAMs logically active inputs and I/Os without adversely affecting RAM performance. Boundary scan allows the user to monitor the logic levels applied to each signal I/O on the RAM, and to shift them out in a serial bit stream.

OPERATION

Boundary scan requires four signal pins for implementation: scan data in (SDI), scan data out (SDO), scan clock (SCK, active high), and scan enable (SE, active high).

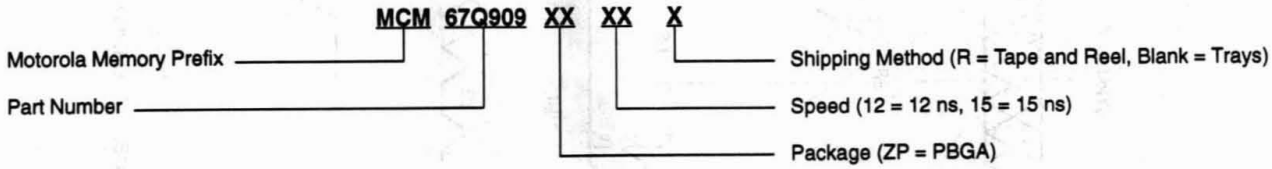
Boundary scan provides three modes of operation: (1) normal RAM operation, (2) scan, and (3) bypass. For normal RAM operation, SCK and SE must be held low. The RAM will always return to normal operation immediately after the RAM receives a rising edge of the RAM input clock (K) with SCK and SE held low. To enter scan mode, SCK is activated. The first rising edge of SCK is used to latch in the data on the scan registers. SE is then driven high to disable additional input data from entering the scan registers. Every falling edge of SCK serially shifts data through the scan registers and onto the SDO pin. To enter bypass mode, simply exercise SCK with SE held low. In this mode, SDI is sampled on the rising edge of SCK. The level found on SDI is then driven out on SDO on the next falling edge of SCK.

BOUNDARY SCAN TIMING DIAGRAM



B1 and B2 = bypass serial data from outside source.
S1 – Sn + 1 = serial scan data from outside source.
S1 – Sn = RAMs input register contents.
Scan order is: A6, A4, A2, A0, D8, Q8, D6, Q6, D4, Q4, D2, Q2, D0, Q0, A18, A1, A3, A5, A7, A8, A9, A10, A11, A12, A13, Q1, D1, Q3, D3, Q5, D5, Q7, D7, A15, A16, A14, A17, $\overline{E}$, $\overline{G}$, $\overline{W}$, K.

ORDERING INFORMATION
(Order by Full Part Number)


MCM 67Q909 XX XX X
Motorola Memory Prefix
Part Number
Shipping Method (R = Tape and Reel, Blank = Trays)
Speed (12 = 12 ns, 15 = 15 ns)
Package (ZP = PBGA)

Full Part Numbers — MCM67Q909ZP12 MCM67Q909ZP15
MCM67Q909ZP12R MCM67Q909ZP15R

5

MCM67Q709

128K x 9 Bit Separate I/O Synchronous Fast Static RAM

86 BUMP PBGA
CASE 896A–02

The Motorola MCM67Q709 is a 1,179,648 bit static random access memory, organized as 131,072 words of 9 bits. It features separate TTL input and output buffers, which are fully I/O compatible at 3.3 V, and incorporates input and output registers on board with high speed SRAM. It also features transparent–write and data pass–through capabilities.

The synchronous design allows for precise cycle control with the use of an external single clock (K). The Addresses (A0 – A16), Data Input (D0 – D8), Data Output (Q0 – Q8), Write–Enable ($\overline{W}$), Chip–Enable ($\overline{E}$), and Output–Enable ($\overline{G}$), are registered in on the rising edge of Clock (K).

The control pins ($\overline{E}$, $\overline{W}$, $\overline{G}$) function differently in comparison to most synchronous SRAMs. This device will not deselect with $\overline{E}$ high. The RAM remains active at all times. If $\overline{E}$ is registered high, the output pins (Q0–Q8) will be driven if $\overline{G}$ is registered low. The Transparent–Write feature allows the output data to track the input data. $\overline{E}$, $\overline{G}$, and $\overline{W}$ must be asserted to perform a Transparent Write (Write and Pass–Through). The input data is available at the ouputs on the next rising edge of clock (K).

The Pass–Through function is always enabled. $\overline{E}$ high disables the write to the array while allowing a pass through cycle to occur on the next rising edge of clock (K). Only a registered $\overline{G}$ high will three–state the outputs.

The MCM67Q709 is available in 86 bump surface mount PBGA (Plastic Ball Grid Array) package.

- Single 5 V ± 5% Power Supply
- Fast Cycle Times: 10/12 ns Max
- Single Clock Operation
- TTL Input and Output Levels (3.3 V I/O Compatible)
- Address, Data Input, $\overline{E}$, $\overline{W}$, $\overline{G}$, Registers on Chip
- 100 MHz Maximum Clock Cycle Time
- Self Timed Write
- Separate Data Input and Output Pins
- Transparent–Write and Pass–Through
- High Output Drive Capability: 50 pF/Output at Rated Access Time
- Boundary Scan Implementation
- PBGA package for high speed operation

PIN NAMES

A0 – A16	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
D0 – D8	Data Inputs
Q0 – Q8	Data Outputs
K	Clock Input
SCK	Scan Clock Input
SE	Scan Enable
SDI	Scan Data Input
SDO	Scan Data Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

PIN ASSIGNMENT

	1	2	3	4	5	6	7	8	9
A		$\overline{E}$	$\overline{W}$	V_{CC}	SDI	SDO	A4	A0	
B	A16	A14	$\overline{G}$	K	V_{SS}	A6	A2	V_{SS}	D8
C	D7	A15	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q8	V_{SS}
D	V_{SS}	Q7	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q6	D6
E	D5	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{CC}
F	V_{CC}	Q5	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D4	Q4
G	D3	Q3	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D2	Q2
H	V_{SS}	D1	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D0	V_{SS}
J	Q1	A12	A10	V_{SS}	A9	A8	A5	A1	Q0
K		A13	A11	SCK	V_{CC}	SE	A7	A3	

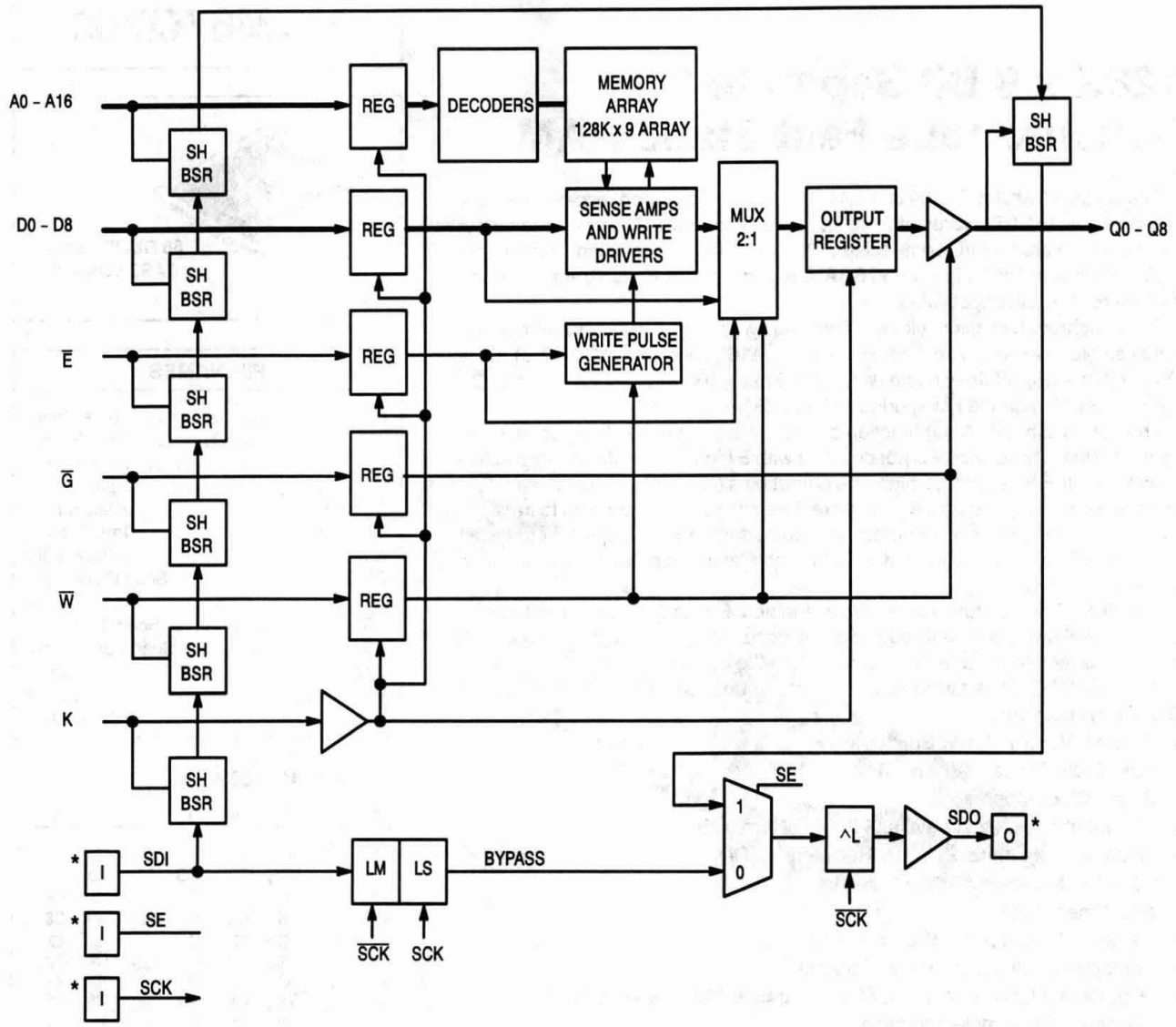
TOP VIEW 86 BUMP Not to Scale

NOT RECOMMENDED FOR NEW DESIGNS SUBSTITUTE MCM67Q709A

5

REV 3
11/4/96

BLOCK DIAGRAM



NOTES:

1. Bypass mode is entered with SE low and SCK cycled.
2. SH BSR = Shadow Bypass Scan Register.
3. 39 bumps used in Boundary Scan. V_{SS}, V_{CC}, NC, SDI, SDO, SE, and SCK not used in Scan Path.
4. SDO Output Sequence A6, A4, A2, A0, D8, Q8, D6, Q6, D4, Q4, D2, Q2, D0, Q0, A1, A3, A5, A7, A8, A9, A10, A11, A12, A13, Q1, D1, Q3, D3, Q5, D5, Q7, D7, A15, A16, A14, $\overline{E}$, $\overline{G}$, $\overline{W}$, K.

*Four added test pins.

TRUTH TABLE

$\overline{E}$ (t_n)	$\overline{W}$ (t_n)	$\overline{G}$ ($t_n + 1$)	Mode	D0 – D8 (t_n)	Q0 – Q8 ($t_n + 1$)	V_{CC} Current
L	L	L	Write and Pass Thru	Valid	D0 – D8 (t_n)	I_{CC}
		H	Write	Valid	High–Z	I_{CC}
H	L	L	Pass Thru	Valid	D0 – D8 (t_n)	I_{CC}
		H	NOP	Don't Care	High–Z	I_{CC}
X	H	L	Read	Don't Care	Q_{out} (t_n)	I_{CC}
		H	Read	Don't Care	High–Z	I_{CC}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	1.5	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This is a synchronous device. All synchronous inputs must meet specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) while the device is selected.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

5

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)		V_{CC}	4.75	5.25	V
Input High Voltage		V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage		V_{IL}	– 0.5*	0.8	V
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	MCM67Q709–10 ns MCM67Q709–12 ns	I_{CCA}	— —	230 220	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	3.3	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address and Data Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance	C_{in}	6	pF
Output Capacitance	C_{out}	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

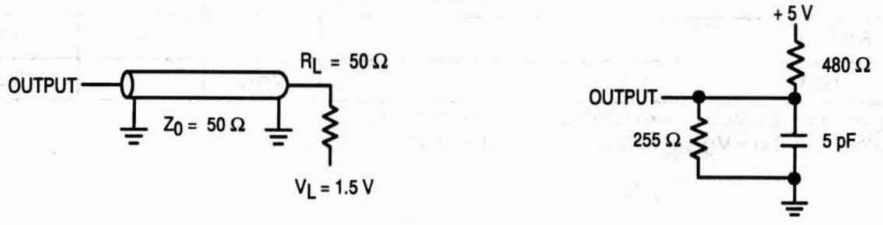
Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... Figure 1a Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM67Q709–10		MCM67Q709–12		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{KHKH}	10	—	12	—	ns	1
Clock Access Time	t_{KHQV}	—	5	—	6	ns	2
Clock Low Pulse Width	t_{KLKH}	4	—	4	—	ns	
Clock High Pulse Width	t_{KHKL}	4	—	4	—	ns	
Clock High to Data Output Invalid	t_{KHQX}	2	—	2	—	ns	
Clock High to Data Output High–Z	t_{KHQZ}	—	5	—	6	ns	
Setup Times: A	t_{AVKH}	2	—	2	—	ns	3
$\overline{W}$	t_{WVKH}						
$\overline{E}$	t_{EVKH}						
$\overline{G}$	t_{GVKH}						
D0 – D8	t_{DVKH}						
Hold Times: A	t_{KHAX}	1	—	1	—	ns	3
$\overline{W}$	t_{KHWX}						
$\overline{E}$	t_{KHEX}						
$\overline{G}$	t_{KHGX}						
D0 – D8	t_{KHDX}						

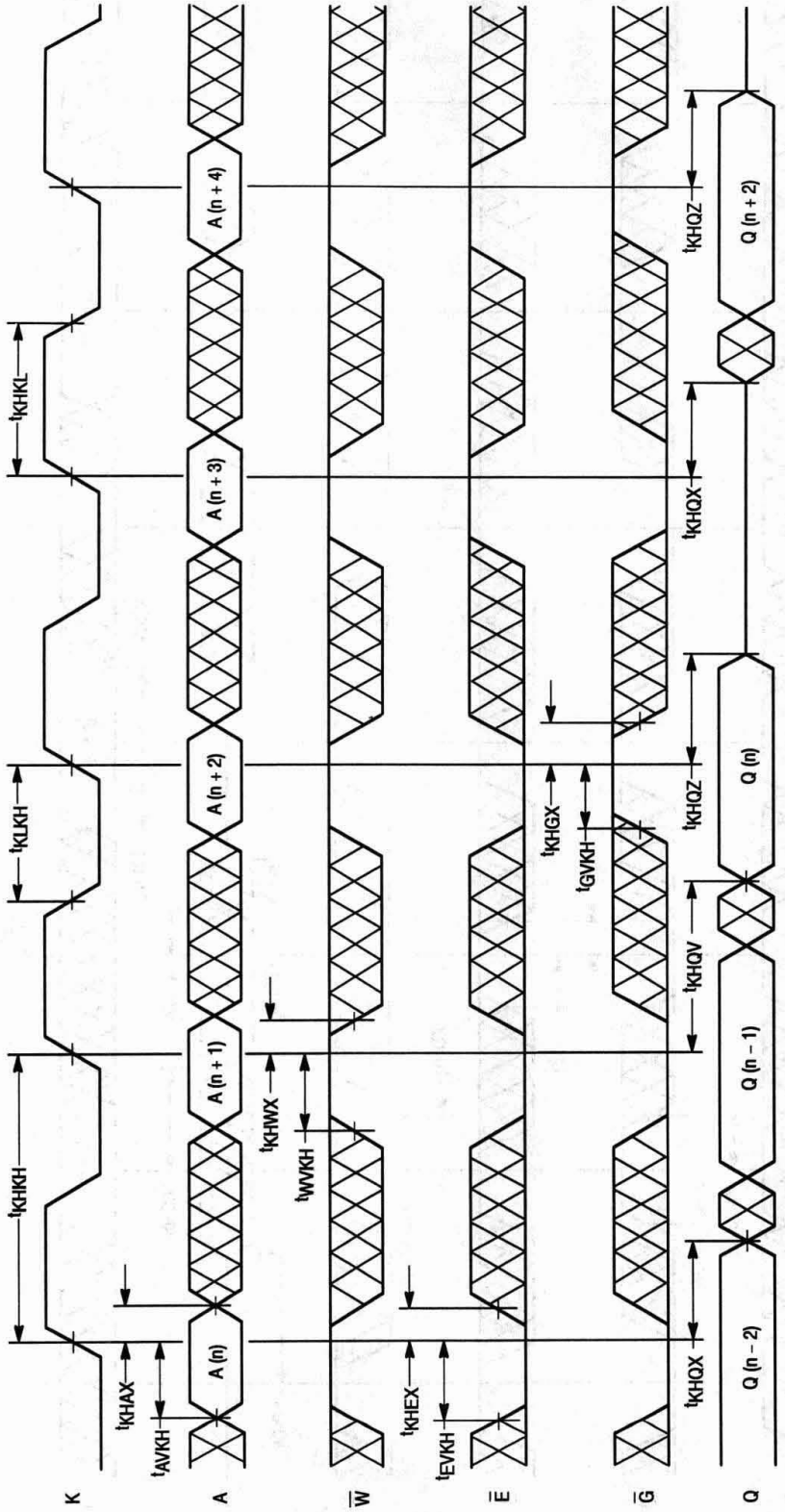
NOTES:
1. All read and write cycles are referenced from K.
2. Valid data from Clock High will be the data stored at the address or the last valid read cycle.
3. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) while the device is selected.



(a) (b)

Figure 1. Test Loads

READ CYCLE TIMING



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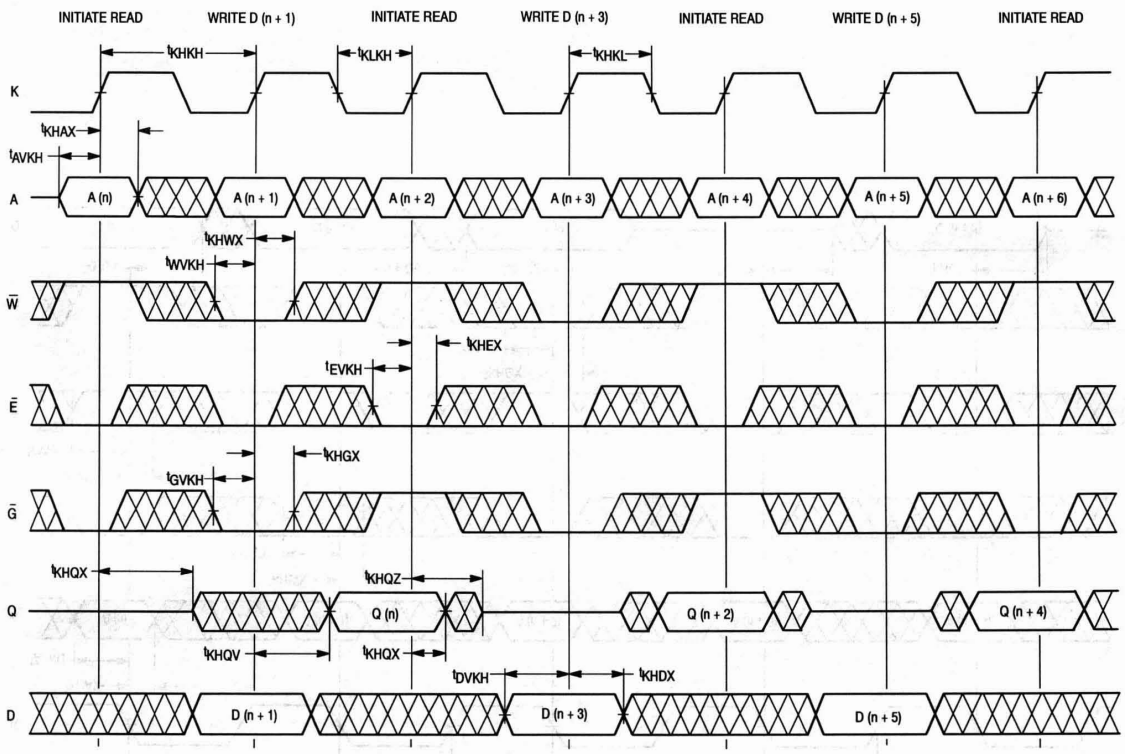
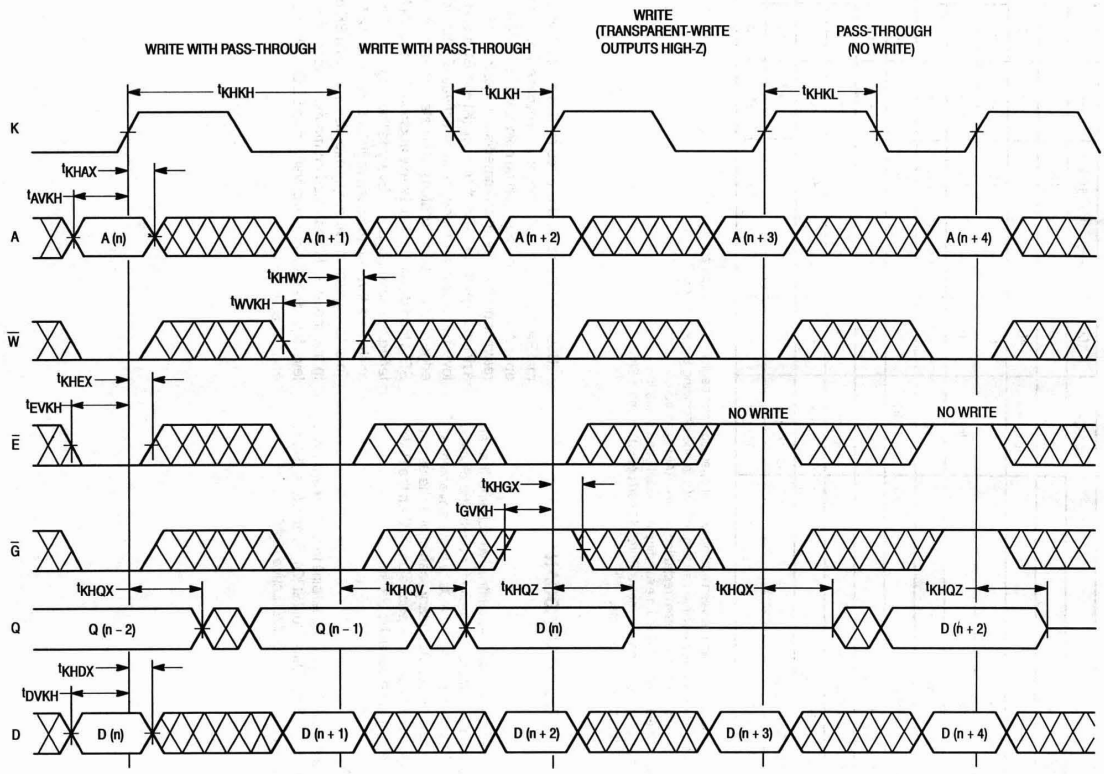
COMBINATION READ/WRITE CYCLE TIMING



TRANSPARENT-WRITE AND PASS-THROUGH CYCLE TIMING



BOUNDARY SCAN CYCLE TIMING

Parameter	Symbol	MCM67Q709–10		MCM67Q709–12		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{CHCH2}	100	—	100	—	ns	
Clock High Pulse Width	t_{CHCL2}	40	—	40	—	ns	
Clock Low Pulse Width	t_{CLCH2}	40	—	40	—	ns	
Scan Mode Setup Time	t_{SS}	10	—	10	—	ns	1
Bypass Mode Setup Time	t_{BS}	10	—	10	—	ns	2
Scan Mode Recovery Time	t_{SR}	100	—	100	—	ns	3
SCK Low to SE Hold High	t_{CLMH}	10	—	10	—	ns	4
SE High to SCK High Setup	t_{MHCH}	10	—	10	—	ns	5
SCK High to SE Low Hold Time	t_{CHML}	10	—	10	—	ns	6
SDI Valid to SCK High Setup	t_{IVCH}	10	—	10	—	ns	
SCK High to SDI Don't Care	t_{CHIX}	10	—	10	—	ns	
SCK Low to SDO Valid	t_{CLOV}	—	20	—	20	ns	

NOTES:
1. The minimum delay required between ending normal operation and beginning scan operations.
2. The minimum delay required between ending Shift Mode and beginning Bypass Mode.
3. The minimum delay required before restarting normal RAM operation.
4. The minimum delay required before executing a Parallel Load operation.
5. The minimum delay required between a Parallel Load operation and a Shift.
6. Minimum Shift command hold time.

5

BOUNDARY SCAN

OVERVIEW

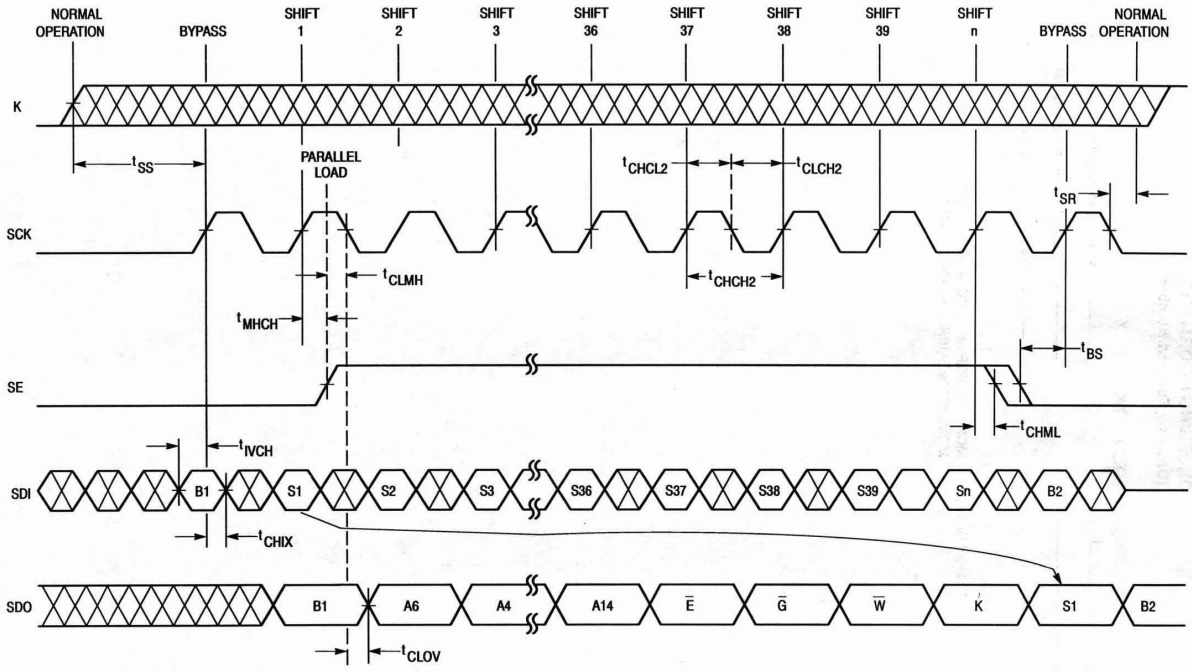
Boundary scan is a simple, non–intrusive scheme that allows verification of electrical continuity for each of a clocked RAM's logically active inputs and I/Os without adversely affecting RAM performance. Boundary scan allows the user to monitor the logic levels applied to each signal I/O on the RAM, and to shift them out in a serial bit stream.

OPERATION

Boundary scan requires four signal pins for implementation: Scan Data In (SDI), Scan Data Out (SDO), Scan Clock (SCK, active high), and Scan Enable (SE, active high).

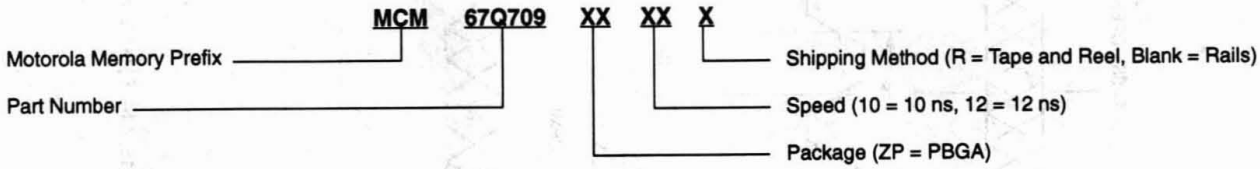
Boundary scan provides three modes of operation: (1) normal RAM operation, (2) scan, and (3) bypass. For normal RAM operation SCK and SE must be held low. The RAM will always return to normal operation immediately after the RAM receives a rising edge of the RAM input clock (K) with SCK and SE held low. To enter scan mode, SCK is activated. The first rising edge of SCK is used to latch in the data on the scan registers. SE is then driven high to disable additional input data from entering the scan registers. Every falling edge of SCK serially shifts data through the scan registers and onto the SDO pin. To enter bypass mode simply exercise SCK with SE held low. In this mode SDI is sampled on the rising edge of SCK. The level found on SDI is then driven out on SDO on the next falling edge of SCK.

BOUNDARY SCAN TIMING DIAGRAM



B1 and B2 = Bypass Serial Data from outside source
S1 – Sn + 1 = Serial Scan Data from outside source
S1 – Sn = RAMs Input Register contents
Scan Order is "A6, A4, A2, A0, D8, Q8, D6, Q6, D4, Q4, D2, Q2, D0, Q0, A1, A3, A5, A7, A8, A9, A10, A11, A12, A13, Q1, D1, Q3, D3, Q5, D5, Q7, D7, A15, A16, A14, $\overline{E}$, $\overline{G}$, $\overline{W}$, $\overline{K}$"

ORDERING INFORMATION
(Order by Full Part Number)

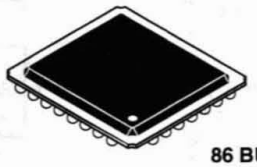

MCM 67Q709 XX XX X
Motorola Memory Prefix
Part Number
Shipping Method (R = Tape and Reel, Blank = Rails)
Speed (10 = 10 ns, 12 = 12 ns)
Package (ZP = PBGA)

Full Part Numbers — MCM67Q709ZP10 MCM67Q709ZP12
MCM67Q709ZP10R MCM67Q709ZP12R

5

MCM67Q709A

128K x 9 Bit Separate I/O Synchronous Fast Static RAM



86 BUMP PBGA
CASE 896A–02

The Motorola MCM67Q709A is a 1,179,648 bit static random access memory, organized as 131,072 words of 9 bits. It features separate TTL input and output buffers, which drive 3.3 V output levels and incorporates input and output registers on board with high speed SRAM. It also features transparent–write and data pass–through capabilities.

The synchronous design allows for precise cycle control with the use of an external single clock (K). The addresses (A0 – A16), data input (D0 – D8), data output (Q0 – Q8), write enable ($\overline{W}$), chip enable ($\overline{E}$), and output enable ($\overline{G}$), are registered in on the rising edge of clock (K).

The control pins ($\overline{E}$, $\overline{W}$, $\overline{G}$) function differently in comparison to most synchronous SRAMs. This device will not deselect with $\overline{E}$ high. The RAM remains active at all times. If $\overline{E}$ is registered high, the output pins (Q0 – Q8) will be driven if $\overline{G}$ is registered low. The transparent write feature allows the output data to track the input data. $\overline{E}$, $\overline{G}$, and $\overline{W}$ must be asserted to perform a transparent write (write and pass–through). The input data is available at the ouputs on the next rising edge of clock (K).

The pass–through function is always enabled. $\overline{E}$ high disables the write to the array while allowing a pass through cycle to occur on the next rising edge of clock (K). Only a registered $\overline{G}$ high will three–state the outputs.

The MCM67Q709A is available in an 86 bump surface mount PBGA (Plastic Ball Grid Array) package.

- Single 5 V ± 5% Power Supply
- Fast Cycle Times: 10/12 ns Max
- Single Clock Operation
- TTL Input and Output Levels (Outputs LVTTL Compatible)
- Address, Data Input, $\overline{E}$, $\overline{W}$, $\overline{G}$ Registers on Chip
- 100 MHz Maximum Clock Cycle Time
- Self Timed Write
- Separate Data Input and Output Pins
- Transparent–Write and Pass–Through
- High Output Drive Capability: 50 pF/Output at Rated Access Time
- Boundary Scan Implementation
- PBGA Package for High Speed Operation

PIN NAMES

A0 – A16	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
D0 – D8	Data Inputs
Q0 – Q8	Data Outputs
K	Clock Input
SCK	Scan Clock Input
SE	Scan Enable
SDI	Scan Data Input
SDO	Scan Data Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

PIN ASSIGNMENT

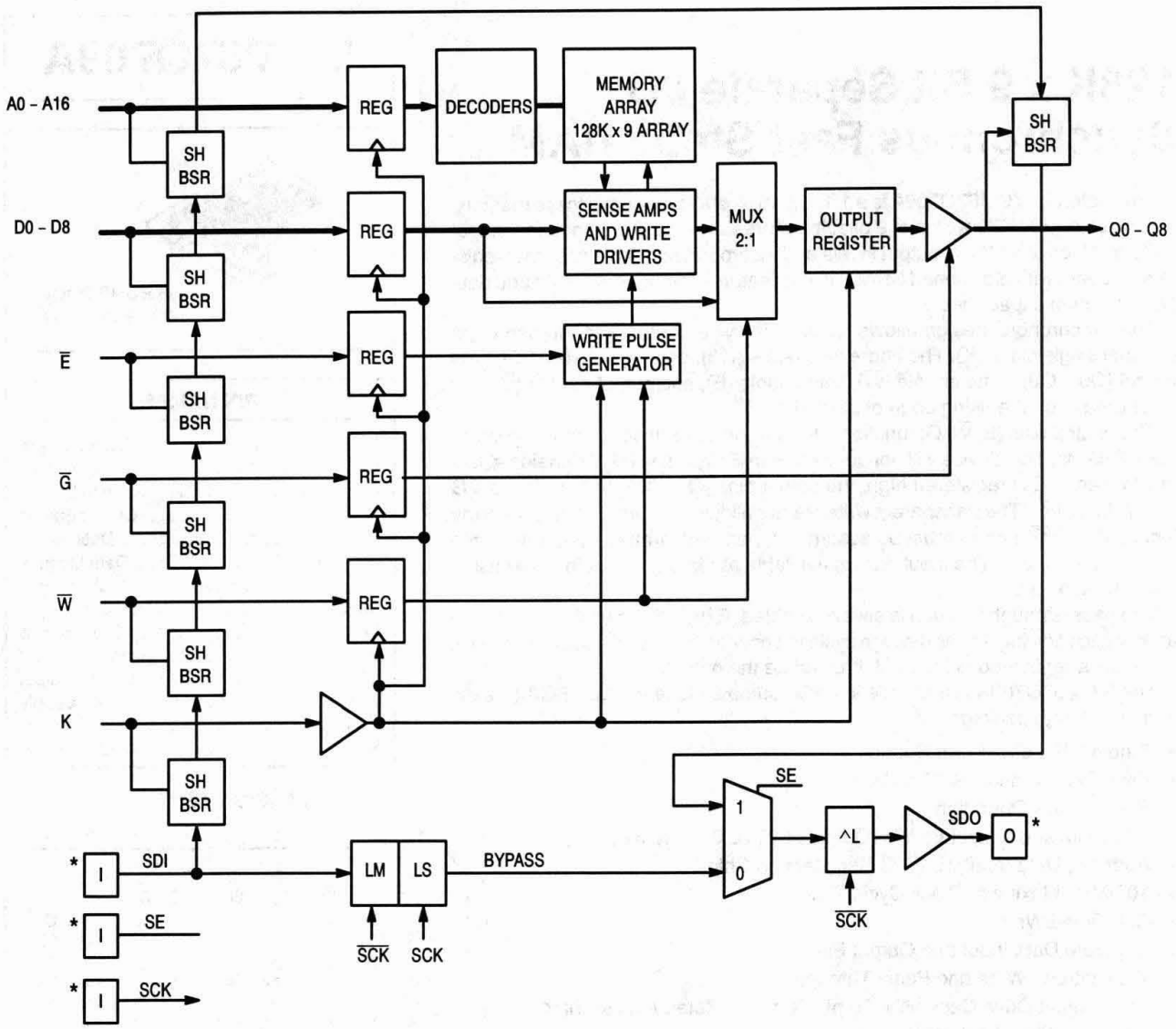
	1	2	3	4	5	6	7	8	9
A		$\overline{E}$	$\overline{W}$	V_{CC}	SDI	SDO	A4	A0	
B	A16	A14	$\overline{G}$	K	V_{SS}	A6	A2	V_{SS}	D8
C	D7	A15	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q8	V_{SS}
D	V_{SS}	Q7	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q6	D6
E	D5	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{CC}
F	V_{CC}	Q5	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D4	Q4
G	D3	Q3	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D2	Q2
H	V_{SS}	D1	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D0	V_{SS}
J	Q1	A12	A10	V_{SS}	A9	A8	A5	A1	Q0
K		A13	A11	SCK	V_{CC}	SE	A7	A3	

TOP VIEW 86 BUMP Not to Scale

5

REV 1
11/6/96

BLOCK DIAGRAM



NOTES:

1. Bypass mode is entered with SE low and SCK cycled.
2. SH BSR = Shadow Bypass Scan Register.
3. 39 bumps used in Boundary Scan. V_{SS}, V_{CC}, NC, SDI, SDO, SE, and SCK not used in Scan Path.
4. SDO Output Sequence A6, A4, A2, A0, D8, Q8, D6, Q6, D4, Q4, D2, Q2, D0, Q0, A1, A3, A5, A7, A8, A9, A10, A11, A12, A13, Q1, D1, Q3, D3, Q5, D5, Q7, D7, A15, A16, A14, $\overline{E}$, $\overline{G}$, $\overline{W}$, K.

* Four added test pins.

TRUTH TABLE

$\overline{E}$ (t_n)	$\overline{W}$ (t_n)	$\overline{G}$ ($t_n + 1$)	Mode	D0 – D8 (t_n)	Q0 – Q8 ($t_n + 1$)	V_{CC} Current
L	L	L	Write and Pass Through	Valid	D0 – D8 (t_n)	I_{CC}
		H	Write	Valid	High–Z	I_{CC}
H	L	L	Pass Through	Valid	D0 – D8 (t_n)	I_{CC}
		H	Pass Through	Don't Care	High–Z	I_{CC}
X	H	L	Read	Don't Care	Q_{out} (t_n)	I_{CC}
		H	Read	Don't Care	High–Z	I_{CC}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	1.5	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This is a synchronous device. All synchronous inputs must meet specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) while the device is selected.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)		V_{CC}	4.75	5.25	V
Input High Voltage		V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage		V_{IL}	– 0.5*	0.8	V
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	MCM67Q709A–10 ns MCM67Q709A–12 ns	I_{CCA}	— —	230 220	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	3.3	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address and Data Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance	C_{in}	6	pF
Output Capacitance	C_{out}	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

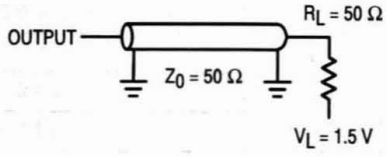
Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... Figure 1a Unless Otherwise Noted

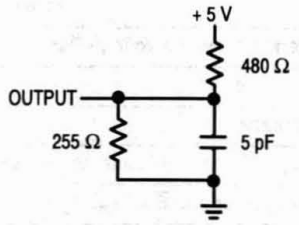
READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM67Q709A–10		MCM67Q709A–12		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{KHKH}	10	—	12	—	ns	1
Clock Access Time	t_{KHQV}	—	5	—	6	ns	2
Clock Low Pulse Width	t_{KLKH}	4	—	4	—	ns	
Clock High Pulse Width	t_{KHKL}	4	—	4	—	ns	
Clock High to Data Output Invalid	t_{KHQX}	2	—	2	—	ns	
Clock High to Data Output High–Z	t_{KHQZ}	—	5	—	6	ns	3
Setup Times: A	t_{AVKH}	2	—	2	—	ns	4
$\overline{W}$	t_{WVKH}						
$\overline{E}$	t_{EVKH}						
$\overline{G}$	t_{GVKH}						
D0 – D8	t_{DVKH}						
Hold Times: A	t_{KHAX}	1	—	1	—	ns	4
$\overline{W}$	t_{KHWX}						
$\overline{E}$	t_{KHEX}						
$\overline{G}$	t_{KHGX}						
D0 – D8	t_{KHDX}						

NOTES:
1. All read and write cycles are referenced from K.
2. Valid data from Clock High will be the data stored at the address or the last valid read cycle.
3. Measured at ± 200 mV from steady state. Tested per High–Z Test Load (See Figure 1b).
4. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) while the device is selected.



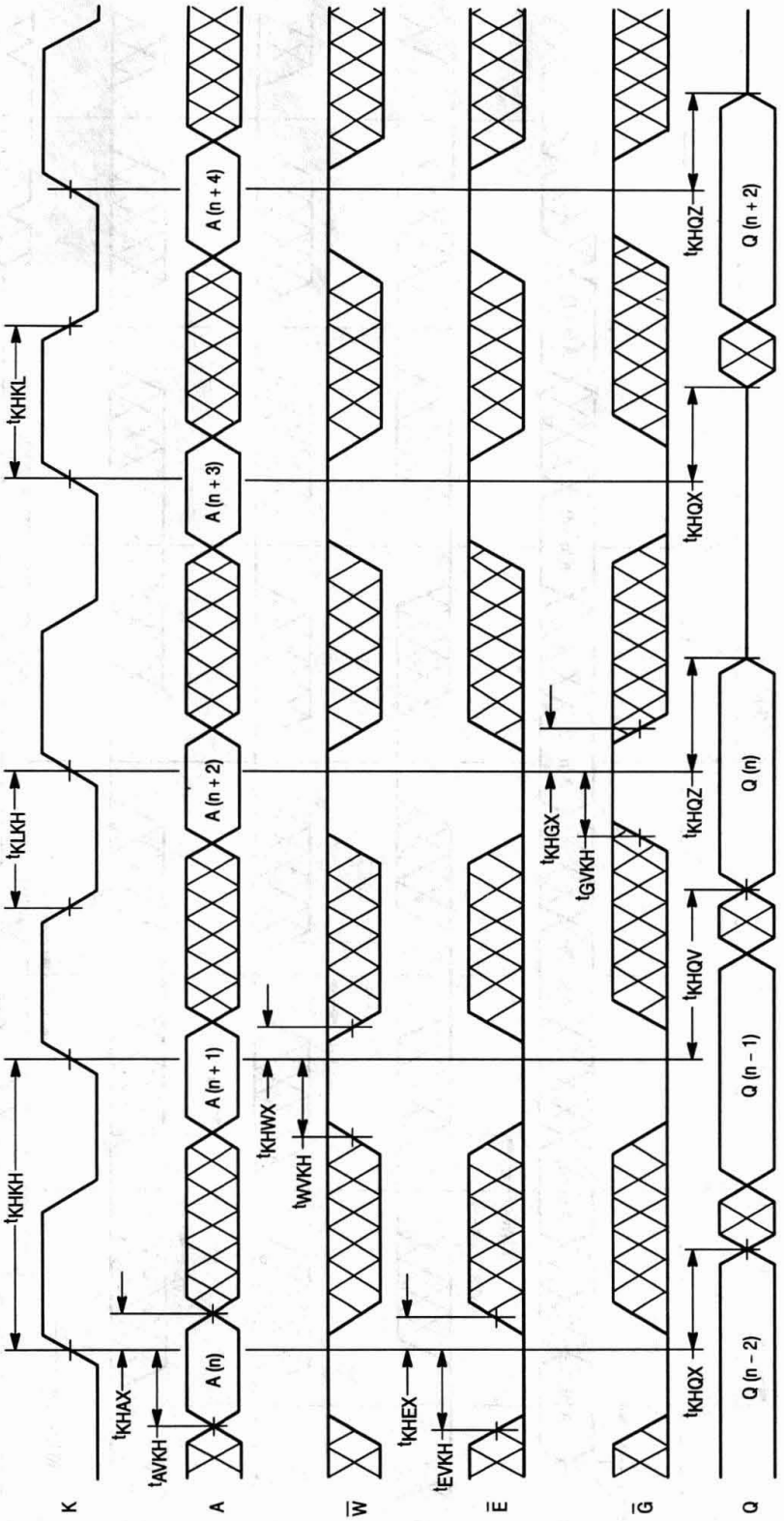
(a)



(b)

Figure 1. Test Loads

READ CYCLE TIMING



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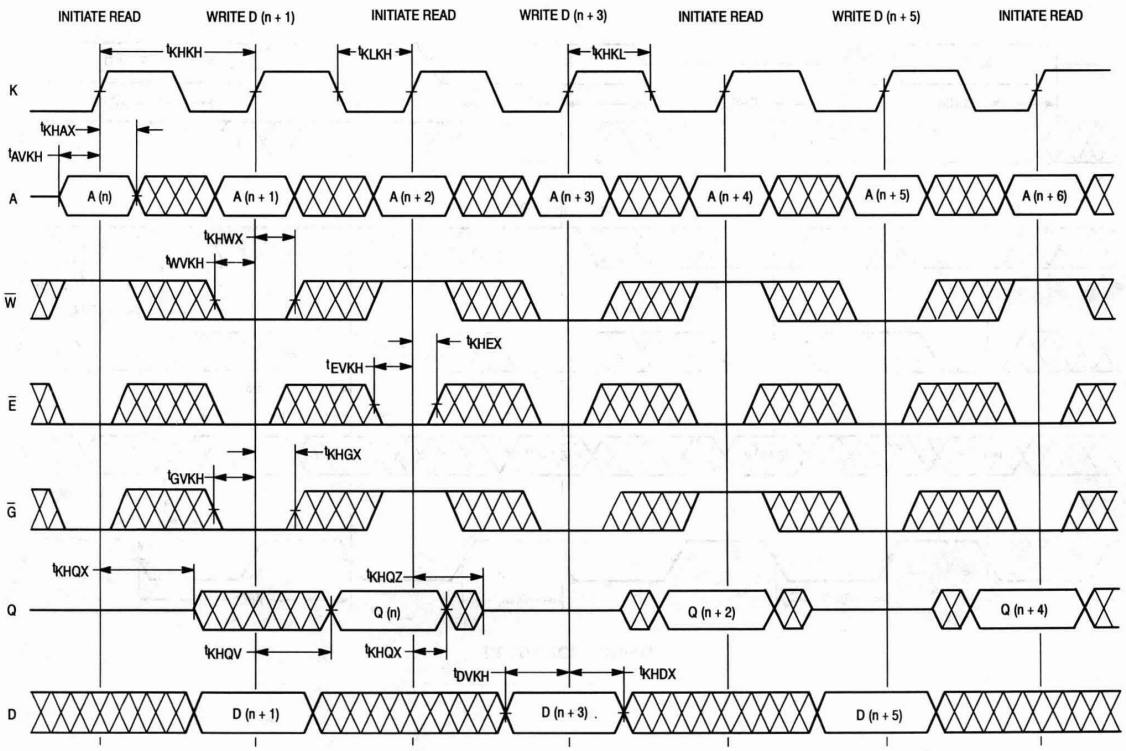
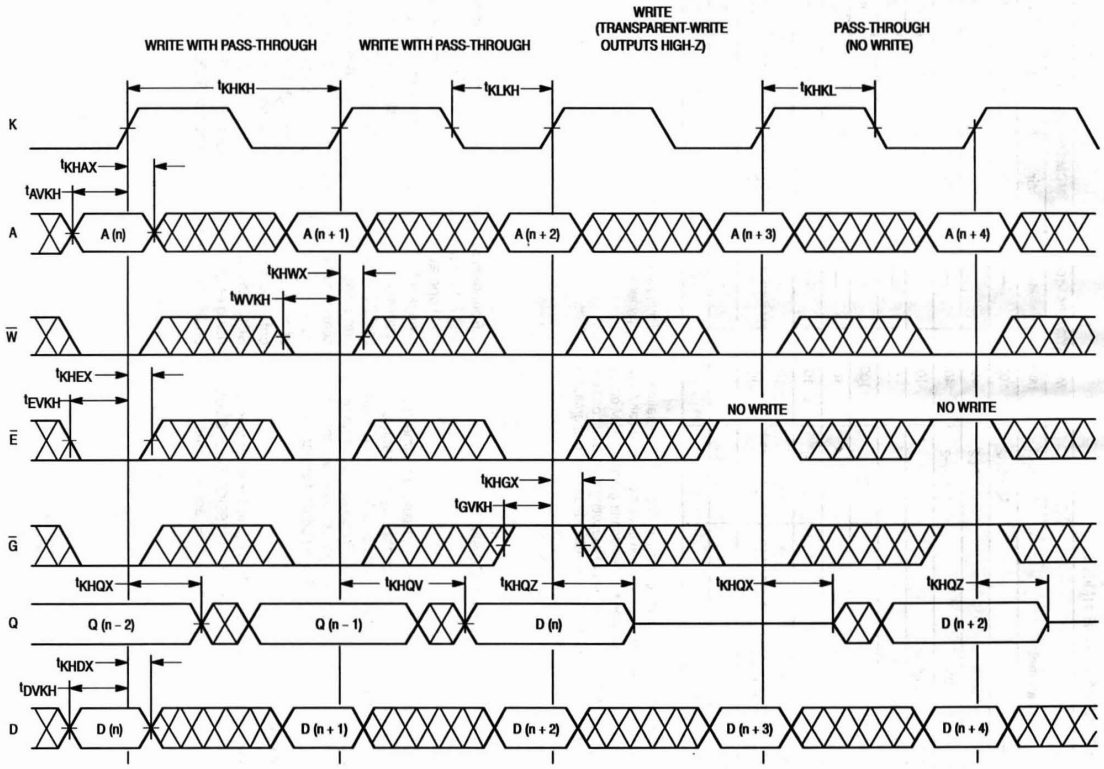
COMBINATION READ/WRITE CYCLE TIMING



TRANSPARENT-WRITE AND PASS-THROUGH CYCLE TIMING



BOUNDARY SCAN CYCLE TIMING

Parameter	Symbol	MCM67Q709A–10		MCM67Q709A–12		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{CHCH2}	100	—	100	—	ns	
Clock High Pulse Width	t_{CHCL2}	40	—	40	—	ns	
Clock Low Pulse Width	t_{CLCH2}	40	—	40	—	ns	
Scan Mode Setup Time	t_{SS}	10	—	10	—	ns	1
Bypass Mode Setup Time	t_{BS}	10	—	10	—	ns	2
Scan Mode Recovery Time	t_{SR}	100	—	100	—	ns	3
SCK Low to SE Hold High	t_{CLMH}	10	—	10	—	ns	4
SE High to SCK High Setup	t_{MHCH}	10	—	10	—	ns	5
SCK High to SE Low Hold Time	t_{CHML}	10	—	10	—	ns	6
SDI Valid to SCK High Setup	t_{IVCH}	10	—	10	—	ns	
SCK High to SDI Don't Care	t_{CHIX}	10	—	10	—	ns	
SCK Low to SDO Valid	t_{CLOV}	—	20	—	20	ns	

NOTES:
1. The minimum delay required between ending normal operation and beginning scan operations.
2. The minimum delay required between ending Shift Mode and beginning Bypass Mode.
3. The minimum delay required before restarting normal RAM operation.
4. The minimum delay required before executing a Parallel Load operation.
5. The minimum delay required between a Parallel Load operation and a Shift.
6. Minimum Shift command hold time.

5

BOUNDARY SCAN

OVERVIEW

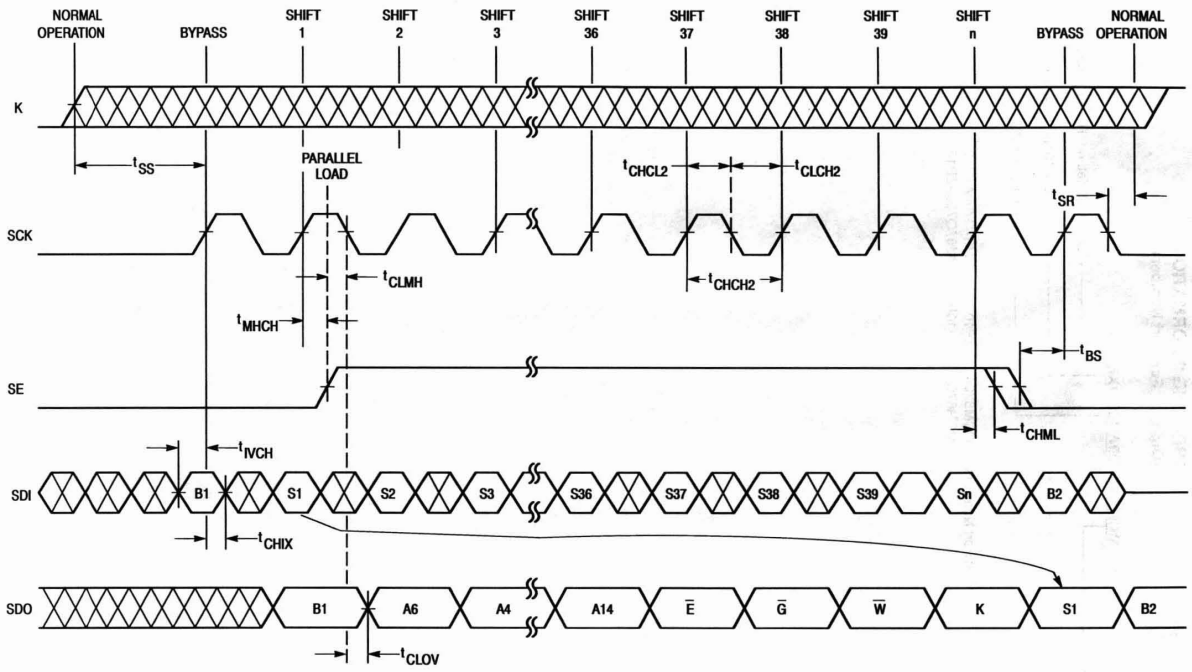
Boundary scan is a simple, non–intrusive scheme that allows verification of electrical continuity for each of a clocked RAM's logically active inputs and I/Os without adversely affecting RAM performance. Boundary scan allows the user to monitor the logic levels applied to each signal I/O on the RAM, and to shift them out in a serial bit stream.

OPERATION

Boundary scan requires four signal pins for implementation: Scan Data In (SDI), Scan Data Out (SDO), Scan Clock (SCK, active high), and Scan Enable (SE, active high).

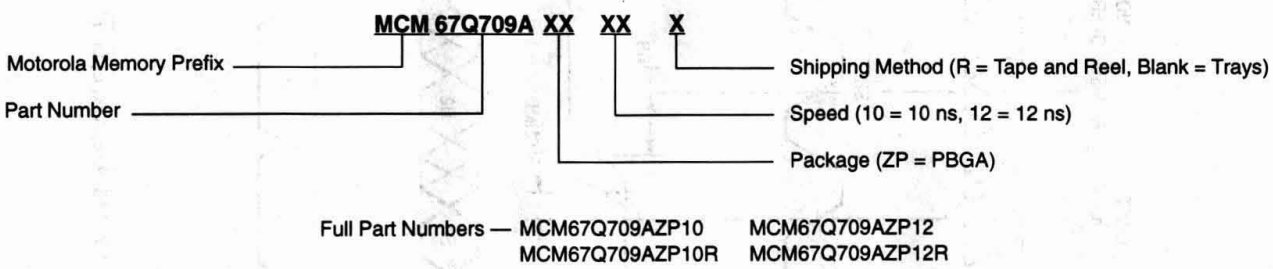
Boundary scan provides three modes of operation: (1) normal RAM operation, (2) scan, and (3) bypass. For normal RAM operation SCK and SE must be held low. The RAM will always return to normal operation immediately after the RAM receives a rising edge of the RAM input clock (K) with SCK and SE held low. To enter scan mode, SCK is activated. The first rising edge of SCK is used to latch in the data on the scan registers. SE is then driven high to disable additional input data from entering the scan registers. Every falling edge of SCK serially shifts data through the scan registers and onto the SDO pin. To enter bypass mode simply exercise SCK with SE held low. In this mode SDI is sampled on the rising edge of SCK. The level found on SDI is then driven out on SDO on the next falling edge of SCK.

BOUNDARY SCAN TIMING DIAGRAM



B1 and B2 = Bypass Serial Data from outside source
S1 – Sn + 1 = Serial Scan Data from outside source
S1 – Sn = RAMs Input Register contents
Scan Order is "A6, A4, A2, A0, D8, Q8, D6, Q6, D4, Q4, D2, Q2, D0, Q0, A1, A3, A5, A7, A8, A9, A10, A11, A12, A13, Q1, D1, Q3, D3, Q5, D5, Q7, D7, A15, A16, A14, Ē, Ḡ, W̄, K"

ORDERING INFORMATION
(Order by Full Part Number)


MCM 67Q709A XX XX X
Motorola Memory Prefix
Part Number
Shipping Method (R = Tape and Reel, Blank = Trays)
Speed (10 = 10 ns, 12 = 12 ns)
Package (ZP = PBGA)

Full Part Numbers — MCM67Q709AZP10 MCM67Q709AZP12
MCM67Q709AZP10R MCM67Q709AZP12R

5

MCM69Q536

Advance Information

32K x 36 Bit Synchronous Separate I/O SRAM

TQ PACKAGE
176 LEAD TQFP
CASE 1101–01

The Motorola MCM69Q536 is a 1 Megabit static random access memory, organized as 32K words of 36 bits. It features separate data input and data output buffers and incorporates input and output registers on board with high speed SRAM.

The MCM69Q536 allows the user to perform transparent writes and data pass through. Two data bus ports are provided — a data input (D) and a data output (Q) port.

The synchronous design allows for precise cycle control with the use of an external single clock (K). Address port, data input (D0 – D35), data output (Q0 – Q35), write enable ($\overline{W}$), chip enables ($\overline{E1}$, E2), and pass–through enable ($\overline{PT}$) are registered on the rising edge of clock (K).

Any given cycle operates on only one address. However, for any cycle, reads and writes can be intermixed. Thus, one can perform a read, a write, or a combination read/write during any one cycle. For a combination read/write, the contents of the array are read before the new data is written.

By using the pass–through function, the output port Q can be made to reflect either the contents of the array or the data presented to the input port D. For read/write or a read cycle with $\overline{G}$ low, the Q port will output the contents of the array. However, if $\overline{PT}$ is asserted, the Q port will instead output the data presented at the D input port.

- Single 3.3 V ± 5% Power Supply
- Fast Access Times: 6/8/10 ns Max
- Sustained Throughput of 2.98 Gigabits/Second
- Single Clock Operation
- Address, Data Input, $\overline{E1}$, E2, $\overline{PT}$, $\overline{W}$, and Data Output Registers on Chip
- 83 MHz Maximum Clock Cycle Time
- Self Timed Write
- Separate Data Input and Data Output Pins
- Pass–Through Feature
- Asynchronous Output Enable ($\overline{G}$)
- LVTTL Compatible I/O
- No Dead Cycles Required for Reads after Writes or for Writes after Reads
- 176 Pin TQFP Package
- Simultaneous Reads and Writes

Suggested Applications

— ATM — Ethernet Switches — Routers
— Cell/Frame Buffers — SNA Switches — Shared Memory

Product Family Configurations

Part Number	Dual Address	Single Address	Dual I/O	Separate I/O
MCM69D536	✓	Note 1	✓	Note 2
MCM69D618	✓	Note 1	✓	Note 2
MCM69Q536		✓		✓
MCM69Q618		✓		✓
MCM67Q709		✓		✓
MCM67Q909		✓		✓

NOTES:
1. Tie AX and AY address ports together for the part to function as a single address part.
2. Tie $\overline{GX}$ high for DQX to be inputs and tie $\overline{WY}$ high and $\overline{GY}$ low for DQY to be outputs.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 2
3/12/97

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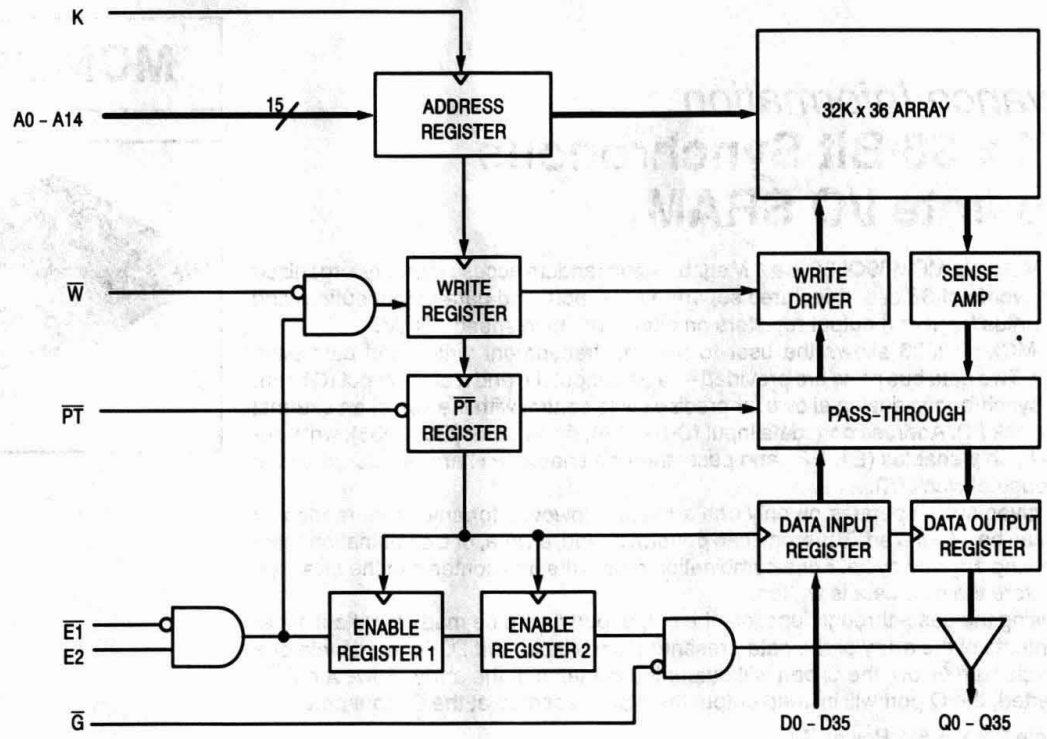
BLOCK DIAGRAM



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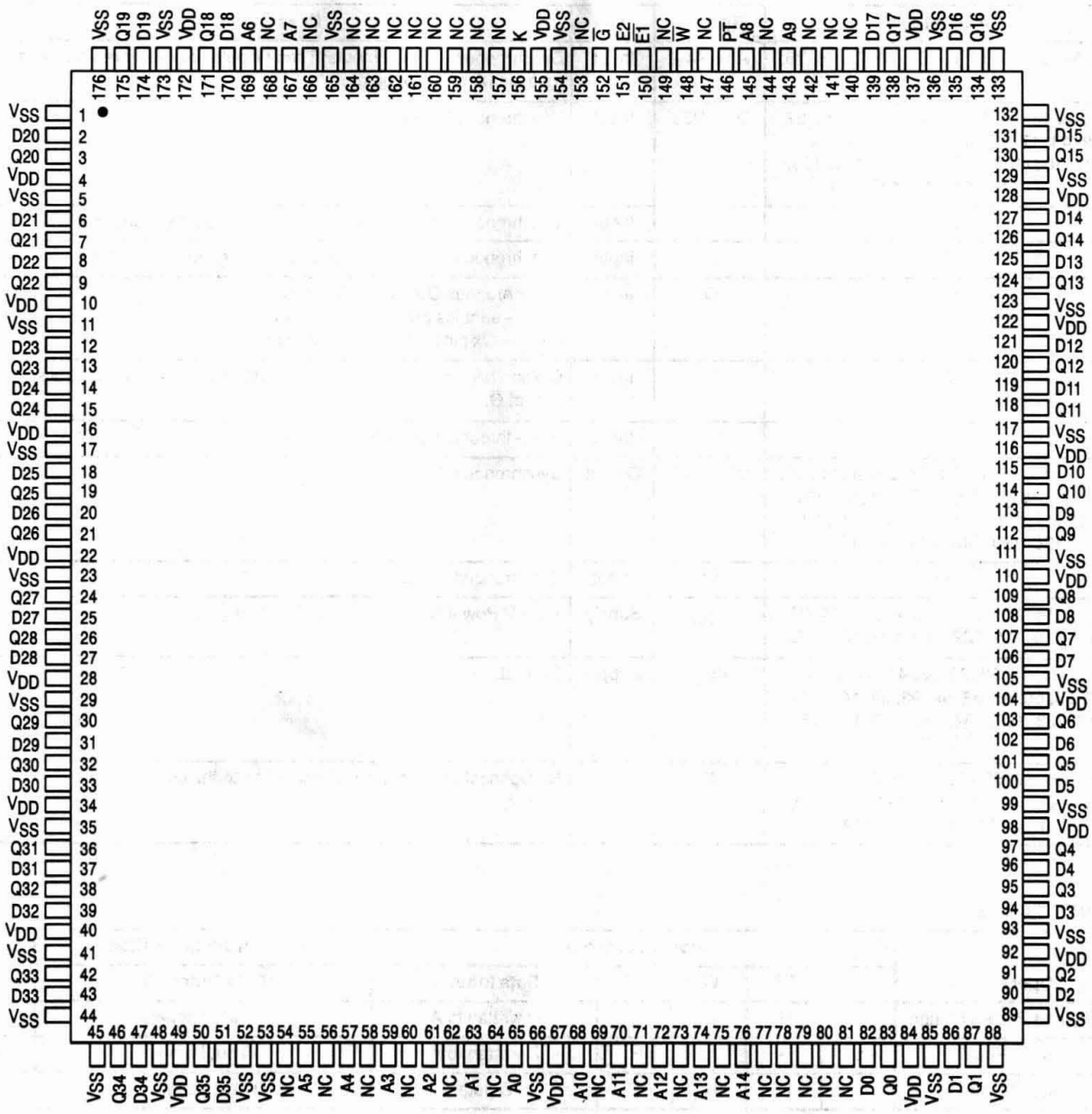
PIN ASSIGNMENT



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PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
55, 57, 59, 61, 63, 65, 68, 70, 72, 74, 76, 143, 145, 167, 169	A0 – A14	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
2, 6, 8, 12, 14, 18, 20, 25, 27, 31, 33, 37, 39, 43, 47, 51, 82, 86, 90, 94, 96, 100, 102, 106, 108, 113. 115, 119, 121, 125, 127, 131, 135, 139, 170, 174	D0 – D35	Input	Synchronous Data Input.
150	E1	Input	Synchronous Chip Enable: Active low for depth expansion.
151	E2	Input	Synchronous Chip Enable: Active high for depth expansion.
152	G	Input	Asynchronous Output Enable Input: Low — enables output buffers (Qx pins). High — Qx pins are high impedance.
156	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$.
146	$\overline{PT}$	Input	Pass–through enable: Synchronous.
3, 7, 9, 13, 15, 19, 21, 24, 26, 30, 32, 36, 38, 42, 46, 50, 83, 87, 91, 95, 97, 101, 103, 107, 109, 112, 114, 118, 120, 124, 126, 130, 143, 138, 171, 175	Q0 – Q35	Output	Synchronous Data Output.
148	$\overline{W}$	Input	Synchronous Write.
4, 10, 16, 22, 28, 34, 40, 49, 67, 84, 98, 104, 110, 116, 122, 128, 137, 155, 172	V_{DD}	Supply	+ 3.3 V Power Supply.
1, 5, 11, 17, 23, 29, 35, 41, 44, 45, 48, 52, 53, 66, 85, 88, 89, 93, 99, 105, 111, 117, 123. 129, 132, 133, 136, 154, 165, 173, 176	V_{SS}	Supply	Ground.
54, 56, 58, 60, 62, 64, 69, 71, 73, 75, 77 – 81, 140, 141, 142, 144, 147, 149, 153, 157 – 164, 166, 168	NC	—	No Connection: There is no connection to the chip.

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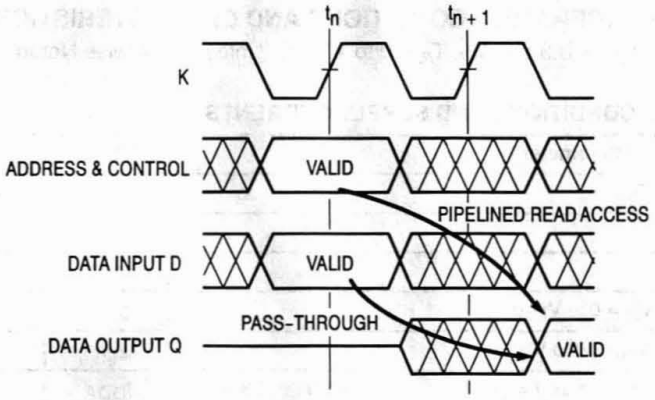
TRUTH TABLE

Operation	Input at t_n Clock					Result from t_{n+1} Clock	Notes
	E1	E2	W	PT	Data Input D	Data Output Q	
Write and Pass–Through	L	H	L	L	D written to A	D data appears	1
Write/Read	L	H	L	H	D written to A	Q out from A	2
Pass–Through	L	H	H	L	D data	D data appears	3
Read	L	H	H	H	Don't Care	Q out from A	4
Deselected	X	L	X	X	Don't Care	Q is high–Z	5
Deselected	H	X	X	X	Don't Care	Q is high–Z	6

NOTES:
1. Write D to array and output D at Q.
2. Output contents of array to Q then write D to array.
3. Output D at Q. Do not write.
4. Output contents of array to Q. Do not write.
5. No operation.
6. No operation.



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{DD}	V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	TBD	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This is a synchronous device. All synchronous inputs must meet specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) while the device is selected.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

5

PACKAGE THERMAL CHARACTERISTICS (See Note 1)

Rating		Symbol	TQFP	Unit	Notes
Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	40 35	°C/W	2
Junction to Board (Bottom)		$R_{\theta JB}$	23	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)		V_{DD}	3.135	3.465	V
Input High Voltage		V_{IH}	2.0	V_{DD} + 0.5**	V
Input Low Voltage		V_{IL}	– 0.5*	0.8	V
Input Leakage Current (All Inputs, V_{in} = 0 to V_{DD})		$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{DD})		$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current (I_{out} = 0 mA) (V_{DD} = max, f = f_{max})	MCM69Q536–6 ns MCM69Q536–8 ns MCM69Q536–10 ns	I_{DDA}	— — —	TBD TBD TBD	mA
CMOS Standby Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}, All Inputs Toggling at CMOS Levels V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{DD} – 0.2 V)	MCM69Q536–6 ns MCM69Q536–8 ns MCM69Q536–10 ns	I_{SB1}	— — —	TBD TBD TBD	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	V_{DD}	V

* V_{IL} ≥ –1.5 V for t ≤ t_{KHKH}/2.
** V_{IH} ≤ V_{DD} + 1.0 V for t ≤ t_{KHKH}/2.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 0 to + 70°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address and Data Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance	C_{in}	6	pF
Output Capacitance	C_{out}	8	pF

5

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... Figure 1 Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter		Symbol	MCM69Q536–6		MCM69Q536–8		MCM69Q536–10		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Cycle Time		t_{KHKH}	12	—	15	—	20	—	ns	1
Clock Access Time		t_{KHQV}	—	6	—	8	—	10	ns	2
Clock Low Pulse Width		t_{KLKH}	4	—	6	—	8	—	ns	
Clock High Pulse Width		t_{KHKL}	4	—	6	—	8	—	ns	
Clock High to Data Output Invalid		t_{KHQX}	0	—	0	—	0	—	ns	
Clock High to Data Output High–Z		t_{KHQZ}	—	5	—	6	—	7	ns	4
Output Enable to Output Valid		t_{GLQV}	—	6	—	8	—	10	ns	
Output Enable to Output Active		t_{GLQX}	0	—	0	—	0	—	ns	4
Output Disable to Output High–Z		t_{GHQZ}	—	5	—	6	—	7	ns	4
Setup Times:	A0 – A15	t_{AVKH}	2.5	—	3	—	3	—	ns	3
	$\overline{W}$	t_{WVKH}								
	$\overline{PT}$	t_{PTVKH}								
	$\overline{E1}$, E2	t_{EVKH}								
	D0 – D17	t_{DVKH}								
Hold Times:	A0 – A15	t_{KHAX}	0.5	—	2	—	2	—	ns	3
	$\overline{W}$	t_{KHWX}								
	$\overline{PT}$	t_{KHPTX}								
	$\overline{E1}$, E2	t_{KHEX}								
	D0 – D17	t_{KHDX}								

NOTES:
1. All read and write cycles are referenced from K.
2. Valid data from Clock High will be the data stored at the address or the last valid read cycle.
3. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) while the device is selected.
4. This parameter is sampled and not 100% tested.

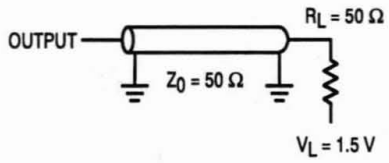


Figure 1. AC Test Load

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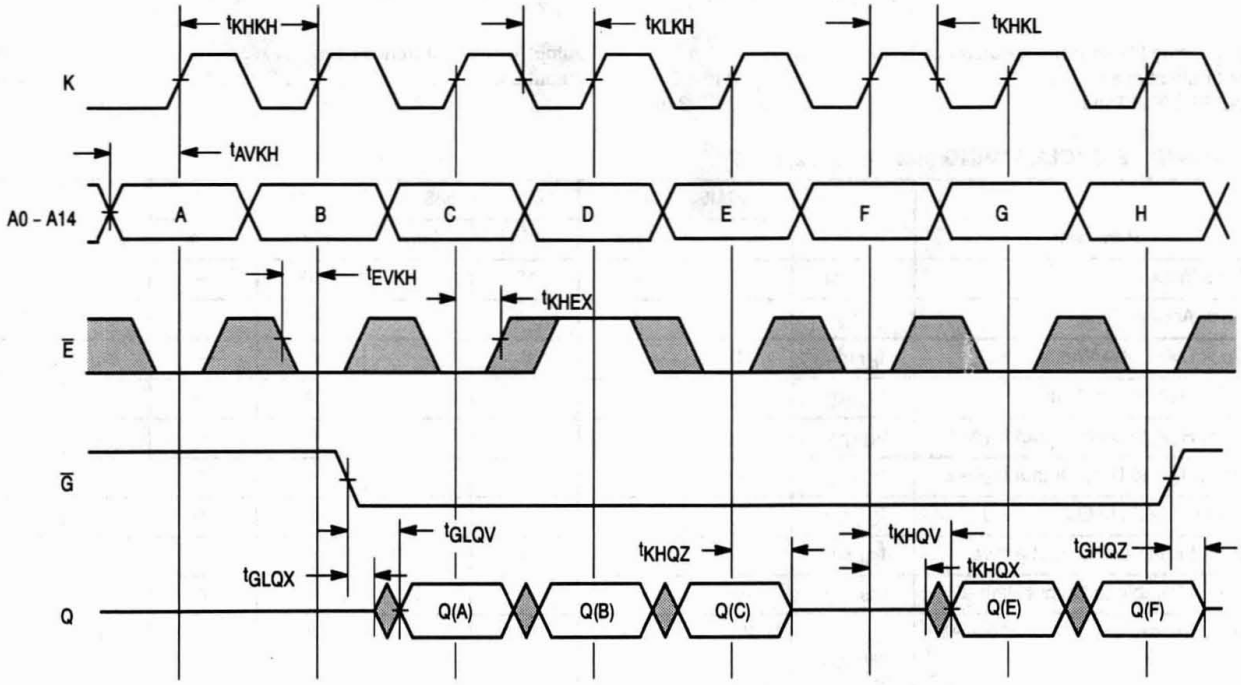
READ CYCLE TIMING



$\overline{E}$ low = $\overline{E1}$ low, E2 high. $\overline{E}$ high = $\overline{E1}$ high or E2 low.

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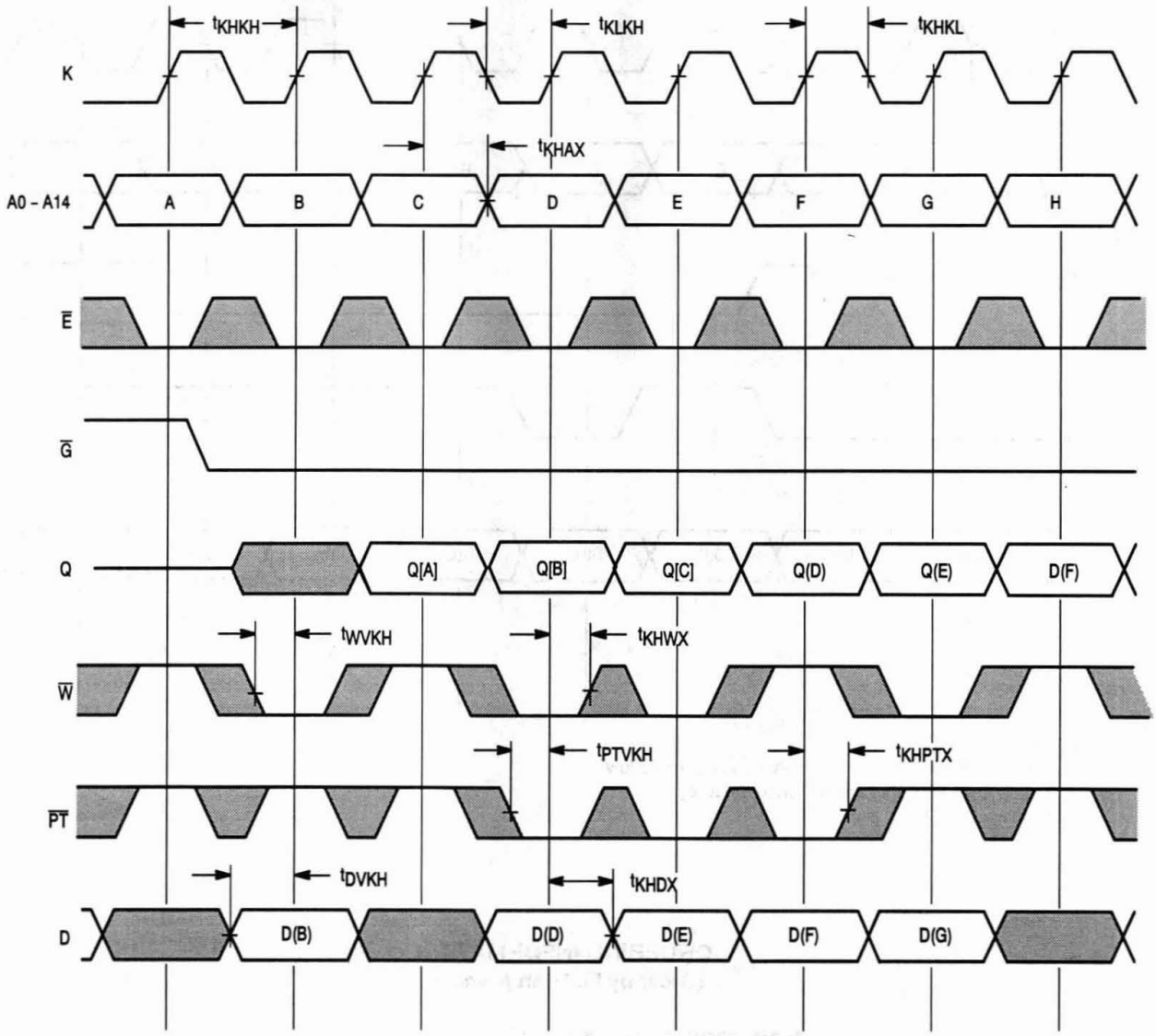
COMBINATION READ/WRITE CYCLE TIMING



NOTES:
1. $\overline{E}$ low = $\overline{E1}$ low and E2 high. $\overline{E}$ high = $\overline{E1}$ high or E2 low.
2. Q[A] = Previous contents of array at address A.
3. Q(A) = Data presented at input port.

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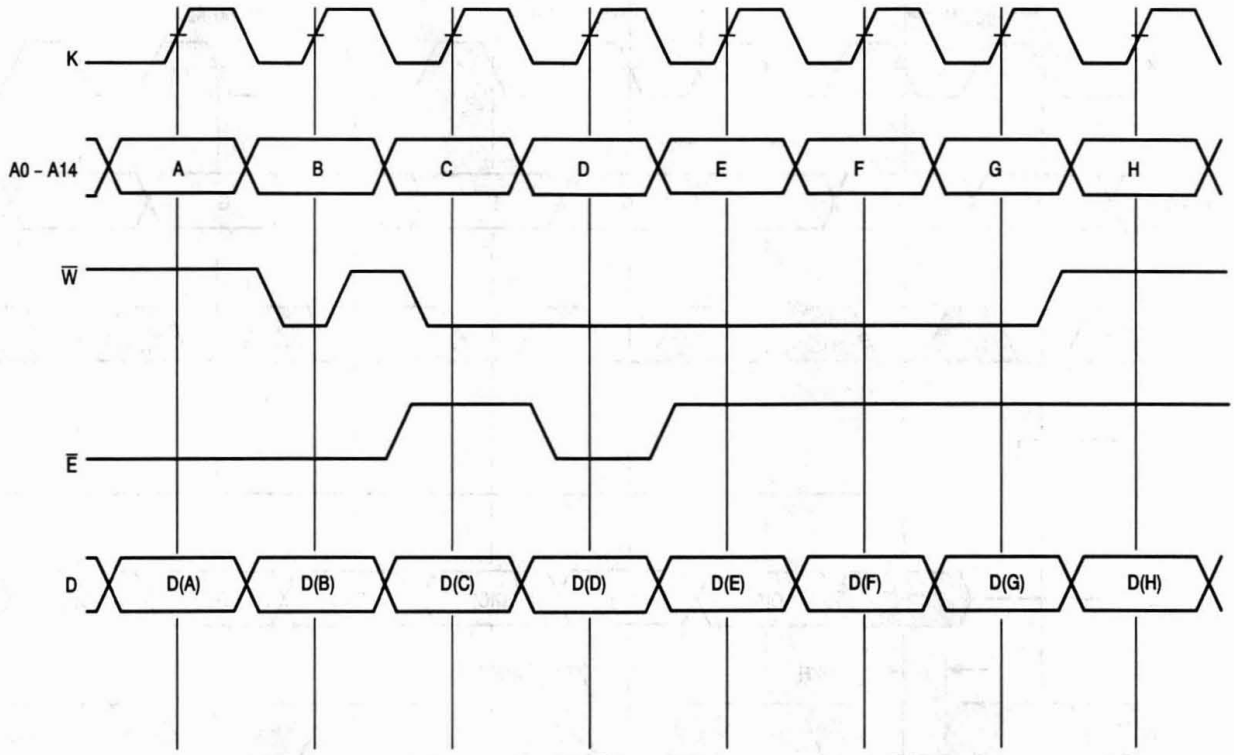
$\overline{E}$ CONTROLLED WRITE



NOTES:
1. $\overline{E}$ low = $\overline{E1}$ low, E2 high. $\overline{E}$ high = $\overline{E1}$ high or E2 low.
2. Only D(B) and D(D) are written to the array.

5

ORDERING INFORMATION
(Order by Full Part Number)

MCM 69Q536 XX XX X

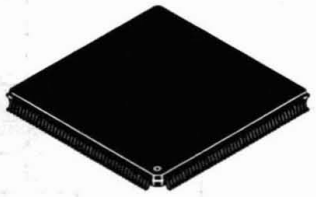
- Motorola Memory Prefix
- Part Number
- Shipping Method (R = Tape and Reel, Blank = Rails)
- Speed (6 = 6 ns, 8 = 8 ns, 10 = 10 ns)
- Package (TQ = TQFP)

Full Part Numbers — MCM69536TQ6 MCM69Q536TQ8 MCM69Q536TQ10
MCM69Q536TQ6R MCM69Q536TQ8R MCM69Q536TQ10R

MCM69D536

Advance Information

32K x 36 Bit Synchronous Dual I/O, Dual Address SRAM



TQ PACKAGE
176 LEAD TQFP
CASE 1101–01

The Motorola MCM69D536 is a 1 Megabit static random access memory, organized as 32K words of 36 bits. It features common data input and data output buffers and incorporates input and output registers on board with high speed SRAM.

The MCM69D536 allows the user to concurrently perform reads, writes, or pass–through cycles in combination on the two data ports. The two address ports AX and AY determine the read or write locations for their respective data ports DQX and DQY.

The synchronous design allows for precise cycle control with the use of an external single clock (K). All signal pins except output enables ($\overline{GX}$) and ($\overline{GY}$) are registered on the rising edge of clock (K).

The Pass–Through feature allows data to be passed from one port to the other, in either direction. The $\overline{PTX}$ input must be asserted to pass data from port X to port Y. The $\overline{PTY}$ will likewise pass data from port Y to port X.

For the case when AX and AY are the same, certain protocols are followed. If both ports are read, the reads occur normally. If one port is written and the other is read, the read from the array will occur before the data is written. If both ports are written, only the data on DQY will be written to the array.

- Single 3.3 V ± 5% Power Supply
- Fast Access Times: 6/8/10 ns Max
- Throughput of 2.98 Gigabits/Second
- Single Clock Operation
- Address, Data Input, $\overline{E1}$, E2, $\overline{PTX}$, $\overline{PTY}$, $\overline{WX}$, $\overline{WY}$, and Data Output Registers on Chip
- 83 MHz Maximum Clock Cycle Time
- Self Timed Write
- Two Bi–Directional Data Buses
- Can Be Configured as Separate I/O
- Pass–Through Feature
- Asynchronous Output Enables ($\overline{GX}$, $\overline{GY}$)
- LVTTL Compatible I/O
- 176 Pin TQFP Package
- Concurrent Reads and Writes

Suggested Applications

— ATM — Ethernet Switches — Routers
— Cell/Frame Buffers — SNA Switches — Shared Memory

Product Family Configurations

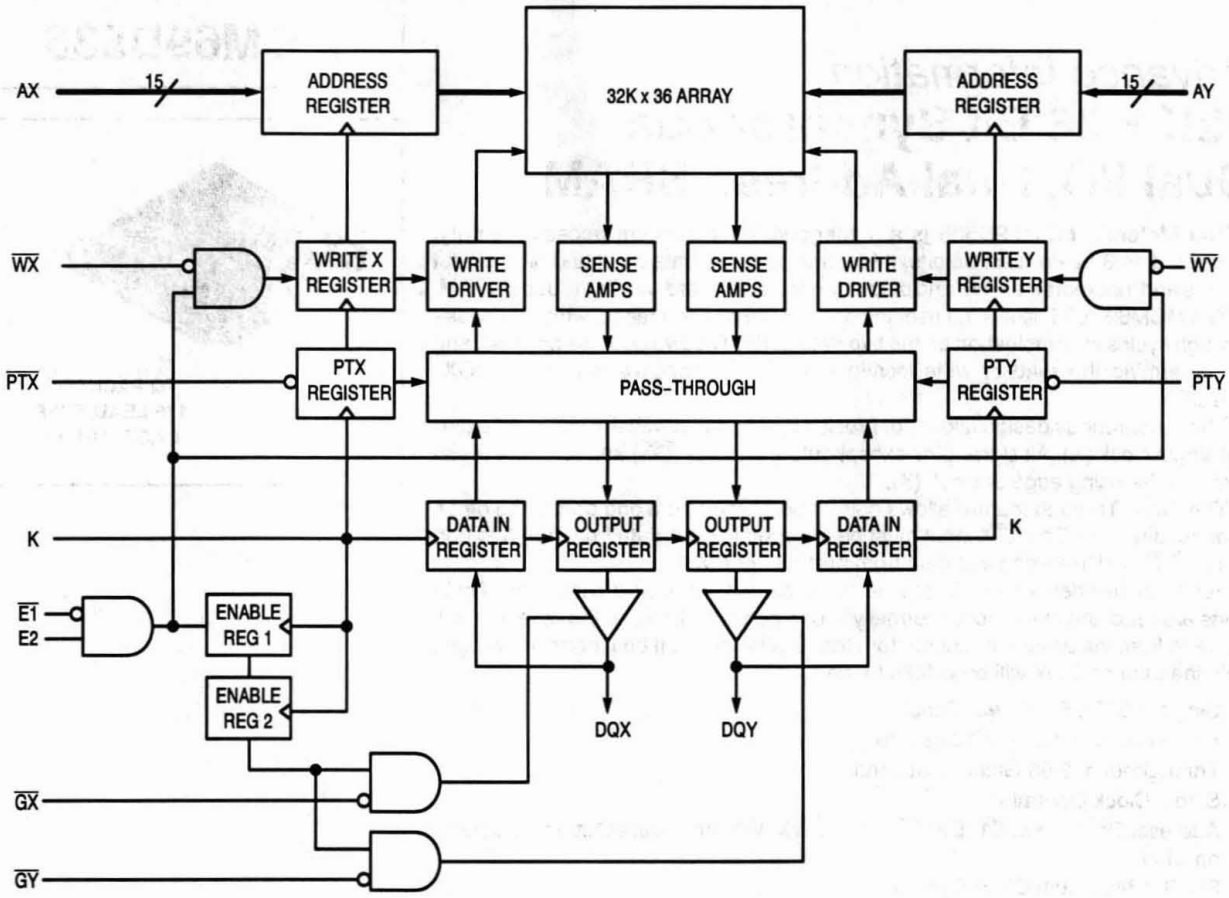
Part Number	Dual Address	Single Address	Dual I/O	Separate I/O
MCM69D536	✓	Note 1	✓	Note 2
MCM69D618	✓	Note 1	✓	Note 2
MCM69Q536		✓		✓
MCM69Q618		✓		✓
MCM67Q709		✓		✓
MCM67Q909		✓		✓

NOTES:
1. Tie AX and AY address ports together for the part to function as a single address part.
2. Tie $\overline{GX}$ high for DQX to be inputs and tie $\overline{WY}$ high and $\overline{GY}$ low for DQY to be outputs.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 1
3/12/97

BLOCK DIAGRAM



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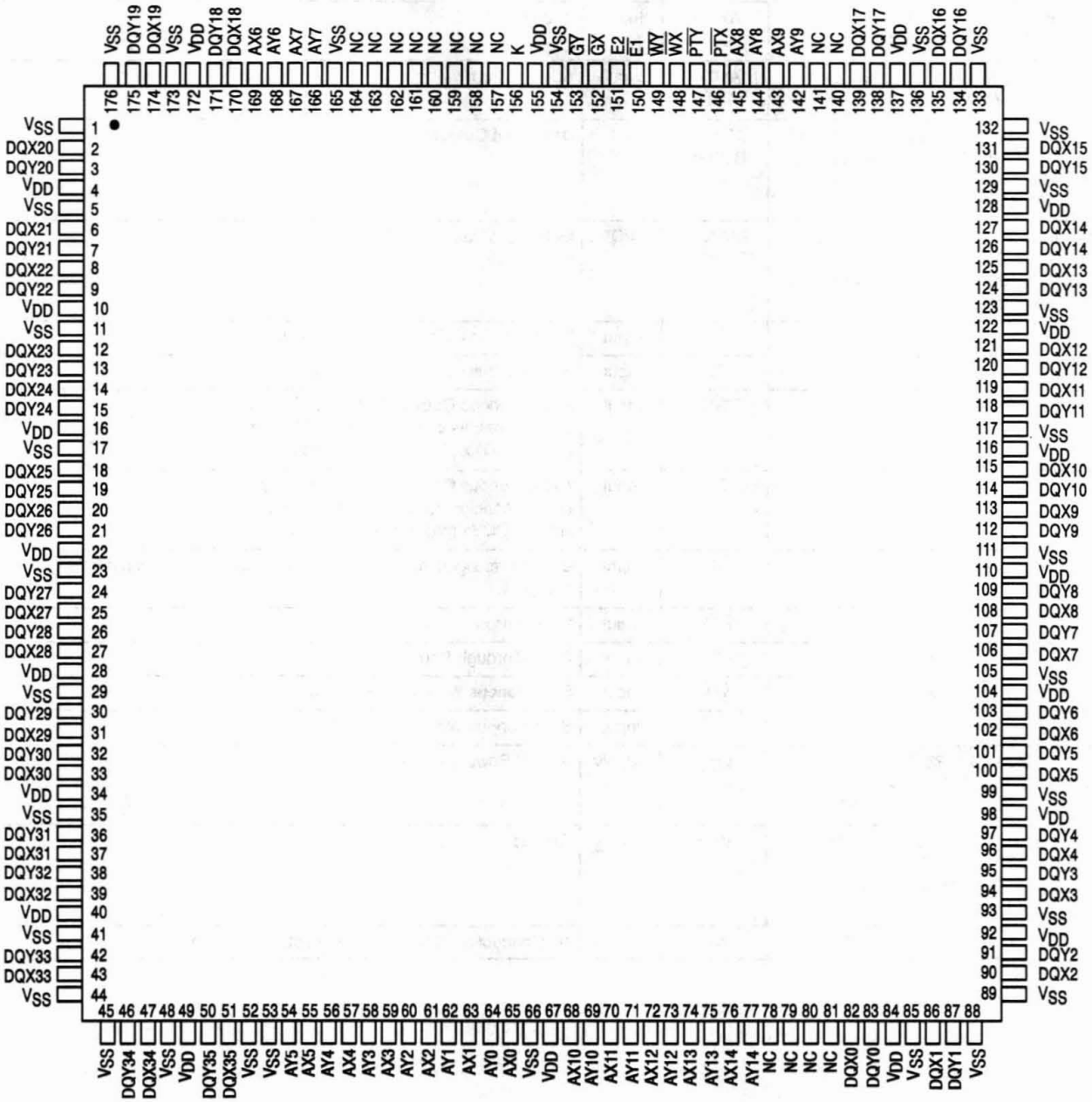
PIN ASSIGNMENT



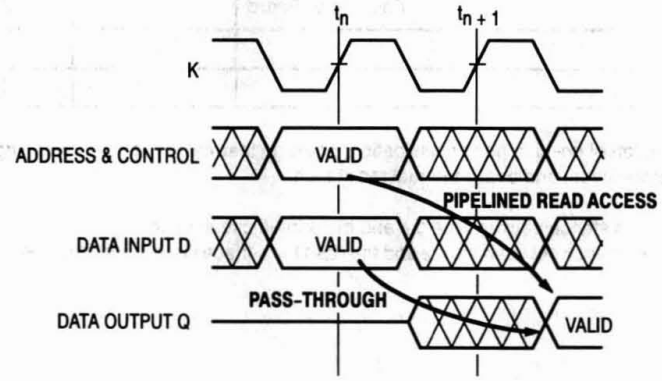
PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
55, 57, 59, 61, 63, 65, 68, 70, 72, 74, 76, 143, 145, 167, 169	AX0 – AX14	Input	Address Port X.
54, 56, 58, 60, 62, 64, 69, 71, 73, 75, 77, 142, 144, 166, 168	AY0 – AY14	Input	Address Port Y.
2, 6, 8, 12, 14, 18, 20, 25, 27, 31, 33, 37, 39, 43, 47, 51, 82, 86, 90, 94, 96, 100, 102, 106, 108, 113. 115, 119, 121, 125, 127, 131, 135, 139, 170, 174	DQX0 – DQX35	I/O	Data Input/Output Port X.
3, 7, 9, 13, 15, 19, 21, 24, 26, 30, 32, 36, 38, 42, 46, 50, 83, 87, 91, 95, 97, 101, 103, 107, 109, 112, 114, 118, 120, 124, 126, 130, 134, 138, 171, 175	DQY0 – DQY35	I/O	Data Input/Output Port Y.
150	$\overline{E1}$	Input	Synchronous Chip Enable: Active low.
151	E2	Input	Synchronous Chip Enable: Active high.
152	$\overline{GX}$	Input	Asynchronous Output Enable Port X Input: Low — enables output buffers (DQXx pins). High — DQXx pins are high impedance.
153	$\overline{GY}$	Input	Asynchronous Output Enable Port Y Input: Low — enables output buffers (DQYx pins). High — DQYx pins are high impedance.
156	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$.
146	$\overline{PTX}$	Input	Pass–Through Port X.
147	$\overline{PTY}$	Input	Pass–Through Port Y.
148	$\overline{WX}$	Input	Synchronous Write Enable Port X.
149	$\overline{WY}$	Input	Synchronous Write Enable Port Y.
4, 10, 16, 22, 28, 34, 40, 49, 67, 84, 92, 98, 104, 110, 116, 122, 128, 137, 155, 172	V_{DD}	Supply	+ 3.3 V Power Supply.
1, 5, 11, 17, 23, 29, 35, 41, 44, 45, 48, 52, 53, 66, 85, 88, 89, 93, 99, 105, 111, 117, 123. 129, 132, 133, 136, 154, 165, 173, 176	V_{SS}	Supply	Ground.
78– 81, 140, 141, 157 – 164	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE (See Notes 1 through 5)

	Input at t_n Clock						
Operation Number	$\overline{E1}$	E2	$\overline{WX}$	$\overline{WY}$	$\overline{PTX}$	$\overline{PTY}$	**Operation**
1	H	X	X	X	X	X	Deselected
2	X	L	X	X	X	X	Deselected
3	L	H	0	X	X	X	Write X Port
4	L	H	X	0	X	X	Write Y Port
5	L	H	X	X	0	X	Pass–Through X to Y
6	L	H	X	X	X	0	Pass–Through Y to X
7	L	H	1	X	1	1	Read X
8	L	H	X	1	1	1	Read Y

NOTES:
1. $\overline{GX}/\overline{GY}$ must be controlled to avoid bus contention issues during write and pass–through cycles.
2. Operation numbers 3 – 6 can be used in any combination.
3. Operation numbers 4 and 7, 3 and 8, 7 and 8 can be combined.
4. Operation number 5 cannot be combined with operation number 7 or 8.
5. Operation number 6 cannot be combined with operation number 7 or 8.



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ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{DD}	V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	TBD	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This is a synchronous device. All synchronous inputs must meet specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) while the device is selected.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

PACKAGE THERMAL CHARACTERISTICS (See Note 1)

Rating		Symbol	TQFP	Unit	Notes
Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	40 35	°C/W	2
Junction to Board (Bottom)		$R_{\theta JB}$	23	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

5

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)		V_{DD}	3.135	3.465	V
Input High Voltage		V_{IH}	2.0	V_{DD} + 0.5**	V
Input Low Voltage		V_{IL}	– 0.5*	0.8	V
Input Leakage Current (All Inputs, V_{in} = 0 to V_{DD})		$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{DD})		$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current (I_{out} = 0 mA) (V_{DD} = max, f = f_{max})	MCM69D536–6 ns MCM69D536–8 ns MCM69D536–10 ns	I_{DDA}	— — —	TBD TBD TBD	mA
CMOS Standby Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}, All Inputs Toggling at CMOS Levels V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{DD} – 0.2 V)	MCM69D536–6 ns MCM69D536–8 ns MCM69D536–10 ns	I_{SB1}	— — —	TBD TBD TBD	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	V_{DD}	V

* V_{IL} ≥ –1.5 V for t ≤ t_{KHKH}/2.
** V_{IH} ≤ V_{DD} + 1.0 V for t ≤ t_{KHKH}/2.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 0 to 70°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address and Data Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance	C_{in}	6	pF
Output Capacitance	C_{out}	8	pF

5

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... Figure 1 Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM69D536–6		MCM69D536–8		MCM69D536–10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	12	—	15	—	20	—	ns	1
Clock Access Time	t_{KHQV}	—	6	—	8	—	10	ns	
Clock Low Pulse Width	t_{KLKH}	4	—	6	—	8	—	ns	
Clock High Pulse Width	t_{KHKL}	4	—	6	—	8	—	ns	
Clock High to Data Output Invalid	t_{KHQX}	0	—	0	—	0	—	ns	
Clock High to Data Output High–Z	t_{KHQZ}	—	5	—	5	—	6	ns	3
Output Enable Low to Data Output Valid	t_{GLQV}	—	6	—	8	—	10	ns	
Output Enable Low to Data Output Low–Z	t_{GLQX}	0	—	0	—	0	—	ns	
Output Enable High to Data Output High–Z	t_{GHQZ}	—	5	—	8	—	10	ns	3
Setup Times: AWR0 – AWR14	t_{AVKH}	2.5	—	3	—	3	—	ns	2
ARD0 – ARD14	t_{AVKH}								
$\overline{W}$	t_{WVKH}								
$\overline{PT}$	t_{PTVKH}								
$\overline{E1}$, E2	t_{EVKH}								
D0 – D35	t_{DVKH}								
Hold Times: AWR0 – AWR14	t_{KHAX}	0.5	—	2	—	2	—	ns	2
ARD0 – ARD14	t_{KHAX}								
$\overline{W}$	t_{KHWX}								
$\overline{PT}$	t_{KHPTX}								
$\overline{E1}$, E2	t_{KHEX}								
D0 – D35	t_{KHDX}								

NOTES:
1. All read and write cycles are referenced from K.
2. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) while the device is selected.
3. This parameter is sampled and not 100% tested.

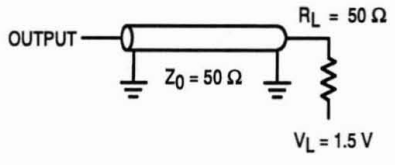
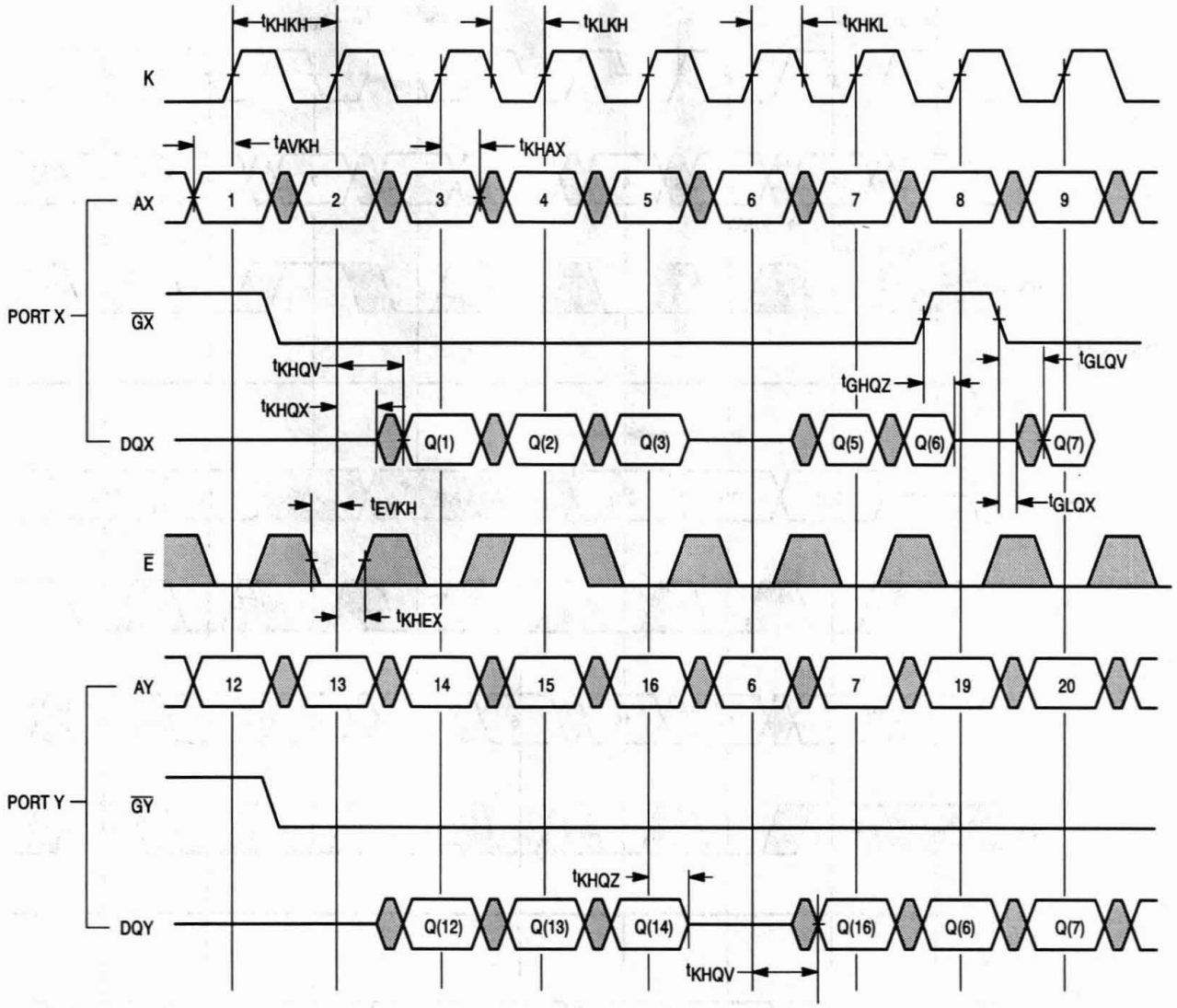


Figure 1. AC Test Load

READ CYCLE TIMING FROM BOTH PORTS ($\overline{WX}$, $\overline{WY}$, $\overline{PTX}$, $\overline{PTY}$ High)



$\overline{E}$ Low = $\overline{E1}$ Low and E2 High. $\overline{E}$ High = $\overline{E1}$ High or E2 Low.

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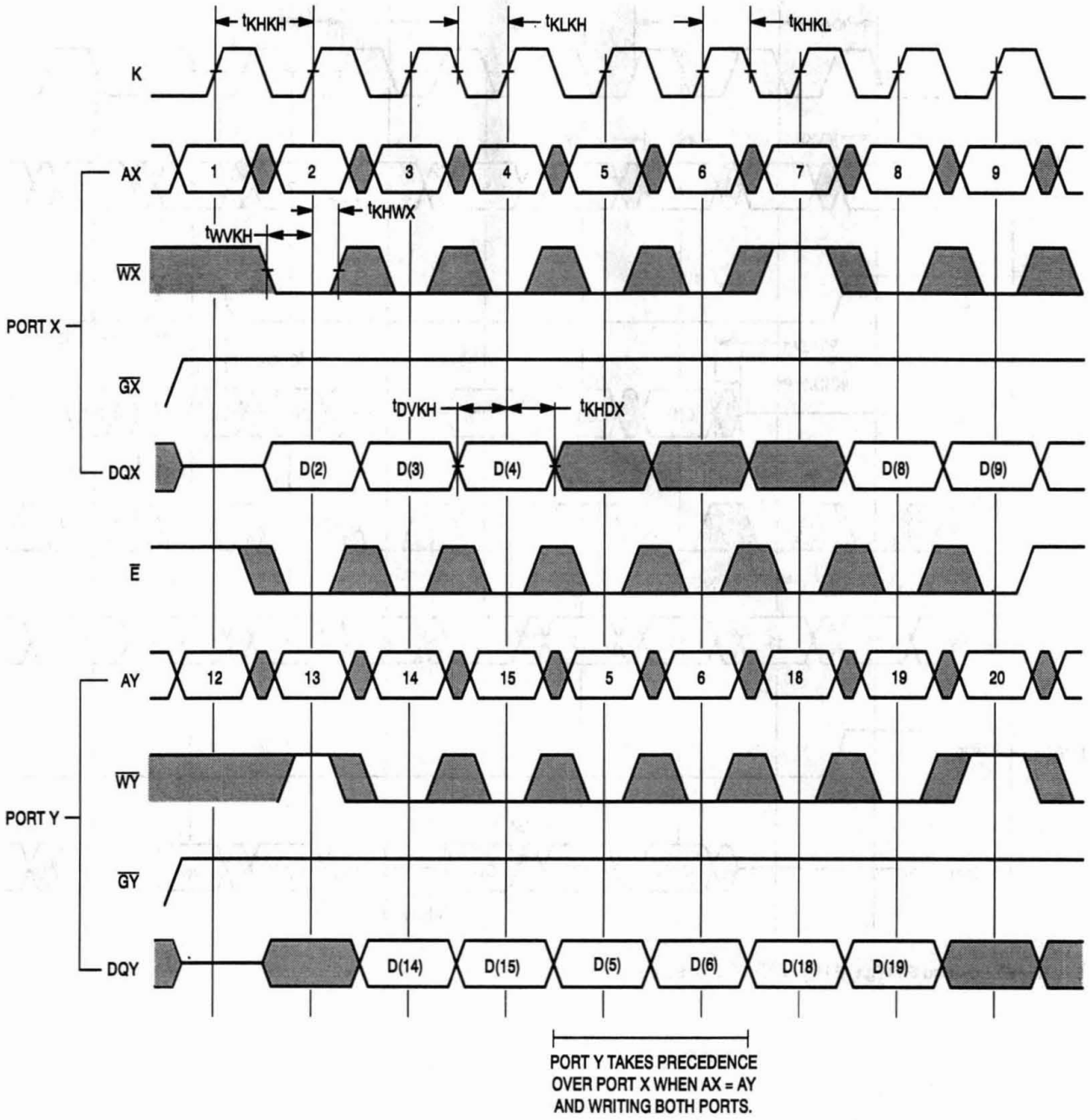
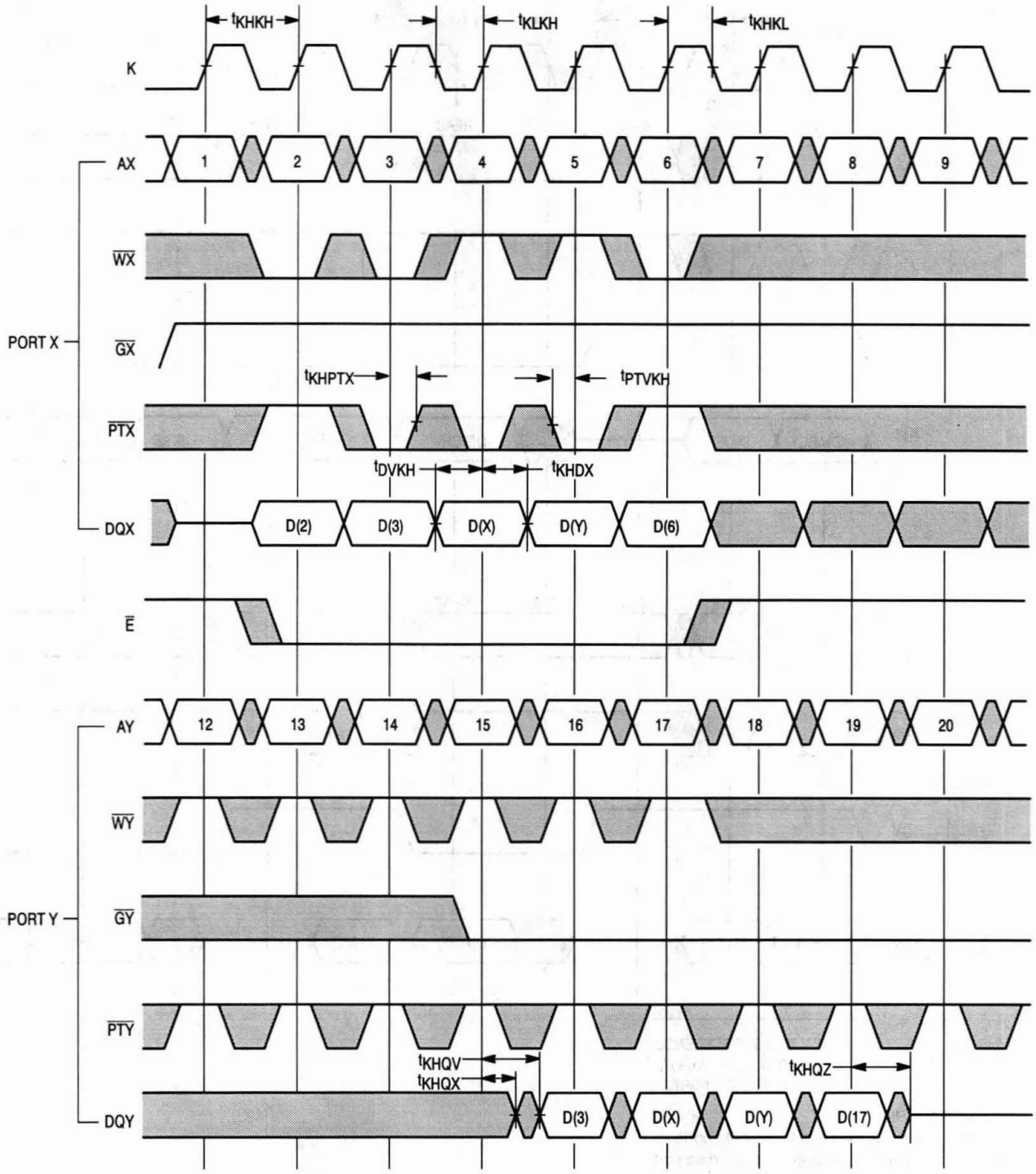
WRITE CYCLE TIMING TO BOTH PORTS ($\overline{PTX}$, $\overline{PTY}$ High)



$\overline{E}$ Low = $\overline{E1}$ Low and E2 High. $\overline{E}$ High = $\overline{E1}$ High or E2 Low.

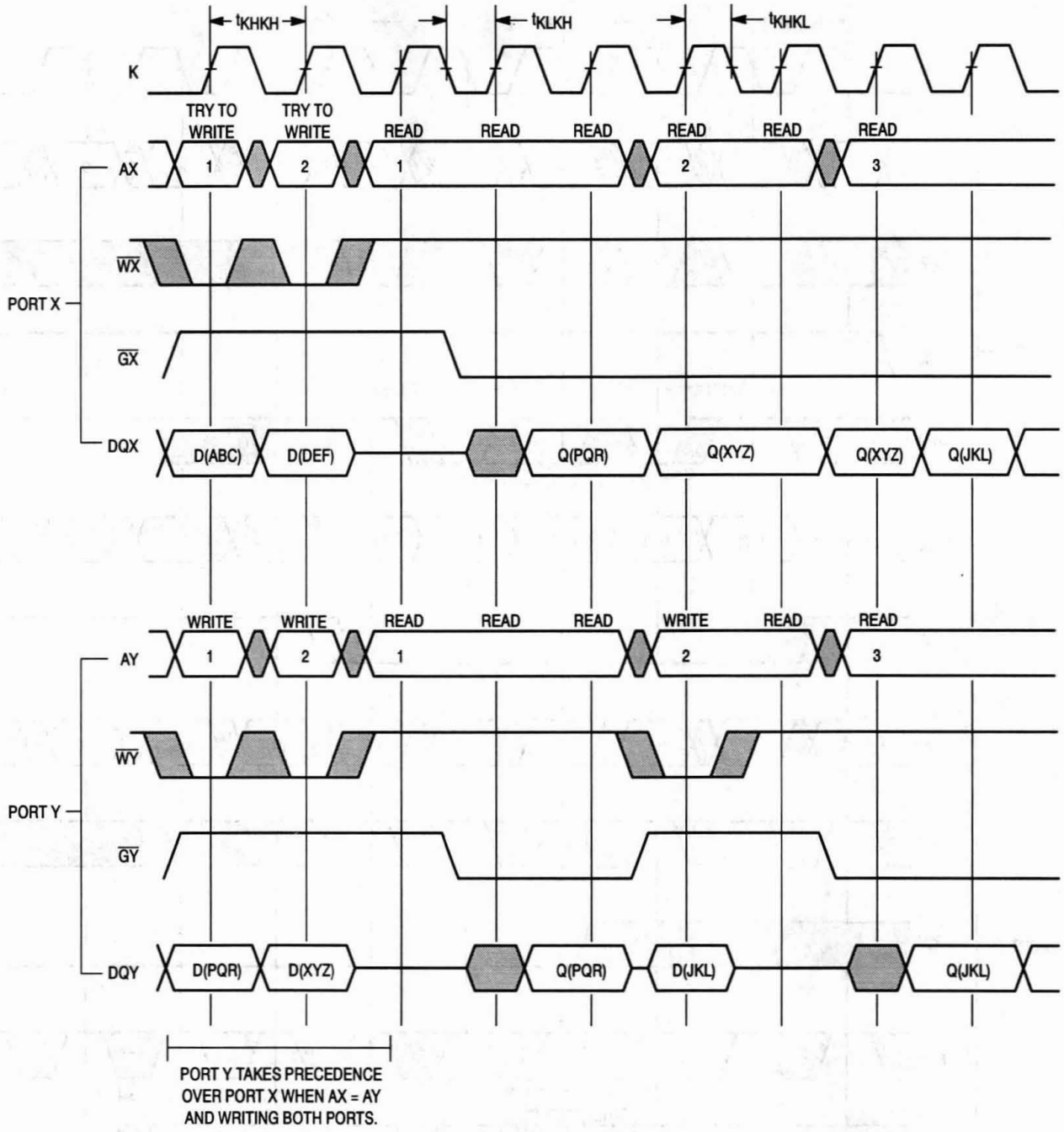
5

WRITE TO PORT X AND PASS THROUGH TO PORT Y (Note 1)



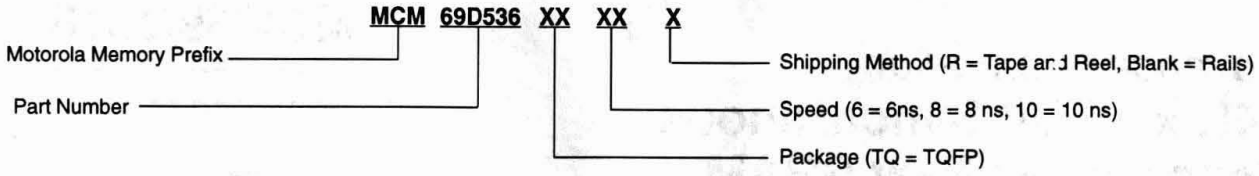
E Low = E1 Low and E2 High. E High = E1 High or E2 Low.
NOTE 1: The timing diagram is valid for the opposite case as well, i.e. writing to Port Y and passing through to Port X.

COMBINATION READ/WRITE WITH SAME ADDRESS ON EACH PORT



$\overline{PTX}$ = $\overline{PTY}$ = High
D(Value) = Value is the input to the data port
Q(Value) = Value is the output from the data port

ORDERING INFORMATION
(Order by Full Part Number)


MCM 69D536 XX XX X
Motorola Memory Prefix
Part Number
Shipping Method (R = Tape and Reel, Blank = Rails)
Speed (6 = 6ns, 8 = 8 ns, 10 = 10 ns)
Package (TQ = TQFP)

Full Part Numbers — MCMD536TQ6 MCM69D536TQ8 MCM69D536TQ10
MCMD536TQ6R MCM69D536TQ8R MCM69D536TQ10R

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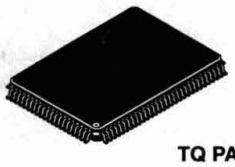
MCM69Q618

Advance Information

64K x 18 Bit Synchronous Separate I/O Fast SRAM



TQ PACKAGE
100 PIN TQFP
CASE 983A–01

The Motorola MCM69Q618 is a 1 Megabit static random access memory, organized as 64K words of 18 bits. It features separate data input and data output buffers and incorporates input and output registers on board with high speed SRAM.

The MCM69Q618 allows the user to perform transparent write and data pass through. Two data bus ports are provided – a data input (D) and a data output (Q) port.

The synchronous design allows for precise cycle control with the use of an external single clock (K). Address port, data input (D0 – D17), data output (Q0 – Q17), write enable ($\overline{W}$), chip enables ($\overline{E1}$, E2), and pass–through enable ($\overline{PT}$) are registered on the rising edge of clock (K).

Any given cycle operates on only one address. However, for any cycle, reads and writes can be intermixed. Thus, one can perform a read, a write, or a combination read/write during any one cycle. For a combination read/write, the contents of the array are read before the new data is written.

By using the pass–through function, the output port Q can be made to reflect either the contents of the array or the data presented to the input port D. For read/write or a read cycle with $\overline{G}$ low, the Q port will output the contents of the array. However, if $\overline{PT}$ is asserted, the Q port will instead output the data presented at the D input port.

- Single 3.3 V ± 5% Power Supply
- Fast Access Times: 6/8/10 ns Max
- Sustained Throughput of 1.49 Gigabits/Second
- Single Clock Operation
- Address, Data Input, $\overline{E1}$, E2, $\overline{PT}$, $\overline{W}$, and Data Output Registers on Chip
- 83 MHz Maximum Clock Cycle Time
- Self Timed Write
- Separate Data Input and Data Output Pins
- Pass–Through Feature
- Asynchronous Output Enable ($\overline{G}$)
- LVTTL Compatible I/O
- No Dead Cycles Required for Reads after Writes or for Writes after Reads
- 100 Pin TQFP Package
- Simultaneous Reads and Writes

Suggested Applications

— ATM — Ethernet Switches — Routers
— Cell/Frame Buffers — SNA Switches — Shared Memory

Product Family Configurations

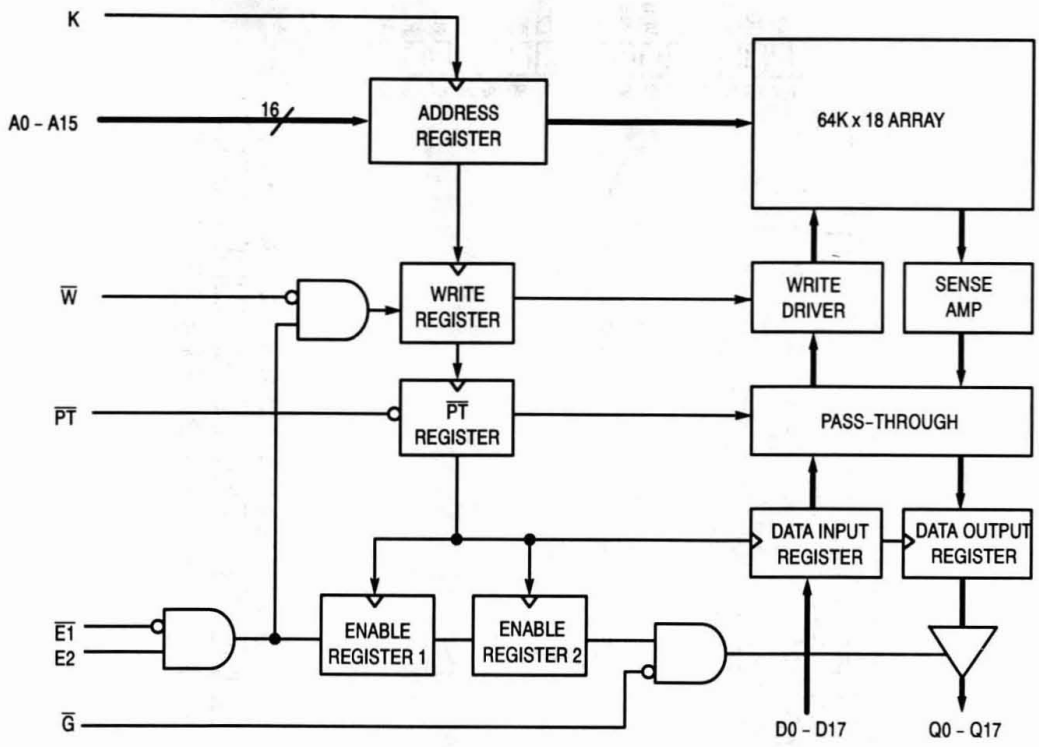
Part Number	Dual Address	Single Address	Dual I/O	Separate I/O
MCM69D536	✓	Note 1	✓	Note 2
MCM69D618	✓	Note 1	✓	Note 2
MCM69Q536		✓		✓
MCM69Q618		✓		✓
MCM67Q709		✓		✓
MCM67Q909		✓		✓

NOTES:
1. Tie AX and AY address ports together for the part to function as a single address part.
2. Tie $\overline{GX}$ high for DQX to be inputs and tie $\overline{WY}$ high and $\overline{GY}$ low for DQY to be outputs.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 3
3/12/97

BLOCK DIAGRAM



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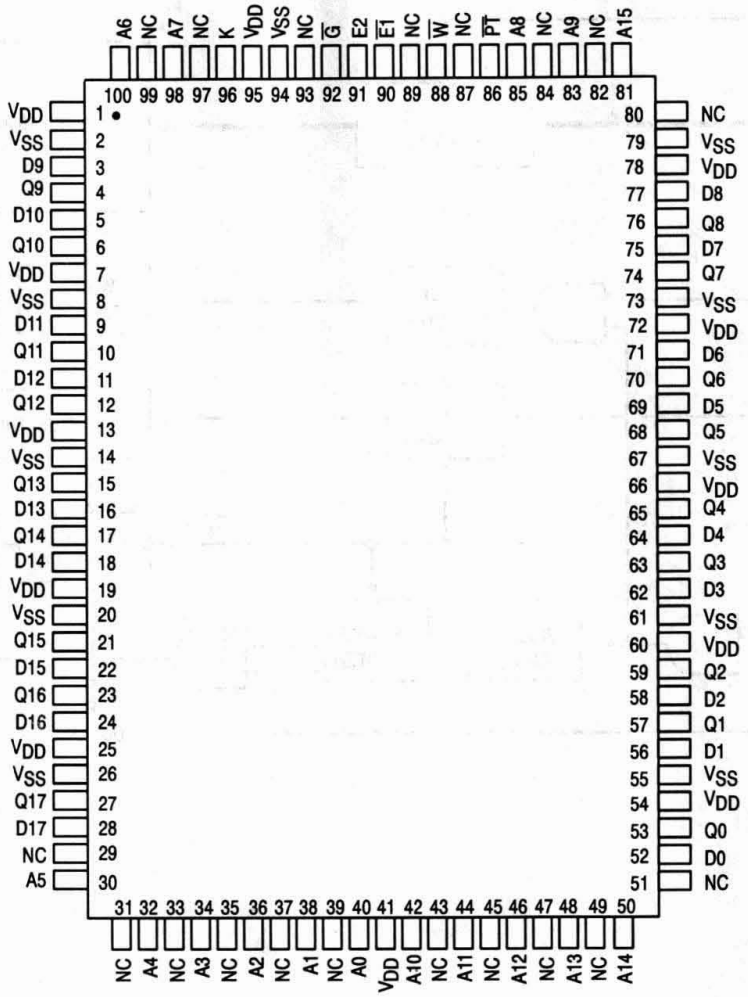
PIN ASSIGNMENT



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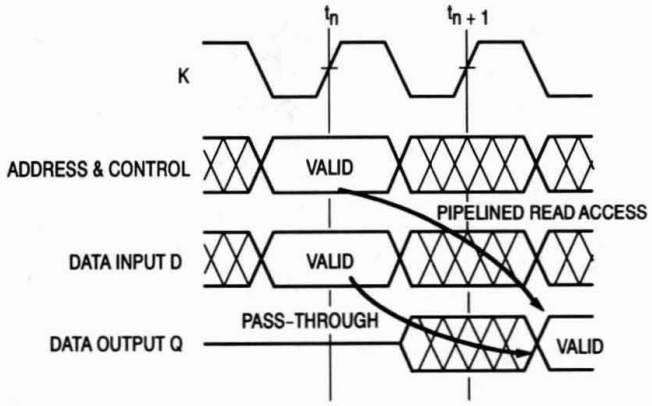
PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
30, 32, 34, 36, 38, 40, 42, 44, 46, 48, 50, 81, 83, 85, 98, 100	A0 – A15	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
3, 5, 9, 11, 16, 18, 22, 24, 28, 52, 56, 58, 62, 64, 69, 71, 75, 77	D0 – D17	Input	Synchronous Data Input.
92	E1	Input	Synchronous Chip Enable: Active low for depth expansion.
93	E2	Input	Synchronous Chip Enable: Active high for depth expansion.
94	G	Input	Asynchronous Output Enable Input: Low — enables output buffers (Qx pins). High — Qx pins are high impedance.
96	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$.
86	$\overline{PT}$	Input	Pass–through enable: Synchronous.
4, 6, 10, 12, 15, 17, 21, 23, 27, 53, 57, 59, 63, 65, 68, 70, 74, 76	Q0 – Q17	Output	Synchronous Data Output.
88	$\overline{W}$	Input	Synchronous Write.
1, 7, 13, 19, 25, 41, 54, 60, 66, 72, 78, 91	V_{DD}	Supply	+ 3.3 V Power Supply.
2, 8, 14, 20, 26, 55, 61, 67, 73, 79, 90	V_{SS}	Supply	Ground.
29, 31, 33, 35, 37, 39, 43, 45, 47, 49, 51, 80, 82, 84, 87, 89, 95, 97, 99	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE

Operation	Input at t_n Clock					Result from t_{n+1} Clock	Notes
	E1	E2	W	PT	Data Input D	Data Output Q	
Write and Pass–Through	L	H	L	L	D written to A	D data appears	1
Write/Read	L	H	L	H	D written to A	Q out from A	2
Pass–Through	L	H	H	L	D data	D data appears	3
Read	L	H	H	H	Don't Care	Q out from A	4
Deselected	X	L	X	X	Don't Care	Q is high–Z	5
Deselected	H	X	X	X	Don't Care	Q is high–Z	6

NOTES:
1. Write D to array and output D at Q.
2. Output contents of array to Q then write D to array.
3. Output D at Q. Do not write.
4. Output contents of array to Q. Do not write.
5. No operation.
6. No operation.



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{DD}	V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	TBD	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This is a synchronous device. All synchronous inputs must meet specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) while the device is selected.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

PACKAGE THERMAL CHARACTERISTICS (See Note 1)

Rating		Symbol	TQFP	Unit	Notes
Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	40 25	°C/W	2
Junction to Board (Bottom)		$R_{\theta JB}$	17	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

5

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)		V_{DD}	3.135	3.465	V
Input High Voltage		V_{IH}	2.0	V_{DD} + 0.5**	V
Input Low Voltage		V_{IL}	– 0.5*	0.8	V
Input Leakage Current (All Inputs, V_{in} = 0 to V_{DD})		$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{DD})		$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current (I_{out} = 0 mA) (V_{DD} = max, f = f_{max})	MCM69Q618–6 ns MCM69Q618–8 ns MCM69Q618–10 ns	I_{DDA}	— — —	TBD TBD TBD	mA
CMOS Standby Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}, All Inputs Toggling at CMOS Levels V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{DD} – 0.2 V)	MCM69Q618–6 ns MCM69Q618–8 ns MCM69Q618–10 ns	I_{SB1}	— — —	TBD TBD TBD	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	V_{DD}	V

* V_{IL} ≥ –1.5 V for t ≤ t_{KHKH}/2.
** V_{IH} ≤ V_{DD} + 1.0 V for t ≤ t_{KHKH}/2.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 0 to 70°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address and Data Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance	C_{in}	6	pF
Output Capacitance	C_{out}	8	pF

5

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... Figure 1 Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter		Symbol	MCM69Q618–6		MCM69Q618–8		MCM69Q618–10		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Cycle Time		t_{KHKH}	12	—	15	—	20	—	ns	1
Clock Access Time		t_{KHQV}	—	6	—	8	—	10	ns	2
Clock Low Pulse Width		t_{KLKH}	4	—	6	—	8	—	ns	
Clock High Pulse Width		t_{KHKL}	4	—	6	—	8	—	ns	
Clock High to Data Output Invalid		t_{KHQX}	0	—	0	—	0	—	ns	
Clock High to Data Output High–Z		t_{KHQZ}	—	5	—	6	—	7	ns	4
Output Enable to Output Valid		t_{GLQV}	—	6	—	8	—	10	ns	
Output Enable to Output Active		t_{GLQX}	0	—	0	—	0	—	ns	4
Output Disable to Output High–Z		t_{GHQZ}	—	5	—	6	—	7	ns	4
Setup Times:	A0 – A15	t_{AVKH}	2.5	—	3	—	3	—	ns	3
	$\overline{W}$	t_{WVKH}								
	$\overline{PT}$	t_{PTVKH}								
	$\overline{E1}$, E2	t_{EVKH}								
	D0 – D17	t_{DVKH}								
Hold Times:	A0 – A15	t_{KHAX}	0.5	—	2	—	2	—	ns	3
	$\overline{W}$	t_{KHWX}								
	$\overline{PT}$	t_{KHPTX}								
	$\overline{E1}$, E2	t_{KHEX}								
	D0 – D17	t_{KHDX}								

NOTES:
1. All read and write cycles are referenced from K.
2. Valid data from Clock High will be the data stored at the address or the last valid read cycle.
3. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) while the device is selected.
4. This parameter is sampled and not 100% tested.

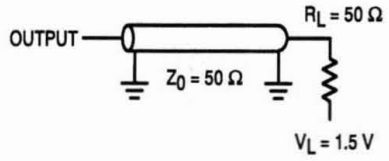
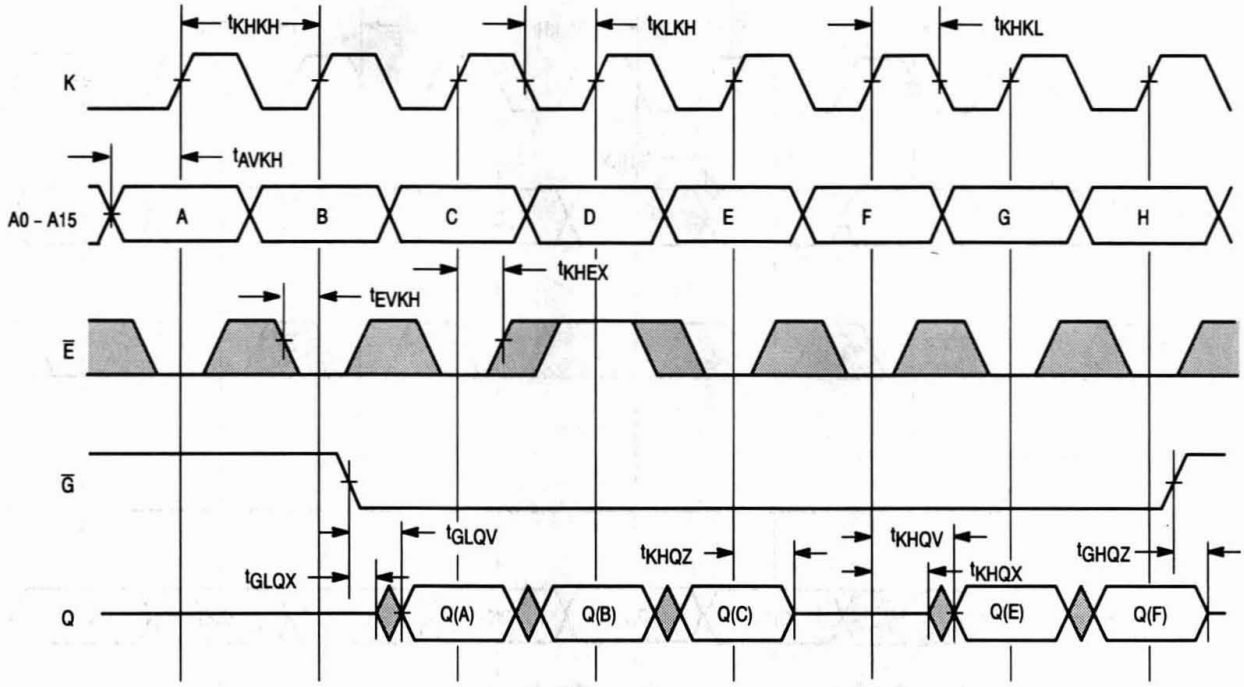


Figure 1. AC Test Load

READ CYCLE TIMING



$\overline{E}$ low = $\overline{E1}$ low, E2 high. $\overline{E}$ high = $\overline{E1}$ high or E2 low.

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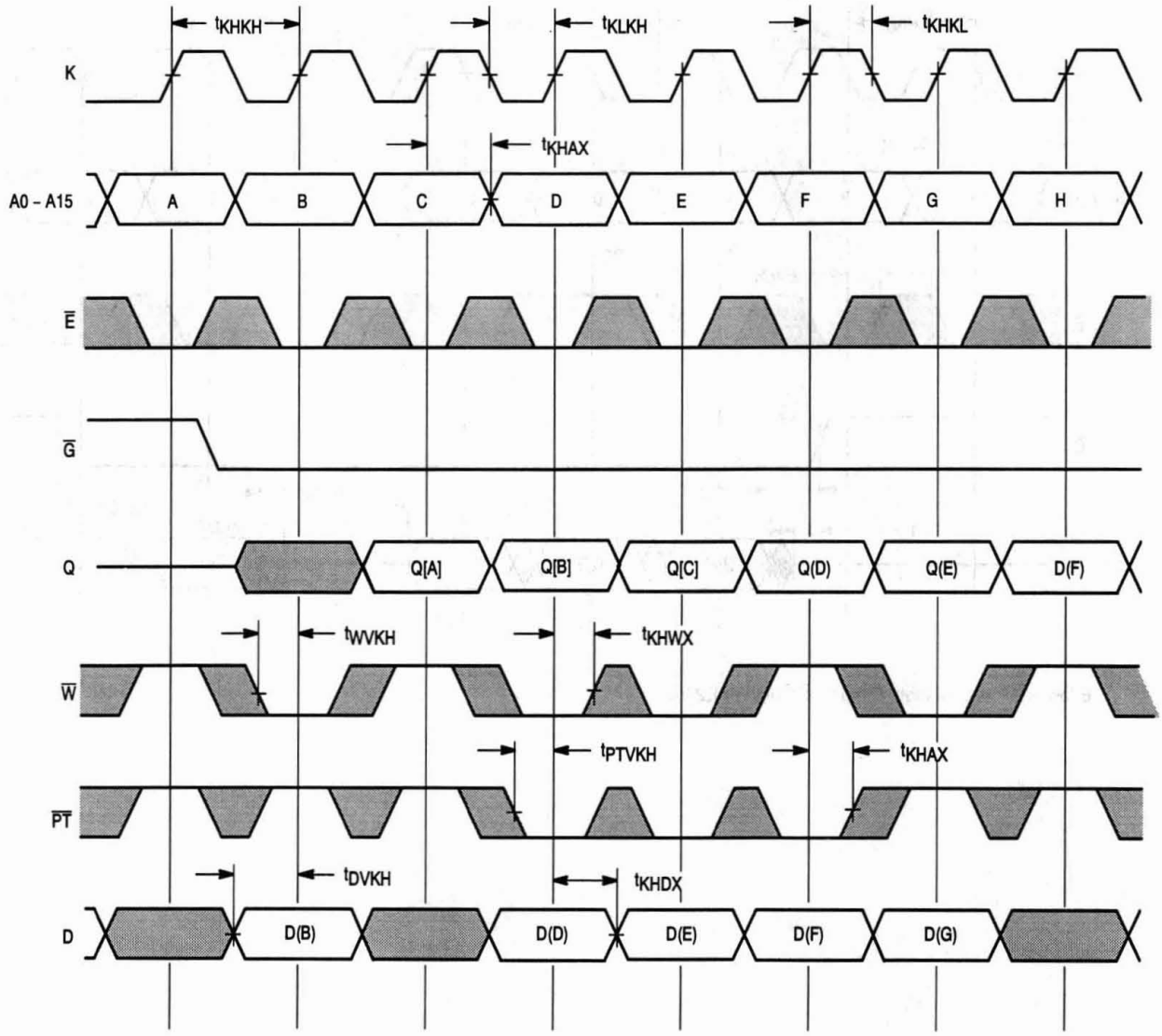
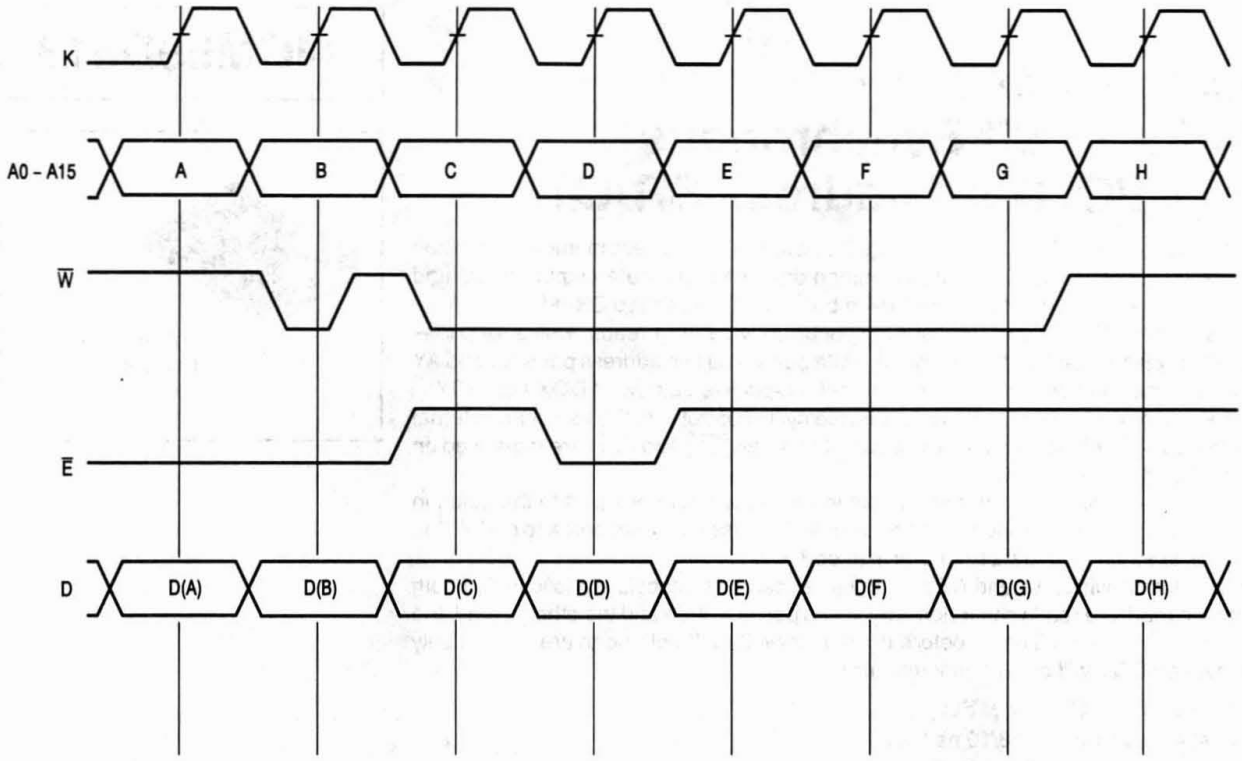
COMBINATION READ/WRITE CYCLE TIMING



NOTES:
1. $\overline{E}$ low = $\overline{E1}$ low and E2 high. $\overline{E}$ high = $\overline{E1}$ high or E2 low.
2. Q[A] = Previous contents of array at address A.
3. Q(A) = Data presented at input port.

5

$\overline{E}$ CONTROLLED WRITE



NOTES:
1. $\overline{E}$ low = $\overline{E1}$ low, E2 high. $\overline{E}$ high = $\overline{E1}$ high or E2 low.
2. Only D(B) and D(D) are written to the array.

5

ORDERING INFORMATION
(Order by Full Part Number)

MCM 69Q618 XX XX X

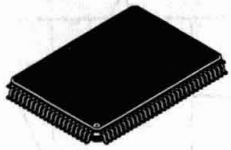
- Motorola Memory Prefix
- Part Number
- Shipping Method (R = Tape and Reel, Blank = Rails)
- Speed (6 = 6 ns, 8 = 8 ns, 10 = 10 ns)
- Package (TQ = TQFP)

Full Part Numbers — MCM69Q618TQ6 MCM69Q618TQ8 MCM69Q618TQ10
MCM69Q618TQ6R MCM69Q618TQ8R MCM69Q618TQ10R

MCM69D618

Advance Information

64K x 18 Bit Synchronous Dual I/O, Dual Address SRAM



TQ PACKAGE
100 LEAD TQFP
CASE 983A–01

The Motorola MCM69D618 is a 1 Megabit static random access memory, organized as 64K words of 18 bits. It features common data input and data output buffers and incorporates input and output registers on board with high speed SRAM.

The MCM69D618 allows the user to concurrently perform reads, writes, or pass–through cycles in combination on the two data ports. The two address ports AX and AY determine the read or write locations for their respective data ports DQX and DQY.

The synchronous design allows for precise cycle control with the use of an external single clock (K). All signal pins except output enables ($\overline{GX}$) and ($\overline{GY}$) are registered on the rising edge of clock (K).

The Pass–Through feature allows data to be passed from one port to the other, in either direction. The $\overline{PTX}$ input must be asserted to pass data from port X to port Y. The $\overline{PTY}$ will likewise pass data from port Y to port X.

For the case when AX and AY are the same, certain protocols are followed. If both ports are read, the reads occur normally. If one port is written and the other is read, the read from the array will occur before the data is written. If both ports are written, only the data on DQY will be written to the array.

- Single 3.3 V ± 5% Power Supply
- Fast Access Times: 6/8/10 ns Max
- Throughput of 1.49 Gigabits/Second
- Single Clock Operation
- Address, Data Input, $\overline{E1}$, E2, $\overline{PTX}$, $\overline{PTY}$, $\overline{WX}$, $\overline{WY}$, and Data Output Registers on Chip
- 83 MHz Maximum Clock Cycle Time
- Self Timed Write
- Two Bi–directional Data Buses
- Can Be Configured as Separate I/O
- Pass–Through Feature
- Asynchronous Output Enables ($\overline{GX}$, $\overline{GY}$)
- LVTTL Compatible I/O
- 100 Pin TQFP Package
- Concurrent Reads and Writes

Suggested Applications

— ATM — Ethernet Switches — Routers
— Cell/Frame Buffers — SNA Switches — Shared Memory

Product Family Configurations

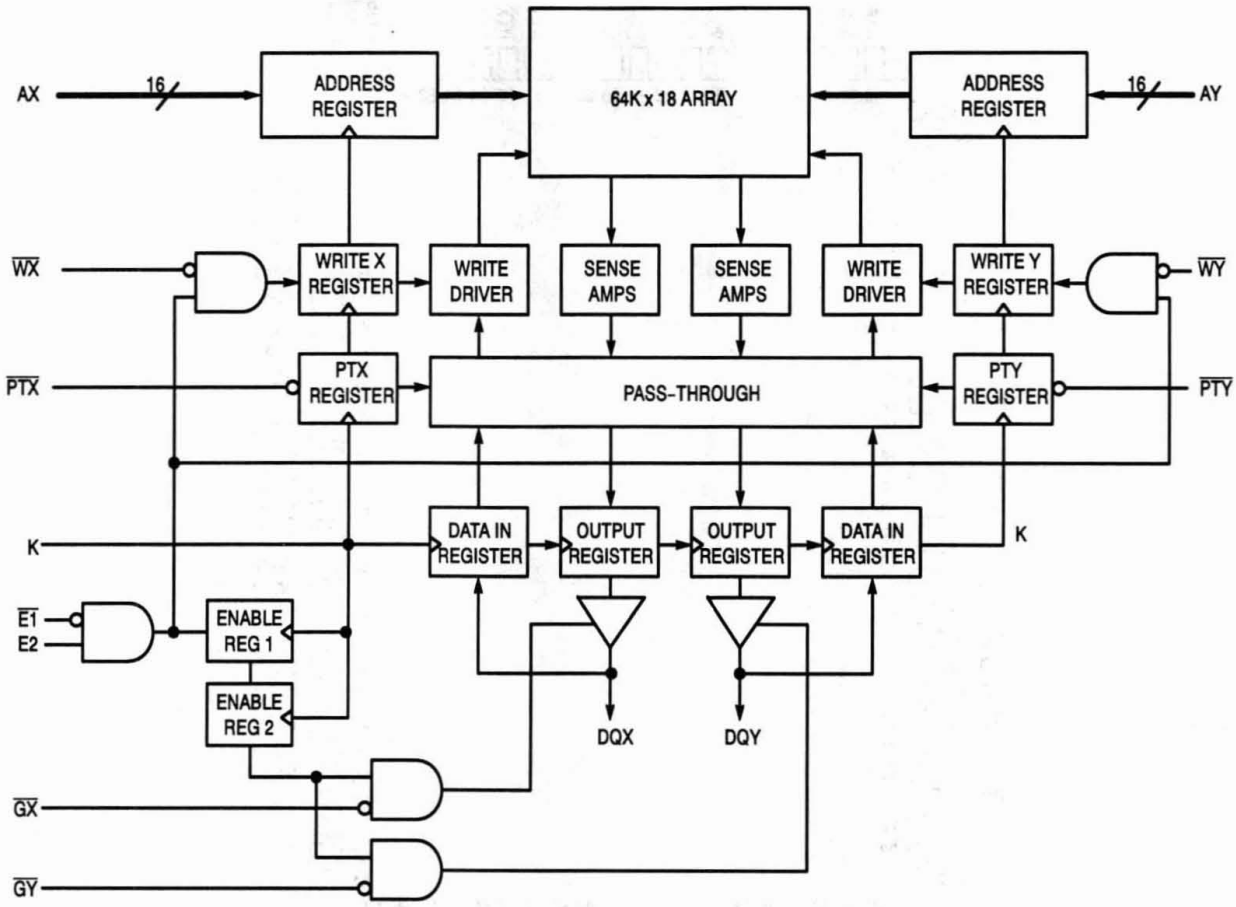
Part Number	Dual Address	Single Address	Dual I/O	Separate I/O
MCM69D536	✓	Note 1	✓	Note 2
MCM69D618	✓	Note 1	✓	Note 2
MCM69Q536		✓		✓
MCM69Q618		✓		✓
MCM67Q709		✓		✓
MCM67Q909		✓		✓

NOTES:
1. Tie AX and AY address ports together for the part to function as a single address part.
2. Tie $\overline{GX}$ high for DQX to be inputs and tie $\overline{WY}$ high and $\overline{GY}$ low for DQY to be outputs.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 1
3/12/97

BLOCK DIAGRAM



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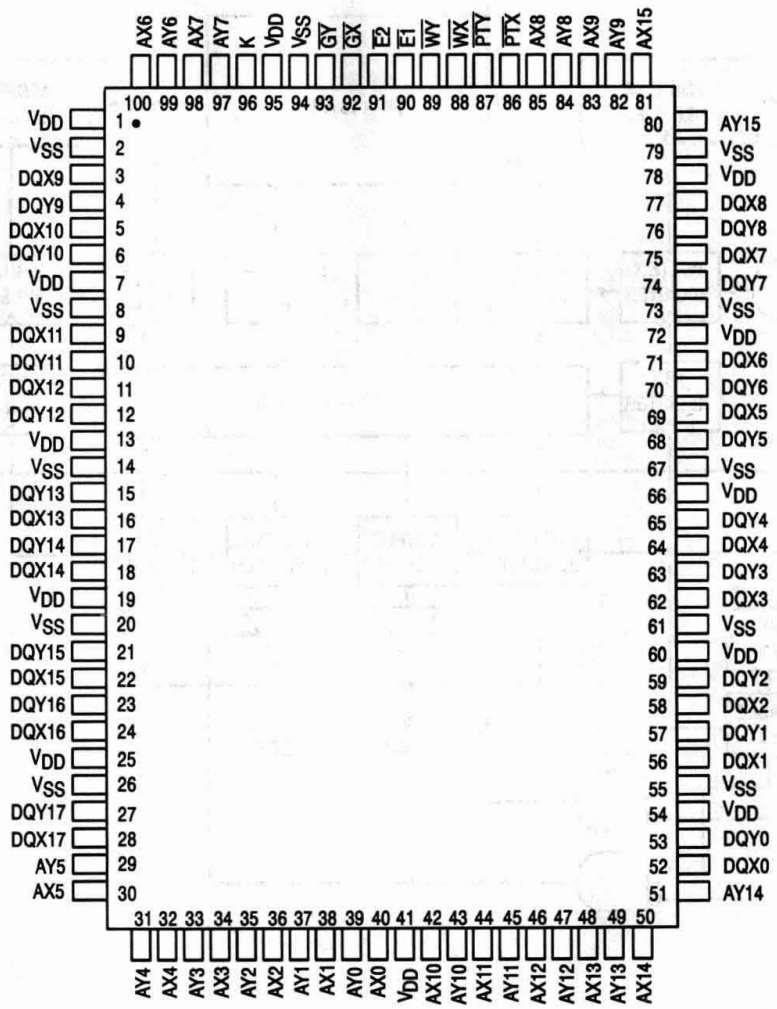
PIN ASSIGNMENT



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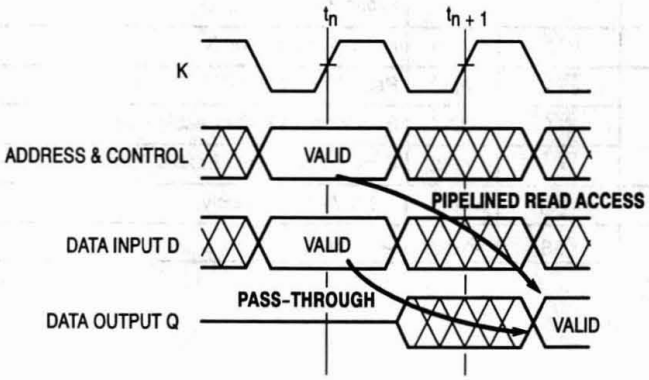
PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
30, 32, 34, 36, 38, 40, 42, 44, 46, 48, 50, 81, 83, 85, 98, 100	AX0 – AX15	Input	Address Port X.
29, 31, 33, 35, 37, 39, 43, 45, 47, 49, 51, 80, 82, 84, 97, 99	AY0 – AY15	Input	Address Port Y.
3, 5, 9, 11, 16, 18, 22, 24, 28, 52, 56, 58, 62, 64, 69, 71, 75, 77	DQX0 – DQX17	I/O	Data Input/Output Port X.
4, 6, 10, 12, 15, 17, 21, 23, 27, 53, 57, 59, 63, 65, 68, 70, 74, 76	DQY0 – DQY17	I/O	Data Input/Output Port Y.
92	$\overline{E1}$	Input	Synchronous Chip Enable: Active low.
93	E2	Input	Synchronous Chip Enable: Active high.
94	$\overline{GX}$	Input	Asynchronous Output Enable Port X Input: Low — enables output buffers (DQXx pins). High — DQXx pins are high impedance.
95	$\overline{GY}$	Input	Asynchronous Output Enable Port Y Input: Low — enables output buffers (DQYx pins). High — DQYx pins are high impedance.
96	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$.
86	$\overline{PTX}$	Input	Pass–Through Port X.
87	$\overline{PTY}$	Input	Pass–Through Port Y.
88	$\overline{WX}$	Input	Synchronous Write Enable Port X.
89	$\overline{WY}$	Input	Synchronous Write Enable Port Y.
1, 7, 13, 19, 25, 41, 54, 60, 66, 72, 78, 91	V_{DD}	Supply	+ 3.3 V Power Supply.
2, 8, 14, 20, 26, 55, 61, 67, 73, 79, 90	V_{SS}	Supply	Ground.

TRUTH TABLE (See Notes 1 through 5)

	Input at t_n Clock						
Operation Number	$\overline{E1}$	E2	$\overline{WX}$	$\overline{WY}$	$\overline{PTX}$	$\overline{PTY}$	**Operation**
1	H	X	X	X	X	X	Deselected
2	X	L	X	X	X	X	Deselected
3	L	H	0	X	X	X	Write X Port
4	L	H	X	0	X	X	Write Y Port
5	L	H	X	X	0	X	Pass–Through X to Y
6	L	H	X	X	X	0	Pass–Through Y to X
7	L	H	1	X	1	1	Read X
8	L	H	X	1	1	1	Read Y

NOTES:
1. $\overline{GX}/\overline{GY}$ must be controlled to avoid bus contention issues during write and pass–through cycles.
2. Operation numbers 3 – 6 can be used in any combination.
3. Operation numbers 4 and 7, 3 and 8, 7 and 8 can be combined.
4. Operation number 5 cannot be combined with operation number 7 or 8.
5. Operation number 6 cannot be combined with operation number 7 or 8.



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{DD}	V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	TBD	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This is a synchronous device. All synchronous inputs must meet specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) while the device is selected.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

PACKAGE THERMAL CHARACTERISTICS (See Note 1)

Rating		Symbol	TQFP	Unit	Notes
Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	40 25	°C/W	2
Junction to Board (Bottom)		$R_{\theta JB}$	17	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V ± 5%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)		V_{DD}	3.135	3.465	V
Input High Voltage		V_{IH}	2.0	V_{DD} + 0.5**	V
Input Low Voltage		V_{IL}	– 0.5*	0.8	V
Input Leakage Current (All Inputs, V_{in} = 0 to V_{DD})		$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{DD})		$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current (I_{out} = 0 mA) (V_{DD} = max, f = f_{max})	MCM69D618–6 ns MCM69D618–8 ns MCM69D618–10 ns	I_{DDA}	— — —	TBD TBD TBD	mA
CMOS Standby Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}, All Inputs Toggling at CMOS Levels V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{DD} – 0.2 V)	MCM69D618–6 ns MCM69D618–8 ns MCM69D618–10 ns	I_{SB1}	— —	TBD TBD TBD	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	V_{DD}	V

* V_{IL} ≥ –1.5 V for t ≤ t_{KHKH}/2.
** V_{IH} ≤ V_{DD} + 1.0 V for t ≤ t_{KHKH}/2.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 0 to + 70°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address and Data Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance	C_{in}	6	pF
Output Capacitance	C_{out}	8	pF

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AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V ± 5%, T_A = 0 to 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... Figure 1 Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM69D618–6		MCM69D618–8		MCM69D618–10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	12	—	15	—	20	—	ns	1
Clock Access Time	t_{KHQV}	—	6	—	8	—	10	ns	
Clock Low Pulse Width	t_{KLKH}	4	—	6	—	8	—	ns	
Clock High Pulse Width	t_{KHKL}	4	—	6	—	8	—	ns	
Clock High to Data Output Invalid	t_{KHQX}	0	—	0	—	0	—	ns	
Clock High to Data Output High–Z	t_{KHQZ}	—	5	—	5	—	6	ns	3
Output Enable Low to Data Output Valid	t_{GLQV}	—	6	—	8	—	10	ns	
Output Enable Low to Data Output Low–Z	t_{GLQX}	0	—	0	—	0	—	ns	
Output Enable High to Data Output High–Z	t_{GHQZ}	—	5	—	8	—	10	ns	3
Setup Times: AWR0 – AWR14	t_{AVKH}	2.5	—	3	—	3	—	ns	2
ARD0 – ARD14	t_{AVKH}								
$\overline{W}$	t_{WVKH}								
$\overline{PT}$	t_{PTVKH}								
$\overline{E1}$, E2	t_{EVKH}								
D0 – D35	t_{DVKH}								
Hold Times: AWR0 – AWR14	t_{KHAX}	0.5	—	2	—	2	—	ns	2
ARD0 – ARD14	t_{KHAX}								
$\overline{W}$	t_{KHWX}								
$\overline{PT}$	t_{KHPTX}								
$\overline{E1}$, E2	t_{KHEX}								
D0 – D35	t_{KHDX}								

NOTES:
1. All read and write cycles are referenced from K.
2. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) while the device is selected.
3. This parameter is sampled and not 100% tested.

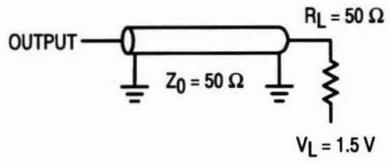
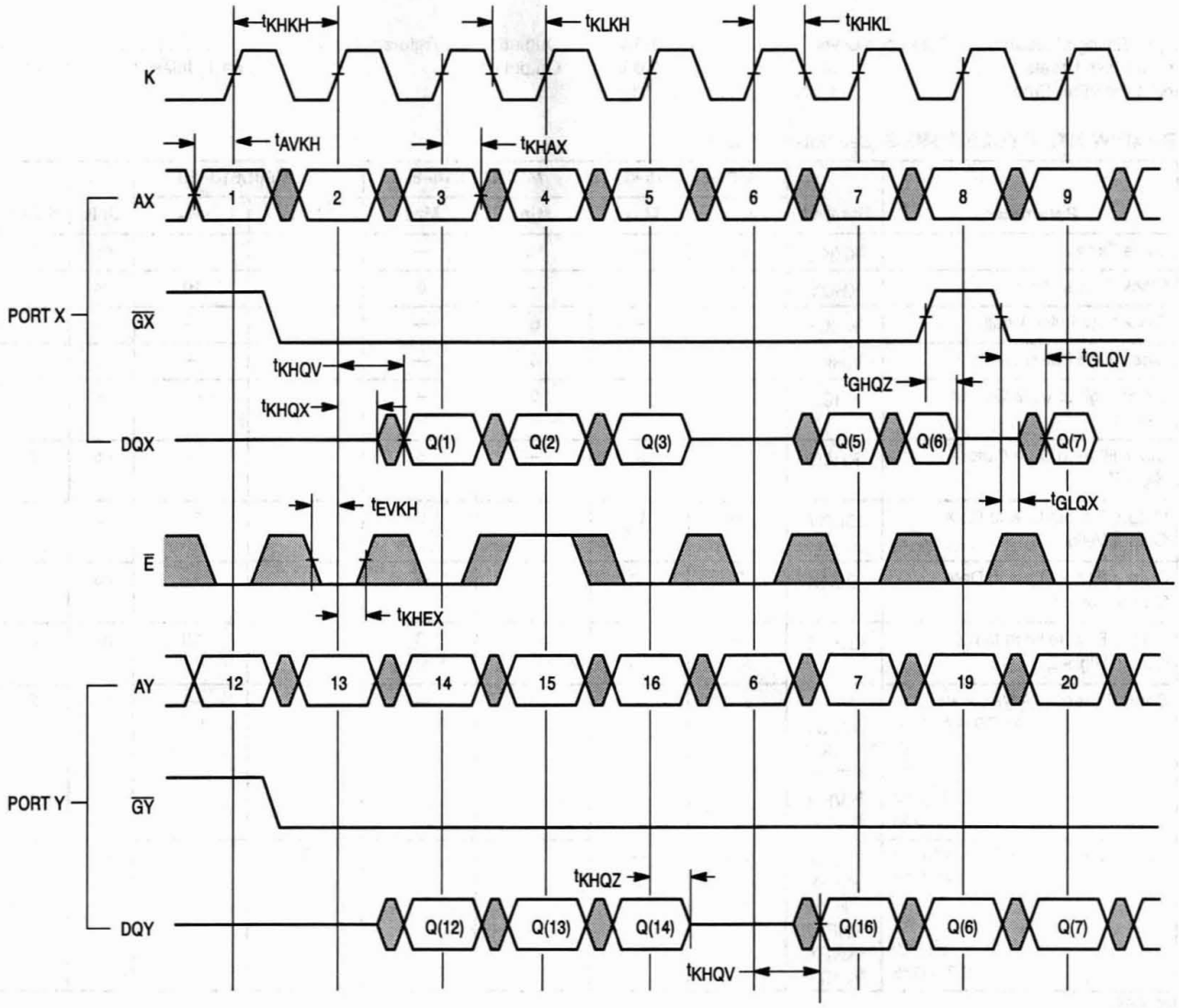


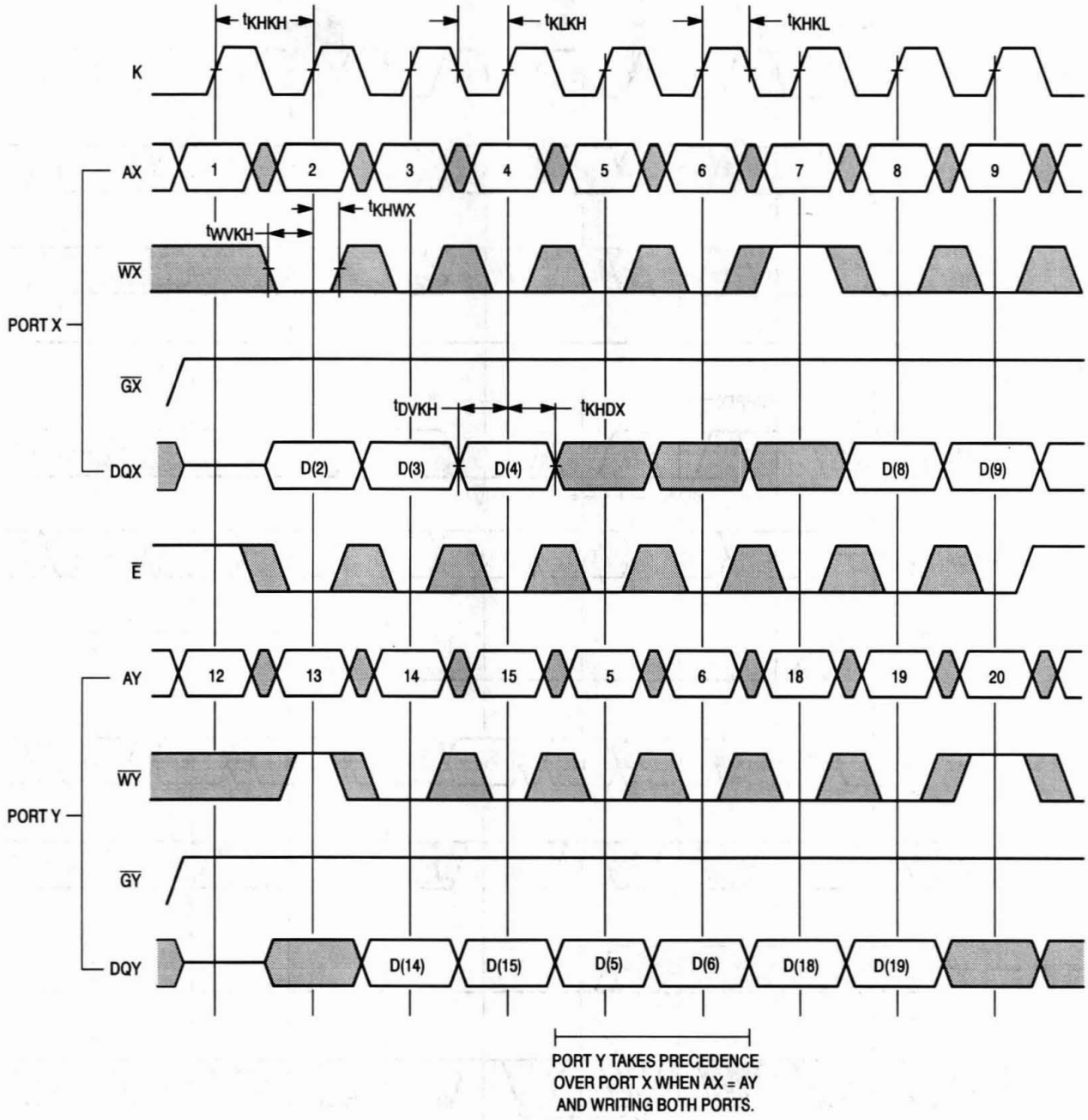
Figure 1. AC Test Load

READ CYCLE TIMING FROM BOTH PORTS ($\overline{WX}$, $\overline{WY}$, $\overline{PTX}$, $\overline{PTY}$ High)



$\overline{E}$ Low = $\overline{E1}$ Low and E2 High. $\overline{E}$ High = $\overline{E1}$ High or E2 Low.

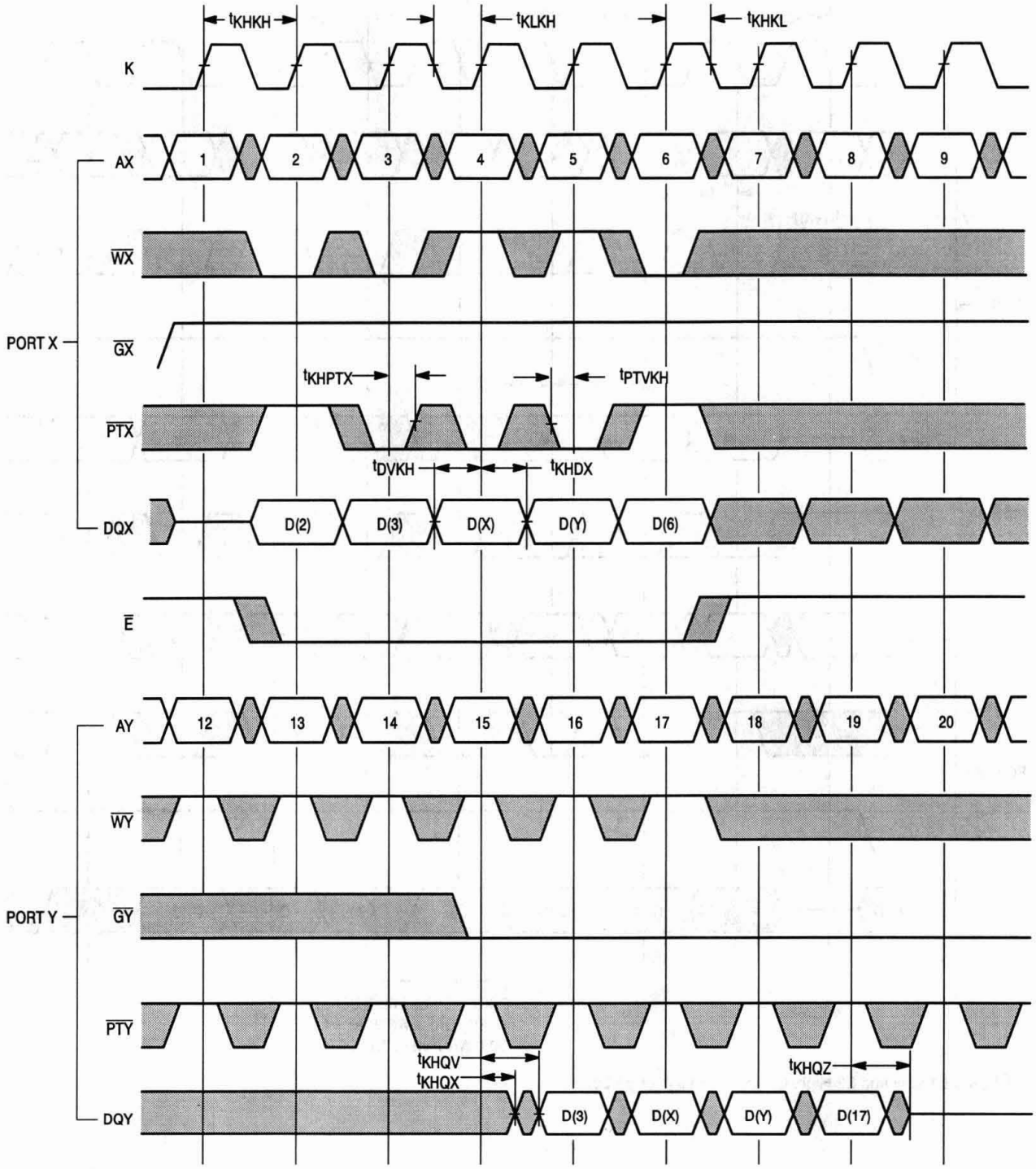
WRITE CYCLE TIMING TO BOTH PORTS ($\overline{PTX}$, $\overline{PTY}$ High)



$\overline{E}$ Low = $\overline{E1}$ Low and E2 High. $\overline{E}$ High = $\overline{E1}$ High or E2 Low.

5

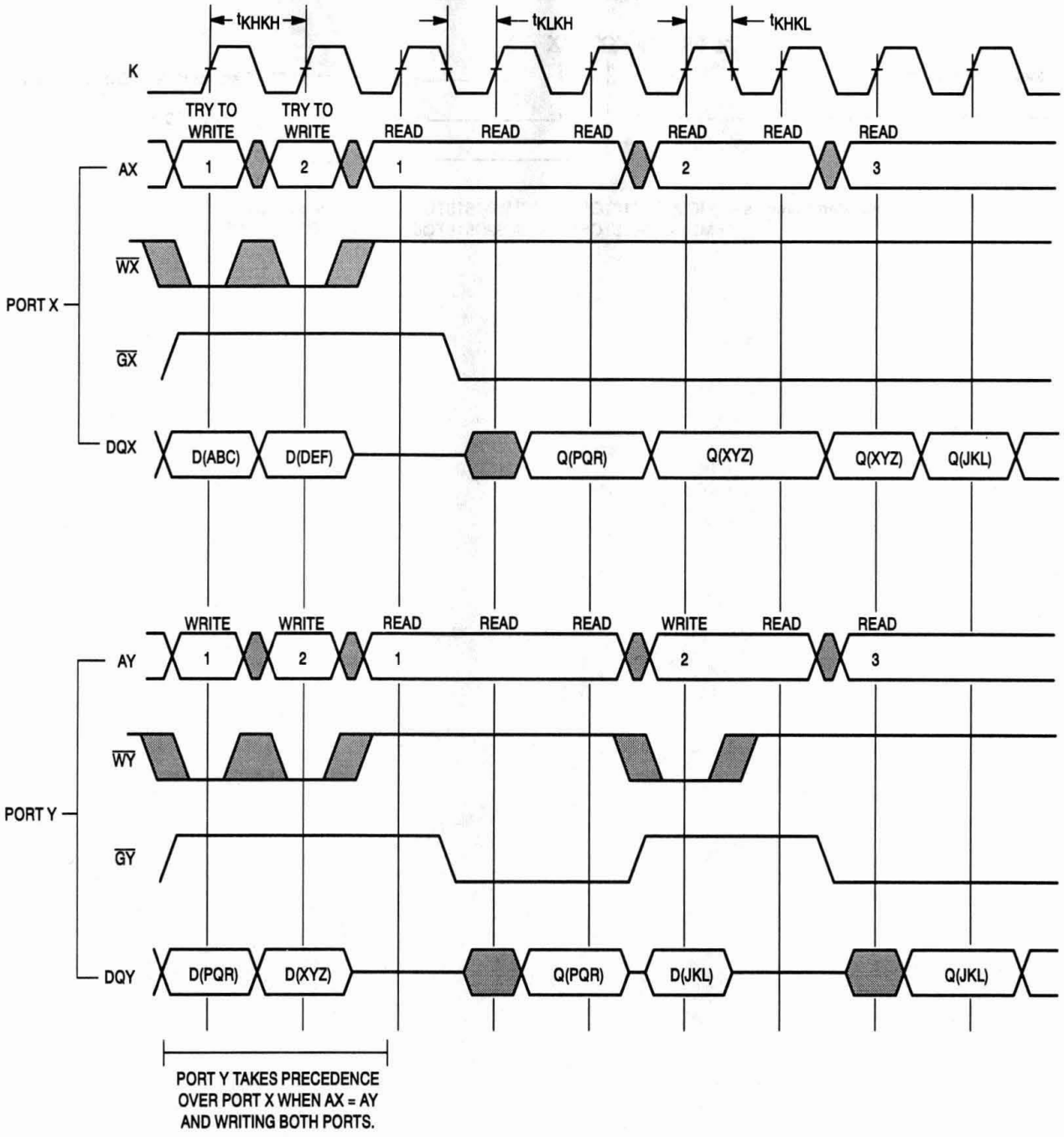
WRITE TO PORT X AND PASS THROUGH TO PORT Y (Note 1)



E Low = E1 Low and E2 High. E High = E1 High or E2 Low.

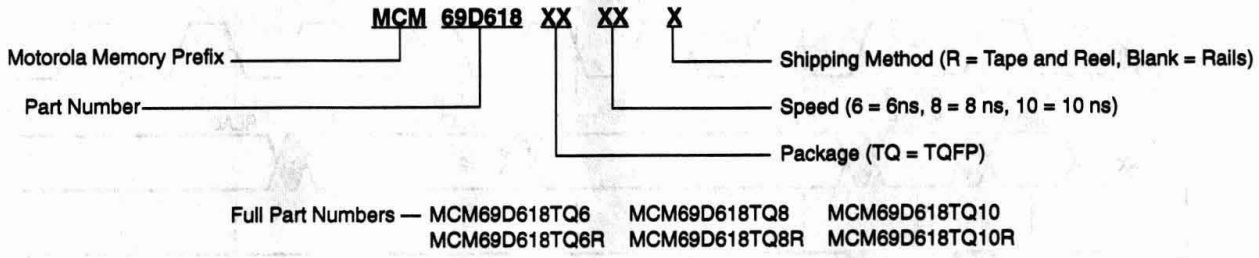
NOTE 1: The timing diagram is valid for the opposite case as well, i.e. writing to Port Y and passing through to Port X.

COMBINATION READ/WRITE WITH SAME ADDRESS ON EACH PORT



$\overline{PTX}$ = $\overline{PTY}$ = High
D(Value) = Value is the input to the data port
Q(Value) = Value is the output from the data port

ORDERING INFORMATION
(Order by Full Part Number)

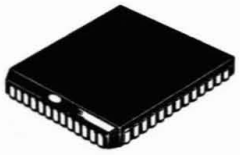

MCM 69D618 XX XX X
Motorola Memory Prefix
Part Number
Shipping Method (R = Tape and Reel, Blank = Rails)
Speed (6 = 6ns, 8 = 8 ns, 10 = 10 ns)
Package (TQ = TQFP)

Full Part Numbers — MCM69D618TQ6 MCM69D618TQ8 MCM69D618TQ10
MCM69D618TQ6R MCM69D618TQ8R MCM69D618TQ10R

5

MCM62990A

16K x 16 Bit Synchronous Fast Static RAM



FN PACKAGE
PLASTIC
CASE 778–02

The MCM62990A is a 262,144 bit synchronous static random access memory organized as 16,384 words of 16 bits. The device integrates a 16K x 16 SRAM core with advanced peripheral circuitry. Inputs to the device fall into two categories: synchronous and asynchronous. All synchronous inputs pass through positive–edge–triggered registers controlled by a single clock input (K). The synchronous inputs include all addresses, the two chip enables (SE and $\overline{SE}$), and the synchronous write enable ($\overline{SW}$).

Asynchronous inputs include the asynchronous byte write strobes ($\overline{AWL}$ and $\overline{AWH}$), output enable ($\overline{G}$), data input (DQ0 – DQ15), and the data latch enable (DL). Input data can be asynchronously latched by DL to provide simplified data–in timings during write cycles.

Address and write control are registered on–chip which greatly simplifies write cycles. Dual write strobes ($\overline{AWL}$ and $\overline{AWH}$) are provided to allow individually writeable bytes. $\overline{AWL}$ controls DQ0 – DQ7, the lower bits while $\overline{AWH}$ controls DQ8 – DQ15, the upper bits. In addition, the AWs allow late write cycles to be aborted if they are "false" during the low period of the clock. Dual chip enables (SE and $\overline{SE}$) are provided, allowing address decoding to be accomplished on–chip when the device is used in a dual bank mode.

An input data latch is provided. When data latch enable (DL) is high, the data latch is in the transparent state. When DL is low, the data latch is in the latched state. This data input latch simplifies write cycles by guaranteeing data hold time in a simple fashion.

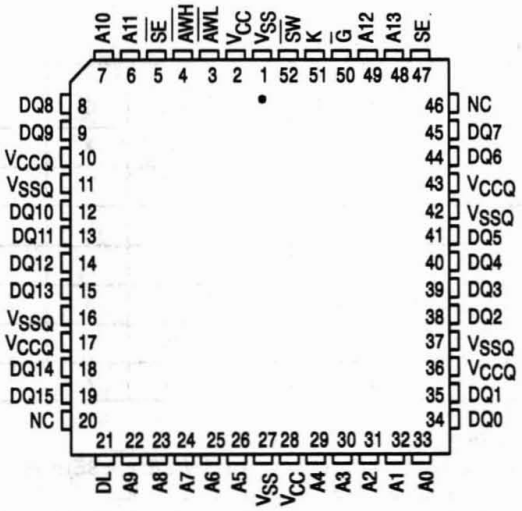
Additional power supply pins have been utilized and placed on the package for maximum performance. In addition, one set of power pins is electrically isolated from the other two and supplies power only to the output buffers. This allows connecting the output buffers to 3.3 V instead of 5.0 V if desired. If 3.3 V output levels are chosen, the output buffer impedance in the "high" state is approximately equal to the impedance in the "low" state which allows simple yet effective transmission line terminations to be achieved.

The MCM62990A will be available in a 52 pin plastic leaded chip carrier (PLCC).

Typical applications for this device are cache memory and tag RAMs, memory in systems which are pipelined and systems which require wide data bus widths and reduced parts count.

- Single 5 V ± 10% Power Supply
- Choice of 5 V or 3.3 V Power Supplies for Output Buffers
- Fast Access Times: 12/15/20/25 ns Max
- Byte Writeable via Dual Write Strobes with Abort Write Capability
- Separate Data Input Latch for Simplified Write Cycles
- Clock Controlled Registered Address, Write Control, and Dual Chip Enables
- Common Data Inputs and Data Outputs
- Output Enable Controlled Three–State Outputs
- High Output Drive Capability: 85 pF/Output at Rated Access Time
- High Board Density 52 Lead PLCC Package

PIN ASSIGNMENT



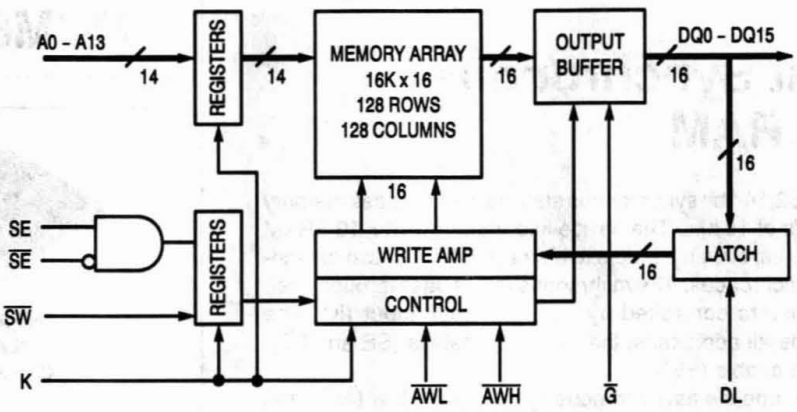
PIN NAMES	
A0 – A13	Address Inputs
K	Clock Input
DL	Data Latch Enable
$\overline{SW}$	Synchronous Write Enable
$\overline{AWL}$	Lower Byte Async Write Strobe
$\overline{AWH}$	Upper Byte Async Write Strobe
SE	Synchronous Chip Enable
$\overline{SE}$	Synchronous Chip Enable
$\overline{G}$	Asynchronous Output Enable
DQ0 – DQ15	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SSQ}	Output Buffer Ground
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

5

REV 2
11/7/96

BLOCK DIAGRAM



TRUTH TABLE (See Notes)

SEs	$\overline{SW}$	$\overline{AWL}$	$\overline{AWH}$	DL	$\overline{G}$	Mode	Supply Current	I/O Status
F	X	X	X	X	X	Deselected Cycle	I_{SB}	High–Z
T	H	X	X	X	H	Read Cycle	I_{CC}	High–Z
T	H	X	X	X	L	Read Cycle	I_{CC}	Data Out
T	L	L	L	H	X	Write Cycle All Bits Transparent Data In	I_{CC}	High–Z
T	L	H	H	X	X	Aborted Write Cycle	I_{CC}	High–Z
T	L	L	H	H	X	Write Cycle Lower 8 Bits Transparent Data In	I_{CC}	High–Z
T	L	H	L	L	X	Write Cycle Upper 8 Bits Latched Data In	I_{CC}	High–Z

NOTES:
1. True (T) is SE = 1 and $\overline{SE}$ = 0.
2. Registered inputs (Addresses, $\overline{SW}$, SE, and $\overline{SE}$) satisfy the specified setup and hold times about the rising edge of clock (K). Data–in satisfies the specified setup and hold times for DL.
3. A transparent write cycle is defined by DL high during the write cycle.
4. A latched write cycle is defined by DL transitioning low during the write cycle and satisfying the specified setup and hold times.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC} and V_{CCQ}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = V_{CCQ} = 5.0$ V ± 10%, $T_A = 0$ to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}**	4.5	5.0	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible) (V_{CCQ} must be ≤ V_{CC} at all times, including power up.)	V_{CCQ}	4.5 3.0	5.0 3.3	5.5 3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)
** V_{CC} must be ≥ V_{CCQ} at all times, including power up.

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, $V_{in} = 0$ to V_{CC})	$I_{lkg(I)}$	—	—	± 1.0	µA
Output Leakage Current ($\overline{G} = V_{IH}$)	$I_{lkg(O)}$	—	—	± 1.0	µA
AC Supply Current ($\overline{G} = V_{IH}$, $I_{out} = 0$ mA, All Inputs = V_{IL} or V_{IH}, $V_{IL} = 0$ V and $V_{IH} \geq 3.0$ V, Cycle Time ≥ t_{KHKH} min)	I_{CCA12} I_{CCA15} I_{CCA20} I_{CCA25}	— — — —	295 275 265 255	350 330 320 310	mA
Standby Current ($\overline{E} = V_{IH}$, $E = V_{IL}$, $I_{out} = 0$ mA, All Inputs = V_{IL} or V_{IH}, $V_{IL} = 0$ V and $V_{IH} \geq 3.0$ V, Cycle Time ≥ t_{KHKH} min)	I_{SB}	—	40	50	mA
Output Low Voltage ($I_{OL} = + 8.0$ mA)	V_{OL}	—	—	0.4	V
Output High Voltage ($I_{OH} = – 4.0$ mA)	V_{OH}	2.4	—	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, $T_A = 25$°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ15)	C_{in}	4	6	pF
Input/Output Capacitance (DQ0 – DQ15)	C_{out}	8	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 3.3 V or 5.0 V ± 10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1a Unless Otherwise Noted

READ AND WRITE CYCLE TIMING (See Notes 2 and 3)

Parameter	Symbol	62990A–12		62990A–15		62990A–20		62990A–25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Times Clock High to Clock High	t_{KHKH}	15	—	15	—	20	—	25	—	ns	
Access Times										ns	4
Clock High to Output Valid	t_{KHQV}	—	12	—	15	—	20	—	25		
Output Enable Low to Output Valid	t_{GLQV}	—	5	—	6	—	8	—	10		
Aborted Write Cycles										ns	
Clock Low to Asynchronous Write Strobes ($\overline{AWL}$, $\overline{AWH}$) High	t_{KLAWxH}	—	0	—	0	—	0	—	0		
Clock High to $\overline{AWx}$ Invalid	t_{KHAWxL}	2	—	2	—	2	—	2	—		
Output Buffer Control										ns	
Asynchronous Output Enable ($\overline{G}$) High to Output High Z	t_{GHQZ}	2	5	2	5	2	5	2	5		1
$\overline{G}$ Low to Output Low Z	t_{GLQX}	2	—	2	—	2	—	2	—		1
Reads:											
Clock (K) High to Output Low Z After Deselect or Write	t_{KHQX1}	8	—	8	—	8	—	8	—		1
Data Out Hold After Clock High	t_{KHQX2}	5	—	5	—	5	—	5	—		5
Writes:											
K High to Output High Z After Read	t_{KHQZ}	3	10	3	10	3	10	3	10		1
Clock										ns	
Clock High Time	t_{KHKL}	4	—	4	—	4	—	4	—		
Clock Low Time	t_{KLKH}	7	—	8	—	10	—	10	—		
Setup Times										ns	
Address Valid to Clock High	t_{AVKH}	3	—	3	—	3	—	3	—		5
Synchronous Write ($\overline{SW}$) Valid to Clock High	t_{SWVKH}	3	—	3	—	3	—	3	—		5
Synchronous Enables (SE, $\overline{SE}$) Valid to Clock High	t_{SEVKH}	3	—	3	—	3	—	3	—		5
Writes:											
Data–In Valid to Clock High	t_{DVKH}	5	—	6	—	6	—	7	—		2, 5
$\overline{AWL}$, $\overline{AWH}$ Low to Clock High	t_{AWxLKH}	6	—	6	—	6	—	7	—		5
Data Latch:											
Data–In Valid to DL Low	t_{DVDLL}	2	—	2	—	2	—	2	—		3, 5
Hold Times										ns	
Clock High to Address Invalid	t_{KHAX}	2	—	2	—	2	—	2	—		5
Clock High to $\overline{SW}$ Invalid	t_{KHSWX}	3	—	3	—	3	—	3	—		5
Clock High to SE, $\overline{SE}$ Invalid	t_{KHSEX}	3	—	3	—	3	—	3	—		5
Writes:											
Clock High to Data–In Invalid	t_{KHDX}	2	—	2	—	2	—	2	—		2, 5
Clock High to $\overline{AWL}$, $\overline{AWH}$ High	t_{KHAWxH}	2	—	2	—	2	—	2	—		5
Clock High to DL High	t_{KHDLH}	2	—	2	—	2	—	2	—		3, 5
Data Latch:											
DL Low to Data–In Invalid	t_{DLLDX}	2	—	2	—	2	—	2	—		3, 5
DL High to Clock High	t_{DLHKH}	5	—	6	—	6	—	7	—		3, 5

NOTES:
1. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} is less than t_{KHQX} and t_{GHQZ} is less than t_{GLQX} for a given device.
2. A transparent write cycle is defined by DL high during the write cycle.
3. A latched write cycle is defined by DL transitioning low during the write cycle and satisfying the specified hold time for the rising edge of clock (K).
4. Into rated load of 85 pF equivalent resistive load (see Figure 1a).
5. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for all rising edges of clock (K) or falling edges of data latch enable (DL).

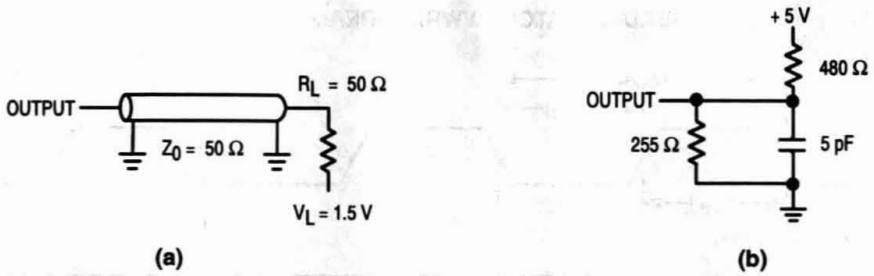
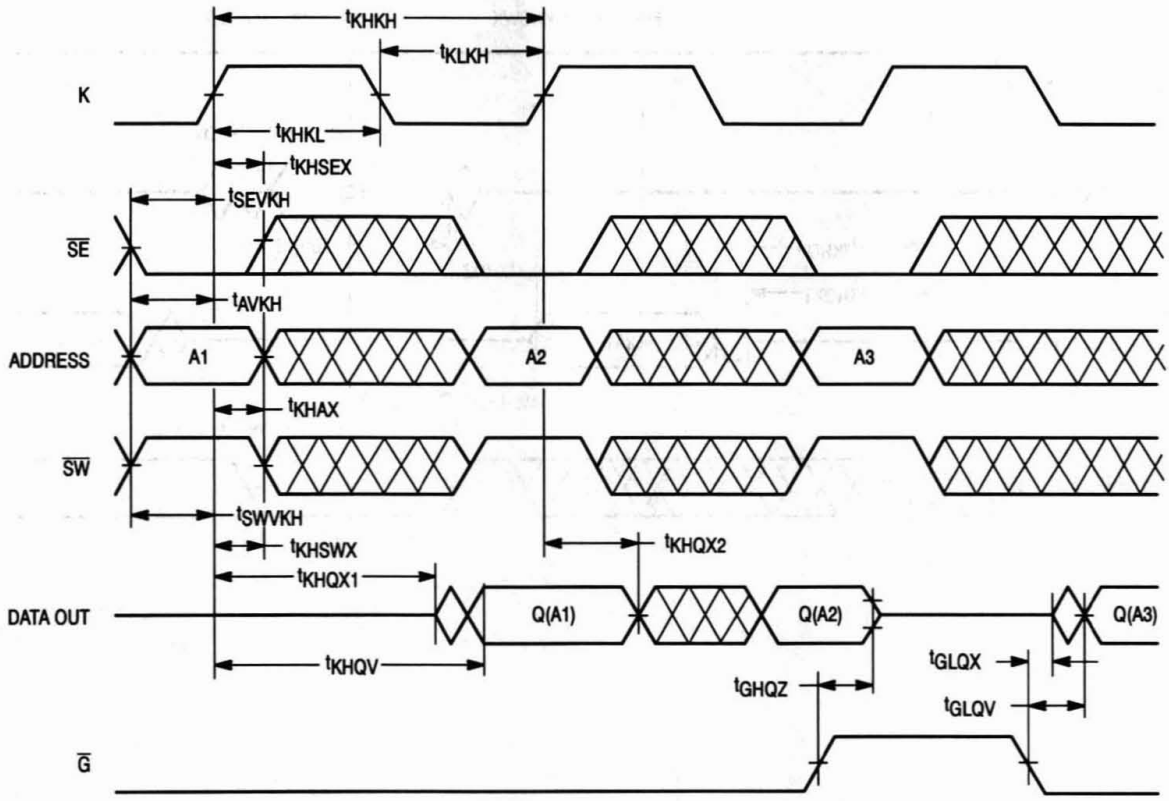


Figure 1. Test Loads

READ CYCLES



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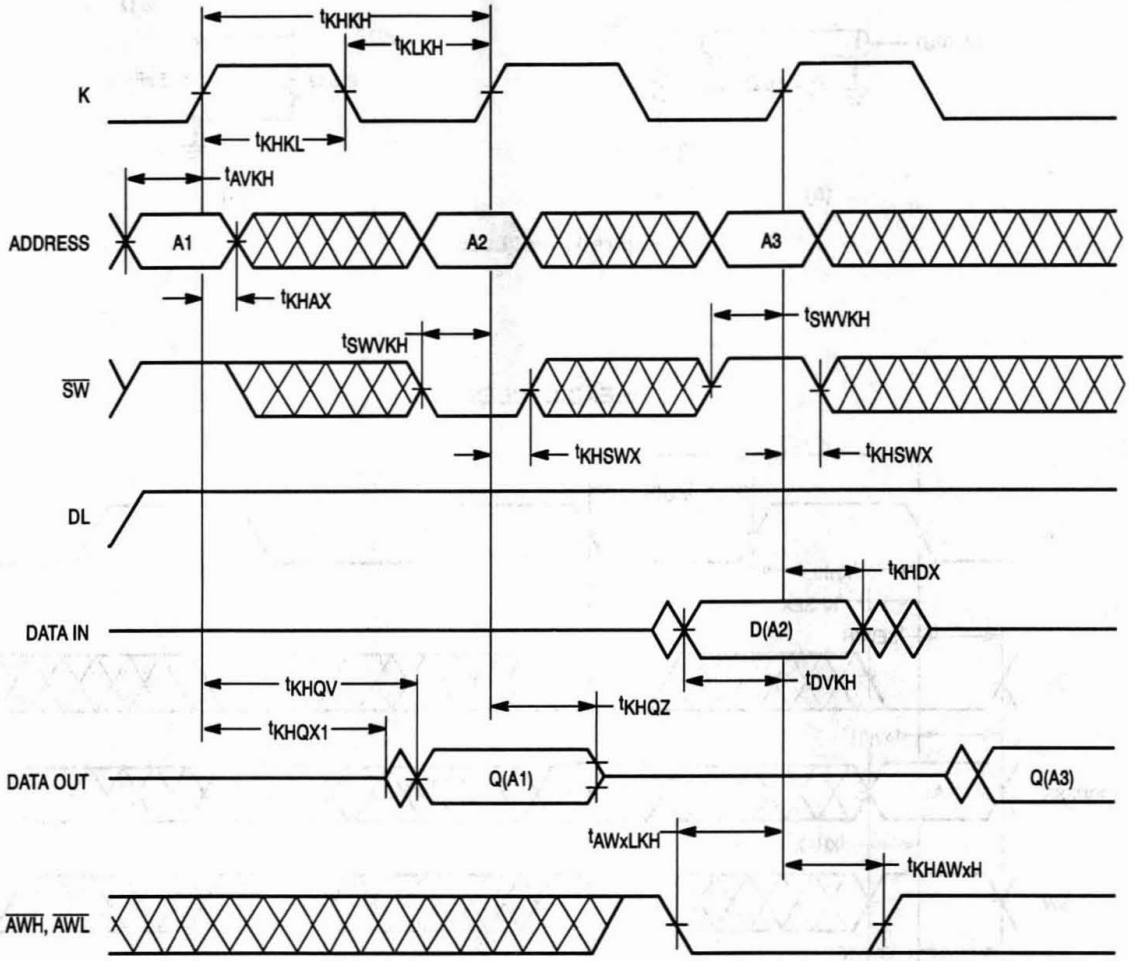
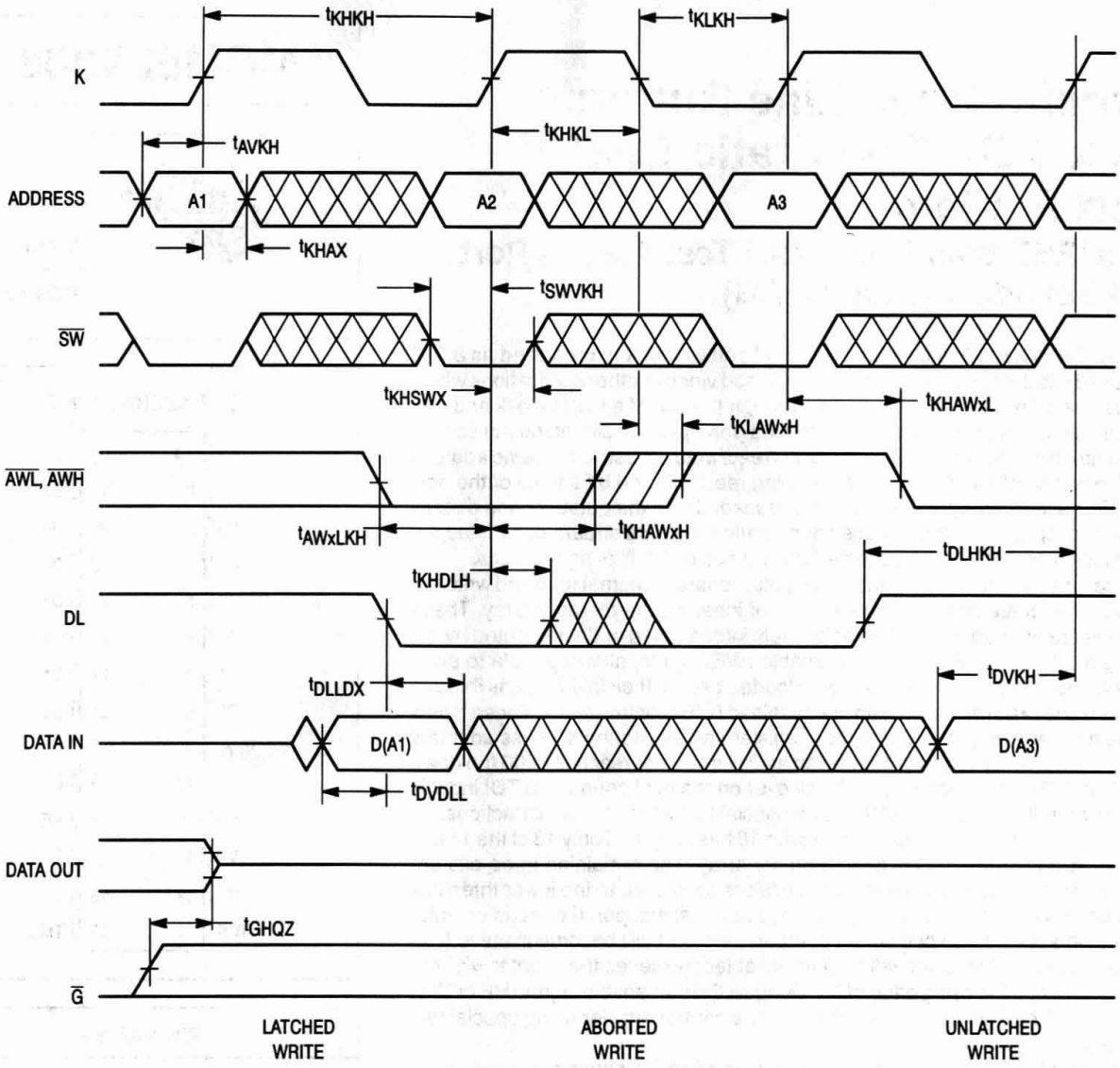
READ–UNLATCHED WRITE–READ CYCLES



WRITE CYCLES



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ORDERING INFORMATION
(Order by Full Part Number)

MCM 62990A FN XX

- Motorola Memory Prefix
- Part Number
- Speed (12 = 12 ns, 15 = 15 ns, 20 = 20 ns 25 = 25 ns)
- Package (FN = PLCC)

Full Part Numbers — MCM62990AFN12 MCM62990AFN15 MCM62990AFN20 MCM62990AFN25

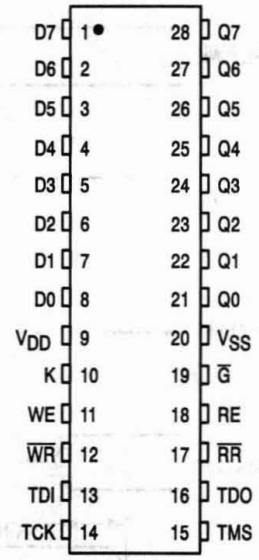
MCM62X308

Synchronous Line Buffer: 8K x 8 Bit Fast Static Dual Ported Memory

With IEEE Standard 1149.1 Test Access Port and Boundary–Scan (JTAG)

J PACKAGE
300 MIL SOJ
CASE 810B–03

PIN ASSIGNMENT



The MCM62X308 is a synchronous, dual ported memory organized as 8,192 words of 8 bits each. It is intended for high speed video or other applications which process data on a line–by–line basis. Through the use of a single clock and port control inputs, separate read and write data ports provide simultaneous access to a common memory array. Simultaneous read/write access to the same address location is also allowed, with old data being read followed by a write of the new data. This allows multiple devices to be cascaded with the output of one directly driving the input of another. In this configuration the data stream can be tapped at strategic interconnect points to perform various digital filtering functions.

Since there are no external address inputs, separate internal read and write address counters are provided as a means of indexing the memory array. These counters are preloaded and then selectively incremented or decremented by asserting read enable (RE) and write enable (WE) inputs, allowing cycle to cycle control. The address counters can be reloaded back to their initial values through the use of the read reload ($\overline{RR}$) and write reload ($\overline{WR}$) control inputs. These inputs initiate the transfer of address reload register values into the address counters which index the memory array. When an address counter reaches 0000 (on down count) or FFFF (on up count), it will roll over on the next count. The TDI input is used to write the reload registers using special test access port instructions.

The read and write address counters are 16 bits long, and only 13 of the 16 bits are required to index the 8K deep memory array. The remaining three bits are used for depth expansion. These three bits are compared to the lower three bits in the control register, and as long as they are equal that port (i.e., read or write) will remain active. If the bits do not compare, the port will become inactive (i.e., for read outputs, high–z; for write inputs, disabled) however, the counter will continue to count on the rising edge of K as long as the port enable signal (RE or WE) is asserted. The TDI input is used to write the control register using special test access port instructions.

The output enable Input can be programmed to be either synchronous or asynchronous through the control register.

The MCM62X308 is available in a 28 pin SOJ package.

- 8K x 8 Fast Access Static Memory Array
- Single 5 V Power Supply — MCM62X308–15–5: ± 5%
  MCM62X308–17: ± 10%
- Synchronous, Simultaneous Read/Write Memory Access
- 50 MHz Maximum Clock Cycle Time, < 15 ns Read Access
- Single Clock Operation
- Separate Read/Write Address Counters with Reload Control
- Separate Up/Down Counter Control for Both Read and Write
- Programmable Output Enable Control (Synchronous or Asynchronous)
- Cascadable I/O Interface
- IEEE Standard 1149.1 Test Port (JTAG)
- Expand ID Register for Depth Expansion
- High Board Density SOJ Package
- Fully TTL Compatible

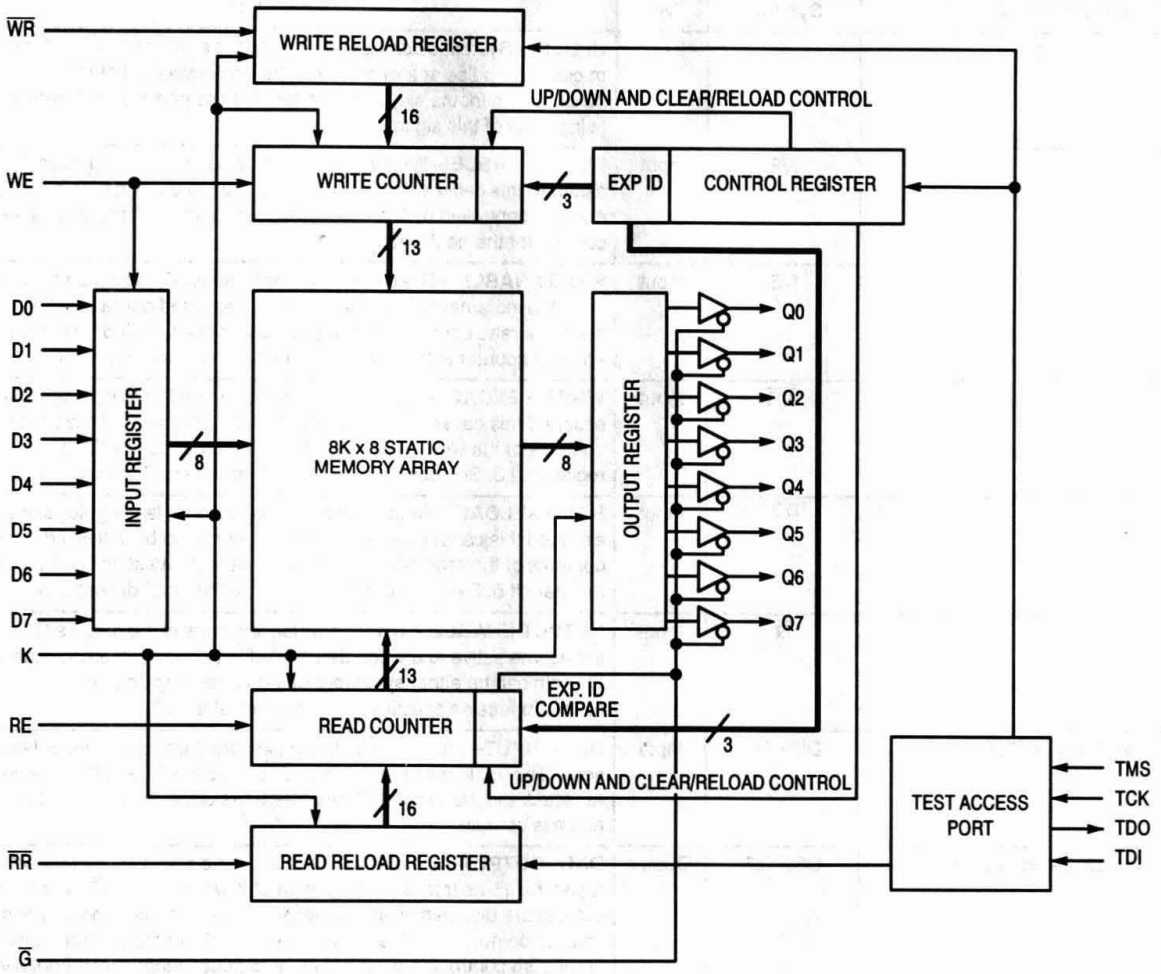
PIN NAMES

K	Clock Input
WE	Write Enable Input
$\overline{WR}$	Write Address Reload Input
RE	Read Enable Input
$\overline{RR}$	Read Address Reload Input
$\overline{G}$	Output Enable Input
D0 – D7	Data Inputs
Q0 – Q7	Data Outputs
TCK	Test Clock Input
TMS	Test Mode Select
TDI	Test Data Input
TDO	Test Data Output
V_{DD}	+ 5 V Power Supply
V_{SS}	Ground

5

REV 2
1/22/97

BLOCK DIAGRAM



TRUTH TABLE (X = Don't Care)

WE	$\overline{WR}$	RE	$\overline{RR}$	$\overline{G}$	Match EXP ID (Read/Write)	Mode (Read/Write)	Supply Current	Q0 – 7 Status
X	L	X	L	L	Match Read/Match Write	Reload, Read/Reload, Write Disable	I_{CC}	Data Out
H	H	H	H	L	Match Read/Match Write	Count, Read/Write, Count	I_{CC}	Data Out
L	H	L	H	L	Match Read/Match Write	Read Count Disable/Write Disable	I_{CC}	Data Out
H	H	H	H	H	Match Read/Match Write	Count, Read/Write, Count	I_{CC}	High–Z
H	H	H	H	X	No Match Read/No Match Write	Count, No Read/No Write, Count	I_{SB}	High–Z
H	H	H	H	X	No Match Read/Match Write	Count, No Read/Write, Count	I_{SB}	High–Z
H	H	H	H	L	Match Read/No Match Write	Count, Read/No Write, Count	I_{CC}	Data Out

5

PIN DESCRIPTIONS

SOJ Pin Locations	Symbol	Type	Description
10	K	Input	**CLOCK** – System clock input pin accepting a minimum 8 ns clock high or clock low pulse at a minimum 20 ns clock cycle. All other synchronous inputs excluding the test access port are captured on the rising edge of this signal.
11	WE	Input	**WRITE ENABLE** – Write enable is captured on K leading edge. When asserted this causes the input data D0 – D7 to be written into the RAM address controlled by the write address counter and increments the counter for the next write.
18	RE	Input	**READ ENABLE** – Read enable is captured on K leading edge. When asserted increments the counter for the next read operation. This causes a read access from the RAM address controlled by the read address counter to be inserted in the output register Q0 – Q7.
12	$\overline{WR}$	Input	**WRITE RELOAD** – Write reload is captured on K leading edge. When asserted this causes the write address counter to be initialized to the contents of the write reload register or "cleared" as specified by control register bit 3. See control register bit 3 for "cleared" description.
17	$\overline{RR}$	Input	**READ RELOAD** – Read reload is captured on K leading edge. When asserted this causes the read address counter to be initialized to the contents of the read reload register or "cleared" as specified by control register bit 5. See control register bit 5 for "cleared" description.
19	$\overline{G}$	Input	**OUTPUT ENABLE** – When asserted low causes the outputs Q0 – Q7 to become active and when deasserted high causes them to High–Z. This pin can be either synchronous with K leading edge or asynchronous as specified by control register bit 7.
8, 7, 6, 5, 4, 3, 2, 1	D0 – D7	Input	**DATA INPUT**– The levels on these pins are captured on the K leading edge. The value captured will be written into the RAM if WE is also asserted and the expand ID bits match the upper three bits of the write address counter.
21, 22, 23, 24, 25, 26, 27, 28	Q0 – Q7	Output	**DATA OUTPUT** – Data outputs are available from the read output register < 15 ns from the rising edge of K when RE or $\overline{RR}$ is asserted. outputs are disabled when the upper three bits of the read address counter do not match the three expand ID bits of the control register. $\overline{G}$ will also control the disabling of the outputs either synchronously or asynchronously. See $\overline{G}$ description.

5

TEST ACCESS PORT PIN DESCRIPTIONS (The Test Access Port Conforms with the IEEE Standard 1149.1. It is also Used to Load Device Specific Registers Used to Configure the MCM62X308.)

SOJ Pin Locations	Symbol	Type	Description
14	TCK	Input	**TEST CLOCK** – Samples and clocks all TAP events. All inputs are captured on TCK rising edge and all outputs propagate from TCK falling edge. It also can take the place of K in device operation in certain test conditions.
15	TMS	Input	**TEST MODE SELECT** – Sampled on the rising edge of TCK. Determines the movement through the TAP state machine (Figure 2). This circuit is designed in such a way that an undriven input will produce a response identical to the application of a logic 1.
13	TDI	Input	**TEST DATA IN** – Sampled on the rising edge of TCK. This is the input side of the serial register placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP state machine and what instruction is active in the TAP instruction register. This circuit is designed in such a way that an undriven input will produce a response identical to the application of a logic 1.
16	TDO	Output	**TEST DATA OUT** – Output that is active depending on the state of the TAP state machine. Output changes off the trailing edge of TCK. This is the output side of the serial register placed between TDI and TDO.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS} = 0)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISITICS

(T_A = 0 to 70 °C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter		Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	MCM62X308–15–5	V_{DD}	4.75	5.0	5.25	V
	MCM62X308–17		4.50	5.0	5.50	
Input High Voltage		V_{IH}	2.2	—	V_{DD} + 0.3	V
Input Low Voltage		V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{DD})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH}, V_{out} = 0 to V_{DD})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, I_{out} = 0 mA, All Inputs ≥ V_{IL} = 0.0 V and V_{IH} ≥ 3.0, Cycle Time = 20 ns)	I_{CCA}	—	120	mA
AC Standby Current (When Expand ID Bits Do Not Match the Read Address Counter, Cycle Time = 20 ns)	I_{SB}	—	100	mA
Output Low Voltage (I_{OL} = + 4.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance (Q0 – Q7, TDO)	C_{out}	6	8	pF

5

AC OPERATING CONDITIONS AND CHARACTERISTICS

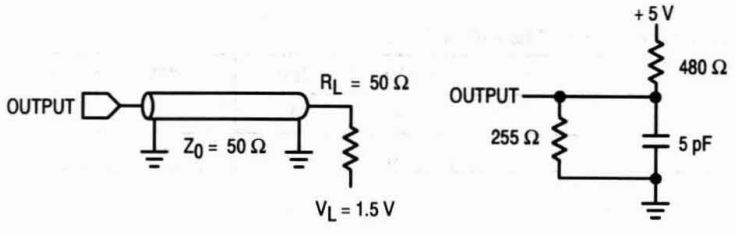
(T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V
Output Load ..... Terminated 50 Ohm Transmission Line

READ/WRITE CYCLE TIMING

Parameter		Symbol	MCM62X308–15–5 Min	MCM62X308–15–5 Max	MCM62X308–17 Min	MCM62X308–17 Max	Unit	Notes
Cycle Time		t_{KHKH}	20	—	22	—	ns	
Clock High Time		t_{KHKL}	8	—	9	—	ns	
Clock Low Time		t_{KLKH}	8	—	9	—	ns	
Clock High to Output Valid		t_{KHQV}	5	15	5	17	ns	
Clock High to Output High–Z		t_{KHQZ}	5	15	5	15	ns	1
Output Enable Low to Output Valid		t_{GLQV}	3	10	3	10	ns	2, 4
Output Enable High to Output High–Z		t_{GHQZ}	0	5	0	5	ns	2, 3, 4
Setup Times:	RE	t_{REVKH}	2	—	2	—	ns	5
	WE	t_{WEVKH}						
	$\overline{WR}$	t_{WRVKH}						
	$\overline{G}$	t_{GVKH}						6
	$\overline{RR}$	t_{RRVKH}	3	—	3	—		5
	Data In	t_{DVKH}	1	—	1	—		5
Hold Times:	RE	t_{KHREX}	2	—	2	—	ns	5
	WE	t_{KHWEX}						
	$\overline{RR}$	t_{KHRRX}						
	$\overline{WR}$	t_{KHWRX}						
	$\overline{G}$	t_{KHGX}						6
	Data In	t_{KHDX}						

NOTES:
1. The outputs High–Z from a clock high edge when the upper three bits of the Read Address Counter do not match the 3 ID Expansion bits.
2. $\overline{G}$ is a don't care when the three ID expansion bits do not match the upper three bits of the Read Address Counter.
3. t_{GLQV} and t_{GHQZ} only apply when $\overline{G}$ is programmed as Asynchronous. (See TAP LDCONT instruction).
4. Transition is measured ± 500 mV from steady–state voltage. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{GHQZ} max is less than t_{GLQV} min for a given device and from device to device.
5. This is a synchronous device. All inputs must meet the specified setup and hold times for ***ALL*** rising edges of Clock except for $\overline{G}$ when it is programmed to be asynchronous.
6. t_{GVKH} and t_{KHGX} only apply when $\overline{G}$ is programmed as synchronous.



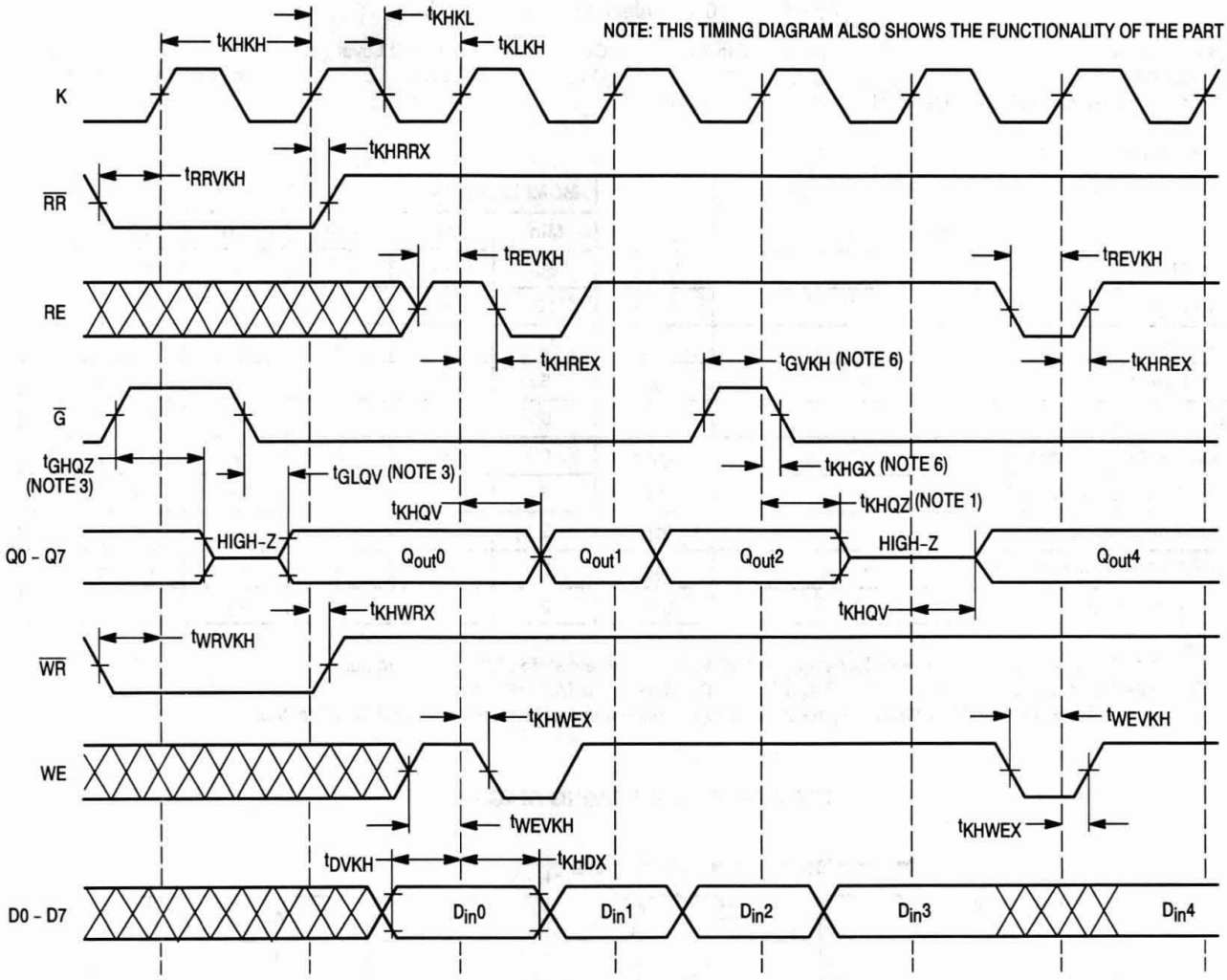
(a) (b)

Figure 1. Test Loads

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ/WRITE CYCLE TIMING DIAGRAM



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AC OPERATING CONDITIONS AND CHARACTERISTICS FOR THE TEST ACCESS PORT (IEEE 1149.1)

(T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V
Output Load ..... 50 Ohm Transmission Line

TAP CONTROLLER TIMING

Parameter	Symbol	MCM62X308–15–5		MCM62X308–17		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{CYC}	30	—	30	—	ns	
Clock High Time	t_{CKH}	12	—	12	—	ns	
Clock Low Time	t_{CKL}	12	—	12	—	ns	
Clock Low to Output Valid	t_A	5	9	5	9	ns	
Clock Low to Output High–Z	t_{CKZ}	0	9	0	9	ns	1
Clock Low to Output Active	t_{CKX}	0	9	0	9	ns	2, 3
Setup Time, Test Mode Select	t_S	2	—	2	—	ns	
Setup Time, Test Data In	t_{SD}	2	—	2	—	ns	
Hold Time, Test Mode Select	t_H	2	—	2	—	ns	
Hold Time, Test Data In	t_{HD}	2	—	2	—	ns	

NOTES:
1. Test Data Out will High–Z from a clock low edge depending on the current state of the TAP state machine.
2. Test Data Out is active only in the SHIFT–IR and SHIFT–DR state of the TAP state machine.
3. Transition is measured ± 500 mV from steady–state voltage. This parameter is sampled and not 100% tested.

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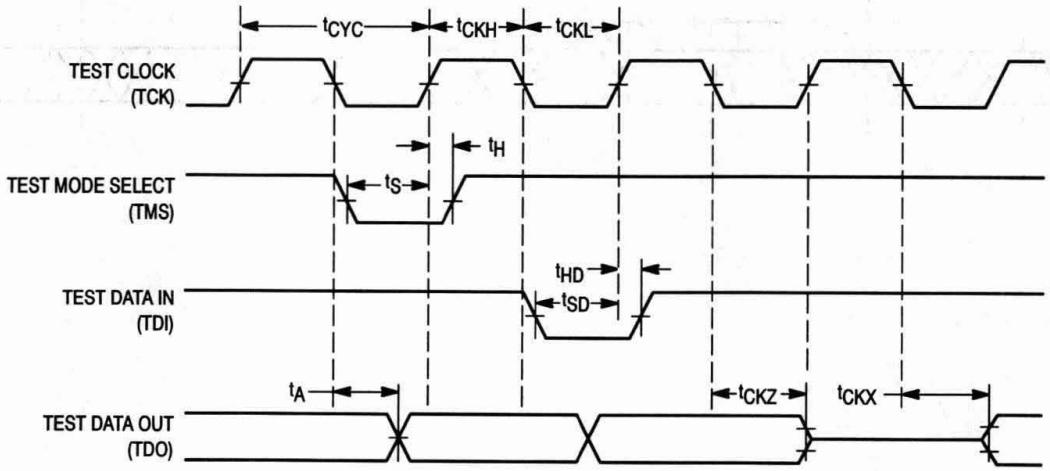
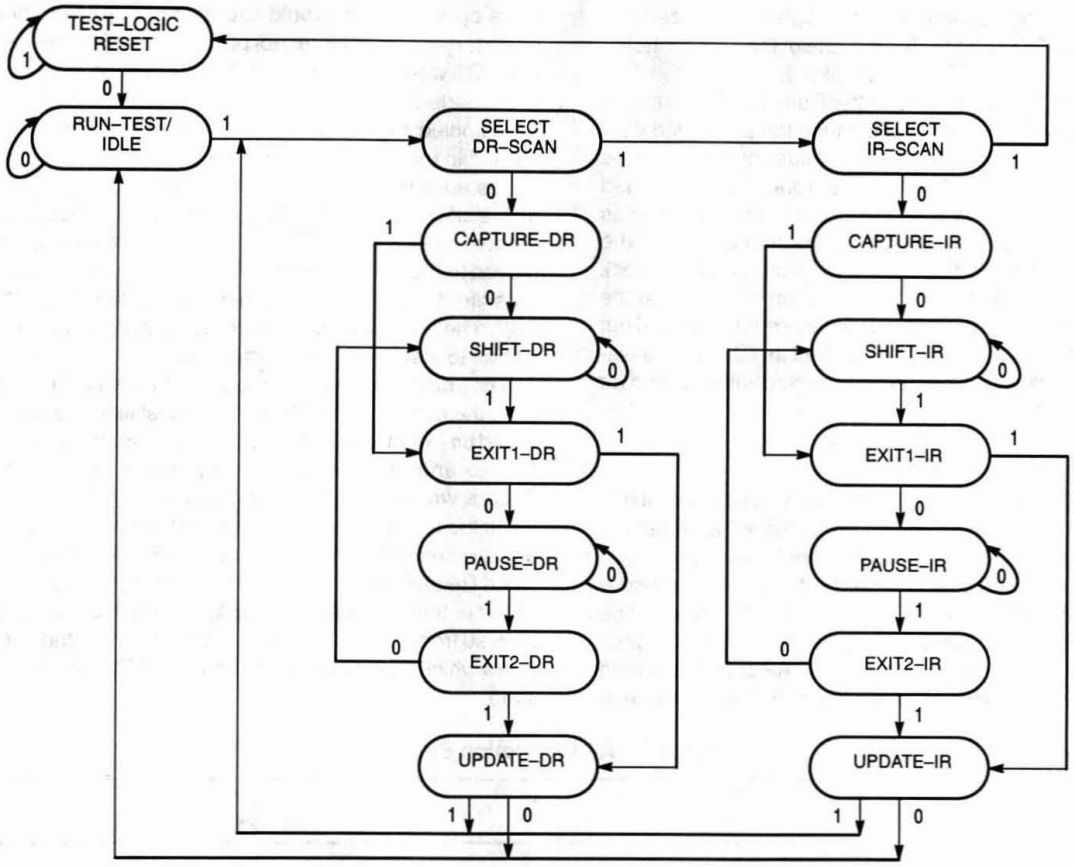
TAP CONTROLLER TIMING DIAGRAM





NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 2. TAP Controller State Diagram

5

TEST ACCESS PORT DESCRIPTIONS

INSTRUCTION SET

A four pin IEEE Standard 1149.1 Test Port (JTAG) is included on this device. There are two classes of instructions; standard instructions as defined in the IEEE 1149.1 standard and device specific, or public, instructions that are used to control the functionality of the device. When the TAP (Test Access Port) controller is in the Shift–IR state the Instruction Register is placed between TDI and TDO. In this state the desired instruction would be serially loaded through the TDI input (while 0101 will be shifted out of TDO). The TAP instruction set for this device is listed in Table 1.

TAP STANDARD INSTRUCTION SET

NOTE: The descriptions in this section are not intended to be used without the supporting IEEE 1149.1–1993 Standard.

SAMPLE/PRELOAD TAP INSTRUCTION

The SAMPLE/PRELOAD TAP instuction is used to allow scanning of the boudary–scan register without causing interference to the normal operation of the chip logic. The 22 bit boundary scan register contains bits for all device signal and clock pins and associated control signals (Table 2). This register is accessible when the SAMPLE/PRELOAD TAP instruction is loaded into the TAP instruction register in the Shift–IR state. When the TAP controller is then moved to the Shift–DR state, the boundary scan register is placed between TDI and TDO. This scan register can then be used prior to the EXTEST instruction to preload the output pins with desired values so that these pins will drive the desired state when the EXTEST instruction is loaded. See the EXTEST instruction explanation below. It could also be used prior to the INTEST instruction to preload values into the input pins. As data is written into TDI, data also streams out of TDO which can be used to pre–sample the inputs and outputs. SAMPLE/PRELOAD would also be used prior to the CLAMP instruction to preload the values on the output pins that will be driven out when the CLAMP instruction is loaded.

Table 2 shows the boundary–scan bit definitions. The first column defines the bit's ordinal position in the boundary–scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 0; the last bit to be shifted is 21. The second column is the pin name and the third column is the pin type.

EXTEST TAP INSTRUCTION

The EXTEST instruction is intended to be used in conjunction with the SAMPLE/PRELOAD instruction to assist in testing board level connectivity. Normally, the SAMPLE/PRELOAD instruction would be used to preload all output pins (i.e., Q0 – Q7). The EXTEST instruction would then be loaded.

During EXTEST the boundary–scan register is placed between TDI and TDO in the Shift–DR state of the TAP controller (Table 2). Once the EXTEST instruction is loaded, the TAP controller would then be moved to the Run–Test/Idle state. In this state one cycle of TCK would cause the preloaded data on the ouput pins to be driven while the values on the input pins would be sampled (Q0 – Q7 will be active only if $\overline{G}$ is preloaded with a zero). Note that TCK, not the Clock pin, K, is used as the clock input while K is only sampled during EXTEST. The input pins are sampled in the Captor–DR state. After one clock cycle of TCK, the TAP controller would then be moved to the Shift–DR state where the sampled values would be shifted out of TDO (and new values would be shifted in TDI). These values would normally be compared to expected values to test for board connectivity.

THE INTEST TAP INSTRUCTION

The INTEST instruction is intended to be used to assist in testing internal device functionality. When the INTEST instruction is loaded the boundary–scan register is placed between TDI and TDO in the Shift–DR state of the TAP controller (Table 2). While in the Shift–DR state, all input pins would be preloaded via the boundary scan register to set up the desired mode (i.e., read, write, reload, etc.). The TAP controller would then be moved to the Run–Test/Idle state. In this state one or more cycles of TCK would cause the preloaded data in the boundary–scan register to be driven while the values of Q0 – Q7 would be sampled (Q0 – Q7 will be active only if $\overline{G}$ is preloaded with a zero, however the values of Q0 – Q7 will be sampled regardless of $\overline{G}$). Only one action will be performed in the Run–Test/Idle state no matter how many clock cycles are input. Note that TCK, not the Clock pin(K), is used as the clock input while K is ignored during INTEST. After one or more clock cycles of TCK, the TAP controller would then be moved to the Shift–DR state where the sampled values would be shifted out of TDO (and new values would be shifted in TDI). These values would normally be compared to expected values to test for device functionality.

Since device functionality can only be verified through sampling the outputs of the device, the most likely use of INTEST would be to first load up the boundary–scan register for a Write Reload and execute the reload in the Run–Test/Idle state. Then a write of the first address would be performed again using the boundary scan register to load up the input registers and executing the write in the Run–Test/Idle state. Lastly, a Read Reload would be executed in the same manner so that the data that had just been written in the first address would be read from the memory array and written into the output registers which would then be shifted out of TDO in the Shift–DR state.

Table 1. TAP Instruction Set

Instruction	Code (Binary)	Description
Standard Instructions:		
BYPASS	1111*	Bypass Instruction
INTEST	0111	Intest Instruction
SAMPLE/PRELOAD	1100	Sample and/or Preload Instruction
EXTEST	0000	Extest Instruction
HIGHZ	1010	High–Z all Output pins while bypass reg. is between TDI and TDO
CLAMP	1001	Clamp Output pins while bypass reg. is between TDI and TDO
Device Specific (Public) Instructions:		
LDRREG	0001	Load Read Address Reload Register
LDWREG	0100	Load Write Address Reload Register
LDBREG	0101	Load both Address Reload Registers (Write then Read)
LDCONT	0010	Load Control Register
RDCOUNT	1000	Read the values of the Read and Write Address Counters
EZWRITE	0011	Serial Write (using Write Address Counter)
EZREAD	0110	Serial Read (using Read Address Counter)
EZREADZ	1110	Serial Read, outputs High–Z

*Default state at power–up.

CLAMP TAP INSTRUCTION

The CLAMP instruction is provided to allow the state of the signals driven from the output pins to be determined from the boundary–scan register while the bypass register is selected as the serial path between TDI and TDO. The signals driven from the output pins will not change while the CLAMP instruction is selected. EXTEST could also be used for this purpose but CLAMP shortens the board scan path by inserting only the bypass register between TDI and TDO. To use CLAMP, the SAMPLE/PRELOAD instruction would be used first to scan in the values to be driven on the output pins when the CLAMP instruction is active. Q0 – Q7 will be active only if $\overline{G}$ is preloaded with a zero.

HIGH–Z TAP INSTRUCTION

The High–Z instruction is provided to allow all the outputs to be placed in an inactive drive state (High–Z). During the High–Z instruction the bypass register is connected between TDI and TDO.

BYPASS TAP INSTRUCTION

The Bypass instruction is the default instruction loaded in at power up. This instruction will place a single shift register between TDI and TDO during the Shift–DR state of the TAP controller. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

Table 2. Sample/Preload Boundary Scan Register Bit Definitions

Bit Number	Pin Name	Pin Type
0	$\overline{RR}$	Input
1	RE	Input
2	$\overline{G}$	Input
3	Q0	Output
4	Q1	Output
5	Q2	Output
6	Q3	Output
7	Q4	Output
8	Q5	Output
9	Q6	Output
10	Q7	Output
11	D7	Input
12	D6	Input
13	D5	Input
14	D4	Input
15	D3	Input
16	D2	Input
17	D1	Input
18	D0	Input
19	K	Input
20	WE	Input
21	$\overline{WR}$	Input

NOTE: K is a sample–only scan bit. It cannot be preloaded for control purposes.

DEVICE SPECIFIC (PUBLIC) INSTRUCTIONS

LDCONT INSTRUCTION

The Control Register is an eight bit register that contains the control bits for the Address Registers and Counters and the Output Enable pin. When the LDCONT TAP instruction is loaded into the Instruction Register, the Control Register is placed between TDI and TDO when the TAP controller is in the Shift–DR state (Table 10). The power–up/preload state and function of the Control bits are found in Table 3.

The Expand ID bits provide system depth expansion. These three bits are compared to the upper three bits in the address counters. As long as the three Expand–ID bits match the three upper bits in the address counters the port will stay active. If they do not match, the port will deactivate (i.e., outputs will High–Z or write will be disabled); however, the counters will continue counting as long as RE and WE remain asserted (i.e., high) at the rising edge of Clock.

The Reload Control bits (3 and 5) are used to control either reloading the Read and Write Address Counters from the Reload Registers or clearing the counter when $\overline{RR}$ or $\overline{WR}$ is asserted. If these bits are set low the counters they control will be cleared to all zeroes if the appropriate reload signal ($\overline{RR}$ or $\overline{WR}$) is asserted and any value in the Reload Register is ignored. This means that if the initial address value desired is address 0000 (or FFFF when counting down) then there is no need to load the Address Reload Registers using the LDRREG, LDWREG, or the LDBREG instructions in the following description. If these bits are set high the counters are loaded up with the values in the Reload Registers when the appropriate reload signal ($\overline{RR}$ or $\overline{WR}$) is asserted.

The Up/Down count bits (4 and 6) determine the direction in which the respective Address Counter will count; if the bit is set low the counter will count up and if set high the counter will count down. If the counters are set to count down and the Reload control is set to the clear counter mode, then the initial value in the counters will be FFFF. To ensure that the counter will function properly, a reload (using $\overline{RR}$ or $\overline{WR}$) is required after the count direction is switched.

The Output Enable control bit (7) determines the functionality of the Output Enable pin, $\overline{G}$. When the bit is low, $\overline{G}$ functions asynchronously. When set high, $\overline{G}$ functions synchronously and must meet the specified setup and hold times to the Clock K.

The Control Register will also be preloaded. When the instruction 0010 (LDCONT) is in the Instruction Register and the controller is in the Capture–DR state the above preload values (all zeroes) will be loaded into the Control Register. All zeroes will also be loaded in the Control Register at power–up.

While new values are shifted in from TDI in the Shift–DR state, all zeroes will be output on TDO for the first eight bits.

LDRREG, LDWREG, AND LDBREG TAP INSTRUCTIONS

There are three instructions that may be used to load the 16 bit address reload registers: LDRREG (Load Read Address Reload Register), LDWREG (Load Write Address Reload Register), and LDBREG (Load both Address Reload Registers, Write followed by Read). Figure 3 illustrates how the Reload registers are placed between TDI and TDO. Tables 7, 8, and 9 describe each register. These instructions would be used only if the user needed to load the Reload Registers with a non–zero value. If the Address Counters are to always be reset to zeroes (or all 1s if counting down) then only the Control Register need be loaded to affect a reset of the counters.

The TAP controller has been set up to make it easier for the user to serially load the Reload Registers. When the TAP controller is clocked into the Capture–IR state (see state diagram) the instruction for loading both registers (0101) will be preloaded into the shift register. This allows the user to go directly to the Update–IR state instead of having to serially shift this instruction in through the TDI port. Once the load instruction has been entered the user can then clock over to the Capture–DR state where the value for the reload register(s) is serially loaded (see Figure 3).

RDCOUNT TAP INSTRUCTION

The RDCOUNT scan register is accessible after the RDCOUNT instruction is loaded into the TAP instruction register in the Shift–IR state and the TAP controller is then moved to the Shift–DR state. This scan register can then be used to shift out the values of the Read and Write Address Counters The RDCOUNT scan–register is a sample only register and can not be used to load values into the counters. See Table 4.

EZWRITE TAP INSTRUCTION AND SCAN PATH

The EZWRITE TAP instruction is provided to allow the user to more easily and quickly write a large number of bytes to the device serially through the TDI port. EZWRITE shortens the scan path for a serial write to just the 8 bit Data in register (see Table 5).

5

The most likely use of this instruction is as follows: the user would first load the Control Register using the LDCONT instruction. This would initialize the Expand ID bits and the Write Counter. The Write Reload Register will need to be loaded using the LDWREG instruction if a non–zero starting address is desired. If 0000 was the first desired count, setting up the Control Register to "clear" the Write counter is all that is required (Bit 3 set to zero). A reload cycle using SAMPLE/PRELOAD ($\overline{WR}$ preloaded low) and INTEST would also have to be run in order to initialize the counter. While still in the INTEST instruction at the Shift–DR state, the proper values of WE and $\overline{WR}$ would then need to be preloaded for proper operation of EZWRITE (WE high and $\overline{WR}$ high). After all this initializing is done, the EZWRITE instruction would be loaded into the TAP instruction register in the Shift–IR state. When the TAP controller is then moved to the Shift–DR state the EZWRITE scan path would be inserted between TDI and TDO. This scan path is composed of the 8 bit Data In register (see Table 5). The 8 bits to be written into the first address would be scanned in (sampled values from the Data In pins would be streaming out of TDO at the same time), then the TAP controller would be moved to the Run–Test/Idle state where one cycle of TCK would write the 8 bits into the address and increment the counter. The TAP controller would then move back to the Shift–DR state so that the next byte to be written can be serially loaded and the process would be repeated until all desired bytes were written. During EZWRITE the Q0 – Q7 pins will be in a High–Z state.

Table 3. Control Register Bit Description

Bit No.	Power Up and Preload State	Function
0 – 2	000	Expand ID bits for comparison with the upper 3 bits of the Read and Write Address counters
3	0	Reload Control of Write Address Counter (0 = clear counter, 1 = reload)
4	0	Up/Down count bit for Write Address Counter (0 = count up, 1 = count down)
5	0	Reload Control of Read Address Counter (0 = clear counter, 1 = reload)
6	0	Up/Down count bit for Read Address Counter (0 = count up, 1 = count down)
7	0	$\overline{G}$ Control (0 = asynchronous, 1 = synchronous)

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EZREAD TAP INSTRUCTION AND SCAN PATH

The EZREAD TAP instruction is provided to allow the user to more easily and quickly read a large number of bytes from the device serially through the TDO port. EZREAD shortens the scan path for a serial read to just the 8 bit Data Out register (see Table 6).

To serially read the device the following would occur: initialization would be much like EZWRITE except that the Read Address Counter should be reladed with the count BEFORE the first one desired. So, if the first read needed to be address 0000 (and the counter is counting up), the Read Reload Register would have to be preloaded with FFFF using the LDRREG instruction. Again, SAMPLE/PRELOAD and INTEST instructions would need to be run to perform a reload cycle followed by another Boundary–scan that set RE and $\overline{RR}$ high in anticipation of the EZREAD instruction. Also, WE should be set low to prevent any unintended writes while reading. After this initializing, the EZREAD instruction would be loaded into the TAP instruction register in the Shift–IR state. The TAP controller would move to the Run–Test/Idle state where one cycle of TCK would increment the counter, read the 8 bits from that address, and load them into the Data Output register. The TAP controller would then move to the Shift–DR state and the EZREAD scan path would be inserted between TDI and TDO. This scan path is composed of the 8 bit Data Out register (see Table 6). In the Shift–DR state the Data Out register would be serially scanned out of the TDO port. This sequence through the TAP state machine would then be repeated until all desired bytes were read. EZREAD keeps the Q0 – Q7 pins active (if $\overline{G}$ is preloaded low) to allow parallel reading of the data out if desired.

EZREADZ TAP INSTRUCTION AND SCAN PATH

The EZREADZ TAP instruction behaves exactly like the EZREAD instruction except that the all outputs are held in a High–Z mode once the instruction is loaded.

DISABLING THE TEST ACCESS PORT AND BOUNDARY SCAN

It is possible to use this device without utilizing the four pins used for the IEEE 1149.1 Test Access Port. To circuit disable the TAP controller without interfering with normal operation of the device TCK must be tied to V_{SS} to preclude midlevel inputs. Although TDI and TMS are designed in such a way that an undriven input will produce a response identical to the application of a logic 1, it is still advisable to tie these inputs to V_{DD} through a 1 k resistor. TDO should remain unconnected.

With the four Test Access Port pins disabled, the device can only be used in its default power–up state. At power up, the device is configured to count up starting at address 0, the reload pins ($\overline{RR}$ and $\overline{WR}$) will clear the counters, the Expand ID bits are set to 000, and the Output Enable pin ($\overline{G}$) is configured as an asynchronous input.

Table 4. RDCOUNT Scan Register Bit Definitions

Bit Number	Bit/Pin Name*	Bit/Pin Type
0	RAC0	Input
1	RAC1	Input
2	RAC2	Input
3	RAC3	Input
4	RAC4	Input
5	RAC5	Input
6	RAC6	Input
7	RAC7	Input
8	RAC8	Input
9	RAC9	Input
10	RAC10	Input
11	RAC11	Input
12	RAC12	Input
13	RAC13#	Input
14	RAC14#	Input
15	RAC15#	Input
16	WAC0	Input
17	WAC1	Input
18	WAC2	Input
19	WAC3	Input
20	WAC4	Input
21	WAC5	Input
22	WAC6	Input
23	WAC7	Input
24	WAC8	Input
25	WAC9	Input
26	WAC10	Input
27	WAC11	Input
28	WAC12	Input
29	WAC13#	Input
30	WAC14#	Input
31	WAC15#	Input

* RAC = Read Address Counter
WAC = Write Address Counter

\# These register bits are compared to the three Expand ID bits in the Control Register. (EX0 – 2). Only when there is a match is the read or write allowed to occur.

NOTE: Bit 0 closest to TDO.

Table 5. EZWRITE Scan Path Bit Definitions

Bit Number	Pin Name	Pin Type
0	D7	Input
1	D6	Input
2	D5	Input
3	D4	Input
4	D3	Input
5	D2	Input
6	D1	Input
7	D0	Input

Table 6. EZREAD and EZREADZ Scan Path Bit Definitions

Bit Number	Bit/Pin Name	Bit/Pin Type
0	Q0	Output
1	Q1	Output
2	Q2	Output
3	Q3	Output
4	Q4	Output
5	Q5	Output
6	Q6	Output
7	Q7	Output

Table 7. LDRREG Scan Path Bit Definitions

Bit Number	Bit/Pin Name*	Bit/Pin Type
0	RRR0	Register bit
1	RRR1	Register bit
2	RRR2	Register bit
3	RRR3	Register bit
4	RRR4	Register bit
5	RRR5	Register bit
6	RRR6	Register bit
7	RRR7	Register bit
8	RRR8	Register bit
9	RRR9	Register bit
10	RRR10	Register bit
11	RRR11	Register bit
12	RRR12	Register bit
13	RRR13	Register bit
14	RRR14	Register bit
15	RRR15	Register bit

* RRR = Read Reload Register

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Table 8. LDBREG Scan Path Bit Definitions

Bit Number	Bit/Pin Name*	Bit/Pin Type
0	RRR0	Register bit
1	RRR1	Register bit
2	RRR2	Register bit
3	RRR3	Register bit
4	RRR4	Register bit
5	RRR5	Register bit
6	RRR6	Register bit
7	RRR7	Register bit
8	RRR8	Register bit
9	RRR9	Register bit
10	RRR10	Register bit
11	RRR11	Register bit
12	RRR12	Register bit
13	RRR13	Register bit
14	RRR14	Register bit
15	RRR15	Register bit
16	WRR0	Register bit
17	WRR1	Register bit
18	WRR2	Register bit
19	WRR3	Register bit
20	WRR4	Register bit
21	WRR5	Register bit
22	WRR6	Register bit
23	WRR7	Register bit
24	WRR8	Register bit
25	WRR9	Register bit
26	WRR10	Register bit
27	WRR11	Register bit
28	WRR12	Register bit
29	WRR13	Register bit
30	WRR14	Register bit
31	WRR15	Register bit

* RRR = Read Reload Register
WRR = Write Reload Register
NOTE: Bit 0 closest to TDO.

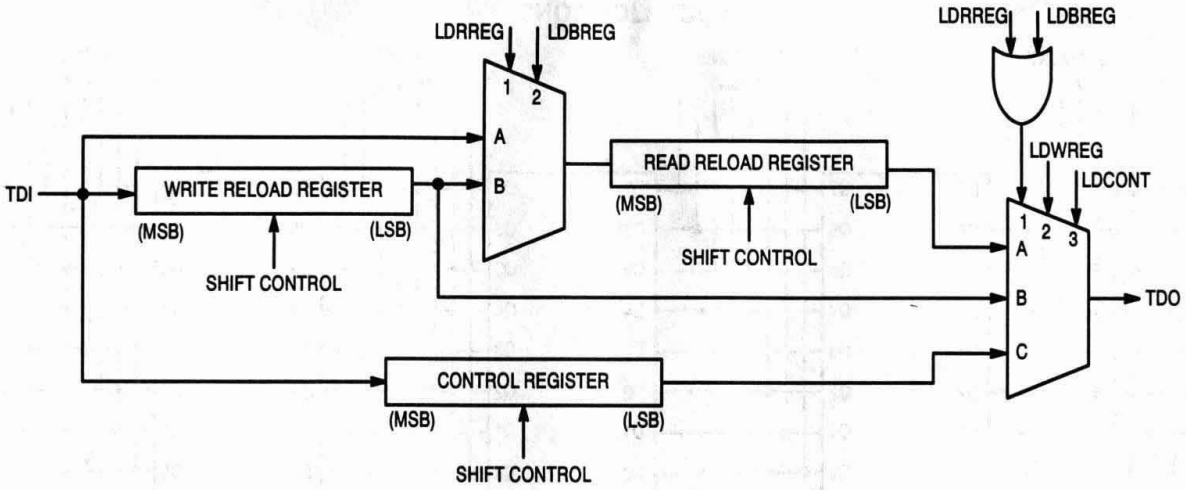
Table 9. LDWREG Scan Path Bit Definitions

Bit Number	Bit/Pin Name*	Bit/Pin Type
0	WRR0	Register bit
1	WRR1	Register bit
2	WRR2	Register bit
3	WRR3	Register bit
4	WRR4	Register bit
5	WRR5	Register bit
6	WRR6	Register bit
7	WRR7	Register bit
8	WRR8	Register bit
9	WRR9	Register bit
10	WRR10	Register bit
11	WRR11	Register bit
12	WRR12	Register bit
13	WRR13	Register bit
14	WRR14	Register bit
15	WRR15	Register bit

* WRR = Write Reload Register

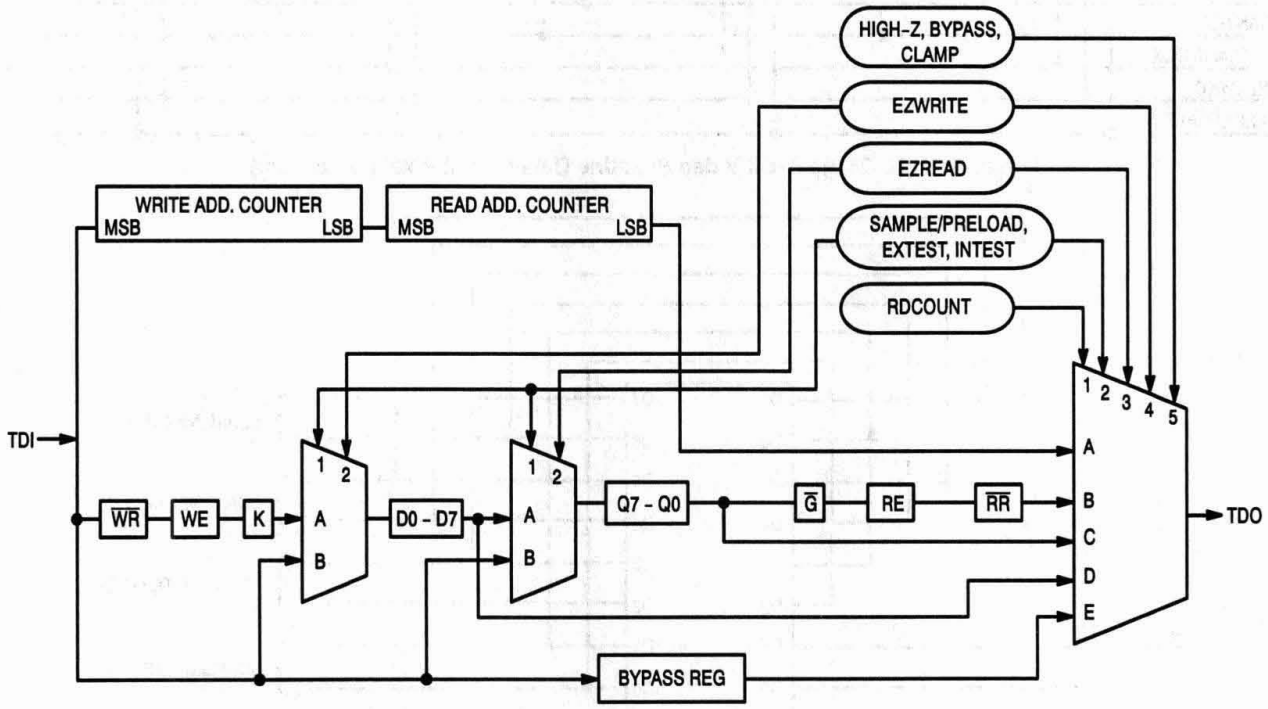
Table 10. LDCONT Scan Path Bit Definitions

Bit Number	Bit/Pin Name	Bit/Pin Type
0	EX0	Register bit
1	EX1	Register bit
2	EX2	Register bit
3	WCC	Register bit
4	UDW	Register bit
5	RCC	Register bit
6	UDR	Register bit
7	G CONT	Register bit



THE LEFT MOST CONTROL SIGNAL ENTERING THE MUX FROM THE TOP(1) SELECTS THE UPPER MOST INPUT ON THE LEFT SIDE OF THE MUX(A). THE RIGHT MOST CONTROL SIGNAL SELECTS THE BOTTOM MOST INPUT.

Figure 3. Register Load Paths



THE LEFT MOST CONTROL SIGNAL ENTERING THE MUX FROM THE TOP(1) SELECTS THE UPPER MOST INPUT ON THE LEFTSIDE OF THE MUX(A). THE RIGHT MOST CONTROL SIGNAL SELECTS THE BOTTOM MOST INPUT.

Figure 4. Boundary Scan Paths

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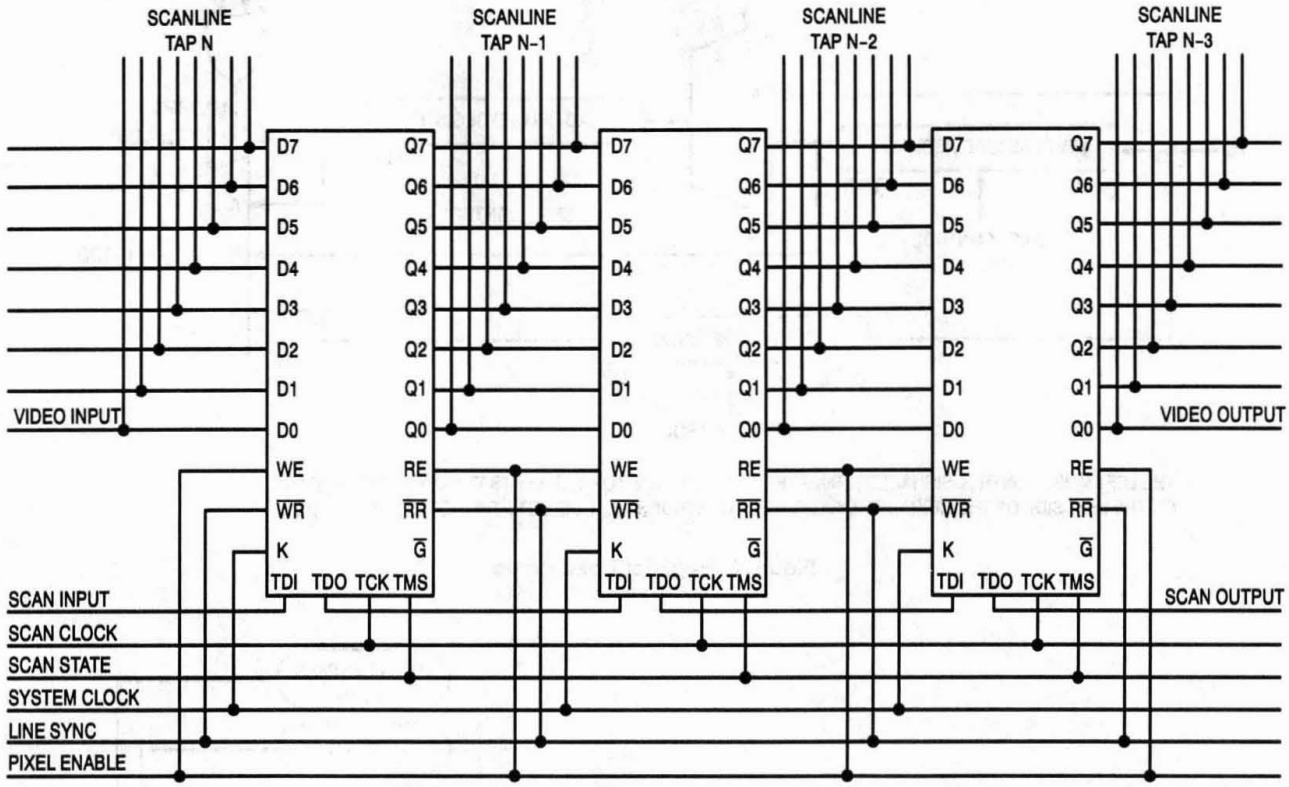

Figure 5. Multi–Stage 8–Bit Video Scanline Delay (8192 Pixels Maximum)

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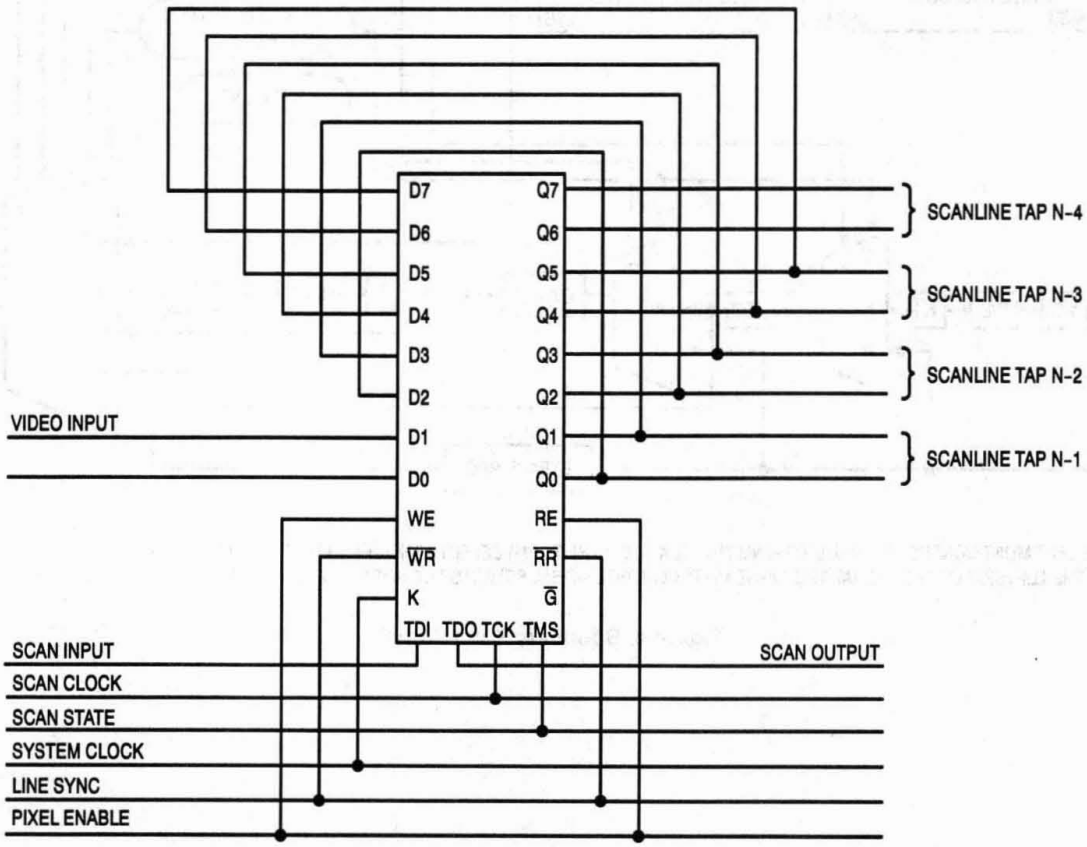

Figure 6. Multi–Stage 2–Bit Video Scanline Delay (8192 Pixels Maximum)

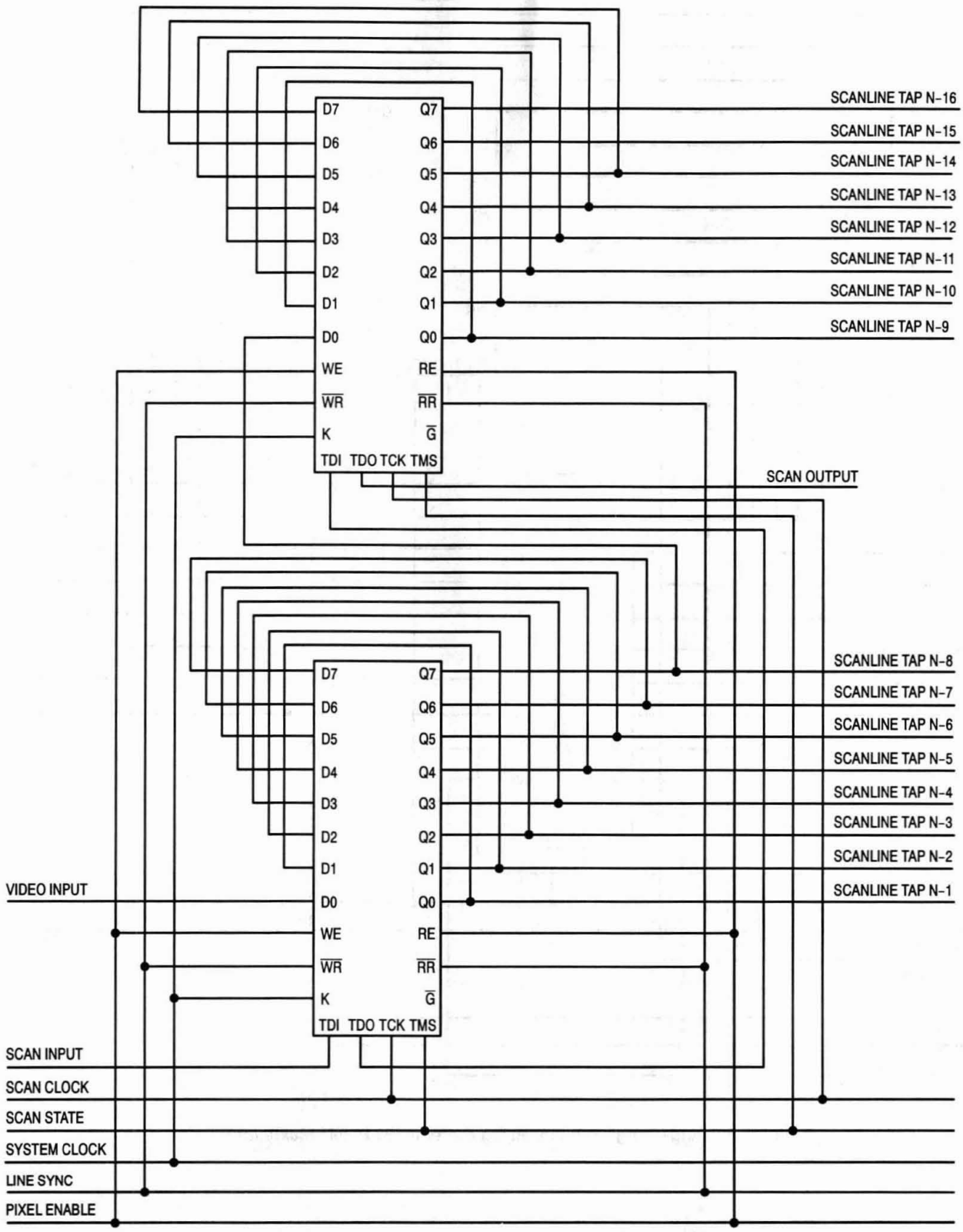

Figure 7. Multi–Stage 1–Bit Video Scanline Delay (8192 Pixels Maximum)

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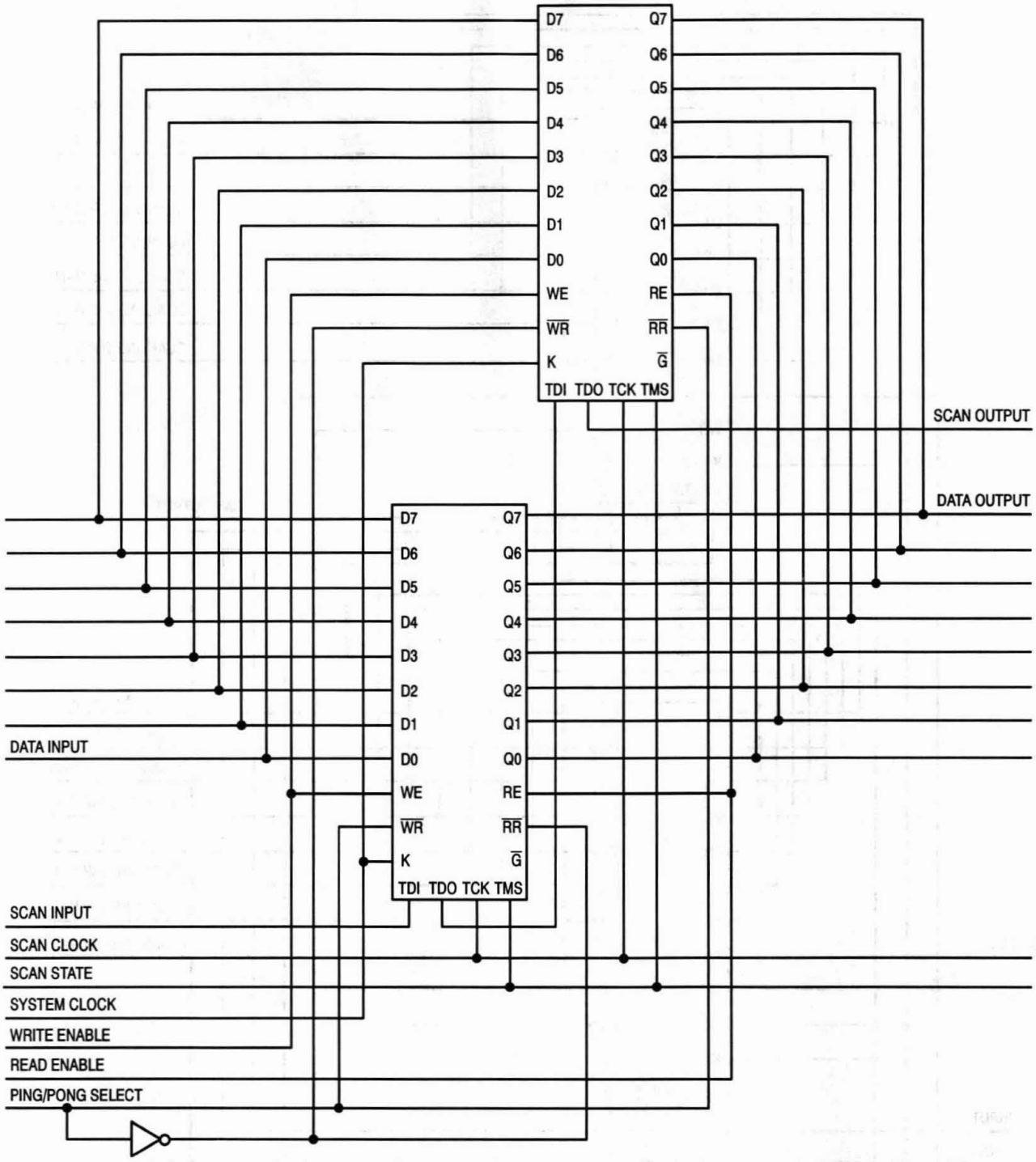

Figure 8. "Ping–Pong" Synchronizing Buffer (8192 Pixels Maximum)

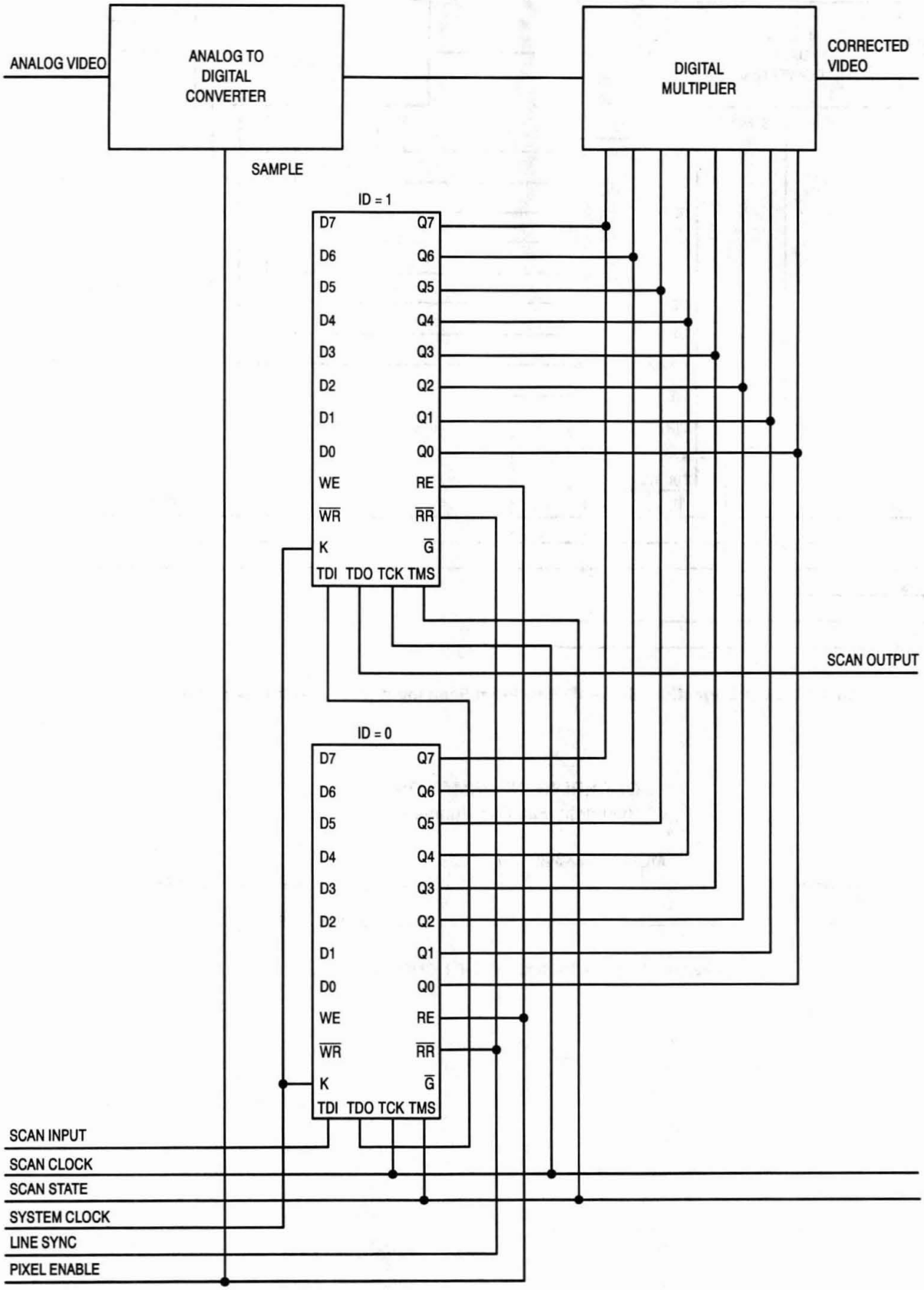

Figure 9. CCD Gain Correction, Buffer Written From Scan Input (16384 Pixels Maximum)

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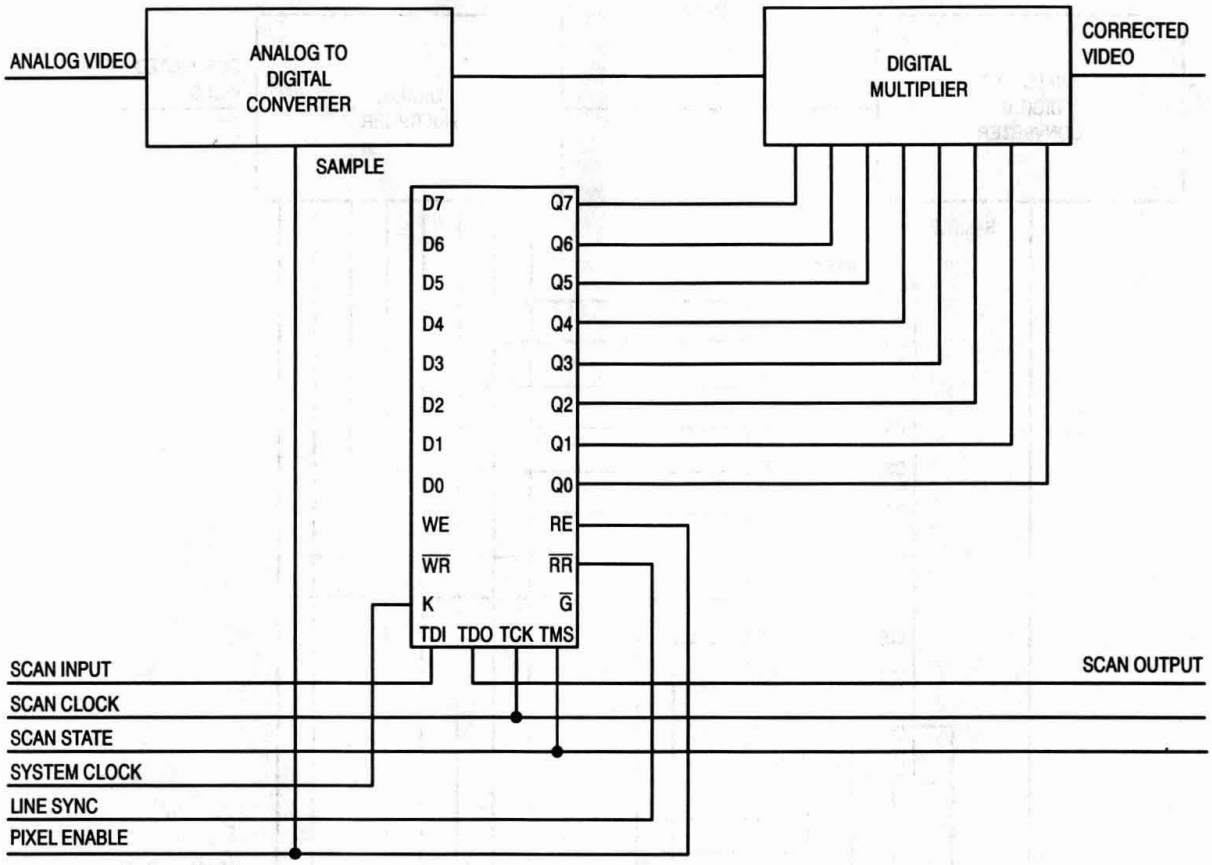


Figure 10. CCD Gain Correction, Buffer Written From Scan Input (8192 Pixels Maximum)

ORDERING INFORMATION
(Order by Full Part Number)

MCM 62X308 J XX

- MCM — Motorola Memory Prefix
- 62X308 — Part Number
- J — Package (J = SOJ)
- XX — Speed (15–5 = 15 ns, 17 = 17 ns)

Full Part Numbers — MCM62X308J15–5 MCM62X308J17

Multichip Module

256K x 72 .. 3.3 V .... MCM72FB8ML ... 6–3
256K x 72 .. 3.3 V .... MCM72PB8ML ... 6–3

PowerPC Processor Applications

1MB ..... 5 V MPC2106B 6–21
512KB ..... 5 V MPC2105B 6–21
512KB ..... 5 V MPC2105P 6–37

Pentium Processor Applications

512KB ..... 3.3 V MCM64PE64 6–51

Networking and Buffer Applications Asynchronous Modules

1M x 32 .... 5 V MCM321024 6–52
512K x 32 .. 5 V MCM32515 6–59

Networking and Buffer Applications Synchronous Modules

8MB ..... 3.3 V MCM72F10 6–66
4MB ..... 3.3 V MCM72F9 6–75
2MB ..... 3.3 V MCM72F8 6–75
1MB ..... 3.3 V MCM72F7 6–85
512KB ..... 3.3 V MCM72F6 6–85

6

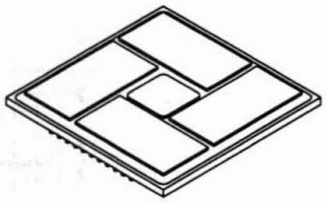
Fast SRAM Modules

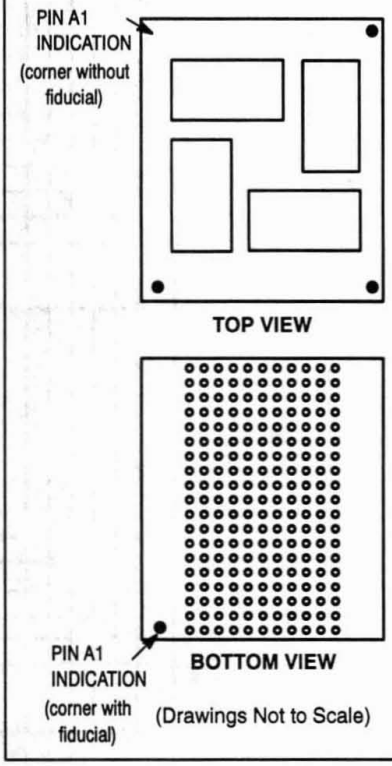
MCM72FB8ML
MCM72PB8ML

Product Preview

256K x 72 Bit BurstRAM™ Multichip Module

MULTICHIP MODULE
PBGA
CASE 1103B–01





The 256K x 72 multichip module uses four 4M bit synchronous fast static RAMs designed to provide a burstable, high performance, secondary cache for the PowerPC™ and other high performance microprocessors. It is organized as 256K words of 72 bits each. This device integrates input registers, an output register (MCM72PB8ML only), a 2–bit address counter, and high speed SRAM onto a single monolithic circuit for reduced parts count in cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (SA), data inputs (DQx), and all control signals except output enable ($\overline{G}$) and linear burst order ($\overline{LBO}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ input pins. Subsequent burst addresses can be generated internally (burst sequence operates in linear or interleaved mode dependent upon the state of $\overline{LBO}$) and controlled by the burst address advance ($\overline{ADV}$) input pin.

Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased timing flexibility for incoming signals.

Synchronous byte write ($\overline{SBx}$), synchronous global write ($\overline{SGW}$), and synchronous write enable ($\overline{SW}$) are provided to allow writes to either individual bytes or to all bytes. The eight bytes are designated as "a" through "h". $\overline{SBa}$ controls DQa, $\overline{SBb}$ controls DQb, etc. Individual bytes are written if the selected byte writes $\overline{SBx}$ are asserted with $\overline{SW}$. All bytes are written if either $\overline{SGW}$ is asserted or if all $\overline{SBx}$ and $\overline{SW}$ are asserted.

The module can be configured as either a pipelined or flow–through SRAM. For read cycles, pipelined SRAMs output data is temporarily stored by an edge–triggered output register and then released to the output buffers at the next rising edge of clock (K). Flow–through SRAMs allow output to simply flow freely from the memory array.

The multichip module operates from a 3.3 V core power supply and all outputs operate on a separate 2.5 V to 3.3 V power supply. All inputs and outputs are JEDEC standard JESD8–5 compatible.

- 3.3 V + 10%, – 5% Core Power Supply, 2.5 V I/O Supply
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Option for Pipeline or Flow–Through (Speeds Guaranteed When Module is Purchased by Appropriate Part Number)
- Selectable Burst Sequencing Order (Linear/Interleaved)
- Single–Cycle Deselect Timing
- Internally Self–Timed Write Cycle
- Byte Write and Global Write Control
- JEDEC BGA Pin Assignment

6

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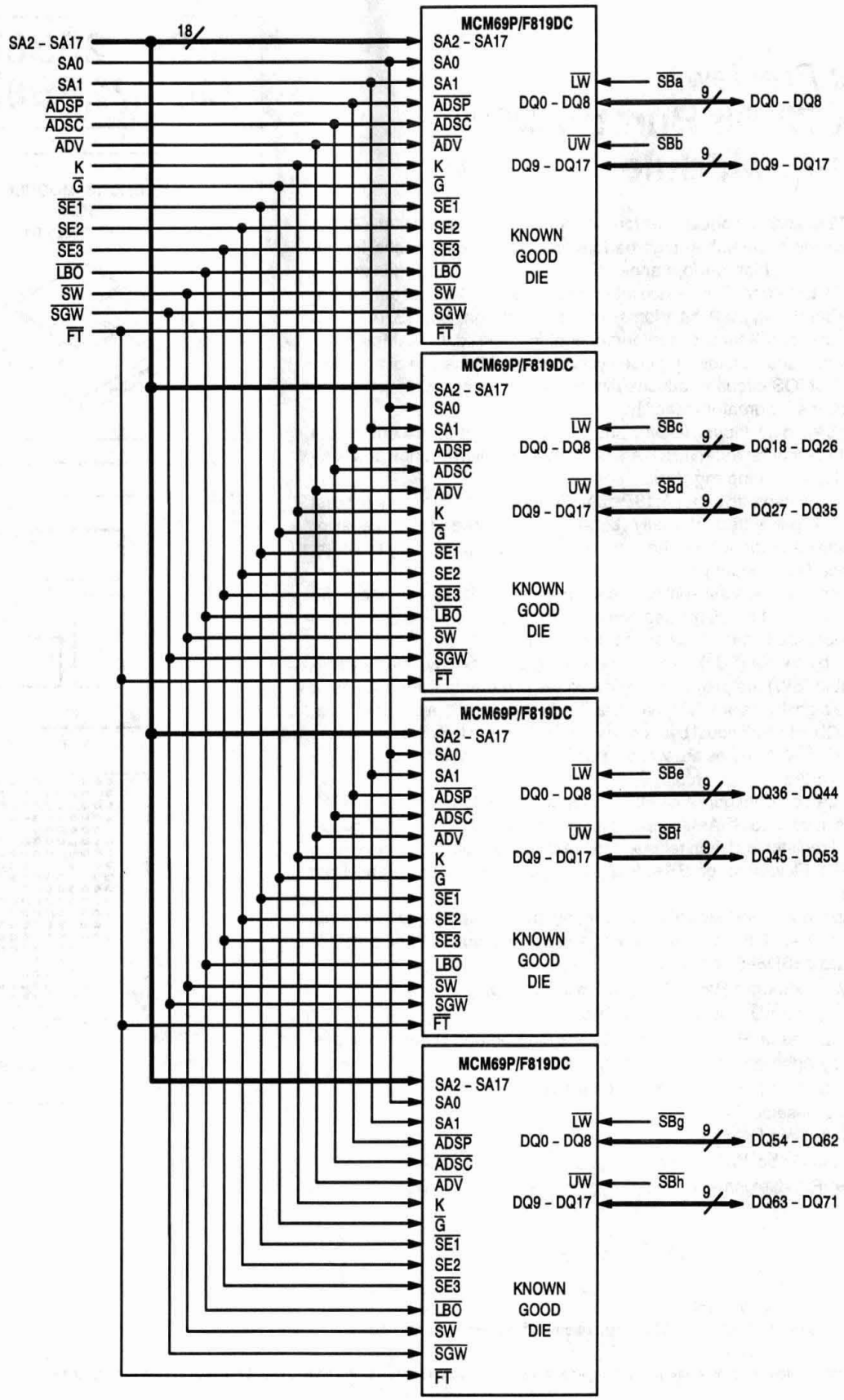
This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

3/12/97

256K X 72 FOUR–CHIP MODULE BLOCK DIAGRAM



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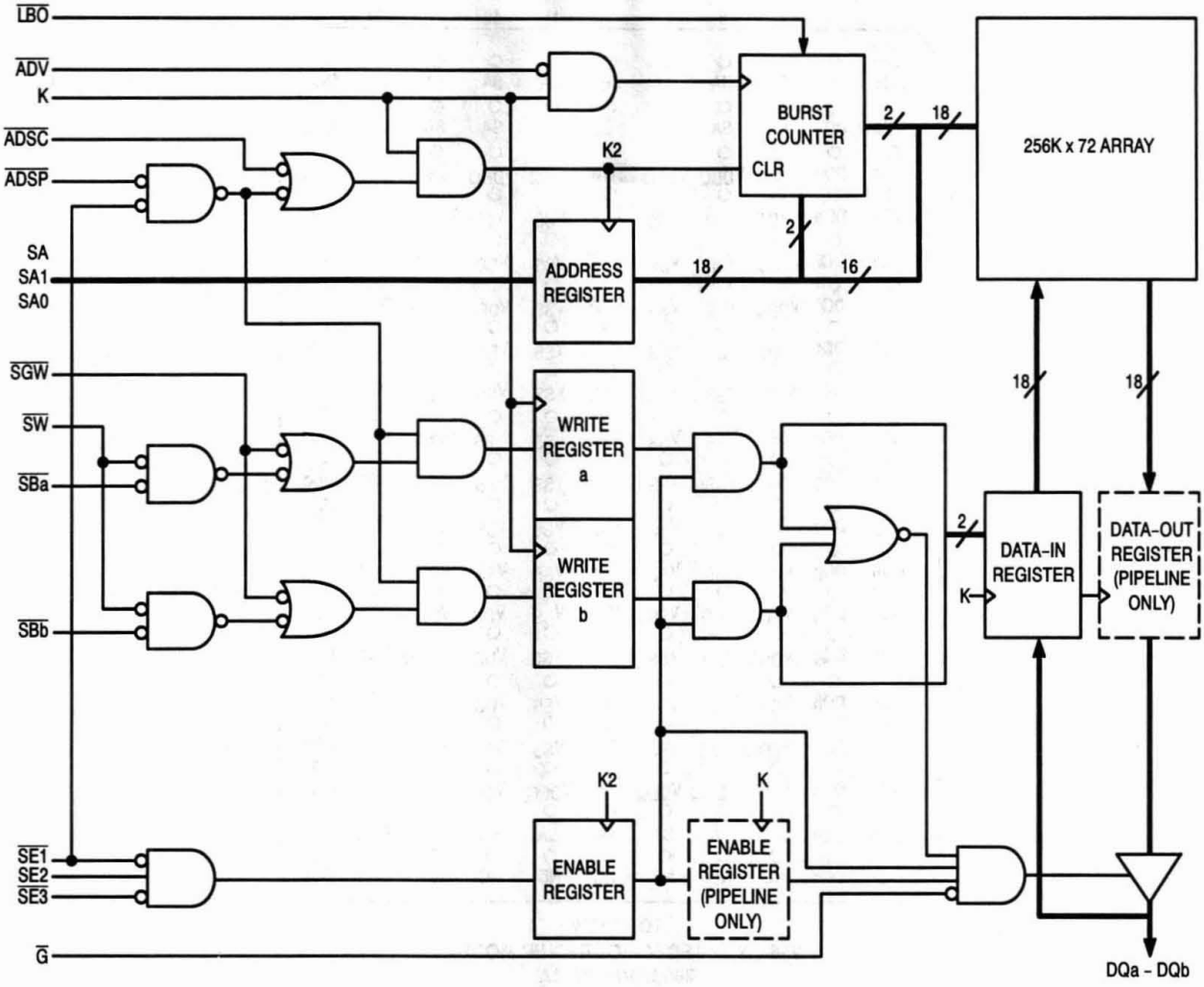
MCM69F819DC AND MCM69P819DC FUNCTIONAL BLOCK DIAGRAM



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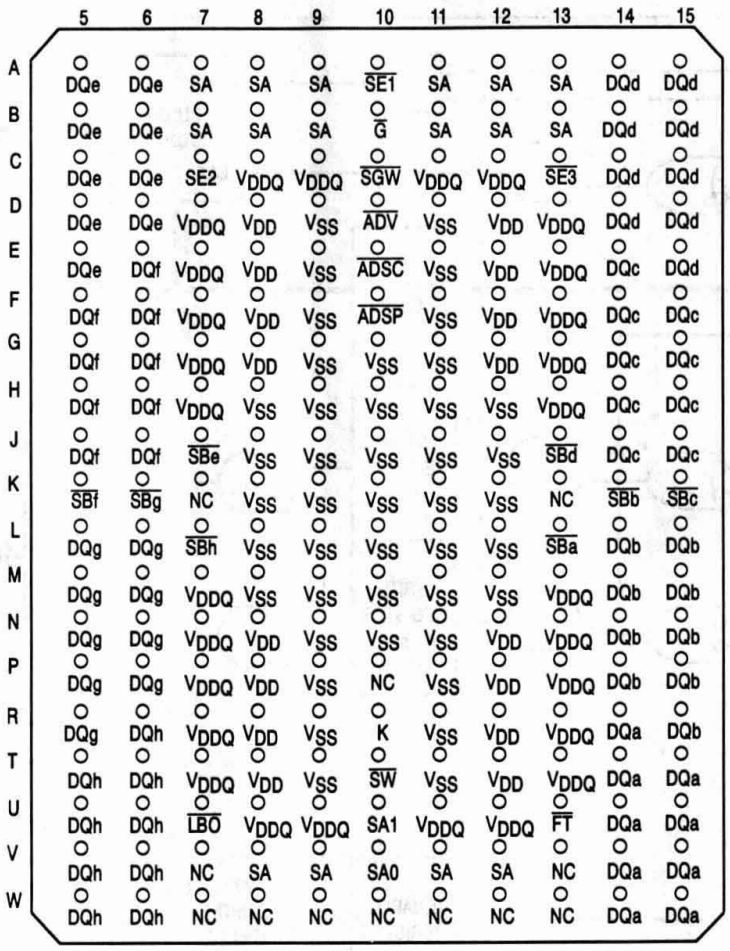
PIN ASSIGNMENT



	5	6	7	8	9	10	11	12	13	14	15
A	DQe	DQe	SA	SA	SA	$\overline{SE1}$	SA	SA	SA	DQd	DQd
B	DQe	DQe	SA	SA	SA	$\overline{G}$	SA	SA	SA	DQd	DQd
C	DQe	DQe	SE2	V_{DDQ}	V_{DDQ}	$\overline{SGW}$	V_{DDQ}	V_{DDQ}	$\overline{SE3}$	DQd	DQd
D	DQe	DQe	V_{DDQ}	V_{DD}	V_{SS}	$\overline{ADV}$	V_{SS}	V_{DD}	V_{DDQ}	DQd	DQd
E	DQe	DQf	V_{DDQ}	V_{DD}	V_{SS}	$\overline{ADSC}$	V_{SS}	V_{DD}	V_{DDQ}	DQc	DQd
F	DQf	DQf	V_{DDQ}	V_{DD}	V_{SS}	$\overline{ADSP}$	V_{SS}	V_{DD}	V_{DDQ}	DQc	DQc
G	DQf	DQf	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQc	DQc
H	DQf	DQf	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	DQc	DQc
J	DQf	DQf	$\overline{SBe}$	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	$\overline{SBd}$	DQc	DQc
K	$\overline{SBf}$	$\overline{SBg}$	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	$\overline{SBb}$	$\overline{SBc}$
L	DQg	DQg	$\overline{SBh}$	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	$\overline{SBa}$	DQb	DQb
M	DQg	DQg	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	DQb	DQb
N	DQg	DQg	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
P	DQg	DQg	V_{DDQ}	V_{DD}	V_{SS}	NC	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
R	DQg	DQh	V_{DDQ}	V_{DD}	V_{SS}	K	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQb
T	DQh	DQh	V_{DDQ}	V_{DD}	V_{SS}	$\overline{SW}$	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
U	DQh	DQh	$\overline{LBO}$	V_{DDQ}	V_{DDQ}	SA1	V_{DDQ}	V_{DDQ}	$\overline{FT}$	DQa	DQa
V	DQh	DQh	NC	SA	SA	SA0	SA	SA	NC	DQa	DQa
W	DQh	DQh	NC	NC	NC	NC	NC	NC	NC	DQa	DQa

TOP VIEW
256K X 72 JEDEC FOUR–CHIP MODULE
209 BUMP PBGA

Not to Scale

6

PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
E10	$\overline{ADSC}$	Input	Synchronous Address Status Controller: Initiates READ, WRITE, or chip deselect cycle.
F10	$\overline{ADSP}$	Input	Synchronous Address Status Processor: Initiates READ, WRITE, or chip deselect cycle (exception — chip deselect does not occur when $\overline{ADSP}$ is asserted and $\overline{SE1}$ is high).
D10	$\overline{ADV}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
(a) R14, T14, T15, U14, U15, V14, V15, W14, W15 (b) L14, L15, M14, M15, N14, N15, P14, P15, R15 (c) E14, F14, F15, G14, G15, H14, H15, J14, J15 (d) A14, A15, B14, B15, C14, C15, D14, D15, E15 (e) A5, A6, B5, B6, C5, C6, D5, D6, E5 (f) E6, F5, F6, G5, G6, H5, H6, J5, J6 (g) L5, L6, M5, M6, N5, N6, P5, P6, R5 (h) R6, T5, T6, U5, U6, V5, V6, W5, W6	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b).
U13	$\overline{FT}$	Input	Flow–Through Input: This pin must remain in steady state (this signal is not registered or latched). It must be tied high or low. Low — flow–through mode. High — pipeline mode.
B10	$\overline{G}$	Input	Asynchronous Output Enable Input: Low — enables output buffers (DQx pins). High — DQx pins are high impedance.
R10	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$ and $\overline{LBO}$.
U7	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst counter (68K/PowerPC). High — interleaved burst counter (486/i960/Pentium).
U10, V10	SA1, SA0	Input	Synchronous Address Inputs: These pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
A7, A8, A9, A11, A12, A13, B7, B8, B9, B11, B12, B13, V8, V9, V11, V12	SA2 – SA17	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
L13, K14, K15, J13, J7, K5, K6, L7 (a) (b) (c) (d) (e) (f) (g) (h)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: "x" refers to the byte being written (byte a, b). $\overline{SGW}$ overrides $\overline{SBx}$.
A10	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high–blocks $\overline{ADSP}$ or deselects chip when $\overline{ADSC}$ is asserted.
C7	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
C13	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
C10	$\overline{SGW}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the $\overline{SBx}$ and $\overline{SW}$ signals. If only byte write signals $\overline{SBx}$ are being used, tie this pin high.
T10	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{SBx}$ pins. If only byte write signals $\overline{SBx}$ are being used, tie this pin low.
D8, D12, E8, E12, F8, F12, G8, G12, N8, N12, P8, P12, R8, R12, T8, T12	V_{DD}	Supply	Core Power Supply.
C8, C9, C11, C12, D7, D13, E7, E13, F7, F13, G7, G13, H7, H13, M7, M13, N7, N13, P7, P13, R7, R13, T7, T13, U8, U9, U11, U12	V_{DDQ}	Supply	I/O Power Supply.

PIN DESCRIPTIONS (continued)

Pin Locations	Symbol	Type	Description
D9, D11, E9, E11, F9, F11, G9 – G11, H8 – H12, J8 – J12, K8 – K12, L8 – L12, M8 – M12, N9 – N11, P9, P11, R9, R11, T9, T11	V_{SS}	Supply	Ground.
K7, K13, P10, V7, V13, W7 – W13	NC	—	No Connection: There is no connection to the chip. For compatibility reasons, it is recommended that this pin be tied low for system designs that do not have a sleep mode associated with the cache/memory controller. Other vendors' RAMs may have implemented the Sleep Mode (ZZ) feature.

TRUTH TABLE (See Notes 1 through 5)

Next Cycle	Address Used	$\overline{SE1}$	SE2	$\overline{SE3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{G}$ [3]	DQx	Write [2, 4]
Deselect	None	1	X	X	X	0	X	X	High–Z	X
Deselect	None	0	X	1	0	X	X	X	High–Z	X
Deselect	None	0	0	X	0	X	X	X	High–Z	X
Deselect	None	X	X	1	1	0	X	X	High–Z	X
Deselect	None	X	0	X	1	0	X	X	High–Z	X
Begin Read	External	0	1	0	0	X	X	X	High–Z	X[5]
Begin Read	External	0	1	0	1	0	X	X	High–Z	READ[5]
Continue Read	Next	X	X	X	1	1	0	1	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	0	DQ	READ
Continue Read	Next	1	X	X	X	1	0	1	High–Z	READ
Continue Read	Next	1	X	X	X	1	0	0	DQ	READ
Suspend Read	Current	X	X	X	1	1	1	1	High–Z	READ
Suspend Read	Current	X	X	X	1	1	1	0	DQ	READ
Suspend Read	Current	1	X	X	X	1	1	1	High–Z	READ
Suspend Read	Current	1	X	X	X	1	1	0	DQ	READ
Begin Write	External	0	1	0	1	0	X	X	High–Z	WRITE
Continue Write	Next	X	X	X	1	1	0	X	High–Z	WRITE
Continue Write	Next	1	X	X	X	1	0	X	High–Z	WRITE
Suspend Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Suspend Write	Current	1	X	X	X	1	1	X	High–Z	WRITE

NOTES:
1. X = Don't Care. 1 = logic high. 0 = logic low.
2. Write is defined as either 1) any $\overline{SBx}$ and $\overline{SW}$ low or 2) $\overline{SGW}$ is low.
3. $\overline{G}$ is an asynchronous signal and is not sampled by the clock K. $\overline{G}$ drives the bus immediately (t_{GLQX}) following $\overline{G}$ going low.
4. On write cycles that follow read cycles, $\overline{G}$ must be negated prior to the start of the write cycle to ensure proper write data setup times. $\overline{G}$ must also remain negated at the completion of the write cycle to ensure proper write data hold times.
5. This read assumes the RAM was previously deselected.

LINEAR BURST ADDRESS TABLE ($\overline{LBO}$ = V_{SS})

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X10	X . . . X11	X . . . X00
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X00	X . . . X01	X . . . X10

INTERLEAVED BURST ADDRESS TABLE ($\overline{LBO}$ = V_{DD})

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00

WRITE TRUTH TABLE

Cycle Type	$\overline{SGW}$	$\overline{SW}$	$\overline{SBa}$	$\overline{SBb}$
Read	H	H	X	X
Read	H	L	H	H
Write Byte a	H	L	L	H
Write Byte b	H	L	H	L
Write All Bytes	H	L	L	L
Write All Bytes	L	X	X	X

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	V_{SS} – 0.5 to + 4.6	V
I/O Supply Voltage (See Note 2)	V_{DDQ}	V_{SS} – 0.5 to V_{DD}	V
Input Voltage Relative to V_{SS} for Any Pin Except V_{DD} (See Note 2)	V_{in}, V_{out}	V_{SS} – 0.5 to V_{DD} + 0.5	V
Input Voltage (Three–State I/O) (See Note 2)	V_{IT}	V_{SS} – 0.5 to V_{DDQ} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Package Power Dissipation	P_D	6.4	W
Temperature Under Bias	T_{bias}	– 10 to 85	°C
Storage Temperature	T_{stg}	– 55 to 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. This is a steady–state DC parameter that is in effect after the power supply has achieved its nominal operating level. Power sequencing can not be controlled and is not allowed.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

PACKAGE THERMAL CHARACTERISTICS – TBD

DC OPERATING CONDITIONS AND CHARACTERISTICS

(3.6 V ≥ V_{DD} ≥ 3.1 V, 110°C ≥ T_J ≥ 20°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.135	3.3	3.6	V
Operating Temperature	T_J	20	—	110	°C
Input Low Voltage	V_{IL}	– 0.3	—	0.8	V
Input High Voltage	V_{IH}	1.7	—	V_{DD} + 0.3	V
I/O Supply Voltage	V_{DDQ}	2.375	2.5	V_{DD}	V

Figure 1. Undershoot Voltage

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input Leakage Current (0 V ≤ V_{in} ≤ V_{DD})	$I_{lkg(I)}$	—	—	± 1	µA	
Output Leakage Current (0 V ≤ V_{in} ≤ V_{DDQ})	$I_{lkg(O)}$	—	—	± 1	µA	
AC Supply Current (Device Selected, All Outputs Open, Cycle Time ≥ t_{KHKH} Min) Includes V_{DD} and V_{DDQ}	I_{DDA}	—	—	1700	mA	1, 2, 3
CMOS Standby Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH})	I_{SB1}	—	—	520	mA	1, 2, 3, 4
Clock Running Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}, All Other Inputs Held to Static CMOS Levels V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{DD} – 0.2 V)	I_{SB2}	—	—	120	mA	4
Output Low Voltage (I_{OL} = 2 mA) V_{DDQ} = 2.5 V (See Figure 5)	V_{OL} V_{OL2}	— —	— —	0.7 0.4	V	
Output High Voltage (I_{OL} = –2 mA) V_{DDQ} = 2.5 V (See Figure 5)	V_{OH} V_{OH2}	1.7 2.4	— —	— —	V	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing.
2. All addresses transition simultaneously low (LSB) then high (MSB).
3. Data states are all zero.
4. Device is deselected as defined by the Truth Table.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, 110°C ≥ T_J ≥ 20°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	—	16	pF
Input/Output Capacitance	$C_{I/O}$	—	—	5	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(3.6 V ≥ V_{DD} ≥ 3.135 V, 110°C ≥ T_J ≥ 20°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.25 V
Input Pulse Levels ..... 0 to 2.5 V
Input Slew Rate (See Figure 4) ..... 1.0 V/ns
Output Timing Reference Level ..... 1.25 V
Output Load ..... See Figure 2 Unless Otherwise Noted
Output Rise/Fall Times (max) ..... 1.8 ns

READ/WRITE CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	Pipeline MCM72PB8ML3.5 166 MHz		Pipeline MCM72PB8ML4 133 MHz		Flow–Through MCM72FB8ML7.5 117 MHz		Flow–Through MCM72FB8ML8 100 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	6	—	7.5	—	8.5	—	10	—	ns	
Clock High Pulse Width	t_{KHKL}	2.4	—	2.8	—	3	—	4	—	ns	3, 6
Clock Low Pulse Width	t_{KLKH}	2.4	—	2.8	—	3	—	4	—	ns	3, 6
Clock Low	t_{KL}	1.5	—	1.9	—	—	—	—	—	ns	3, 6
Clock High	t_{KH}	1.3	—	1.7	—	—	—	—	—	ns	3, 6
Clock Access Time	t_{KHQV}	—	3.5	—	4	—	7.5	—	8	ns	3
Output Enable to Output Valid	t_{GLQV}	—	3.5	—	3.8	—	3.5	—	3.5	ns	3
Clock High to Output Active	t_{KHQX1}	0	—	0	—	0	—	0	—	ns	3, 4, 5
Clock High to Output Change	t_{KHQX2}	1.5	—	1.5	—	2	—	2	—	ns	3, 5
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	ns	3. 4.5
Output Disable to Q High–Z	t_{GHQZ}	—	3.5	—	3.8	—	3.5	—	3.5	ns	3, 4, 5
Clock High to Q High–Z	t_{KHQZ}	1.5	6	1.5	7.5	2	3.5	2	3.5	ns	3, 4, 5
Setup Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	t_{ADKH} t_{ADSKH} t_{DVKH} t_{WVKH} t_{EVKH}	1.5	—	1.5	—	2	—	2	—	ns	3
Hold Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	t_{KHAX} t_{KHADSX} t_{KHDX} t_{KHWX} t_{KHEX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	3

NOTES:
1. Write is defined as either any $\overline{SBx}$ and $\overline{SW}$ low or $\overline{SGW}$ is low. Chip Enable is defined as $\overline{SE1}$ low, SE2 high, and $\overline{SE3}$ low whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. Tested per AC Test Load, Figure 2.
4. Measured at ± 200 mV from steady state.
5. This parameter is sampled and not 100% tested.
6. In order to reduce test correlation issues and to reduce the effects of application specific input edge rate variations on correlation between data sheet parameters and actual system performance, FSRAM AC parametric specifications are always specified at $V_{DDQ}/2$. In some design exercises, it is desirable to evaluate timing using other reference levels. Since the maximum test input edge rate is known and is given in the AC Test Conditions section of the data sheet as 1 V/ns, one can easily interpolate timing values to other reference levels. Figure 3 shows interpolation to DC V_{IH} and DC V_{IL} levels.

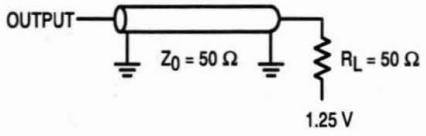


Figure 2. AC Test Load

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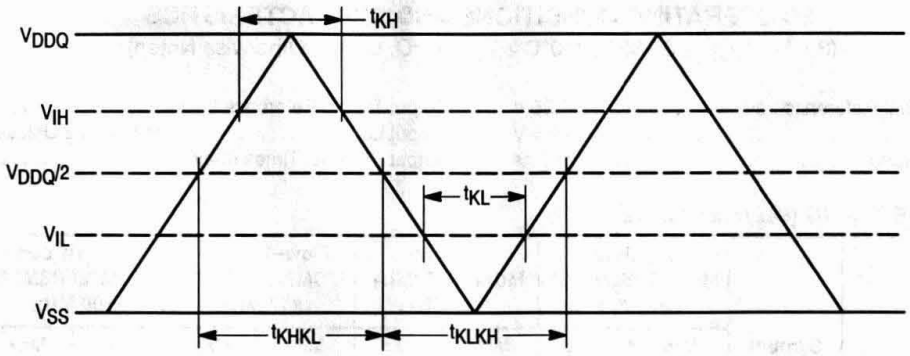
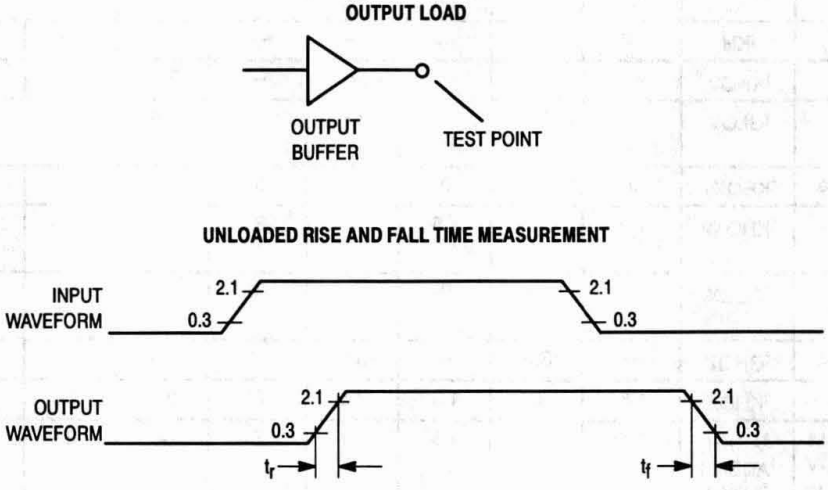


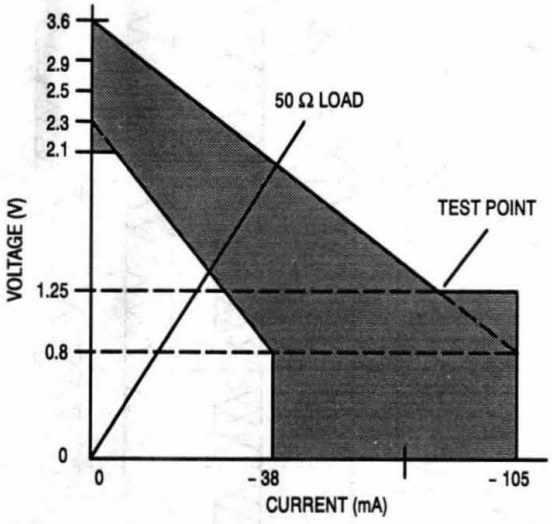
Figure 3. Interpolation to DC V_{IH} and DC V_{IL} Levels



NOTES:
1. Input waveform has a slew rate of 1 V/ns.
2. Rise time is measured from 0.3 to 2.1 V unloaded.
3. Fall time is measured from 2.1 to 0.3 V unloaded.

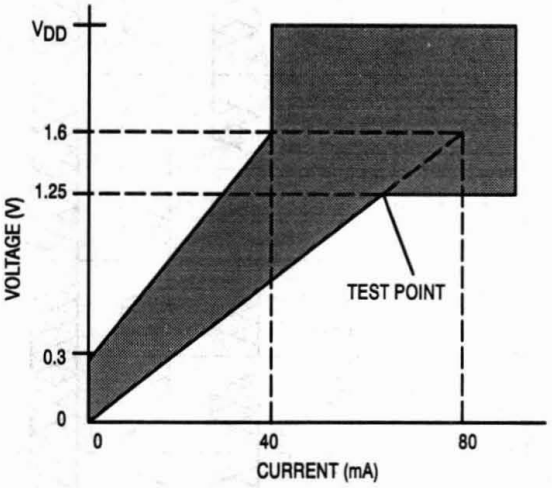
Figure 4. Unloaded Rise and Fall Time Characterization

PULL-UP		
VOLTAGE (V)	I (mA) MIN	I (mA) MAX
- 0.5	- 38	- 105
0	- 38	- 105
0.8	- 38	- 105
1.25	- 26	- 83
1.5	- 20	- 70
2.3	0	- 30
2.7	0	- 10
2.9	0	0
3.4	0	0
3.6	0	0



(a) Pull–Up

PULL-DOWN		
VOLTAGE (V)	I (mA) MIN	I (mA) MAX
- 0.5	0	0
0	0	0
0.4	10	20
0.8	20	40
1.25	31	63
1.6	40	80
2.8	40	80
3.2	40	80
3.4	40	80
3.6	46	120



(b) Pull–Down

Figure 5. Typical Output Buffer Characteristics

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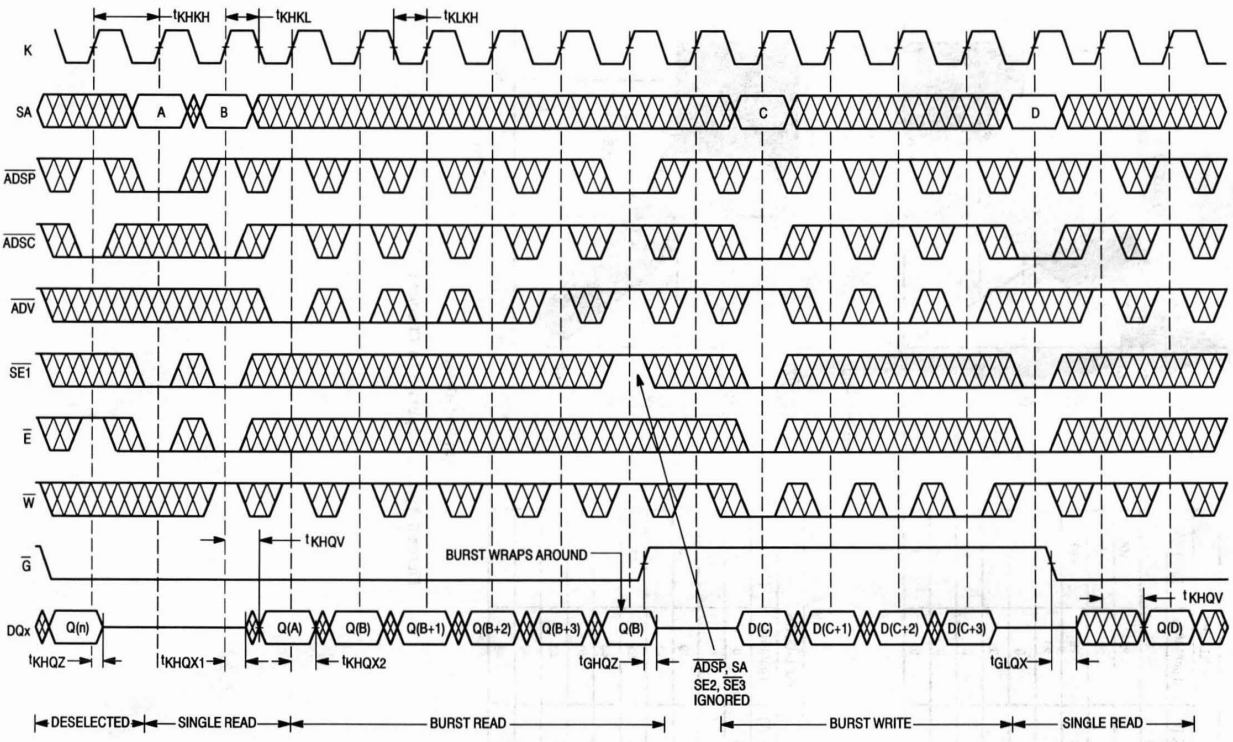
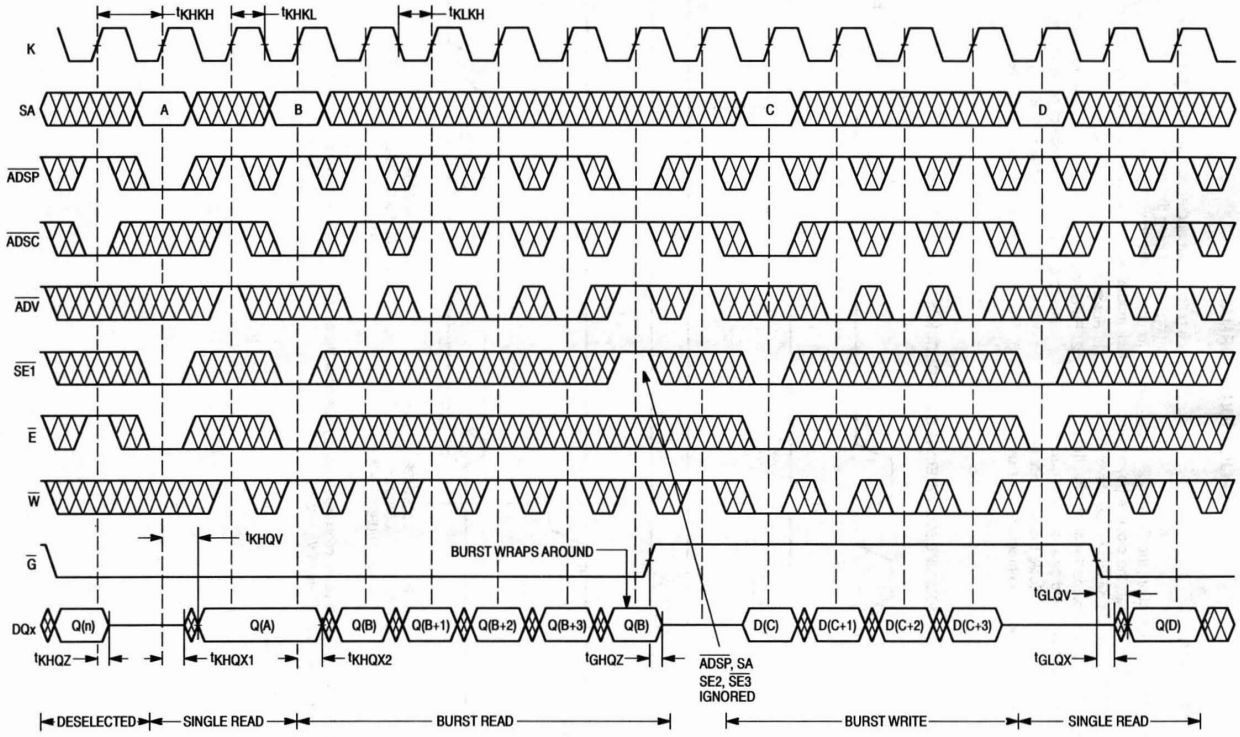
MCM72PB8ML PIPELINE READ/WRITE CYCLES



NOTE: $\overline{E}$ low = SE2 high and $\overline{SE3}$ low.
$\overline{W}$ low = $\overline{SGW}$ low and/or $\overline{SW}$ and $\overline{SBx}$ low.

MCM72FB8ML FLOW–THROUGH READ/WRITE CYCLES



NOTE: $\overline{E}$ low = SE2 high and $\overline{SE3}$ low.
$\overline{W}$ low = $\overline{SGW}$ low and/or $\overline{SW}$ and $\overline{SBx}$ low.

STOP CLOCK OPERATION

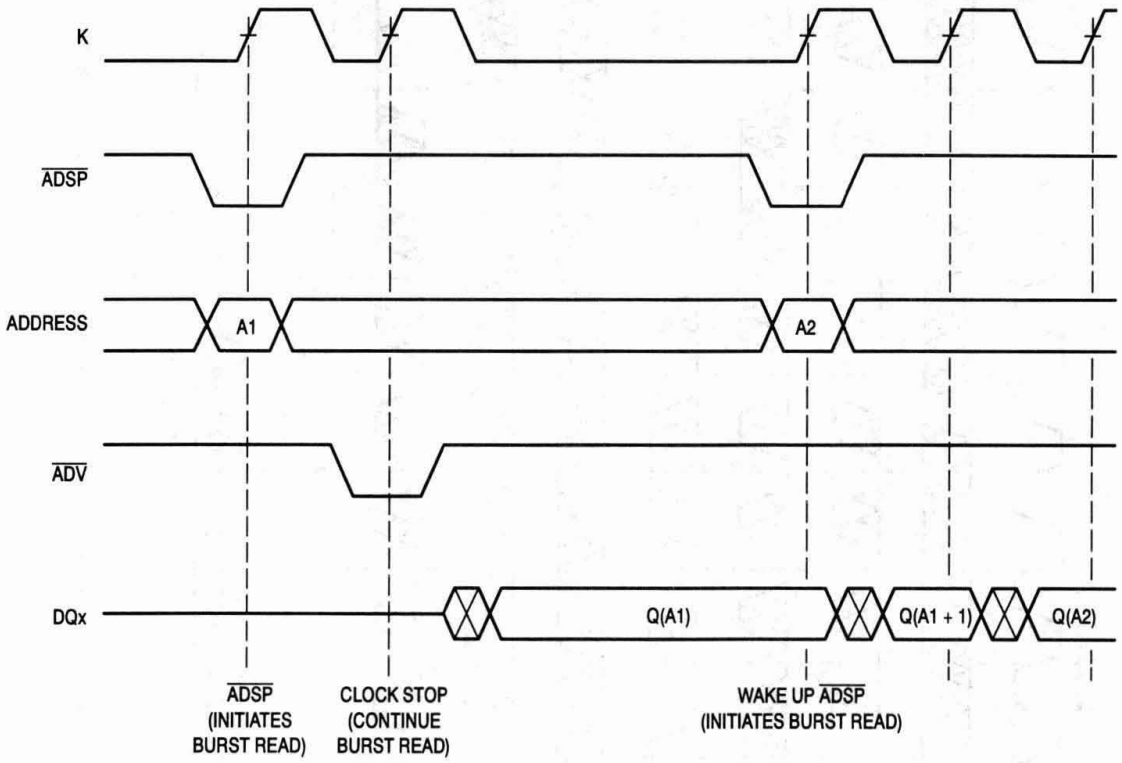
In the stop clock mode of operation, the SRAM will hold all state and data values even though the clock is not running (full static operation). The SRAM design allows the clock to start with $\overline{ADSP}$ and $\overline{ADSC}$, and stops the clock after the last write data is latched, or the last read data is driven out.

When starting and stopping the clock, the AC clock timing and parametrics must be strictly maintained. For example, clock pulse width and edge rates must be guaranteed when starting and stopping the clocks.

To achieve the lowest power operation for all three stop clock modes, stop read, stop write, and stop deselect:

1. Force the clock to a low state.
2. Force the control signals to an inactive state (this guarantees any potential source of noise on the clock input will not start an unplanned on activity).
3. Force the address inputs to a low state.

MCM72PB8ML PIPELINE STOP CLOCK WITH READ TIMING



NOTE: For lowest possible power consumption during stop clock, the addresses should be driven to a low state (V_{IL}). Best results are obtained if $V_{IL} < 0.2$ V.

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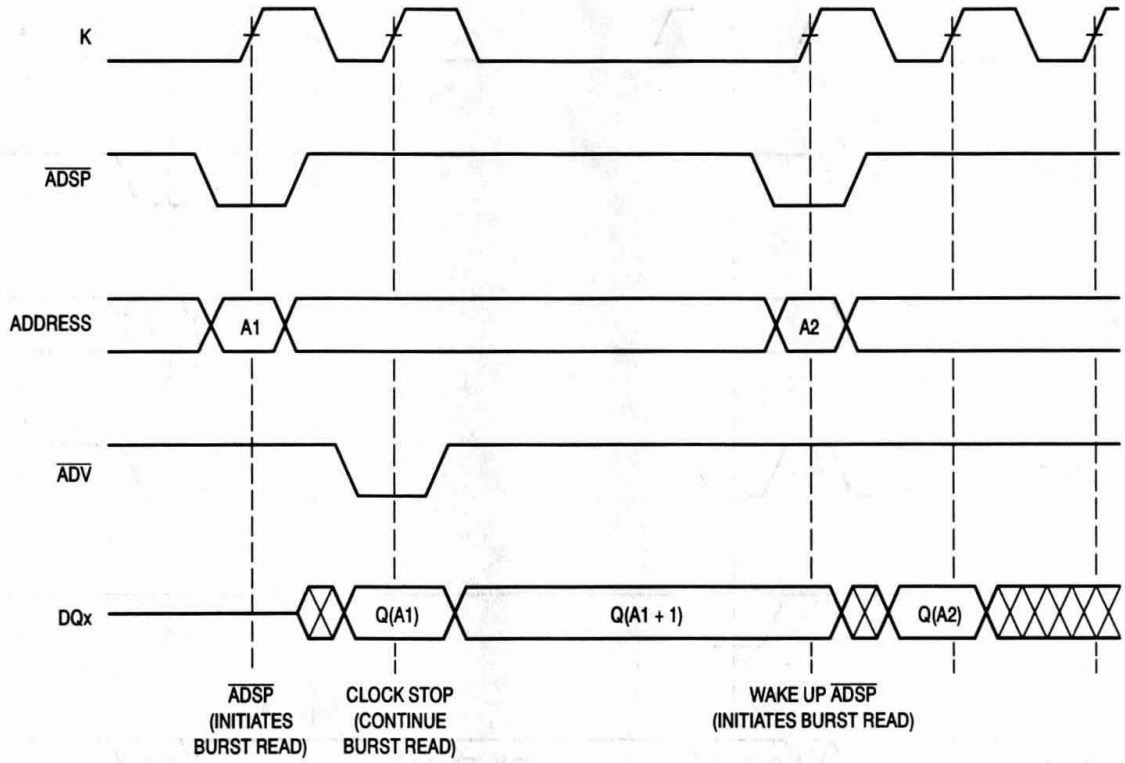
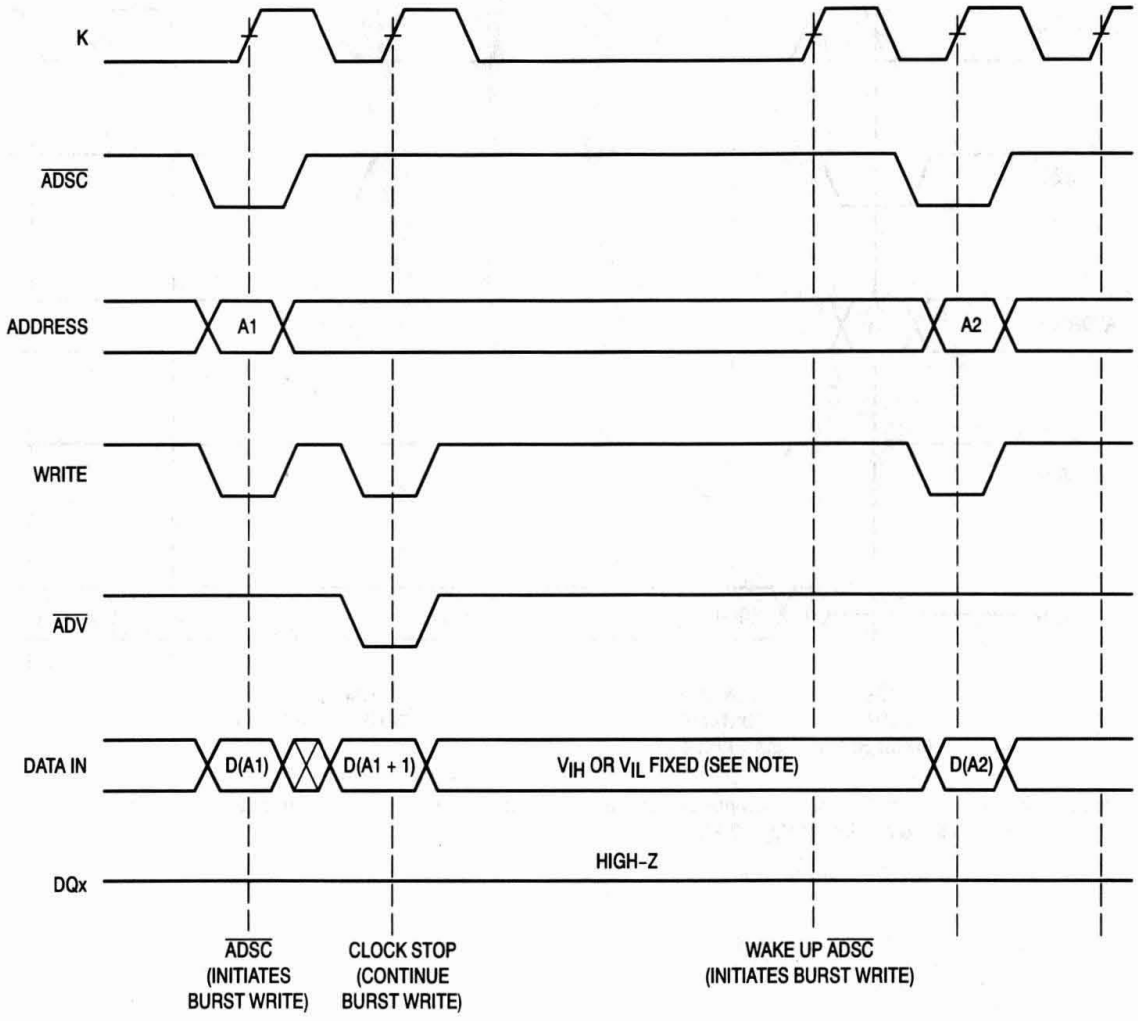
MCM72FB8ML FLOW–THROUGH STOP CLOCK WITH READ TIMING



NOTE: For lowest possible power consumption during stop clock, the addresses should be driven to a low state (V_{IL}). Best results are obtained if V_{IL} < 0.2 V.

6

STOP CLOCK WITH WRITE TIMING



NOTE: While the clock is stopped, DATA IN must be fixed in a high (V_{IH}) or low (V_{IL}) state to reduce the DC current of the input buffers. For lowest power operation, all data and address lines should be held in a low (V_{IL}) state and control lines held in an inactive state.

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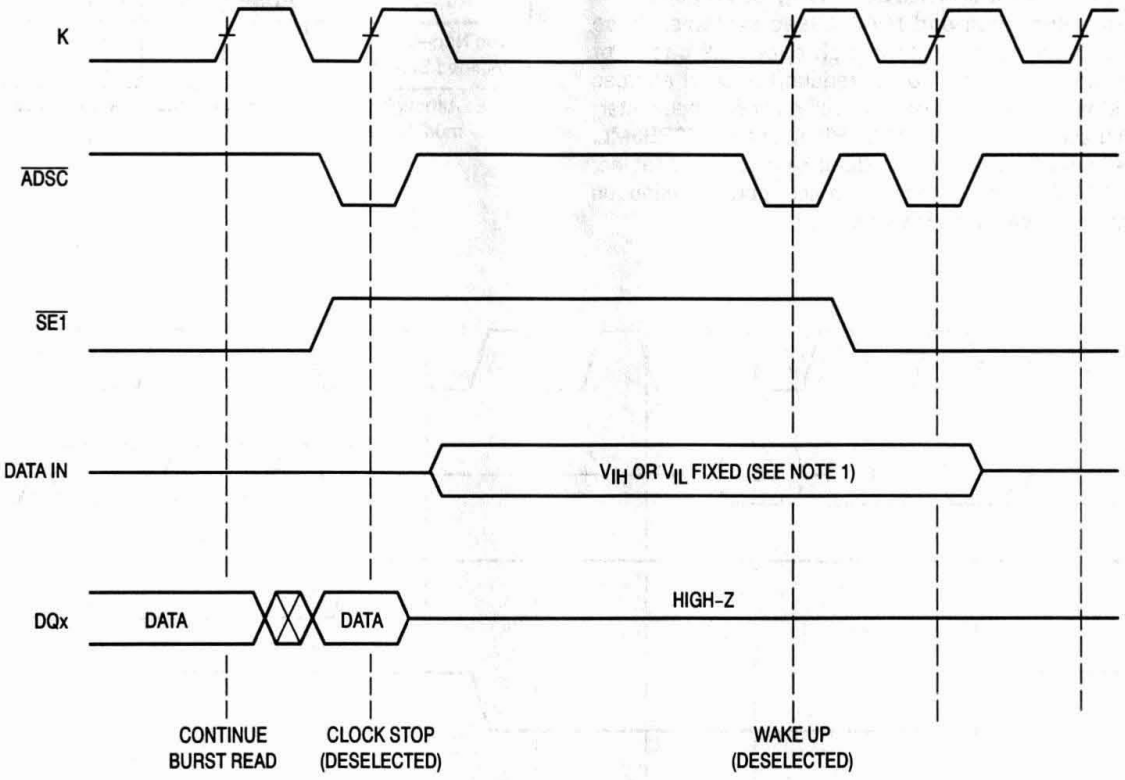
STOP CLOCK WITH DESELECT OPERATION TIMING



NOTES:

1. While the clock is stopped, DATA IN must be fixed in a high (V_{IH}) or low (V_{IL}) state to reduce the DC current of the input buffers. For lowest power operation, all data and address lines should be held in a low (V_{IL}) state and control lines held in an inactive state.
2. For best possible power savings, the data–in should be driven low.

6

NON–BURST SYNCHRONOUS OPERATION

Although this BurstRAM has been designed for PowerPC–based and other high end MPU–based systems, these SRAMs can be used in other high speed L2 cache or memory applications that do not require the burst address feature. Most L2 caches designed with a synchronous interface can make use of the MCM72FB8ML or MCM72PB8ML. The burst counter feature of the BurstRAM can be disabled, and the SRAM can be configured to act upon a continuous stream of addresses. See Figure 6.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

Non–Burst	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
Sync Non–Burst, Pipelined SRAM	H	L	H	L	X

NOTE: Although X is specified in the table as a don't care, the pin must be tied either high or low.

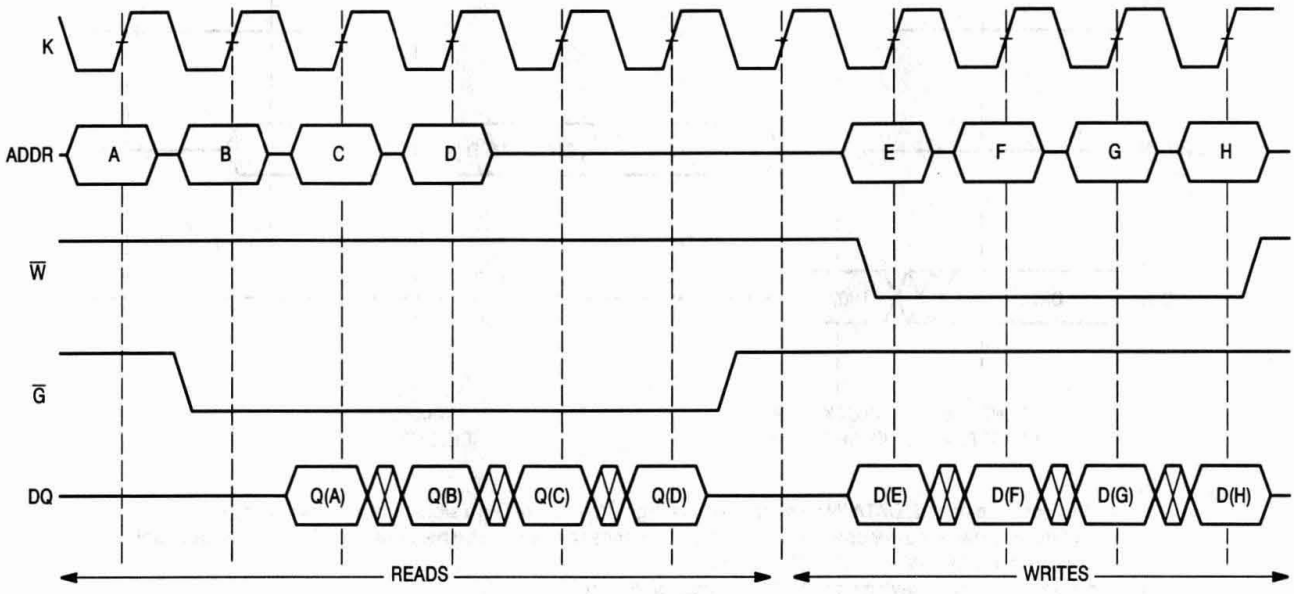


Figure 6. Configured as Non–Burst Synchronous SRAM

6

ORDERING INFORMATION
(Order by Full Part Number)

	MCM	72FB8 72PB8	XX	X	X
Motorola Memory Prefix					
Part Number					
					Blank = Trays, R = Tape and Reel
					Speed for MCM72FB8 (7.5 = 7.5 ns, 8 = 8 ns) Speed for MCM72PB8 (3.5= 3.5 ns, 4 = 4 ns)
					Package (ML = Multichip Module on Laminate)

Full Part Numbers —		
	MCM72FB8ML7.5	MCM72FB8ML8
	MCM72FB8ML7.5R	MCM72FB8ML8R
	MCM72PB8ML3.5	MCM72PB8ML4
	MCM72PB8ML3.5R	MCM72PB8ML4R

512KB and 1MB BurstRAM™ Secondary Cache Modules for PowerPC™ PReP/CHRP Platforms

MPC2105B
MPC2106B

The MPC2105B and the MPC2106B are designed to provide burstable, high performance L2 cache for the PowerPC 60x microprocessor family in conformance with the PowerPC Reference Platform (PReP) and the PowerPC Common Hardware Reference Platform (CHRP) specifications.

The MPC2105B and MPC2106B utilize synchronous BurstRAMs. The modules are configured as 64K x 72, and 128K x 72 bits in a 178 (89 x 2) pin DIMM format. The MPC2105B uses four of the 3 V 64K x 18; the MPC2106B uses eight of the 3 V 64K x 18. For tag bits, a 5 V cache tag RAM configured as 16K x 12 for tag field plus 16K x 2 for valid and dirty status bits is used.

Bursts can be initiated with the $\overline{ADS}$ signal. Subsequent burst addresses are generated internal to the BurstRAM by the $\overline{CNTEN}$ signal.

Write cycles are internally self timed and are initiated by the rising edge of the clock (CLKx) inputs. Eight write enables are provided for byte write control.

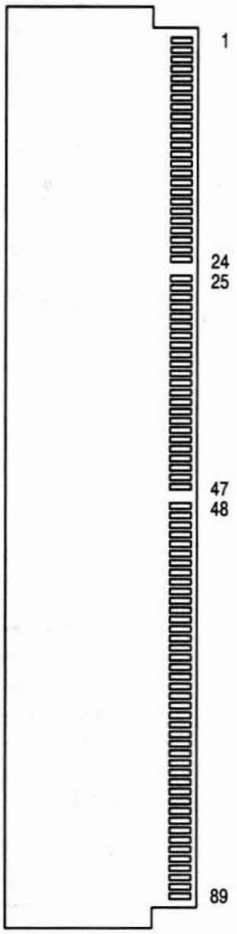
Presence detect pins are available for auto configuration of the cache control.

The module family pinout will support 5 V and 3.3 V components for a clear path to lower voltage and power savings. Both power supplies must be connected.

All of these cache modules are plug and pin compatible with each other.

- PowerPC–style Burst Counter on Chip
- Flow–Through Data I/O
- Plug and Pin Compatibility
- Multiple Clock Pins for Reduced Loading
- All Cache Data and Tag I/Os are LVTTL (3.3 V) Compatible
- Three State Outputs
- Byte Write Capability
- Fast Module Clock Rates: Up to 66 MHz
- Fast SRAM Access Times: 10 ns for Tag RAM Match
  9 ns for Data RAM
- Decoupling Capacitors for Each Fast Static RAM
- High Quality Multi–Layer FR4 PWB With Separate Power and Ground Planes
- 178 Pin Card Edge Module
- Burndy Connector, Part Number: ELF178KSC–3Z50

178–LEAD CARD EDGE
TOP VIEW
MPC2105B CASE 1132A–01
MPC2106B CASE 1132–01



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BurstRAM is a trademark of Motorola.
The PowerPC name is a trademark of IBM Corp., used under license therefrom.

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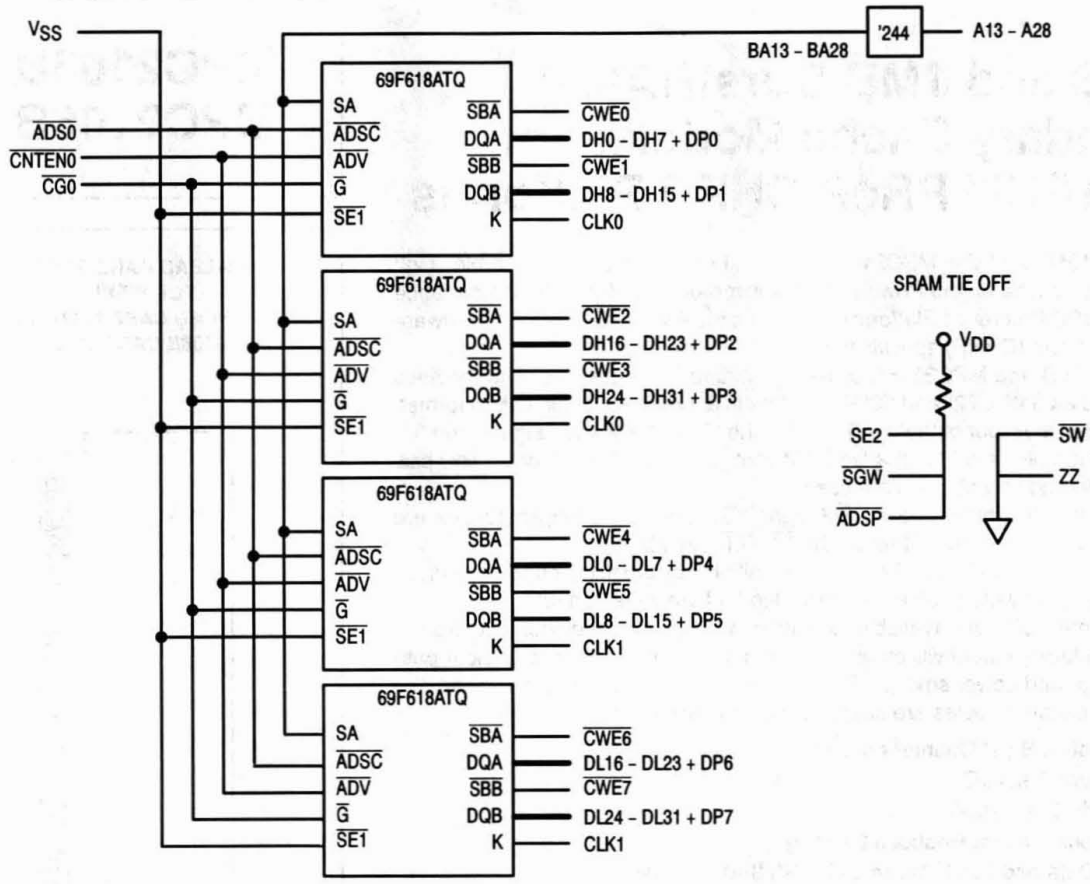
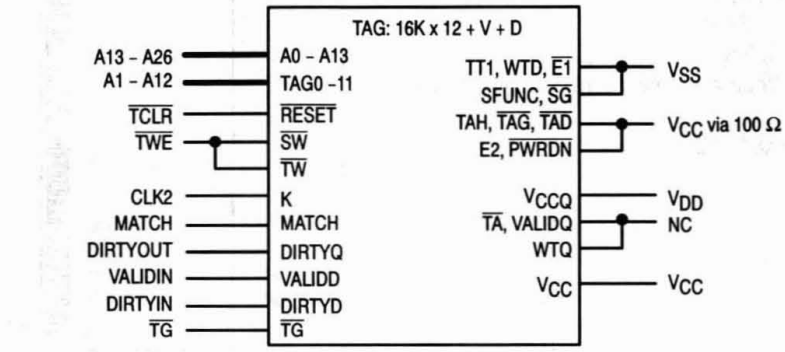
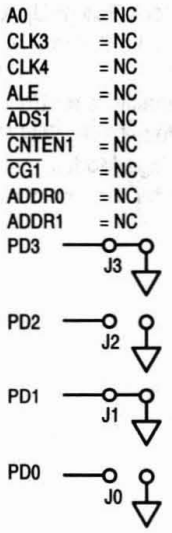
MPC2105B BLOCK DIAGRAM

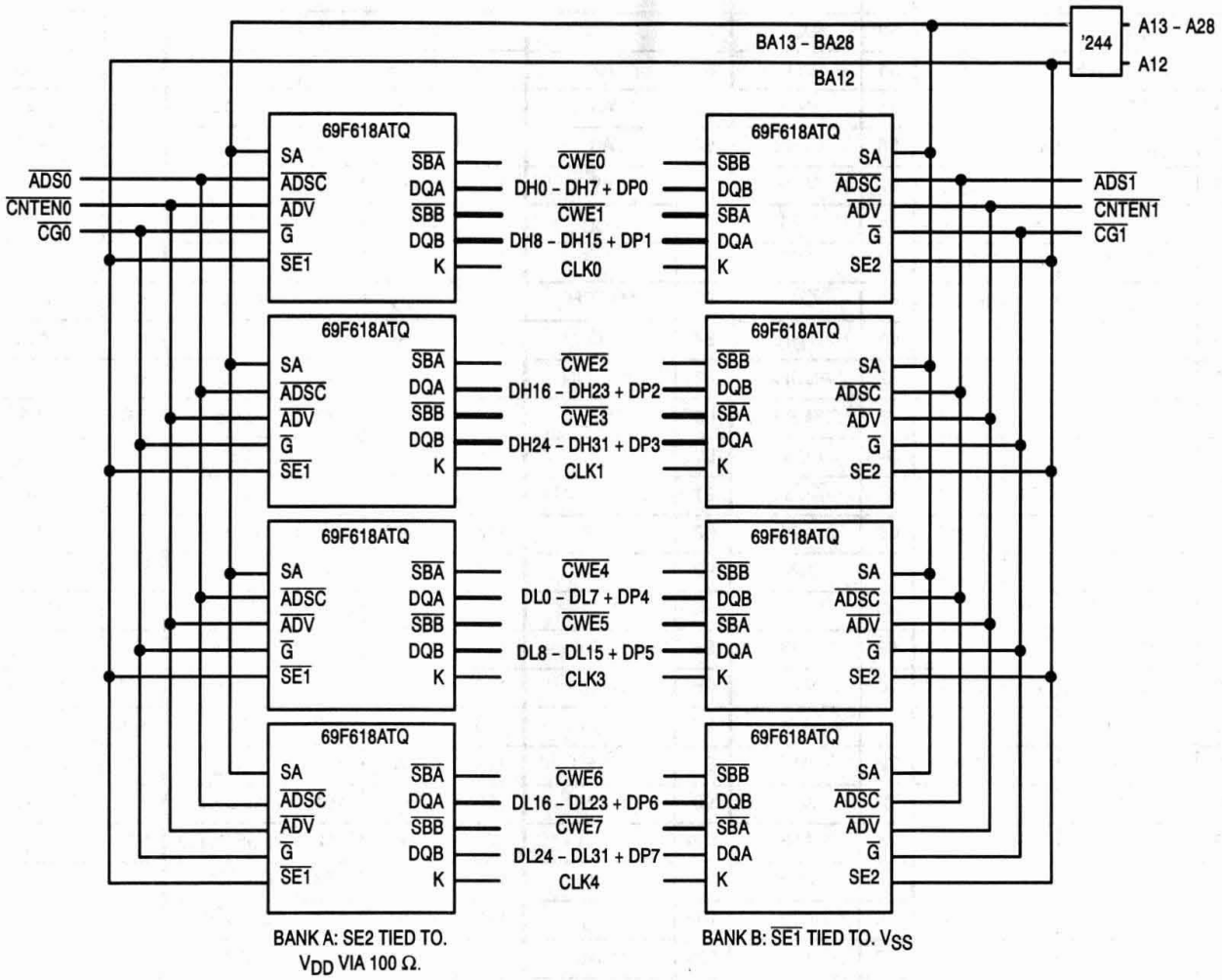


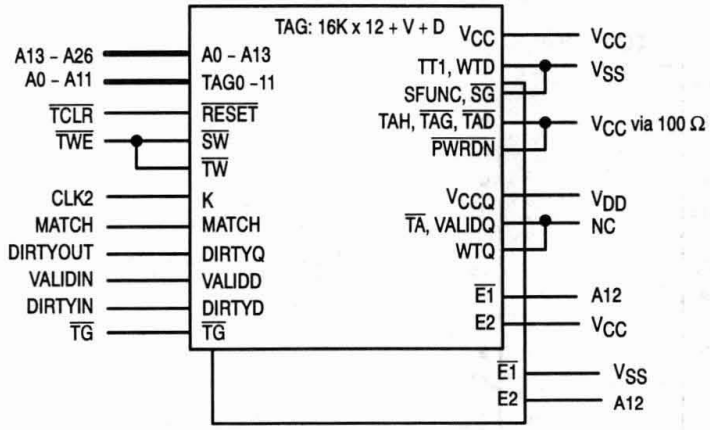




Note: BA28 is tied to SA0 on SRAM;
BA27 is tied to SA1 on SRAM;
STANDBY is tied to $\overline{SE3}$ on SRAM.

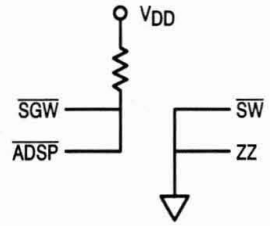
MPC2106B BLOCK DIAGRAM



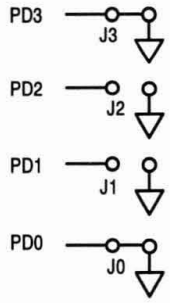


Note: BA28 is tied to SA0 on SRAM;
BA27 is tied to SA1 on SRAM;
STANDBY is tied to SE3 on SRAM.

SRAM TIE OFF



ALE = NC
ADDR0 = NC
ADDR1 = NC



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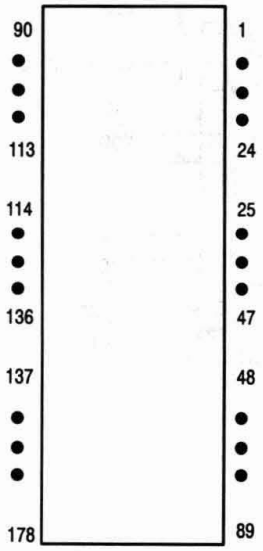
PIN ASSIGNMENT 178–LEAD DIMM

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	27	DH0	53	DL1	79	V_{SS}	105	DH14	131	DL17	157	A22
2	PD0/IDSCLK	28	DP0	54	DL0	80	A7	106	DH13	132	$\overline{CWE6}$	158	A20
3	PD2	29	V_{SS}	55	V_{SS}	81	A5	107	V_{CC}	133	DL15	159	V_{SS}
4	DH30	30	CLK1	56	CLK2	82	A3	108	DH10	134	DL13	160	A18
5	DH28	31	V_{SS}	57	V_{SS}	83	A0	109	DH8	135	V_{SS}	161	A16
6	DH26	32	DL28	58	DP4	84	V_{CC}	110	$\overline{CWE1}$	136	DL10	162	A15
7	DH24	33	DL26	59	$\overline{CG0}$	85	$\overline{TCLR}$	111	DH6	137	DL8	163	A14
8	V_{DD}	34	DL24	60	$\overline{CG1}$	86	MATCH	112	V_{DD}	138	$\overline{CWE5}$	164	V_{DD}
9	DP3	35	DP7	61	V_{DD}	87	$\overline{TG}$	113	DH4	139	DL6	165	A10
10	DH22	36	V_{CC}	62	ADDR0	88	DIRTYIN	114	V_{SS}	140	V_{DD}	166	A8
11	DH20	37	DL22	63	RESERVED	89	V_{SS}	115	CLK0	141	DL5	167	A6
12	DH19	38	DL20	64	$\overline{ADS0}$	90	V_{SS}	116	V_{SS}	142	DL2	168	V_{SS}
13	V_{SS}	39	DL18	65	$\overline{ADS1}$	91	PD1/IDSDATA	117	DH1	143	V_{SS}	169	A4
14	DH17	40	DL16	66	A28	92	PD3	118	$\overline{CWE0}$	144	CLK3	170	A2
15	DP2	41	V_{SS}	67	A26	93	DH31	119	DL31	145	V_{SS}	171	A1
16	DH15	42	DP6	68	A25	94	DH29	120	DL30	146	CLK4	172	BURSTMODE
17	DH12	43	DL14	69	A23	95	DH27	121	V_{SS}	147	V_{SS}	173	V_{CC}
18	V_{CC}	44	DL12	70	V_{SS}	96	DH25	122	DL29	148	$\overline{CWE4}$	174	VALIDIN
19	DH11	45	DL11	71	A21	97	V_{DD}	123	DL27	149	ALE	175	$\overline{TWE}$
20	DH9	46	V_{SS}	72	A19	98	$\overline{CWE3}$	124	DL25	150	V_{DD}	176	STANDBY
21	DP1	47	DL9	73	A17	99	DH23	125	V_{CC}	151	ADDR1	177	DIRTYOUT
22	DH7	48	DP5	74	A13	100	DH21	126	$\overline{CWE7}$	152	RESERVED	178	V_{SS}
23	V_{DD}	49	DL7	75	V_{DD}	101	DH18	127	DL23	153	$\overline{CNTEN0}$		
24	DH5	50	DL4	76	A12	102	V_{SS}	128	DL21	154	$\overline{CNTEN1}$		
25	DH3	51	V_{DD}	77	A11	103	DH16	129	DL19	155	A27		
26	DH2	52	DL3	78	A9	104	$\overline{CWE2}$	130	V_{SS}	156	A24		

NOTE: V_{CC} and V_{DD} must be connected on all modules.

TOP VIEW



PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
66, 67, 68, 69, 71, 72, 73, 74, 76, 77, 78, 80, 81, 82, 83, 155, 156, 157, 158, 160, 161, 162, 163, 165, 166, 167, 169, 170, 171	A0 – A28	Input	Address Inputs – (MSB:0, LSB:28).
62	ADDR0	Input	Least significant address bit when asynchronous Data RAMs are used.
151	ADDR1	Input	Next to least significant address bit when asynchronous Data RAMs are used.
64, 65	$\overline{ADS0}$, $\overline{ADS1}$	Input	Data RAM Address Strobe – For MPC2105B use $\overline{ADS0}$ only. For MPC2106B use $\overline{ADS0}$, $\overline{ADS1}$..
149	ALE	Input	Data RAM Address Latch Enable – Use for asynchronous Data RAM only.
172	BURSTMODE	Input	Burstmode. 0 = Linear, 1 = Interleaved.
59, 60	$\overline{CG0}$, $\overline{CG1}$	Input	Data RAM Output Enables. – For MPC2105B use $\overline{CG0}$ only. For MPC2106B use $\overline{CG0}$, $\overline{CG1}$.
30, 56, 115, 144, 146	CLK0 – CLK4	Input	Clock Inputs – CLK2 is for Tag RAM, CLK0, 1, 3, and 4 are for Data RAMs only. For MPC2106B use all the clocks. For MPC2105B use CLK0 – CLK2 only.
153, 154	$\overline{CNTEN0}$, $\overline{CNTEN1}$	Input	Data RAM Count Enables – For MPC2105B use $\overline{CNTEN0}$ only. For MPC2106B use $\overline{CNTEN0}$, $\overline{CNTEN1}$.
98, 104, 110, 118, 126, 132, 138, 148	$\overline{CWE0}$ – $\overline{CWE7}$	Input	Data RAM Write Enables – (MSB:0, LSB:7).
4, 5, 6, 7, 10, 11, 12, 14, 16, 17, 19, 20, 22, 24, 25, 26, 27, 93, 94, 95, 96, 99, 100, 101, 103, 105, 106, 108, 109, 111, 113, 117	DH0 – DH31	I/O	High Data Bus – (MSB:0, LSB:31).
88	DIRTYIN	Input	Dirty input bit.
177	DIRTYOUT	Output	Dirty output bit.
32, 33, 34, 37, 38, 39, 40, 43, 44, 45, 47, 49, 50, 52, 53, 54, 119, 120, 122, 123, 124, 127, 128, 129, 131, 133, 134, 136, 137, 139, 141, 142	DL0 – DL31	I/O	Low Data Bus – (MSB:0, LSB:31).
9, 15, 21, 28, 35, 42, 48, 58	DP0 – DP7	I/O	Data Parity Bits – (MSB:0, LSB:7)
86	MATCH	Output	Tag RAM active high match indication.
2	PD0/IDSCLK	Input	Presence detect bit 0/EEPROM serial clock. (EEPROM option only).
91	PD1/IDSDATA	I/O	Presence detect bit 1/EEPROM serial data. (EEPROM option only).
3, 92	PD2, PD3	Output	Presence detect bits.
63, 152	RESERVED		Reserved pin.
176	STANDBY	Input	Standby pin. Reduces standby power consumption.
85	$\overline{TCLR}$	Input	Tag RAM clear.
87	$\overline{TG}$	Input	Tag RAM output enable.
175	$\overline{TWE}$	Input	Tag RAM write enable.
174	VALIDIN	Input	Tag RAM valid bit.
18, 36, 84, 107, 125, 173	V_{CC}	Input	+ 5 V power supply. Must be connected.
8, 23, 51, 61, 75, 97, 112, 140, 150, 164	V_{DD}	Input	+ 3.3 V power supply. Must be connected.
1, 13, 29, 31, 41, 46, 55, 57, 70, 79, 89, 90, 102, 114, 116, 121, 130, 135, 143, 145, 147, 159, 168, 178	V_{SS}	Input	Ground.

DATA RAM MCM69F618A SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

STANDBY	$\overline{ADSx}$	$\overline{CNTENx}$	$\overline{CWEx}$	CLKx	Address Used	Operation
H	L	X	X	L–H	N/A	Deselected
L	L	X	L	L–H	External Address	Write Cycle, Begin Burst
L	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{CG}$ must meet set–up and hold times for the low–to–high transition of clock (CLK0 – CLK4).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{CG}$	I/O Status
Read	L	Data Out (DQ0 – DQ8)
Read	H	High–Z
Write	X	High–Z — Data In
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{CG}$ must be high before the input data required set–up time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS}		V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	Data RAM Tag	I_{out}	± 30 ± 20	mA
Power Dissipation	MPC2105B MPC2106B	P_D	4.6 9.2	W
Temperature Under Bias		T_{bias}	– 10 to + 85	°C
Operating Temperature		T_A	0 to +70	°C
Storage Temperature		T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, V_{DD} = 3.3 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC} V_{DD}	4.75 3.00	5.25 3.60	V
Input High Voltage	V_{IH}	2.2	V_{DD} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{DD} + 0.3 V dc; V_{IH} (max) = V_{DD} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{DD})	Data RAM Tag	$I_{lkg(I)}$	—	± 1.0 ± 5.0	µA
Output Leakage Current ($\overline{CG}$ = V_{IH}, V_{out} = 0 to V_{DD})	Data RAM Tag	$I_{lkg(O)}$	—	± 1.0 ± 5.0	µA
TTL Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
TTL Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter		Symbol	Max	Unit
AC Supply Current (CG = V_{IH}, E = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ 20 ns)	MPC2105B MPC2106B	I_{DDA}	900 1800	mA
	MPC2105B MPC2106B	I_{CCA}	320 640	mA
AC Standby Current (E = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH} V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ 20 ns)	MPC2105B MPC2106B	$I_{SB1}(V_{DD})$	440 880	mA
	MPC2105B MPC2106B	$I_{SB1}(V_{CC})$	320 640	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	(A13 – A28) (Data RAM Control Pins) (CLK0 – CLK4) (Tag Control Pins)	C_{in}	— 16 8 —	15 20 10 5	pF
Tag Output Capacitance	(MATCH, DIRTYOUT)	C_{out}	—	7	pF
Data RAM Input/Output Capacitance	(DH0 – DH31, DL0 – DL31)	$C_{I/O}$	6	8	pF
Tag Input/Output Capacitance	(A0 – A11)	$C_{I/O}$	—	7	pF

6

DATA RAMs AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, V_{DD} = 3.3 V ± 10% T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1 Unless Otherwise Noted

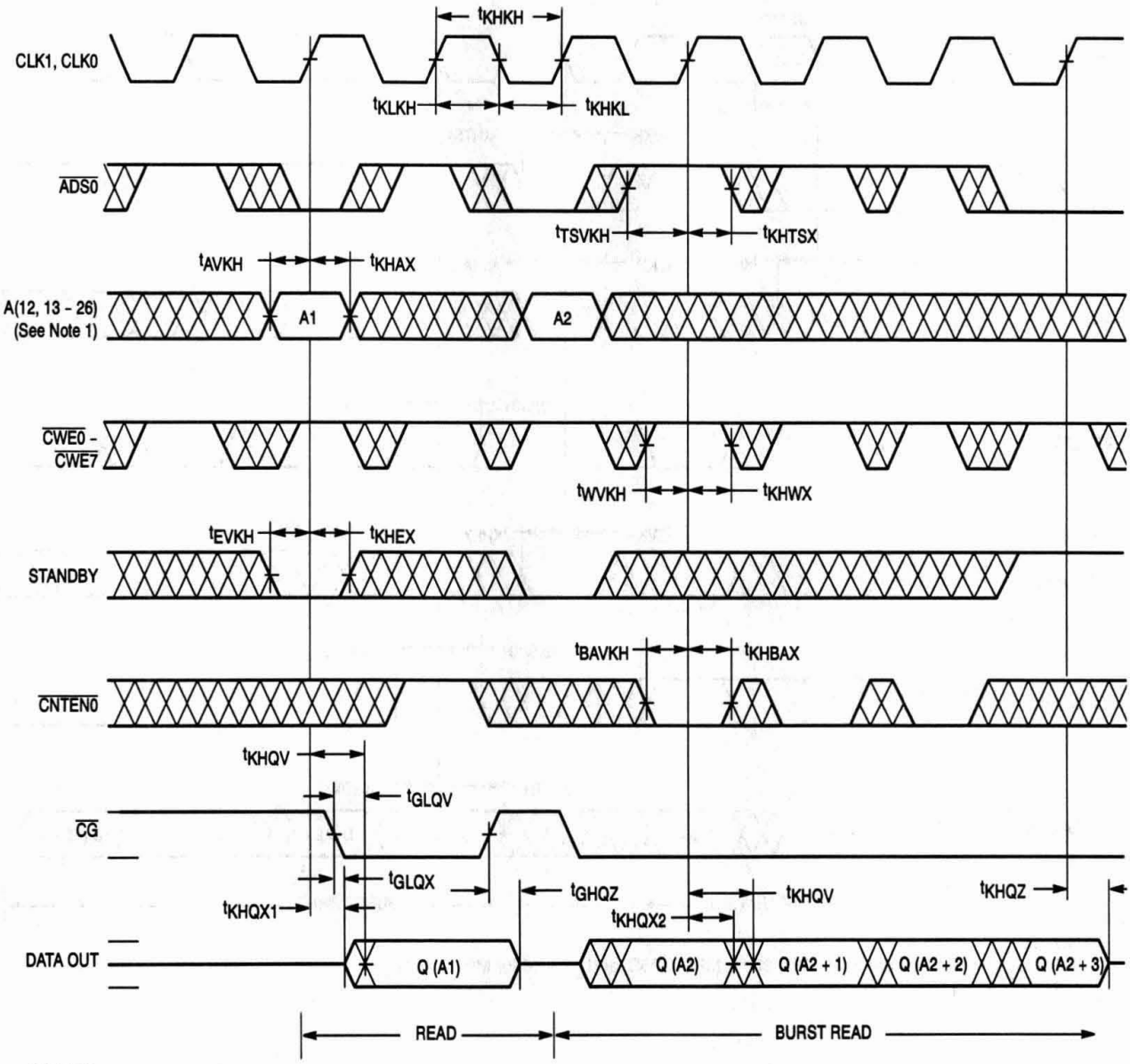
SYNCHRONOUS DATA RAMs READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter		Symbol	MPC2105B MPC2106B Min	MPC2105B MPC2106B Max	Unit	Notes
Cycle Time		t_{KHKH}	15	—	ns	
Clock Access Time		t_{KHQV}	—	9	ns	4
Output Enable to Output Valid		t_{GLQV}	—	5	ns	
Clock High to Output Active		t_{KHQX1}	6	—	ns	
Clock High to Output Change		t_{KHQX2}	3	—	ns	
Output Enable to Output Active		t_{GLQX}	0	—	ns	
Output Disable to Q High–Z		t_{GHQZ}	2	6	ns	
Clock High to Q High–Z		t_{KHQZ}	—	6	ns	
Clock High Pulse Width		t_{KHKL}	5	—	ns	
Clock Low Pulse Width		t_{KLKH}	5	—	ns	
Setup Time	Address	t_{AVKH}	7.5	—	ns	5, 6
Setup Times:	Address Status Data In Write Address Advance Chip Enable	t_{SVKH} t_{DVKH} t_{WVKH} t_{BAVKH} t_{EVKH}	2.5	—	ns	5
Hold Times:	Address Address Status Data In Write Address Advance Chip Enable	t_{KHAX} t_{KHTSX} t_{KHDX} t_{KHWX} t_{KHBAX} t_{KHEX}	0.5	—	ns	5

6

NOTES:
1. In setup and hold times, W (write) refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. All read and write cycle timings are referenced from CLK or $\overline{CG}$.
3. $\overline{CG}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
4. Maximum access times are guaranteed for all possible PowerPC external bus cycles.
5. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of CLK whenever $\overline{TSP}$ or $\overline{TSC}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of CLK when the chip is enabled. Chip enable must be valid at each rising edge of clock for the device (when $\overline{TSP}$ or $\overline{TSC}$ is low) to remain enabled.
6. 5 ns of setup delay is incurred in address buffers.

SYNCHRONOUS DATA RAM READ CYCLE



NOTES:
1. Cache addresses used are: 13 – 26 for MPC2105B; and 12 – 26 for MPC2106B.
2. Q1 (A2) represents the first ouput from the external address A2; Q2 (A2) represents the next output data in the burst sequence with A2 as the base address.

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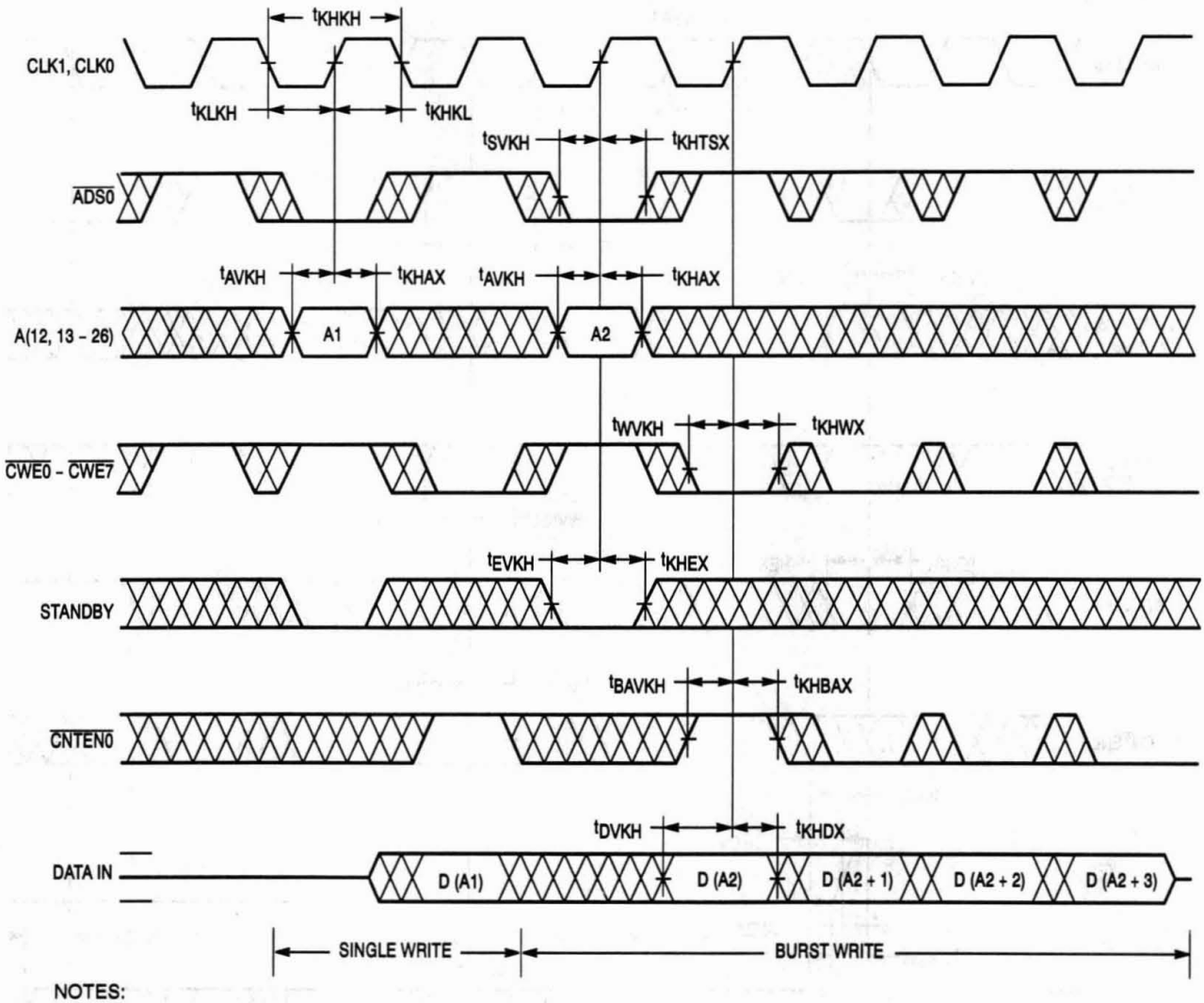
SYNCHRONOUS DATA RAM WRITE CYCLE



NOTES:
1. Cache addresses used are: 13 – 26 for MPC2105B; and 12 – 26 for MPC2106B.
2. $\overline{CG0} = V_{IH}$

6

RESET FUNCTION TRUTH TABLE (See Notes 1 and 2)

$\overline{TCLR}$	CLK	$\overline{TWE}$	TAG0 – TAG11	DIRTYOUT	MATCH	Operation	POWER
L	L – H	H	High–Z	L(3)	L(3)	Reset Status	Active
L	L – H	L	—	—	—	Not Allowed	—

NOTES:
1. H = V_{IH}, L = V_{IL}, X = don't care, — = undefined.
2. $\overline{TG}$ is X for this table.
3. These are output states.

READ FUNCTION TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{TG}$	$\overline{TWE}$	CLK	TAG0 – TAG11	VALIDIN	DIRTYIN	DIRTYOUT	MATCH	Operation
L	H	X	D_{out}	—	—	D_{out}	D_{out}	Read Tag I/O
H	X	X	High–Z	—	—	—	—	Tag I/O Disable

WRITE FUNCTION TRUTH TABLE (See Notes 1 and 2)

$\overline{TG}$	$\overline{TWE}$	CLK	TAG0 – TAG11	VALIDIN	DIRTYIN	DIRTYOUT	MATCH	Operation
H	L	L – H	D_{in}	—	—	—	L	Write Tag I/O
L	L	L – H	—	—	—	—	—	Not Allowed

NOTES:
1. H = V_{IH}, L = V_{IL}, X = don't care, — = undefined.
2. This table applies when $\overline{RESET}$ and $\overline{PWRDN}$ are high.
3. D_{out} in this case is the same as D_{in}. The input data is written through to the outputs during the write operation.

MATCH FUNCTION TRUTH TABLE (See Notes 1 through 4)

$\overline{TG}$	$\overline{TWE}$	TAG0 – TAG11	VALIDIN(4)	DIRTYIN(4)	MATCH	Operation
X	X	—	—	—	D_{out}	Selected
L	H	D_{out}	—	—	L	Read Tag I/O
H	L	D_{in}	D_{in}	D_{in}	L	Write Tag I/O, Status Bits
H	H	TAG_{in}	L	—	L	Invalid Data – Dedicated Status Bits
H	H	TAG_{in}	H	—	H	Match – Dedicated Status Bits

NOTES:
1. H = V_{IH}, L = V_{IL}, X = don't care, — = undefined.
2. M = high if TAG_{in} equals the memory contents at the address; M = low if TAG_{in} does not equal the contents at that address.
3. $\overline{PWRDN}$ and $\overline{RESET}$ are high for this table. $\overline{GS}$ and CLK are X.
4. This column represents the stored memory cell data for the given status bit at the selected address.

TAG RAM AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... Figure 1 Unless Otherwise Noted

TAG RAM READ CYCLE (See Notes 1 through 4)

Parameter	Symbol	Tag RAM		Unit
		Min	Max	
Clock Access Time	t_{KHQV}	—	10	ns
Output Enable to Output Valid	t_{GLQV}	—	8	ns
Output Enable to Output Active	t_{GLQX}	0	—	ns
Output Disable to Q High–Z	t_{GHQZ}	1	6	ns
Status Bit Hold from Address Change	t_{AXSX}	3	—	ns
Address Access Time Status Bits	t_{AVSV}	—	10	ns
Tag Bit Hold from Address Change	t_{AVQX}	3	—	ns
Address Access Time Tag Bits	t_{AVQV}	—	12	ns

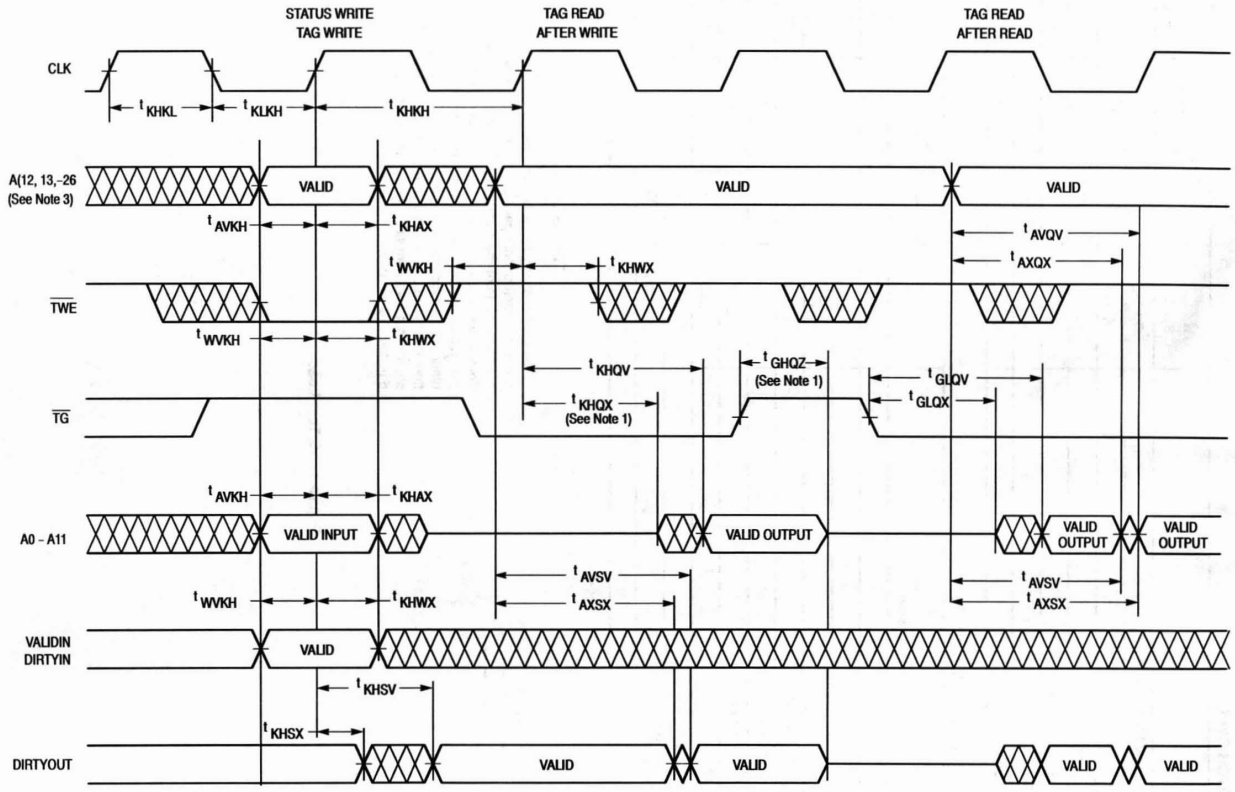
NOTES:
1. Setup and hold times, W (write) refers to $\overline{TWE}$.
2. A read cycle is defined by $\overline{TWE}$ high. A write cycle is defined by $\overline{TWE}$ low.
3. Maximum access times are guaranteed for all possible MC68040 and PowerPC external bus cycles.
4. Tag reads are asynchronous.

TAG RAM WRITE CYCLE (See Notes 1 through 4)

Parameter		Symbol	Tag RAM		Unit
			Min	Max	
Cycle Time		t_{KHKH}	15	—	ns
Clock High Pulse Width		t_{KHKL}	4.5	—	ns
Clock Low Pulse Width		t_{KLKH}	4.5	—	ns
Clock High to Output Active		t_{KHQX}	1.5	—	ns
Setup Times	Address Write	t_{AVKH} t_{WVKH}	3	—	ns
Hold Times	Address Write	t_{KHAX} t_{KHWX}	1.5	—	ns
Status Output Hold		t_{KHSX}	0	—	ns
Clock High to Status Bits Valid		t_{KHSV}	—	9	ns

NOTES:
1. Setup and hold times, W (write) refers to $\overline{TWE}$.
2. A read cycle is defined by $\overline{TWE}$ high. A write cycle is defined by $\overline{TWE}$ low.
3. Maximum access times are guaranteed for all possible MC68040 and PowerPC external bus cycles.
4. Tag writes are synchronous.

TAG RAM WRITE AND READ CYCLES (See Note 2)



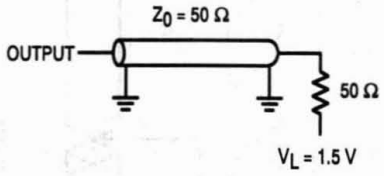
NOTES:
1. Transition is measured plus or minus 200 mV from steady state.
2. $\overline{TCLR}$ = High.
3. Cache addresses used are: A13 – A26 for MPC2105B, A12 – A26 for MPC2106B.

TAG RAM MATCH CYCLE

Parameter	Symbol	Tag RAM		Unit
		Min	Max	
Clock High Write to MATCH Invalid	t_{KHML}	—	7	ns
Clock High Read to MATCH Valid	t_{KHMV}	—	10	ns
Address Valid to MATCH Valid	t_{AVMV}	—	10	ns
MATCH Valid Hold from Address Change	t_{AXMX}	2	—	ns
$\overline{TG}$ Low to MATCH Invalid	t_{GLML}	—	7	ns
$\overline{TG}$ High to MATCH Valid	t_{GHMX}	—	8	ns

TAG RAM RESET ($\overline{TCLR}$) CYCLE

Parameter	Symbol	Tag RAM		Unit
		Min	Max	
$\overline{TCLR}$ Setup Time	t_{STC}	4	—	ns
$\overline{TCLR}$ Hold Time	t_{HTC}	1	—	ns
Status Bit Reset Time	t_{SRST}	—	60	ns
Status Bit Hold from $\overline{TCLR}$ Low	t_{SHRS}	2	—	ns
$\overline{TCLR}$ Low to MATCH Invalid	t_{RSML}	—	10	ns
$\overline{TCLR}$ High to MATCH Valid	t_{RSMV}	—	100	ns
$\overline{TCLR}$ Low to TAG High–Z	t_{RSQZ}	—	10	ns
$\overline{TCLR}$ High to TAG Active	t_{RSQX}	—	100	ns
STANDBY Setup to $\overline{TCLR}$ Low	t_{PDSR}	30	—	ns
$\overline{TCLR}$ High to $\overline{TWE}$ Low	t_{RHWX}	80	—	ns

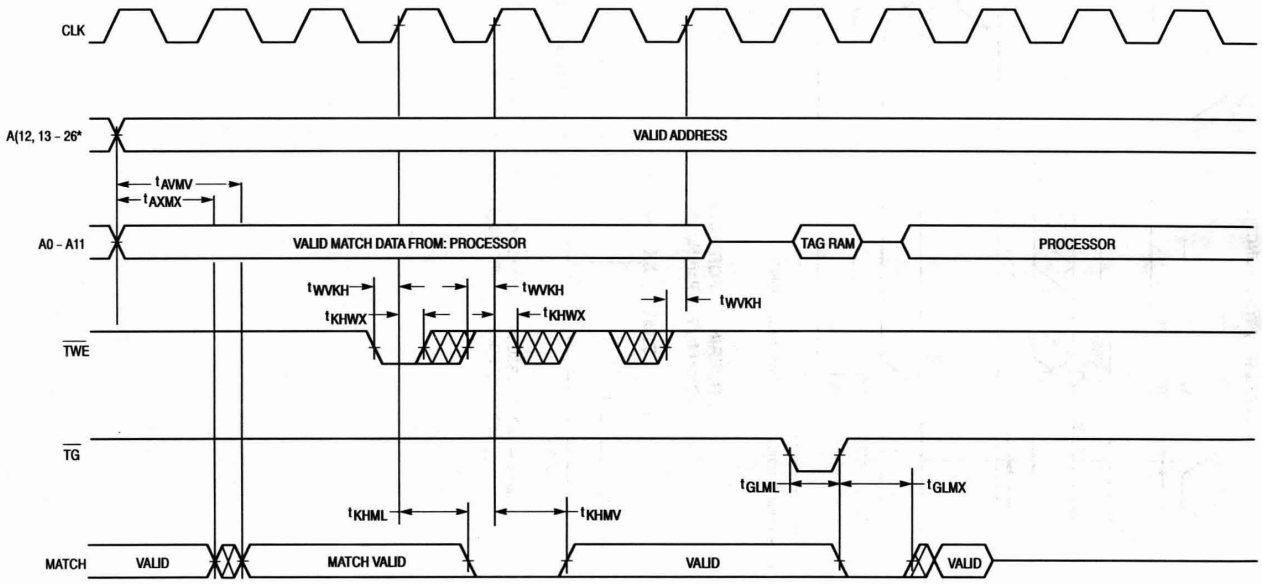


TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

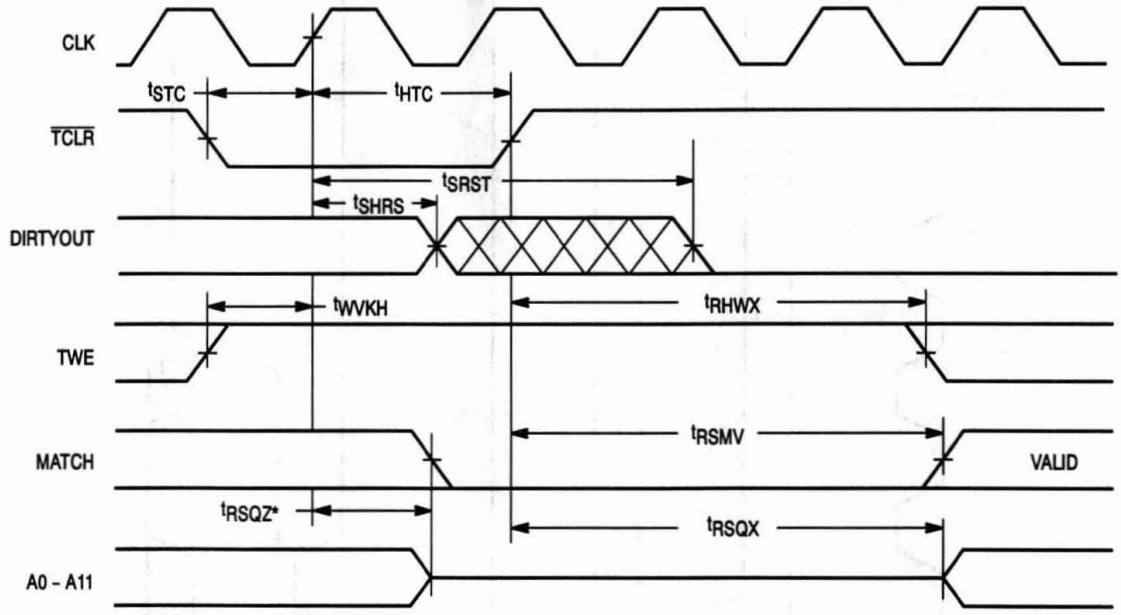
Figure 1. AC Test Load

TAG RAM MATCH CYCLE



* Cache addresses used are: A13 – A26 for MPC2105B, A12 – A26 for MPC2106B.

TAG RAM $\overline{\text{TCLR}}$ FUNCTION



* Transition is measured plus or minus 200 mV from steady state.

ORDERING INFORMATION
(Order by Full Part Number)

MPC 210xB XX XX

- MPC — Motorola Memory Prefix
- 210xB — Part Number
- XX — Package (SG = Gold Pad SIMM)
- XX — Speed (66 = 66 MHz)

Full Part Numbers — MPC2105BSG66 (MPC2105B = 512KB, synchronous)
MPC2106BSG66 (MPC2106B = 1MB, synchronous)

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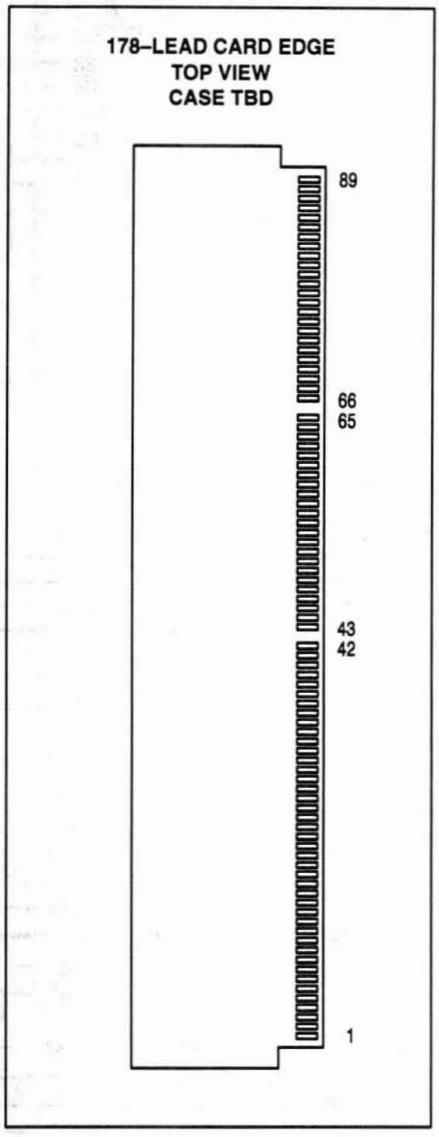
MPC2105P

Product Preview

512KB BurstRAM™ Secondary Cache Module for PowerPC™ PReP/CHRP Platforms



The MPC2105P (512KB) is designed to provide burstable, high performance L2 cache for the PowerPC 60x microprocessor family in conformance with the PowerPC Reference Platform (PReP) and the PowerPC Common Hardware Reference Platform (CHRP) specifications.

The MPC2105P utilizes synchronous BurstRAMs. It is configured as 64K x 64 bits and uses two of the 3.3 V 64K x 32 data RAMs. The module is in a 178 (89 x 2) pin DIMM format. For tag bits on the MPC2105P, a 5 V cache tag RAM configured as 16K x 14 for tag field plus 16K x 2 for valid and dirty status bits is used.

Bursts can be initiated with the $\overline{ADS}$ signal. Subsequent burst addresses are generated internally to the BurstRAM by the $\overline{CNTEN}$ signal.

Write cycles are internally self–timed and are initiated by the rising edge of the clock (CLKx) inputs. Writes are global.

Presence detect pins are available for auto configuration of the cache control.

The module pinout will support 5 V and 3.3 V components for a clear path to lower voltage and power savings. Both power supplies must be connected.

All of these cache modules are plug and pin compatible with each other.

- PowerPC–Style Burst Counter On Chip
- Pipeline Data I/O
- Plug and Pin Compatibility
- Multiple Clock Pins for Reduced Loading
- All Cache Data and Tag I/Os are LVTTL (3.3 V) Compatible
- Three State Outputs
- Buffered Addresses to Data RAMs for Reduced Loading
- Fast Module Clock Rates: Up to 66 MHz
- Fast SRAM Access Times: 9 ns for Tag RAM Match
  8 ns for Data RAM
- Decoupling Capacitors for Each Fast Static RAM
- High Quality Multi–Layer FR4 PWB With Separate Power and Ground Planes
- 178 Pin Card Edge Module
- Burndy Connector, Part Number: ELF178KSC–3Z50

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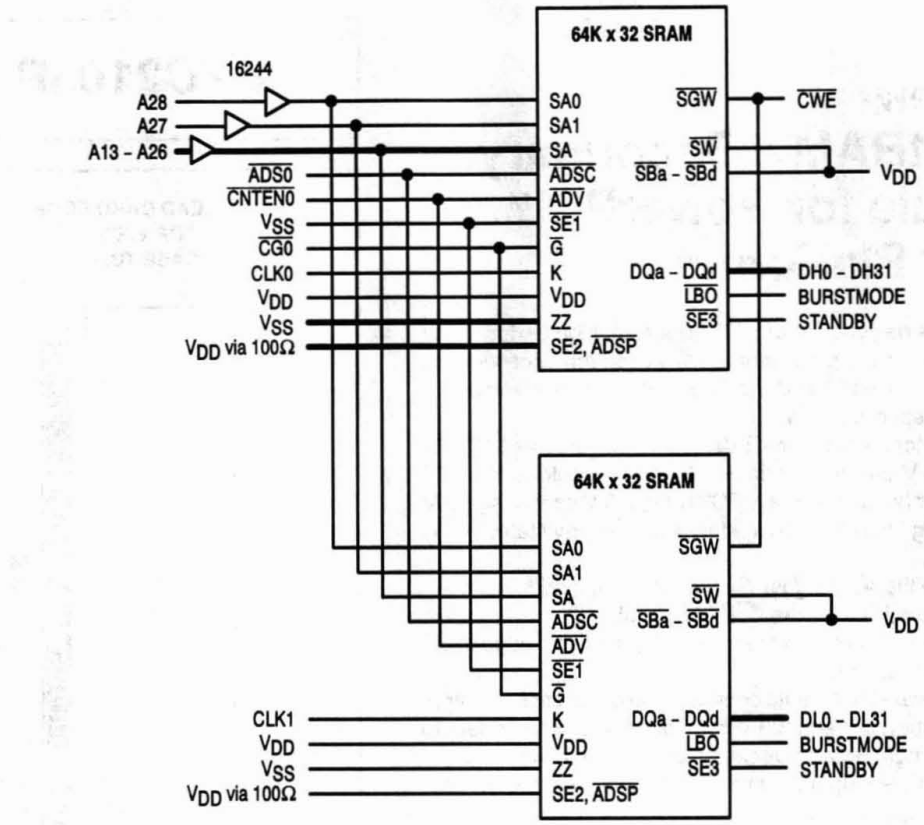
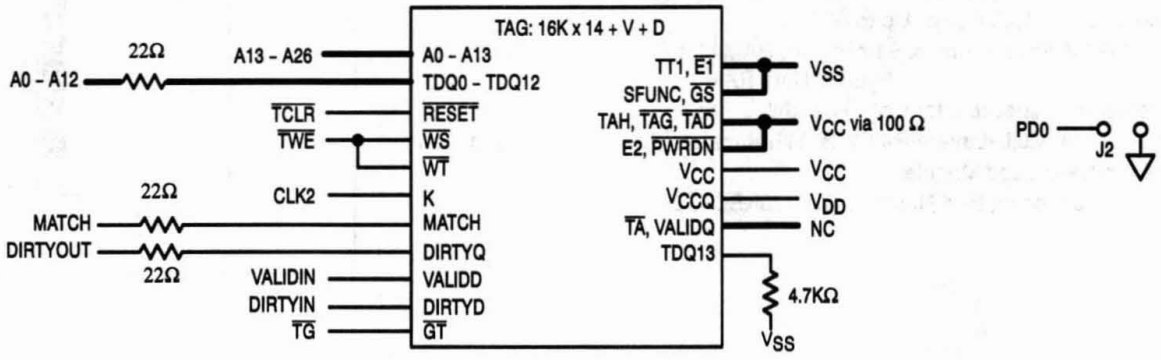
BurstRAM is a trademark of Motorola.
The PowerPC name is a trademark of IBM Corp., used under license therefrom.

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

3/18/97

BLOCK DIAGRAM



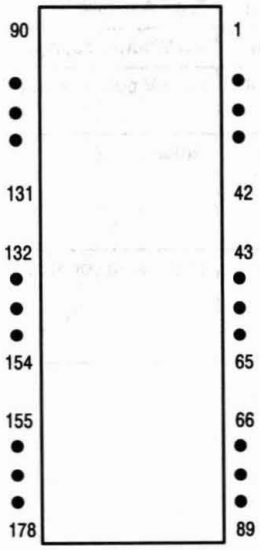


PIN ASSIGNMENT 178–LEAD DIMM

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	27	DH0	53	DL1	79	V_{SS}	105	DH14	131	DL17	157	A22
2	V_{DD}	28	V_{DD}	54	DL0	80	A7	106	DH13	132	NC	158	A20
3	PD0	29	V_{SS}	55	V_{SS}	81	A5	107	V_{SS}	133	DL15	159	V_{SS}
4	DH30	30	CLK1	56	CLK2	82	A3	108	DH10	134	DL13	160	A18
5	DH28	31	V_{SS}	57	V_{SS}	83	A0	109	DH8	135	V_{SS}	161	A16
6	DH26	32	DL28	58	V_{SS}	84	V_{CC}	110	NC	136	DL10	162	A15
7	DH24	33	DL26	59	$\overline{CG0}$	85	$\overline{TCLR}$	111	DH6	137	DL8	163	A14
8	V_{DD}	34	DL24	60	NC	86	MATCH	112	V_{DD}	138	NC	164	V_{DD}
9	V_{SS}	35	V_{DD}	61	V_{DD}	87	$\overline{TG}$	113	DH4	139	DL6	165	A10
10	DH22	36	V_{SS}	62	NC	88	DIRTYIN	114	V_{SS}	140	V_{DD}	166	A8
11	DH20	37	DL22	63	V_{SS}	89	V_{SS}	115	CLK0	141	DL5	167	A6
12	DH19	38	DL20	64	$\overline{ADS0}$	90	V_{SS}	116	V_{SS}	142	DL2	168	V_{SS}
13	V_{SS}	39	DL18	65	NC	91	V_{DD}	117	DH1	143	V_{SS}	169	A4
14	DH17	40	DL16	66	A28	92	V_{SS}	118	NC	144	V_{DD}	170	A2
15	V_{SS}	41	V_{SS}	67	A26	93	DH31	119	DL31	145	V_{SS}	171	A1
16	DH15	42	V_{DD}	68	A25	94	DH29	120	DL30	146	V_{SS}	172	BURSTMODE
17	DH12	43	DL14	69	A23	95	DH27	121	V_{SS}	147	V_{SS}	173	V_{CC}
18	V_{SS}	44	DL12	70	V_{SS}	96	DH25	122	DL29	148	$\overline{CWE}$	174	VALIDIN
19	DH11	45	DL11	71	A21	97	V_{DD}	123	DL27	149	NC	175	$\overline{TWE}$
20	DH9	46	V_{SS}	72	A19	98	NC	124	DL25	150	V_{DD}	176	STANDBY
21	V_{SS}	47	DL9	73	A17	99	DH23	125	V_{SS}	151	NC	177	DIRTYOUT
22	DH7	48	V_{SS}	74	A13	100	DH21	126	NC	152	V_{SS}	178	V_{SS}
23	V_{DD}	49	DL7	75	V_{DD}	101	DH18	127	DL23	153	$\overline{CNTEN0}$		
24	DH5	50	DL4	76	A12	102	V_{SS}	128	DL21	154	NC		
25	DH3	51	V_{DD}	77	A11	103	DH16	129	DL19	155	A27		
26	DH2	52	DL3	78	A9	104	NC	130	V_{SS}	156	A24		

NOTE: V_{CC} and V_{DD} must be connected on all modules.

TOP VIEW – CASE TBD



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PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
66, 67, 68, 69, 71, 72, 73, 74, 76, 77, 78, 80, 81, 82, 83, 155, 156, 157, 158, 160, 161, 162, 163, 165, 166, 167, 169, 170, 171	A0 – A28	Input	Address Inputs — (MSB:0, LSB:28).
64	$\overline{ADS0}$	Input	Data RAM Address Strobe.
172	BURSTMODE	Input	Burstmode. 0 = Linear, 1 = Interleaved.
59	$\overline{CG0}$	Input	Data RAM Output Enable.
30, 56, 115	CLK0 – CLK2	Input	Clock Inputs — CLK2 is for Tag RAM, CLK0 and CLK1 are for Data RAMs only.
153	$\overline{CNTEN0}$	Input	Data RAM Count Enable.
138, 148	$\overline{CWE0}$ – $\overline{CWE1}$	Input	Data RAM Write Enables — (MSB:0, LSB:1).
4, 5, 6, 7, 10, 11, 12, 14, 6, 17, 19, 20, 22, 24, 25, 26, 27, 93, 94, 95, 96, 99, 100, 101, 103, 105, 106, 108, 109, 111, 113, 117	DH0 – DH31	I/O	High Data Bus — (MSB:0, LSB:31).
88	DIRTYIN	Input	Dirty input bit.
177	DIRTYOUT	Output	Dirty output bit.
32, 33, 34, 37, 38, 39, 40, 43, 44, 45, 47, 49, 50, 52, 53, 54, 119, 120, 122, 123, 124, 127, 128, 129, 131, 133, 134, 136, 137, 139, 141, 142	DL0 – DL31	I/O	Low Data Bus — (MSB:0, LSB:31).
86	MATCH	Output	Tag RAM active high match indication.
2	PD0/IDSCLK	Input	Presence detect bit 0/EEPROM serial clock. (EEPROM option only).
91	PD1/IDSDATA	I/O	Presence detect bit 1/EEPROM serial data. (EEPROM option only).
3, 92	PD2, PD3	Output	Presence detect bits.
63, 152	RESERVED		Reserved pin.
176	STANDBY	Input	Standby pin. Reduces standby power consumption.
85	$\overline{TCLR}$	Input	Tag RAM clear.
87	$\overline{TG}$	Input	Tag RAM output enable.
175	$\overline{TWE}$	Input	Tag RAM write enable.
174	VALIDIN	Input	Tag RAM valid bit.
84, 173	V_{CC}	Input	+ 5 V power supply. Must be connected.
8, 23, 51, 61, 75, 97, 112, 140, 150, 164	V_{DD}	Input	+ 3.3 V power supply. Must be connected.
1, 13, 29, 31, 41, 46, 55, 57, 70, 79, 89, 90, 102, 114, 116, 121, 130, 135, 143, 145, 147, 159, 168, 178	V_{SS}	Input	Ground.
9, 15, 18, 21, 28, 35 – 36, 42, 48, 58, 60, 62, 65, 98, 104, 107, 110, 118, 125 – 126, 132, 144, 146, 149, 151, 154	NC	—	There is no connection to the module.

TRUTH TABLE (See Notes 1 through 4)

Next Cycle	Address Used	Standby	$\overline{ADS0}$	$\overline{CNTEN0}$	$\overline{CG0}$ [2]	DHx/DLx	$\overline{CWEx}$ [2]
Deselect	None	1	0	X	X	High–Z	X
Begin Read	External	0	0	X	X	High–Z	1[4]
Continue Read	Next	X	1	0	1	High–Z	1
Continue Read	Next	X	1	0	0	DQ	1
Suspend Read	Current	X	1	1	1	High–Z	1
Suspend Read	Current	X	1	1	0	DQ	1
Begin Write	External	0	0	X	X	High–Z	0
Continue Write	Next	X	1	0	X	High–Z	0
Suspend Write	Current	X	1	1	X	High–Z	0

NOTES:
1. X = Don't Care. 1 = logic high. 0 = logic low.
2. $\overline{CG0}$ is an asynchronous signal and is not sampled by the clock CLK0. $\overline{CG0}$ drives the bus immediately (t_{GLQX}) following $\overline{CG0}$ going low.
3. On write cycles that follow read cycles, $\overline{CG0}$ must be negated prior to the start of the write cycle to ensure proper write data setup times. $\overline{CG0}$ must also remain negated at the completion of the write cycle to ensure proper write data hold times.
4. This READ assumes the RAM was previously deselected.

ASYNCHRONOUS TRUTH TABLE

Operation	$\overline{CG0}$	I/O Status
Read	L	Data Out (DHx/DLx)
Read	H	High–Z
Write	X	High–Z
Deselected	X	High–Z
Sleep	X	High–Z

LINEAR BURST ADDRESS TABLE (Burst Mode = V_{SS})

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X10	X . . . X11	X . . . X00
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X00	X . . . X01	X . . . X10

INTERLEAVED BURST ADDRESS TABLE (Burst Mode = V_{DD})

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating		Symbol	Value	Unit
Power Supply Voltage	Tag Data RAM	V_{CC} V_{DD}	– 0.5 to + 7.0 – 0.5 to + 4.6	V
Voltage Relative to V_{SS}	Tag Data RAM	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5 – 0.5 to V_{DD} + 0.5	V
Output Current (per I/O)	Tag Data RAM	I_{out}	± 20 ± 30	mA
Power Dissipation		P_D	3.86	W
Temperature Under Bias		T_{bias}	– 10 to + 85	°C
Operating Temperature		T_A	0 to +70	°C
Storage Temperature		T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, V_{DD} = 3.3 V + 10%, – 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC} V_{DD}	4.75 3.135	5.25 3.60	V
Input High Voltage	V_{IH}	2.2	V_{DD} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{DD} + 0.3 V dc; V_{IH} (max) = V_{DD} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{DD})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{CG}$ = V_{IH}, V_{out} = 0 to V_{DD})	$I_{lkg(O)}$	—	± 1.0	µA
TTL Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
TTL Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	Max	Unit
AC Supply Current ($\overline{CG}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ 20 ns)	I_{DDA}	700	mA
	I_{CCA}	320	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH} V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ 20 ns)	I_{SB1} (V_{DD})	240	mA
	I_{SB1} (V_{CC})	320	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit
Input Capacitance	(A13 – A28) (Data RAM Control Pins) (CLK0 – CLK2) (Tag Control Pins)	C_{in}	15 10 5 5	pF
Tag Output Capacitance	(MATCH, DIRTYOUT)	C_{out}	7	pF
Data RAM Input/Output Capacitance	(DH0 – DH31, DL0 – DL31)	$C_{I/O}$	8	pF
Tag Input/Output Capacitance	(A0 – A11)	$C_{I/O}$	7	pF

DATA RAMs AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, V_{DD} = 3.3 V + 10%, – 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1 Unless Otherwise Noted

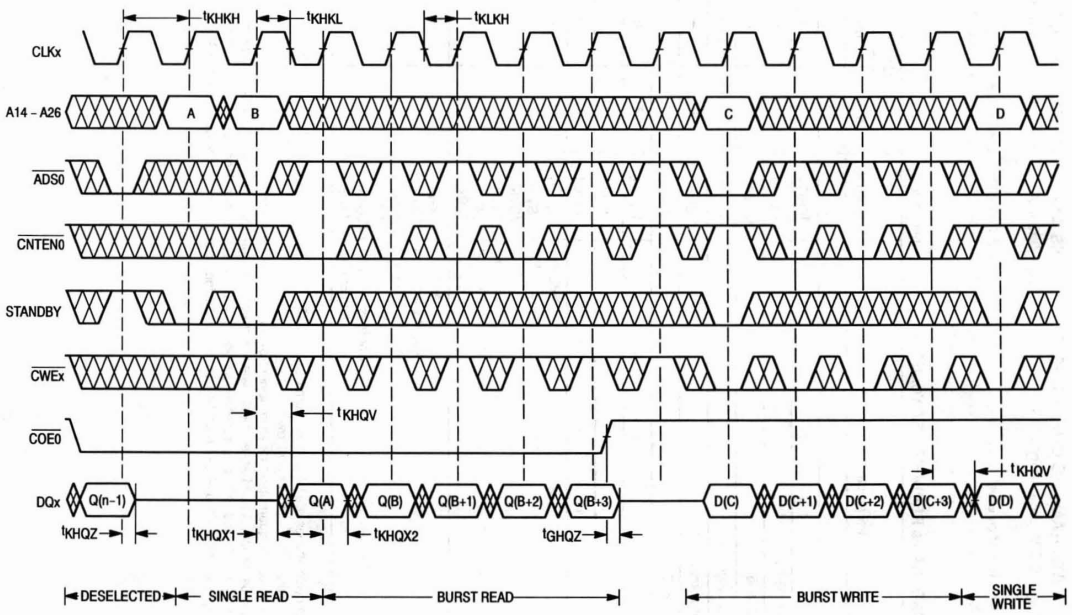
SYNCHRONOUS DATA RAMs READ/WRITE CYCLE TIMING (See Notes 1 and 2)

Parameter		Symbol	MPC2105P Min	MPC2105P Max	Unit	Notes
Cycle Time		t_{KHKH}	15	—	ns	
Clock Access Time		t_{KHQV}	—	8	ns	3
Output Enable to Output Valid		t_{GLQV}	—	6	ns	
Clock High to Output Active		t_{KHQX1}	0	—	ns	
Clock High to Output Change		t_{KHQX2}	2	—	ns	
Output Enable to Output Active		t_{GLQX}	0	—	ns	
Output Disable to Q High–Z		t_{GHQZ}	—	8	ns	
Clock High to Q High–Z		t_{KHQZ}	2	8	ns	
Clock High Pulse Width		t_{KHKL}	5	—	ns	
Clock Low Pulse Width		t_{KLKH}	5	—	ns	
Setup Times:	Address	t_{AVKH}	2.5	—	ns	4
	Address Status	t_{SVKH}				
	Data In	t_{DVKH}				
	Write	t_{WVKH}				
	Address Advance	t_{BAVVKH}				
	Chip Enable	t_{EVKH}				
Hold Times:	Address	t_{KHAX}	0.5	—	ns	4
	Address Status	t_{KHTSX}				
	Data In	t_{KHDX}				
	Write	t_{KHWX}				
	Address Advance	t_{KHBAX}				
	Chip Enable	t_{KHEX}				

NOTES:
1. All read and write cycle timings are referenced from CLK or $\overline{CG0}$.
2. $\overline{CG}$ is a don't care when $\overline{CWE}_X$ is sampled low.
3. Maximum access times are guaranteed for all possible PowerPC external bus cycles.
4. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of CLK whenever $\overline{ADS0}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of CLK when the chip is enabled. Chip enable must be valid at each rising edge of clock for the device (when $\overline{ADS0}$ is low) to remain enabled.

6

READ/WRITE CYCLES



RESET FUNCTION TRUTH TABLE (See Notes 1 and 2)

$\overline{TCLR}$	CLK	$\overline{TWE}$	TAG0 – TAG11	DIRTYOUT	MATCH	Operation	POWER
L	L – H	H	High–Z	L(3)	L(3)	Reset Status	Active
L	L – H	L	—	—	—	Not Allowed	—

NOTES:
1. H = V_{IH}, L = V_{IL}, X = don't care, — = undefined.
2. $\overline{TG}$ is X for this table.
3. These are output states.

READ FUNCTION TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{TG}$	$\overline{TWE}$	CLK	TAG0 – TAG11	VALIDIN	DIRTYIN	DIRTYOUT	MATCH	Operation
L	H	X	D_{out}	—	—	D_{out}	D_{out}	Read Tag I/O
H	X	X	High–Z	—	—	—	—	Tag I/O Disable

WRITE FUNCTION TRUTH TABLE (See Notes 1 and 2)

$\overline{TG}$	$\overline{TWE}$	CLK	TAG0 – TAG11	VALIDIN	DIRTYIN	DIRTYOUT	MATCH	Operation
H	L	L – H	D_{in}	—	—	—	L	Write Tag I/O
L	L	L – H	—	—	—	—	—	Not Allowed

NOTES:
1. H = V_{IH}, L = V_{IL}, X = don't care, — = undefined.
2. This table applies when $\overline{RESET}$ and $\overline{PWRDN}$ are high.
3. D_{out} in this case is the same as D_{in}. The input data is written through to the outputs during the write operation.

MATCH FUNCTION TRUTH TABLE (See Notes 1 through 4)

$\overline{TG}$	$\overline{TWE}$	TAG0 – TAG11	VALIDIN(4)	DIRTYIN(4)	MATCH	Operation
X	X	—	—	—	D_{out}	Selected
L	H	D_{out}	—	—	L	Read Tag I/O
H	L	D_{in}	D_{in}	D_{in}	L	Write Tag I/O, Status Bits
H	H	TAG_{in}	L	—	L	Invalid Data — Dedicated Status Bits
H	H	TAG_{in}	H	—	H	Match — Dedicated Status Bits

NOTES:
1. H = V_{IH}, L = V_{IL}, X = don't care, — = undefined.
2. M = high if TAG_{in} equals the memory contents at the address; M = low if TAG_{in} does not equal the contents at that address.
3. $\overline{PWRDN}$ and $\overline{RESET}$ are high for this table. $\overline{GS}$ and CLK are X.
4. This column represents the stored memory cell data for the given status bit at the selected address.

TAG RAM AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... Figure 1 Unless Otherwise Noted

TAG RAM READ CYCLE (See Notes 1 through 4)

Parameter	Symbol	Tag RAM		Unit
		Min	Max	
Clock Access Time	t_{KHQV}	—	10	ns
Output Enable to Output Valid	t_{GLQV}	—	8	ns
Output Enable to Output Active	t_{GLQX}	0	—	ns
Output Disable to Q High–Z	t_{GHQZ}	1	6	ns
Status Bit Hold from Address Change	t_{AXSX}	3	—	ns
Address Access Time Status Bits	t_{AVSV}	—	10	ns
Tag Bit Hold from Address Change	t_{AVQX}	3	—	ns
Address Access Time Tag Bits	t_{AVQV}	—	12	ns

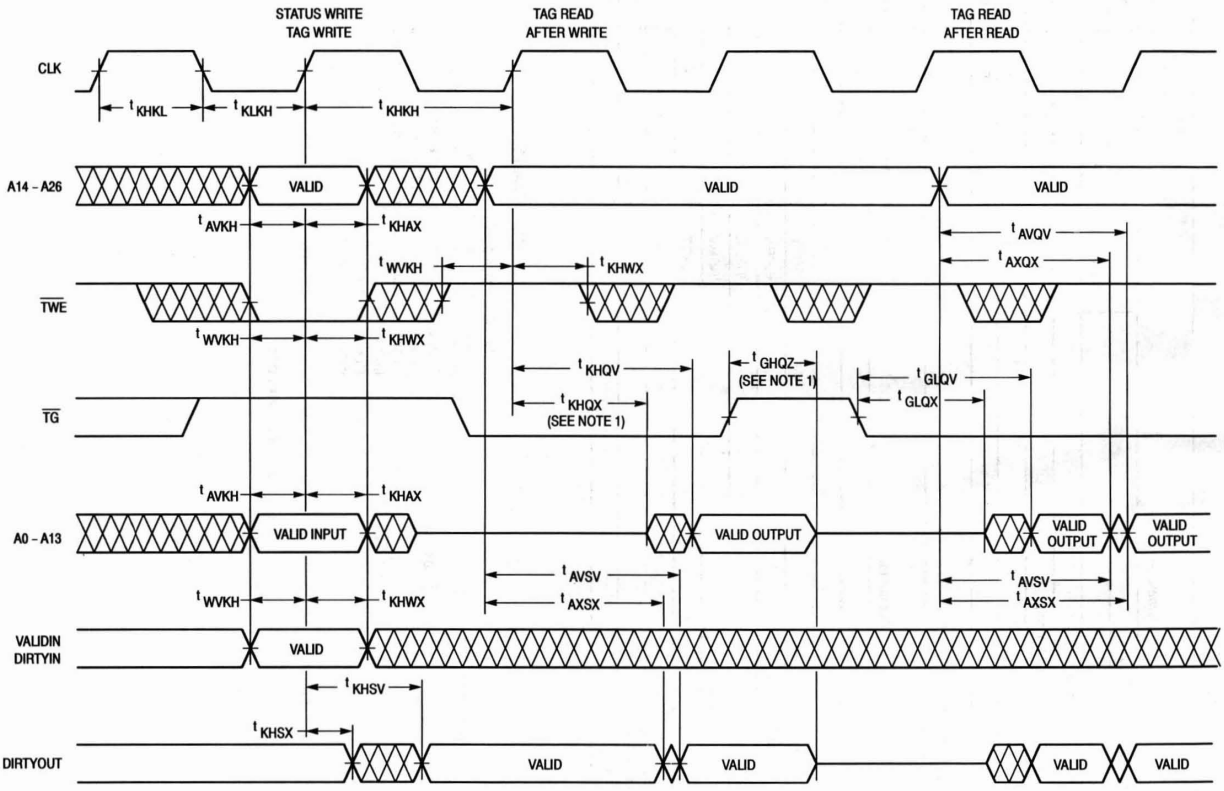
NOTES:
1. Setup and hold times, W (write) refers to $\overline{TWE}$.
2. A read cycle is defined by $\overline{TWE}$ high. A write cycle is defined by $\overline{TWE}$ low.
3. Maximum access times are guaranteed for all possible MC68040 and PowerPC external bus cycles.
4. Tag reads are asynchronous.

TAG RAM WRITE CYCLE (See Notes 1 through 4)

Parameter		Symbol	Tag RAM		Unit
			Min	Max	
Cycle Time		t_{KHKH}	15	—	ns
Clock High Pulse Width		t_{KHKL}	4.5	—	ns
Clock Low Pulse Width		t_{KLKH}	4.5	—	ns
Clock High to Output Active		t_{KHQX}	1.5	—	ns
Setup Times	Address Write	t_{AVKH} t_{WVKH}	3	—	ns
Hold Times	Address Write	t_{KHAX} t_{KHWX}	1.5	—	ns
Status Output Hold		t_{KHSX}	0	—	ns
Clock High to Status Bits Valid		t_{KHSV}	—	9	ns

NOTES:
1. Setup and hold times, W (write) refers to $\overline{TWE}$.
2. A read cycle is defined by $\overline{TWE}$ high. A write cycle is defined by $\overline{TWE}$ low.
3. Maximum access times are guaranteed for all possible MC68040 and PowerPC external bus cycles.
4. Tag writes are synchronous.

TAG RAM WRITE AND READ CYCLES (See Note 2)



NOTES:
1. Transition is measured plus or minus 200 mV from steady state.
2. $\overline{TCLR}$ = High.

TAG RAM MATCH CYCLE

Parameter	Symbol	Tag RAM		Unit
		Min	Max	
Clock High Write to MATCH Invalid	t_{KHML}	—	7	ns
Clock High Read to MATCH Valid	t_{KHMV}	—	10	ns
Address Valid to MATCH Valid	t_{AVMV}	—	10	ns
MATCH Valid Hold from Address Change	t_{AXMX}	2	—	ns
$\overline{TG}$ Low to MATCH Invalid	t_{GLML}	—	7	ns
$\overline{TG}$ High to MATCH Valid	t_{GHMX}	—	8	ns

TAG RAM RESET ($\overline{TCLR}$) CYCLE

Parameter	Symbol	Tag RAM		Unit
		Min	Max	
$\overline{TCLR}$ Setup Time	t_{STC}	4	—	ns
$\overline{TCLR}$ Hold Time	t_{HTC}	1	—	ns
Status Bit Reset Time	t_{SRST}	—	60	ns
Status Bit Hold from $\overline{TCLR}$ Low	t_{SHRS}	2	—	ns
$\overline{TCLR}$ Low to MATCH Invalid	t_{RSML}	—	10	ns
$\overline{TCLR}$ High to MATCH Valid	t_{RSMV}	—	100	ns
$\overline{TCLR}$ Low to TAG High–Z	t_{RSQZ}	—	10	ns
$\overline{TCLR}$ High to TAG Active	t_{RSQX}	—	100	ns
STANDBY Setup to $\overline{TCLR}$ Low	t_{PDSR}	30	—	ns
$\overline{TCLR}$ High to $\overline{TWE}$ Low	t_{RHWX}	80	—	ns

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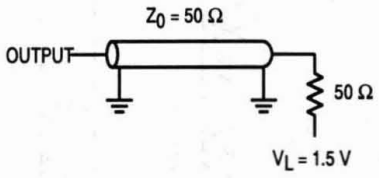
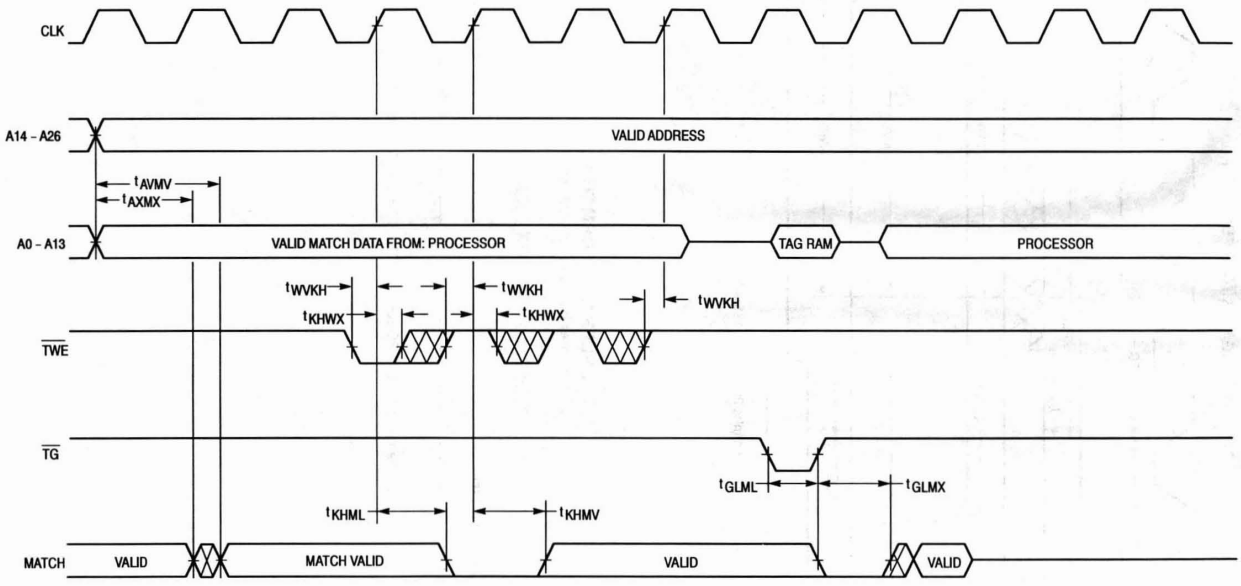


Figure 1. AC Test Load

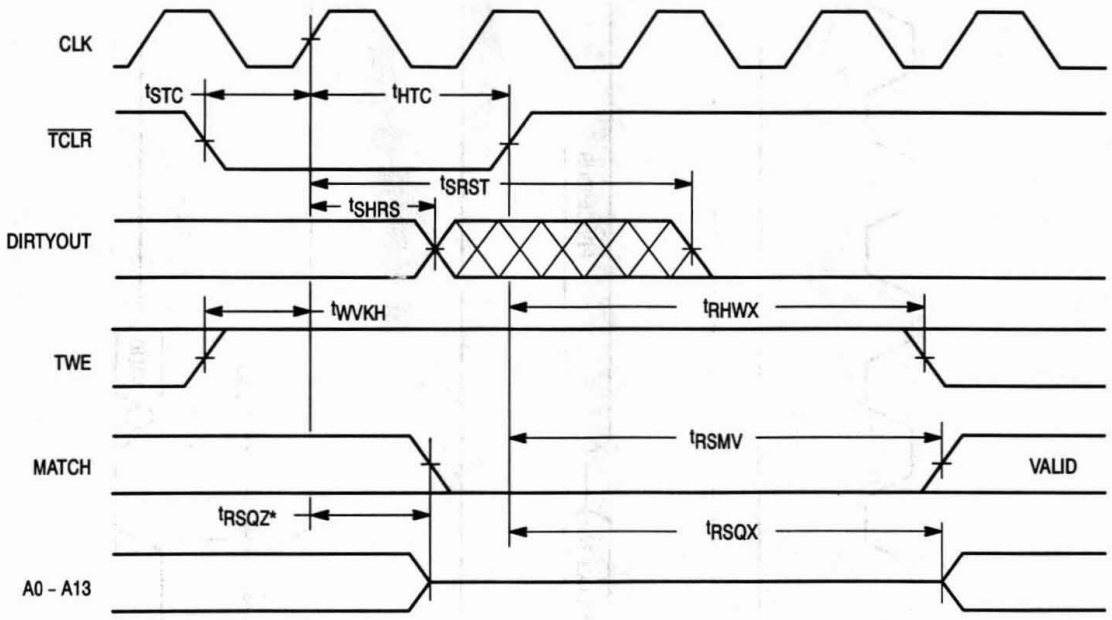
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

TAG RAM MATCH CYCLE



TAG RAM $\overline{\text{TCLR}}$ FUNCTION



* Transition is measured plus or minus 200 mV from steady state.

ORDERING INFORMATION
(Order by Full Part Number)

MPC 2105P XX XX

- MPC — Motorola Memory Prefix
- 2105P — Part Number
- XX — Package (DG = Gold Pad DIMM)
- XX — Speed (66 = 66 MHz)

Full Part Numbers — MPC2105PDG66 MPC2105P = 512KB, synchronous pipelined

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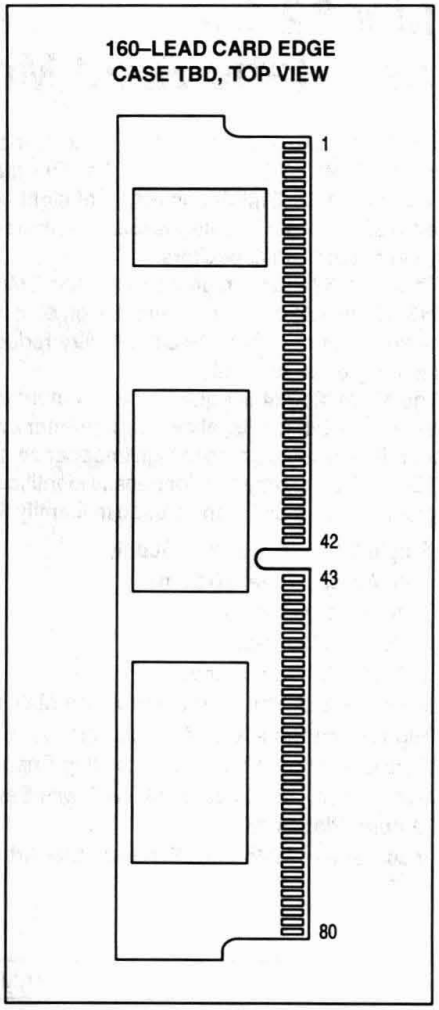
MCM64PE64

Advance Information

512K Pipelined BurstRAM™ Secondary Cache Module for Pentium™



The MCM64PE64 (512KB) module is designed to provide a burstable, high performance, L2 cache for the Pentium microprocessor in conjunction with Intel's Triton II chip set. The MCM64PE64 is configured as 64K x 64 bits. It is packaged in a 160–pin card edge memory module. The module uses two 3.3 V, 64K x 32 BurstRAMs for the data RAMs and one 3.3 V, 32K x 8 FSRAM for the 8–bit tag RAM.

Bursts can be initiated with either address status processor ($\overline{ADSP}$) or cache address status ($\overline{CADS}$). Subsequent burst addresses are generated internal to the BurstRAM by the cache burst advance ($\overline{CADV}$) input pin.

Write cycles are internally self timed and are initiated by the rising edge of the clock (CLK0) input. Eight write enables are provided for byte write control.

PD0 – PD3 map into the Triton II chip set for auto–configuration of the cache control.

- 8–Bit Cache Tag
- Pentium–Style Burst Counter on Chip
- Pipelined Data Out
- 160–Pin Card Edge Module
- Address Pipeline Supported by $\overline{ADSP}$ Disabled with $\overline{Ex}$
- All Cache Data and Tag I/Os are TTL Compatible
- Three State Outputs
- Byte Write Capability
- Fast Module Clock Rate: 66, 75 MHz
- Fast SRAM Access Times: 12, 15 ns for Tag RAMs
  7, 8 ns for Data RAMs
- One–Cycle Deselect Data RAMs
- Decoupling Capacitors for Each Fast Static RAM
- Single 3.3 V + 10%, – 5% Power Supply
- Burndy Connector, Part Number: CELP2X80SC3Z48
- Intel COAST 3.0 Option III Compliant

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BurstRAM is a trademark of Motorola.
Pentium is a trademark of Intel Corp.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

3/17/97

MCM321024

Advance Information

1M x 32 Bit Fast Static RAM Module

The MCM321024 is an 32M bit static random access memory module organized as 1,048,576 words of 32 bits. The module is a 72–lead single in–line memory module (SIMM) consisting of eight MCM6249 fast static RAMs packaged in 32–lead SOJ packages and mounted on a printed circuit board along with sixteen decoupling capacitors.

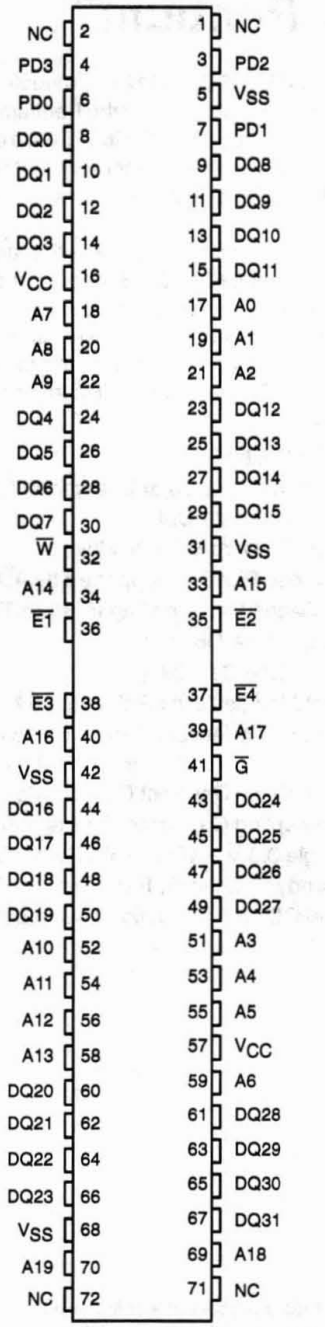
The MCM6249 is a high performance CMOS fast static RAM organized as 1,048,576 words of 4 bits. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM321024 is equipped with output enable ($\overline{G}$) and four separate byte enable ($\overline{E1}$ – $\overline{E4}$) inputs, allowing for greater system flexibility. The $\overline{G}$ input, when high, will force the outputs to high impedance. $\overline{Ex}$ high will do the same for byte x.

PD0 – PD3 are reserved for density identification. PD0 and PD2 are connected to ground. These pins can be used to identify the density of the memory module.

- Single 5 V ± 10% Power Supply
- Fast Access Time: 20/25 ns
- Three–State Outputs
- Fully TTL Compatible
- JEDEC Standard Pinout
- Power Requirement: 1520/1400 mA Maximum, Active AC
- High Board Density SIMM Package
- Byte Operation: Four Separate Chip Enables, One for Each Byte (Eight Bits)
- High Quality Six–Layer FR4 PWB with Separate Internal Power and Ground Planes
- Incorporates Motorola's State–of–the–Art Fast Static RAMs

PIN ASSIGNMENT
TOP VIEW
72 LEAD SIMM — CASE TBD



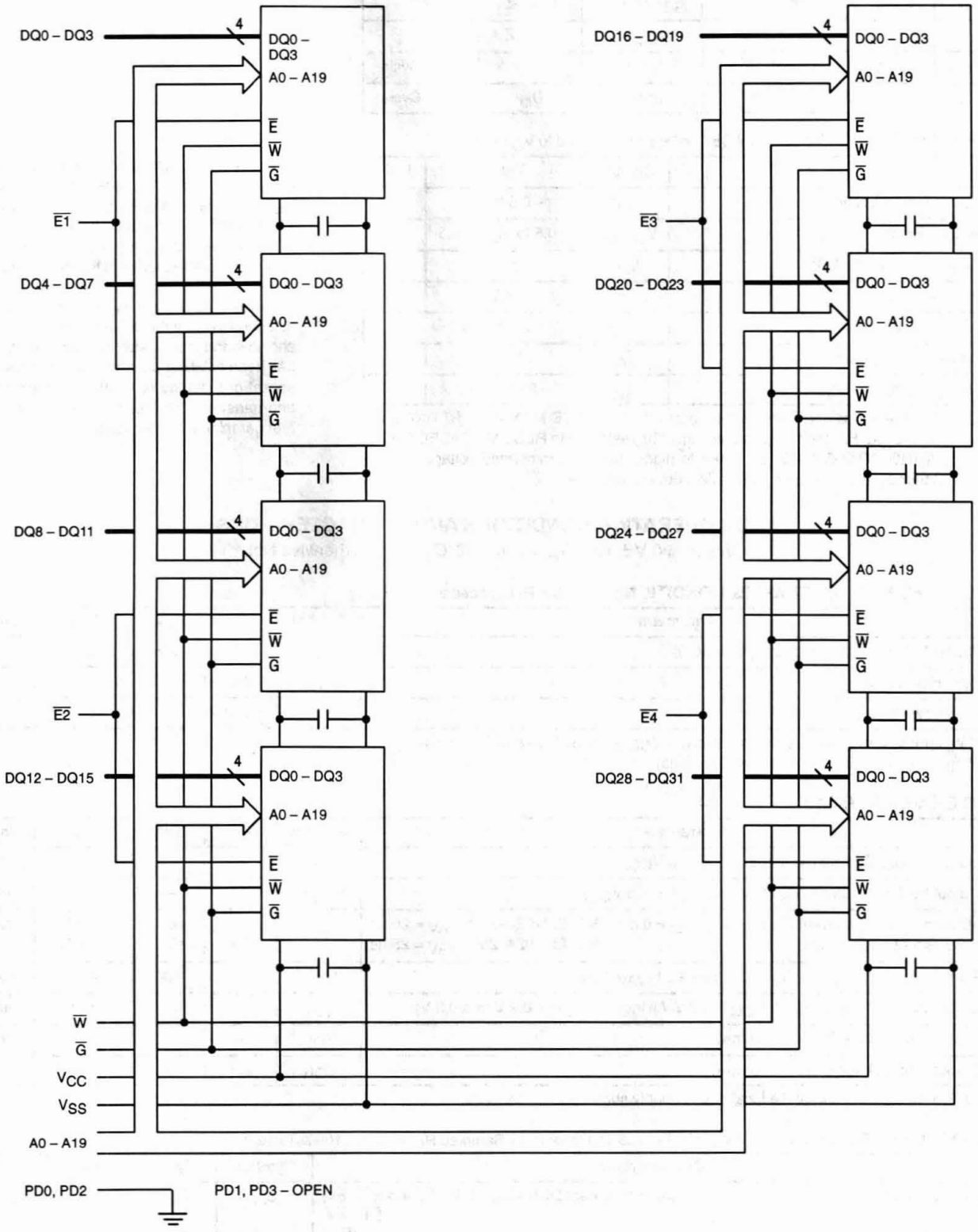
PIN NAMES	
A0 – A19	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$ – $\overline{E4}$	Byte Enables
DQ0 – DQ31	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
PD0 – PD3	Package Density
NC	No Connect

For proper operation of the device, V_{SS} must be connected to ground.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 1
11/15/96

FUNCTIONAL BLOCK DIAGRAM
1M x 32 MEMORY MODULE



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TRUTH TABLE

$\overline{Ex}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1} or I_{SB2}	High–Z	—
L	H	H	Read	I_{CCA}	High–Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	D_{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	8.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperatrue	T_{stg}	– 25 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

The devices on this module contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

These CMOS memory circuits have been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The module is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

* V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns)
** V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

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DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 8	µA
Output Leakage Current ($\overline{G}$, $\overline{Ex}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	—	± 8	µA
AC Active Supply Current ($\overline{G}$, $\overline{Ex}$ = V_{IL}, I_{out} = 0 mA, Cycle time ≥ t_{AVAV} min) MCM321024–20: t_{AVAV} = 20 ns MCM321024–25: t_{AVAV} = 25 ns	I_{CCA}	— —	1440 1320	1520 1400	mA
AC Standby Current ($\overline{Ex}$ = V_{IH}, Cycle time ≥ t_{AVAV} min)	I_{SB1}	—	400	480	mA
CMOS Standby Current ($\overline{Ex}$ ≥ V_{CC} – 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V)	I_{SB2}	—	80	120	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

NOTE: Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	(All pins except DQ0 – DQ31, $\overline{W}$, $\overline{G}$, and $\overline{E1}$ – $\overline{E4}$) $\overline{E1}$ – $\overline{E4}$ $\overline{W}$, $\overline{G}$	C_{in}	32 10 40	48 14 64	pF
Input/Output Capacitance	(DQ0 – DQ31)	C_{out}	8	9	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V

Output Load ..... See Figure 1a Unless Otherwise Noted
Input Rise/Fall Time ..... 3 ns

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM321024–20		MCM321024–25		Unit	Notes
		Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	20	—	25	—	ns	3
Address Access Time	t_{AVQV}	—	20	—	25	ns	
Enable Access Time	t_{ELQV}	—	20	—	25	ns	
Output Enable Access Time	t_{GLQV}	—	7	—	9	ns	
Output Hold from Address Change	t_{AXQX}	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	5	—	ns	4,5,6
Output Enable to Output Active	t_{GLQX}	0	—	0	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	0	9	0	10	ns	4,5,6
Output Enable High to Output High–Z	t_{GHQZ}	0	9	0	10	ns	4,5,6
Power Up Time	t_{ELICCH}	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	—	20	—	25	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1b.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}). See Read Cycle 1.

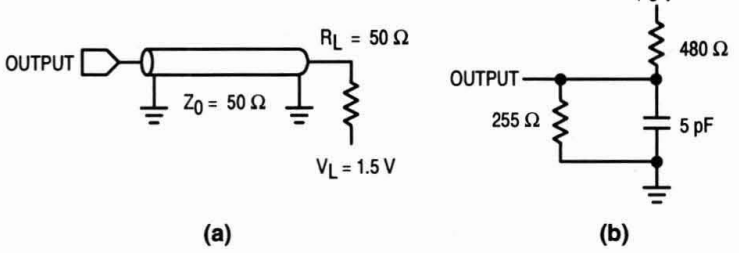

Figure 1. Test Loads

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

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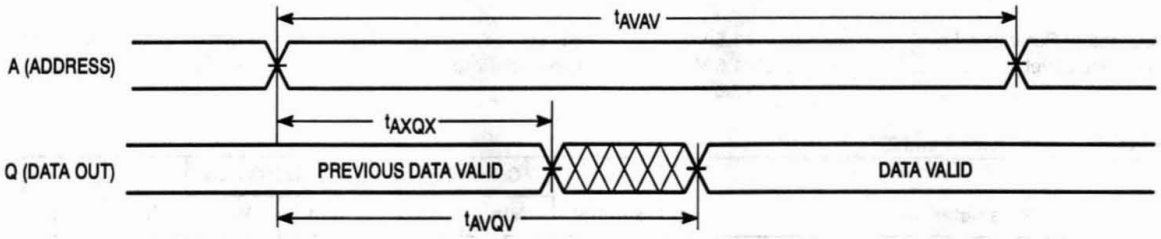
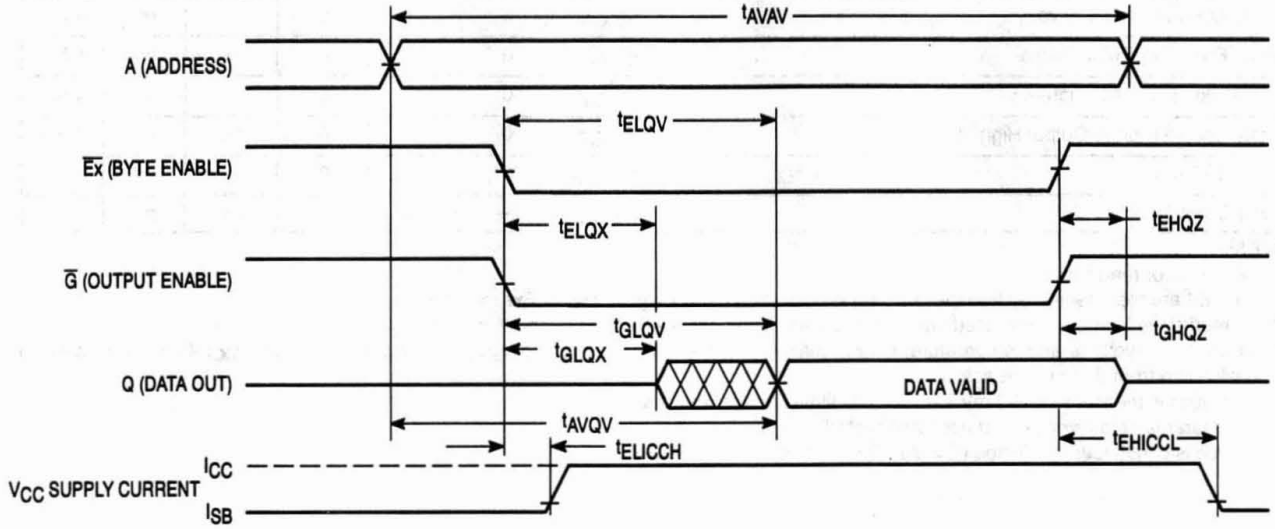
READ CYCLE 1 (See Note 7 Above)



READ CYCLE 2 (See Note)



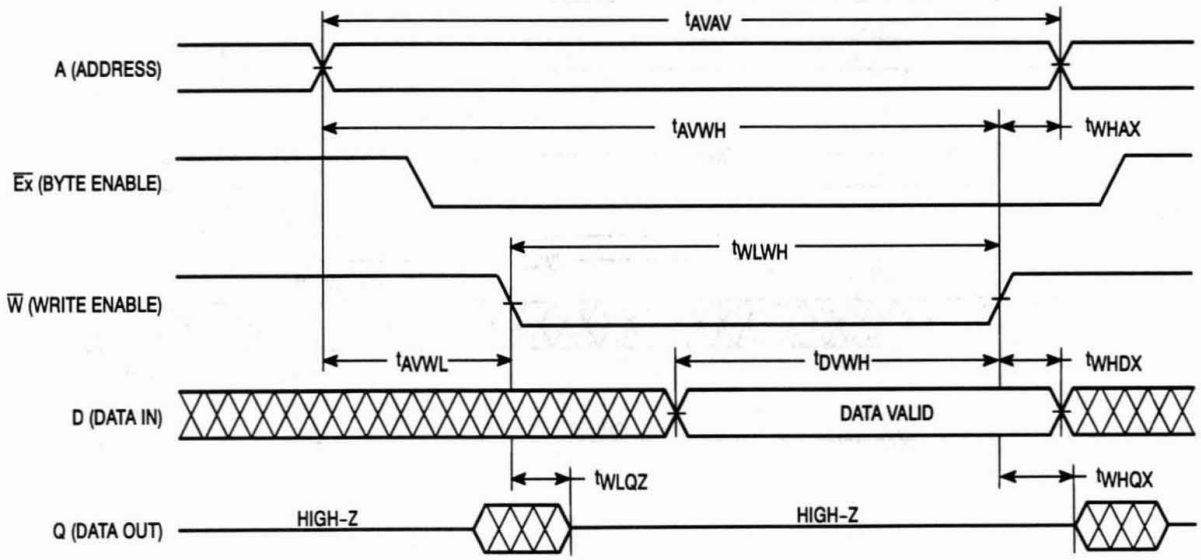
NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM321024–20		MCM321024–25		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	15	—	17	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	15	—	17	—	ns	
Data Valid to End of Write	t_{DVWH}	10	—	10	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	9	0	10	ns	4,5,6
Write High to Output Active	t_{WHQX}	5	—	5	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted. $\overline{G}$ is a don't care when $\overline{W}$ is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1b.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1



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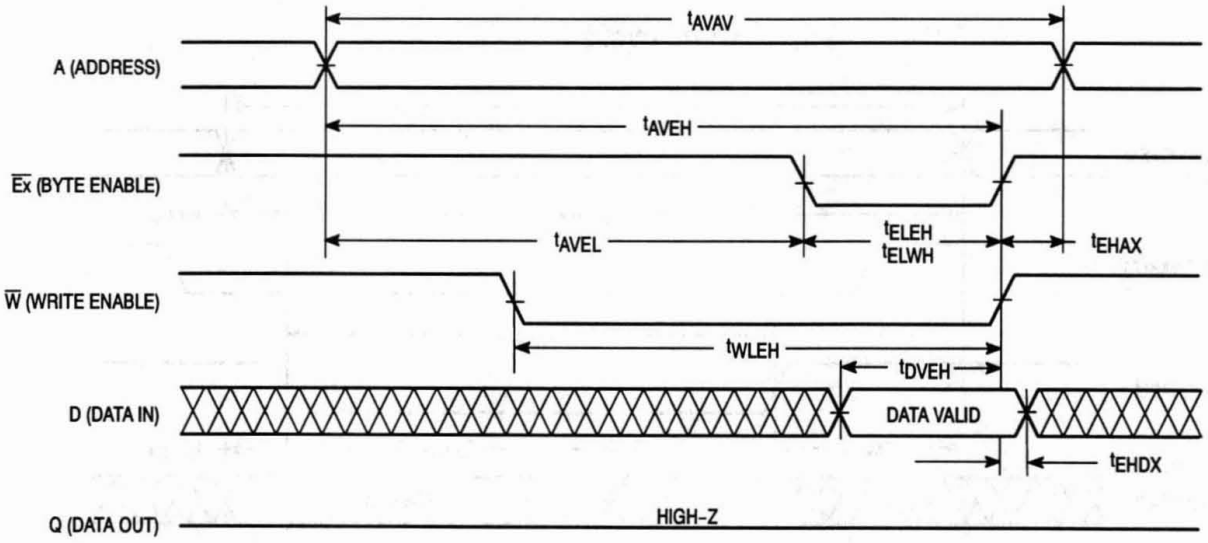
WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM321024–20		MCM321024–25		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	15	—	17	—	ns	
Enable to End of Write	t_{ELEH}	15	—	17	—	ns	4,5
Enable to End of Write	t_{ELWH}	15	—	17	—	ns	
Write Pulse Width	t_{WLEH}	15	—	17	—	ns	
Data Valid to End of Write	t_{DVEH}	10	—	10	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted. $\overline{G}$ is a don't care when $\overline{W}$ is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



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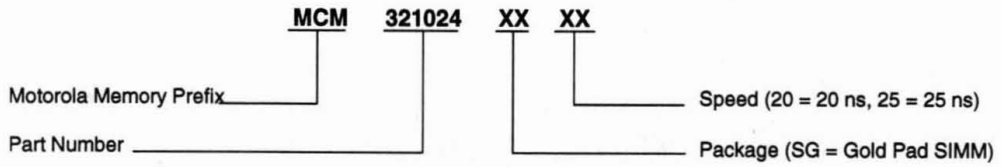
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM321024SG20 MCM321024SG25

MCM32515

Advance Information

512K x 32 Bit Fast Static RAM Module

The MCM32515 is a 16M bit static random access memory module organized as 524,288 words of 32 bits. The module is offered in a 72–lead single in–line memory module (SIMM). Four MCM6246 fast static RAMs, packaged in 36–lead SOJ packages are mounted on a printed circuit board along with eight decoupling capacitors.

The MCM6246 is a high–performance CMOS fast static RAM organized as 524,288 words of 8 bits. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM32515 is equipped with output enable ($\overline{G}$) and four separate byte enable ($\overline{E1}$ – $\overline{E4}$) inputs, allowing for greater system flexibility. The $\overline{G}$ input, when high, will force the outputs to high impedance. $\overline{Ex}$ high will do the same for byte x.

- Single 5 V ± 10% Power Supply
- Fast Access Times: 20/25 ns
- Three–State Outputs
- Fully TTL Compatible
- JEDEC Standard Pinout
- Power Requirement: 800/740 mA Maximum, Active AC
- High Board Density SIMM Package
- Byte Operation: Four Separate Chip Enables, One for Each Byte
- High Quality Six–Layer FR4 PWB with Separate Internal Power and Ground Planes
- Incorporates Motorola's State–of–the–Art Fast Static RAMs

PIN NAMES

A0 – A18	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$ – $\overline{E4}$	Byte Enables
DQ0 – DQ31	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
PD0 – PD3	Package Density
NC	No Connect

For proper operation of the device, V_{SS} must be connected to ground.

PIN ASSIGNMENT
TOP VIEW
72-LEAD SIMM – CASE TBD

NC	2	1	NC
PD3	4	3	PD2
PD0	6	5	V_{SS}
DQ0	8	7	PD1
DQ1	10	9	DQ8
DQ2	12	11	DQ9
DQ3	14	13	DQ10
V_{CC}	16	15	DQ11
A7	18	17	A0
A8	20	19	A1
A9	22	21	A2
DQ4	24	23	DQ12
DQ5	26	25	DQ13
DQ6	28	27	DQ14
DQ7	30	29	DQ15
$\overline{W}$	32	31	V_{SS}
A14	34	33	A15
$\overline{E1}$	36	35	$\overline{E2}$
$\overline{E3}$	38	37	$\overline{E4}$
A16	40	39	A17
V_{SS}	42	41	$\overline{G}$
DQ16	44	43	DQ24
DQ17	46	45	DQ25
DQ18	48	47	DQ26
DQ19	50	49	DQ27
A10	52	51	A3
A11	54	53	A4
A12	56	55	A5
A13	58	57	V_{CC}
DQ20	60	59	A6
DQ21	62	61	DQ28
DQ22	64	63	DQ29
DQ23	66	65	DQ30
V_{SS}	68	67	DQ31
NC	70	69	A18
NC	72	71	NC

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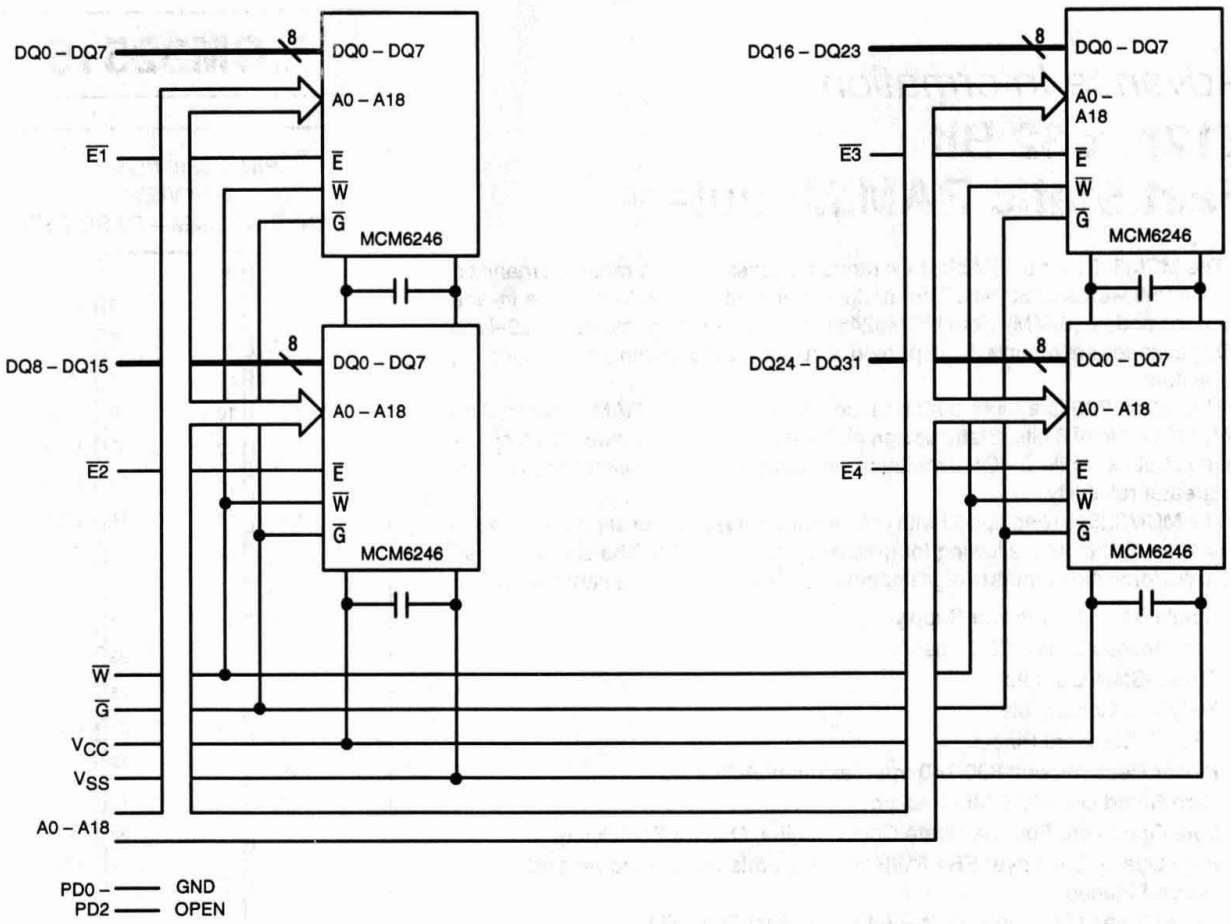
This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 2
4/7/97

FUNCTIONAL BLOCK DIAGRAM
512K x 32 MEMORY MODULE



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TRUTH TABLE

$\overline{Ex}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1} or I_{SB2}	High–Z	—
L	H	H	Read	I_{CCA}	High–Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	D_{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	4.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperatrue	T_{stg}	– 25 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

The devices on this module contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

These CMOS memory circuits have been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The module is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns)
**V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 4	µA
Output Leakage Current ($\overline{G}$, $\overline{Ex}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	—	± 4	µA
AC Active Supply Current ($\overline{G}$, $\overline{Ex}$ = V_{IL}, I_{out} = 0 mA, Cycle time ≥ t_{AVAV} min) MCM32515–20: t_{AVAV} = 20 ns MCM32515–25: t_{AVAV} = 25 ns	I_{CCA}	— —	760 700	800 740	mA
AC Standby Current ($\overline{Ex}$ = V_{IH}, Cycle time ≥ t_{AVAV} min)	I_{SB1}	—	220	240	mA
CMOS Standby Current ($\overline{Ex}$ ≥ V_{CC} – 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V)	I_{SB2}	—	40	60	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

NOTE: Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	(All pins except DQ0 – DQ31, $\overline{W}$, $\overline{G}$, and $\overline{E1}$ – $\overline{E4}$) ($\overline{E1}$ – $\overline{E4}$) ($\overline{W}$, $\overline{G}$)	C_{in}	16 10 20	24 14 32	pF
Input/Output Capacitance	(DQ0 – DQ31)	C_{out}	8	9	pF

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AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V

Output Load ..... See Figure 1a Unless Otherwise Noted
Input Rise/Fall Time ..... 3 ns

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM32515–20		MCM32515–25		Unit	Notes
		Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	20	—	25	—	ns	3
Address Access Time	t_{AVQV}	—	20	—	25	ns	
Enable Access Time	t_{ELQV}	—	20	—	25	ns	
Output Enable Access Time	t_{GLQV}	—	7	—	9	ns	
Output Hold from Address Change	t_{AXQX}	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	5	—	ns	4,5,6
Output Enable to Output Active	t_{GLQX}	0	—	0	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	0	9	0	10	ns	4,5,6
Output Enable High to Output High–Z	t_{GHQZ}	0	9	0	10	ns	4,5,6
Power Up Time	t_{ELICCH}	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	—	20	—	25	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GHQX} min, both for a given device and from device to device.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1b.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).

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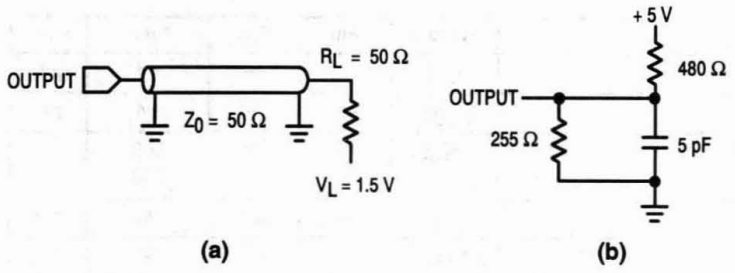
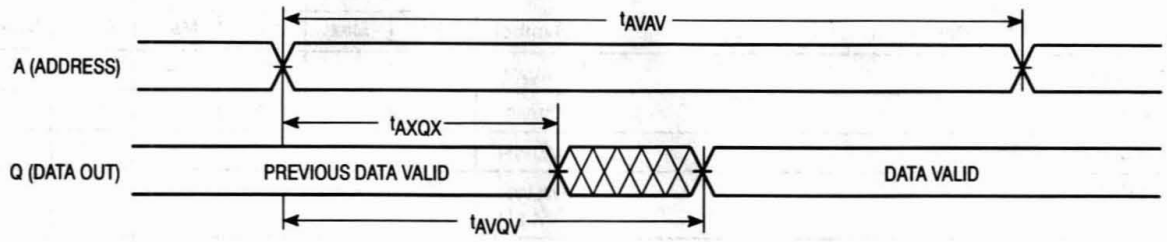


TIMING LIMITS

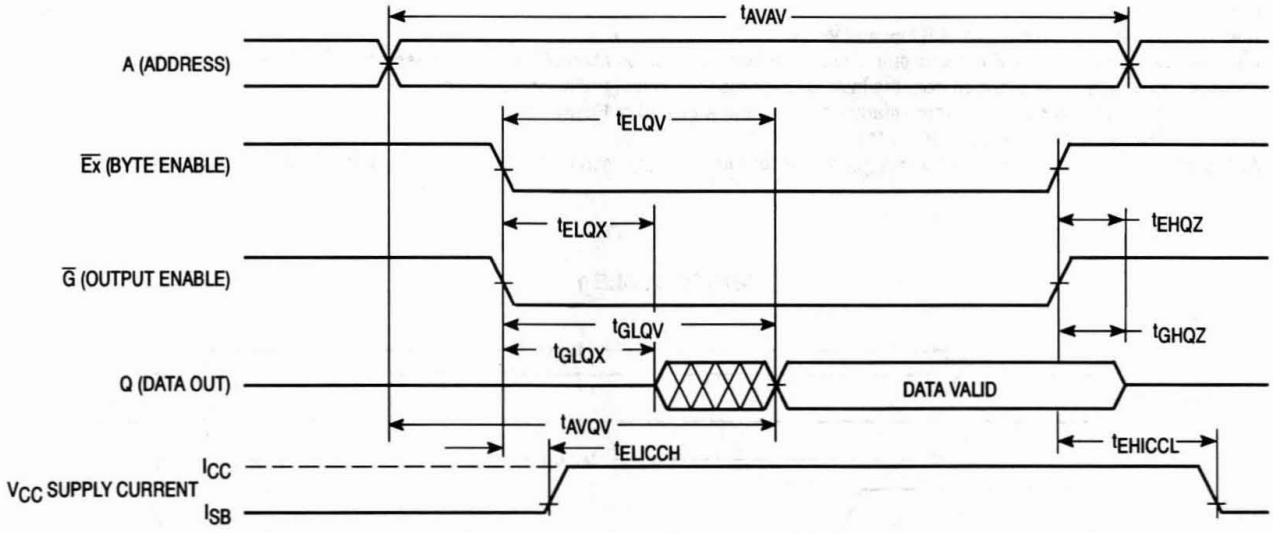
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Figure 1. Test Loads

READ CYCLE 1 (See Note 7 Above)



READ CYCLE 2 (See Note)



NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low.

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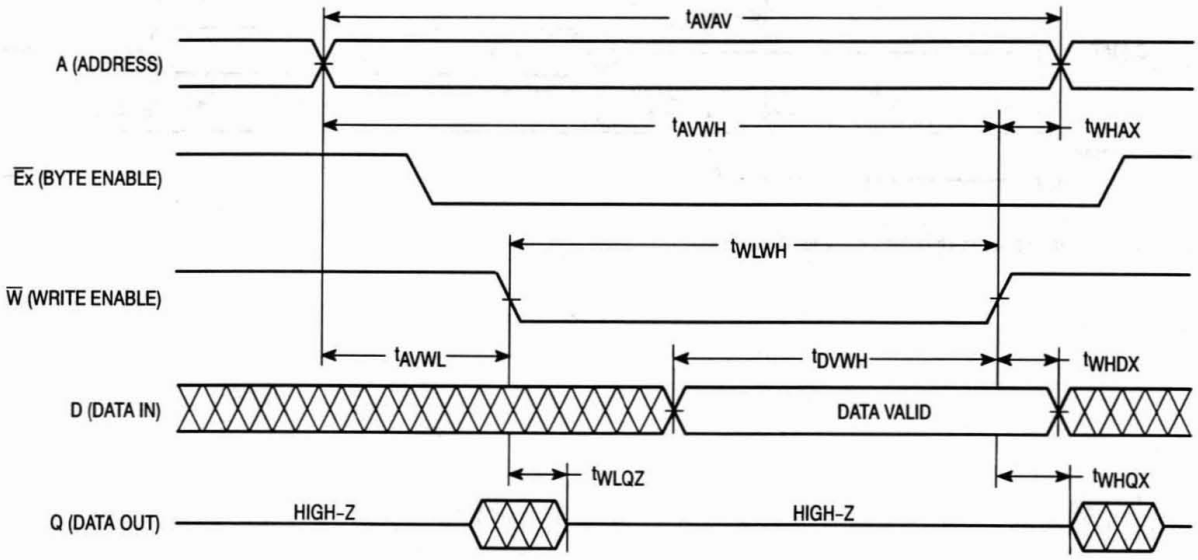
WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM32515–20		MCM32515–25		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	15	—	17	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	15	—	17	—	ns	
Data Valid to End of Write	t_{DVWH}	10	—	10	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	9	0	10	ns	4,5,6
Write High to Output Active	t_{WHQX}	5	—	5	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted. $\overline{G}$ is a don't care when $\overline{W}$ is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1b.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

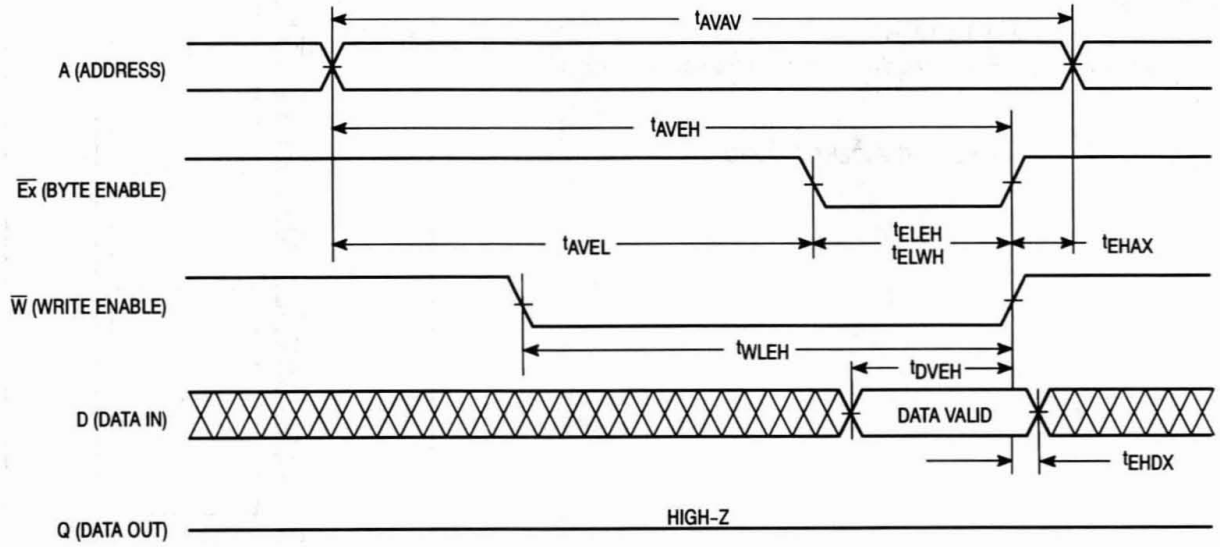


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

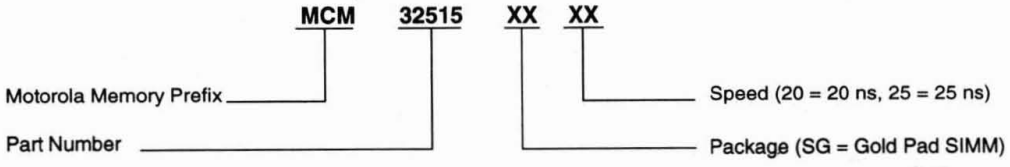
Parameter	Symbol	MCM32515–20		MCM32515–25		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	15	—	17	—	ns	
Enable to End of Write	t_{ELEH}	15	—	17	—	ns	4,5
Enable to End of Write	t_{ELWH}	15	—	17	—	ns	
Write Pulse Width	t_{WLEH}	15	—	17	—	ns	
Data Valid to End of Write	t_{DVEH}	10	—	10	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted. $\overline{G}$ is a don't care when $\overline{W}$ is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

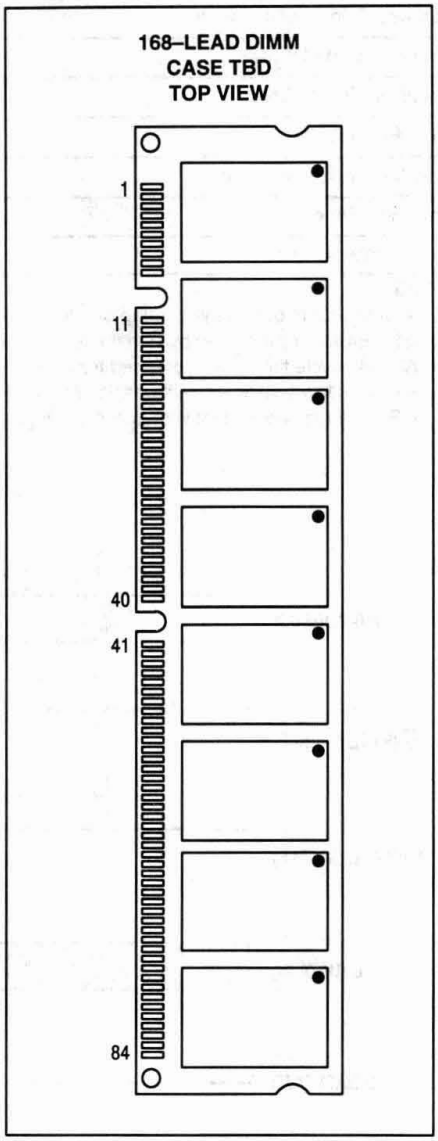


Full Part Numbers — MCM32515SG20 MCM32515SG25

MCM72F10

Advance Information

8MB Synchronous Fast Static RAM Module



The MCM72F10 (2MB) is configured as 1M x 72 bits. It is packaged in a 168–pin dual–in–line memory module DIMM. The module uses Motorola's 3.3 V, 256K x 18 bit flow–through BurstRAMs™.

Address (A), data inputs (DQ, DP), and all control signals except output enable ($\overline{G}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

Write cycles are internally self–timed and initiated by the rising edge of the clock (K) input. This feature provides increased timing flexibility for incoming signals. Synchronous byte write ($\overline{W}$) allows writes to either individual bytes or to both bytes.

- Single 3.3 V + 10%, – 5% Power Supply
- Plug and Pin Compatibility with 1MB, 2MB, and 4MB
- Multiple Clock Pins for Reduced Loading
- All Inputs and Outputs are LVTTL Compatible
- Byte Write Capability
- Fast SRAM Access Times: 8/9/12 ns
- High Quality Multi–Layer FR4 PWB With Separate Power and Ground Planes
- 168–Pin DIMM Module
- Burndy Connector, Part Number: ELF178KSC–3Z50

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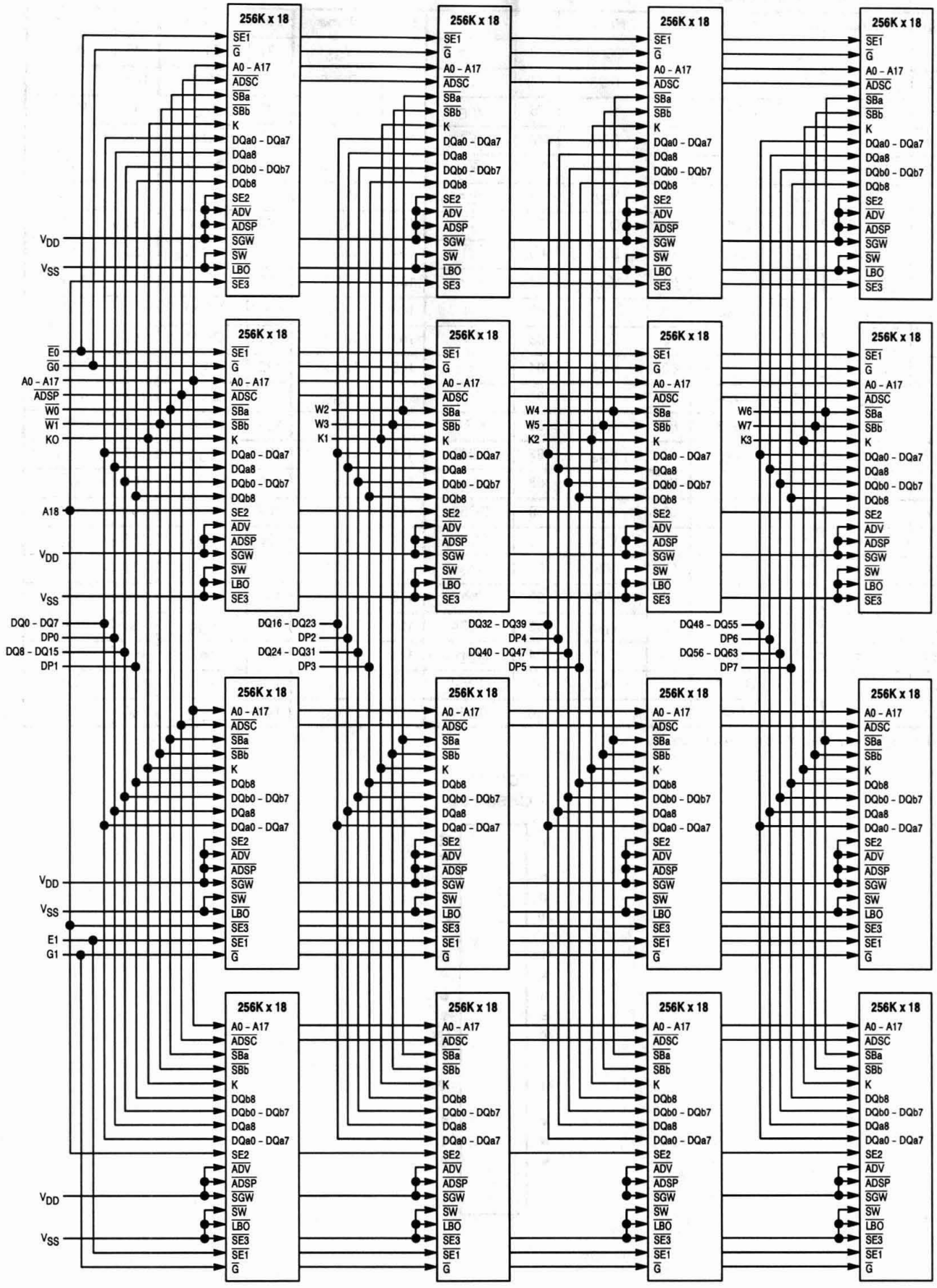
BurstRAM is a trademark of Motorola.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

3/17/97

BLOCK DIAGRAM



PIN ASSIGNMENT 168–LEAD DIMM

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	25	V_{SS}	49	DQ10	73	V_{SS}	97	V_{SS}	121	DP2	145	A15
2	DQ63	26	DQ35	50	DQ8	74	K1	98	DQ48	122	DQ22	146	A13
3	DQ62	27	DQ33	51	V_{SS}	75	V_{SS}	99	DQ47	123	V_{DD}	147	V_{DD}
4	V_{DD}	28	V_{SS}	52	DQ7	76	$\overline{W7}$	100	V_{SS}	124	DQ20	148	A11
5	DQ60	29	K3	53	DQ5	77	$\overline{W5}$	101	DQ45	125	DQ18	149	A9
6	DQ58	30	V_{SS}	54	V_{SS}	78	V_{SS}	102	DQ43	126	V_{SS}	150	V_{SS}
7	V_{SS}	31	DP3	55	DQ3	79	$\overline{W3}$	103	V_{SS}	127	DQ16	151	A7
8	DQ56	32	DQ30	56	DQ1	80	$\overline{W1}$	104	DQ41	128	DQ15	152	A5
9	DQ55	33	V_{DD}	57	V_{DD}	81	V_{SS}	105	DP4	129	V_{SS}	153	V_{SS}
10	V_{SS}	34	DQ28	58	NC	82	$\overline{G1}$	106	V_{DD}	130	DQ13	154	A3
11	DQ53	35	DQ26	59	A18	83	$\overline{E1}$	107	DQ38	131	DQ11	155	A1
12	DQ51	36	V_{SS}	60	V_{SS}	84	V_{SS}	108	DQ36	132	V_{SS}	156	$\overline{ADSP}$
13	V_{SS}	37	DQ24	61	A16	85	V_{SS}	109	V_{SS}	133	DQ9	157	V_{SS}
14	DQ49	38	DQ23	62	A14	86	DP7	110	DQ34	134	DP0	158	K0
15	DP5	39	V_{SS}	63	V_{SS}	87	DQ61	111	DQ32	135	V_{DD}	159	V_{SS}
16	V_{DD}	40	DQ21	64	A12	88	V_{SS}	112	V_{SS}	136	DQ6	160	$\overline{W6}$
17	DQ46	41	DQ19	65	A10	89	DQ59	113	K2	137	DQ4	161	$\overline{W4}$
18	DQ44	42	V_{SS}	66	V_{SS}	90	DQ57	114	V_{SS}	138	V_{SS}	162	V_{SS}
19	V_{SS}	43	DQ17	67	A8	91	V_{SS}	115	DQ31	139	DQ2	163	$\overline{W2}$
20	DQ42	44	DP1	68	A6	92	DP6	116	DQ29	140	DQ0	164	$\overline{W0}$
21	DQ40	45	V_{DD}	69	V_{DD}	93	DQ54	117	V_{SS}	141	V_{SS}	165	V_{DD}
22	V_{SS}	46	DQ14	70	A4	94	V_{DD}	118	DQ27	142	NC	166	$\overline{G0}$
23	DQ39	47	DQ12	71	A2	95	DQ52	119	DQ25	143	A17	167	$\overline{E0}$
24	DQ37	48	V_{SS}	72	A0	96	DQ50	120	V_{SS}	144	V_{SS}	168	V_{SS}

NOTE: V_{DD} must be connected on all modules.

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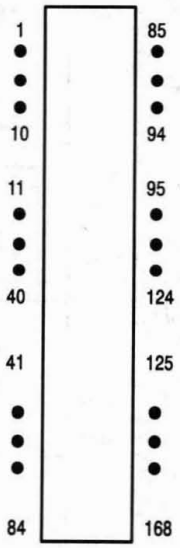
TOP VIEW
CASE TBD



PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
59, 61, 62, 64, 65, 67, 68, 70, 71, 72, 143, 145, 146, 148, 149, 151, 152, 154, 155	A0 – A18	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
156	$\overline{ADSP}$	Input	Synchronous Addresss Status Controller: Initiates read, write, or chip deselect cycle.
15, 31, 44, 86, 92, 105, 121, 134	DP0 – DP7		Synchronous Parity Data Inputs/Outputs.
2, 3, 5, 6, 8, 9, 11, 12, 14, 17, 18, 20, 21, 23, 24, 26, 27, 32, 34, 35, 37, 38, 40, 41, 43, 46, 47, 49, 50, 52, 53, 55, 56, 87, 89, 90, 93, 95, 96, 98, 99, 101, 102, 104, 107, 108, 110, 111, 115, 116, 118, 119, 122, 124, 125, 127, 128, 130, 131, 133, 136, 137, 139, 140	DQ0 – DQ63	I/O	Synchronous Data Inputs/Outputs.
83, 167	$\overline{E0}$, $\overline{E1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high — blocks $\overline{ADSP}$ or deselcts chip when $\overline{ADSC}$ is asserted.
82, 166	$\overline{G0}$, $\overline{G1}$	Input	Asynchronous Output Enable Input: Low — enables output buffer. High — DQx pins are high impedance.
29, 74, 113, 158	K0 – K3	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$ and $\overline{LBO}$.
76, 77, 79, 80, 160, 161, 163, 164	$\overline{W0}$ – $\overline{W7}$	Input	Synchronous Byte Write Inputs: x refers to the byte being written (byte a, b).
4, 16, 33, 45, 57, 69, 94, 106, 123, 135, 147, 165	V_{DD}	Supply	Power Supply: 3.3 V + 10%, – 5%.
1, 7, 10, 13, 19, 22, 25, 28, 30, 36, 39, 42, 48, 51, 54, 60, 63, 66, 73, 75, 78, 81, 84, 85, 88, 91, 97, 100, 103, 109, 112, 114, 117, 120, 126, 129, 132, 138, 141, 144, 150, 153, 157, 159, 162, 168	V_{SS}	Supply	Ground.
58, 142	NC		No Connection: There is no connection to the chip.

DATA RAM MCM69F618A SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, 3, and 4)

Next Cycle	Address Used	$\overline{E}$	$\overline{ADSP}$	$\overline{G}$	DQx	WRITE
Deselect	None	1	0	X	High–Z	X
Begin Read	External Address	0	0	0	DQ	Read
Read	Current	X	1	1	High–Z	Read
Read	Current	X	1	0	DQ	Read
Begin Write	External	0	0	X	High–Z	Write
Write	Current	X	1	X	High–Z	Write

NOTES:
1. X = don't care, 1 = logic high, 0 = logic low.
2. Write is defined as any $\overline{Wx}$ low.
3. $\overline{G}$ is an asynchronous signal and is not sampled by the clock K. $\overline{G}$ drives the bus immediately (t_{GLQX}) following $\overline{G}$ going low.
4. On write cycles that follow read cycles, $\overline{G}$ must be negated prior to the start of the write cycle to ensure proper write data setup times. $\overline{G}$ must also remain negated at the completion of the write cycle to ensure proper write data hold times.

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} (See Note 2)	V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V
Input Voltage Three State I/O (See Note 2)	V_{IT}	V_{SS} – 0.5 to V_{DD} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	4.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. This is a steady–state DC parameter that is in effect after the power supply has achieved its nominal operating level. Power sequencing can not be controlled and is not allowed.
3. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

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PACKAGE THERMAL CHARACTERISTICS — PBGA

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	41 19	°C/W	1, 2
Junction to Board (Bottom)		$R_{\theta JB}$	11	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	19	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(3.6 V ≥ V_{DD} ≥ 3.1 V, T_J = 20 to + 110°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{DD}	3.135	3.3	3.6	V
Input High Voltage	V_{IH}	1.7	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	– 0.3*	—	0.7	V

* V_{IL} ≥ – 2.0 V for t ≤ t_{KHKH}/2.

Figure 1. Undershoot Voltage

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (0 V ≤ V_{in} ≤ V_{DD})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current (0 V ≤ V_{in} ≤ V_{DD})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit
AC Supply Current (Device Selected, All Outputs Open, Cycle Time ≥ t_{KHKH} min)	MCM72F10DG8 MCM72F10DG9 MCM72F10DG12	I_{DDA}	—	3580 3480 3380	mA
CMOS Standby Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}		I_{SB1}	—	3040	mA
Clock Running Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}, All Other Inputs Held to Static CMOS Levels V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{DD} – 0.2 V)		I_{SB2}	—	1360	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_J = 20 to 110 °C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	Address, $\overline{ADSP}$ $\overline{E}$, $\overline{G}$ Other Inputs	C_{in}	74 42 26	90 50 30	pF
I/O Capacitance		$C_{I/O}$	38	42	pF

MASS (Periodically Sampled Rather Than 100% Tested)

Parameter	Max	Unit
Mass	36	g

AC OPERATING CONDITIONS AND CHARACTERISTICS

(3.6 V ≥ V_{DD} ≥ 3.1 V, T_J = 20 to + 110°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.25 V
Input Pulse Levels ..... 0 to 2.5 V
Input Slew Rate (See Notes 1 and 2) ..... 1.0 V/ns
Output Timing Reference Level ..... 1.25 V
Output Load ..... See Figure 2 Unless Otherwise Noted
Output Rise/Fall Time ..... 1.8 ns

DATA RAMs READ/WRITE CYCLE TIMING (See Notes 1, 2, 3)

Parameter	Symbol	MCM72F10–8		MCM72F10–9		MCM72F10–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	10	—	11	—	16.6	—	ns	
Clock Access Time	t_{KHQV}	—	8	—	9	—	12	ns	4
Output Enable to Output Valid	t_{GLQV}	—	3.5	—	3.5	—	5	ns	4
Clock High to Output Active	t_{KHQX1}	0	—	0	—	0	—	ns	4, 5, 6, 7
Clock High to Output Change	t_{KHQX2}	2	—	2	—	2	—	ns	4, 6
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4, 5, 6
Output Disable to Q–High–Z	t_{GHQZ}	—	3.5	—	3.5	—	3.5	ns	4, 5, 6
Clock High to Q–High–Z	t_{KHQZ}	2	3.5	2	3.5	2	3.5	ns	4, 5, 6, 7
Clock High Pulse Width	t_{KHKL}	4	—	4.5	—	5	—	ns	
Clock Low Pulse Width	t_{KLKH}	4	—	4.5	—	5	—	ns	
Setup Times: Address	t_{AVKH}	2	—	2	—	2	—	ns	
$\overline{ADSP}$	t_{ADKH}								
Data In	t_{DVKH}								
Write	t_{WVKH}								
Chip Enable	t_{EVKH}								
Hold Times: Address	t_{KHAX}	0.5	—	0.5	—	0.5	—	ns	
$\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$	t_{KHADX}								
Data In	t_{KHDX}								
Write	t_{KHWX}								
Chip Enable	t_{KHEX}								

NOTES:
1. In setup and hold times, write refers to either any $\overline{SBx}$ and $\overline{SW}$ or $\overline{SGW}$ is low.
2. Chip enable is defined as $\overline{SE1}$ low, SE2 high, and $\overline{SE3}$ low whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted.
3. All read and write cycle timings are referenced from K or $\overline{G}$.
4. Tested per AC Test Load (Figure 2).
5. Measured at ± 200 mV from steady state. Tested per High–Z Test Load (Figure 2).
6. This parameter is sampled and not 100% tested.
7. At any given voltage and temperature, t_{KHQZ} (Max) is less than t_{KHQX1} (Min) for a given device and from device to device.

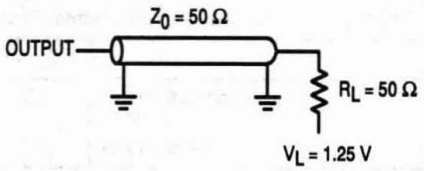
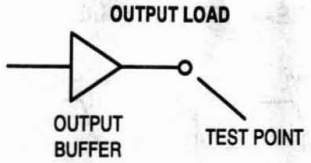
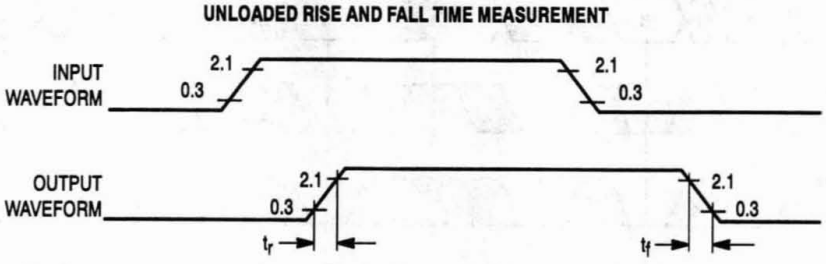


Figure 2. AC Test Load

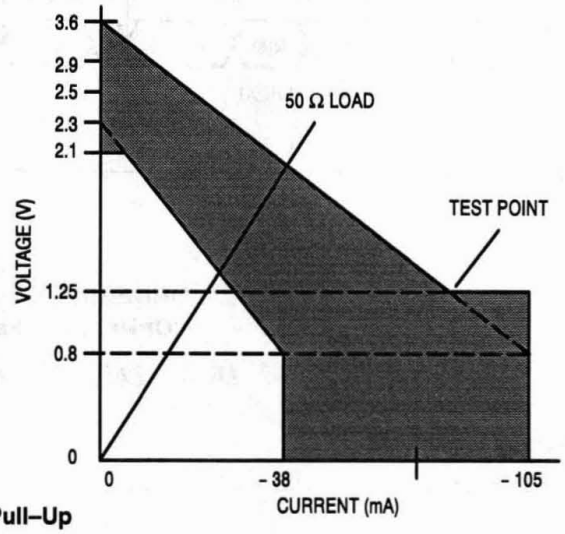




NOTES:
1. Input waveform has a slew rate of 1 V/ns.
2. Rise time is measured from 0.3 to 2.1 V unloaded.
3. Fall time is measured from 2.1 to 0.3 V unloaded.

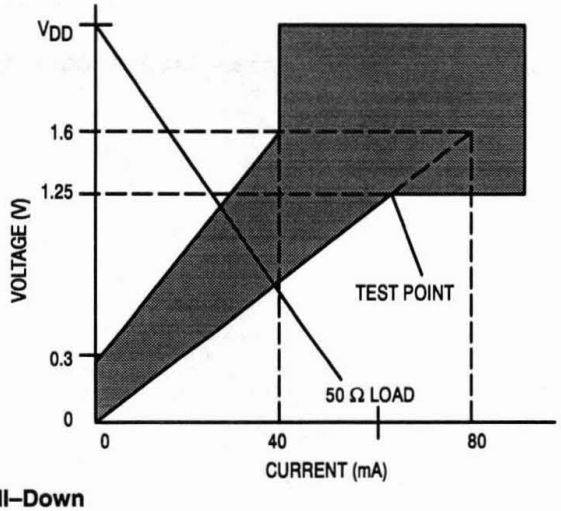
Figure 3. Unloaded Rise and Fall Time Characterization

PULL-UP		
VOLTAGE (V)	I (mA) MIN	I (mA) MAX
- 0.5	- 38	- 105
0	- 38	- 105
0.8	- 38	- 105
1.25	- 26	- 83
1.5	- 20	- 70
2.3	0	- 30
2.7	0	- 10
2.9	0	0
3.4	0	0
3.6	0	0



(a) Pull–Up

PULL-DOWN		
VOLTAGE (V)	I (mA) MIN	I (mA) MAX
- 0.5	0	0
0	0	0
0.4	10	20
0.8	20	40
1.25	31	63
1.6	40	80
2.8	40	80
3.2	40	80
3.4	40	80
3.6	46	120



(b) Pull–Down

Figure 4. Output Buffer Characteristics

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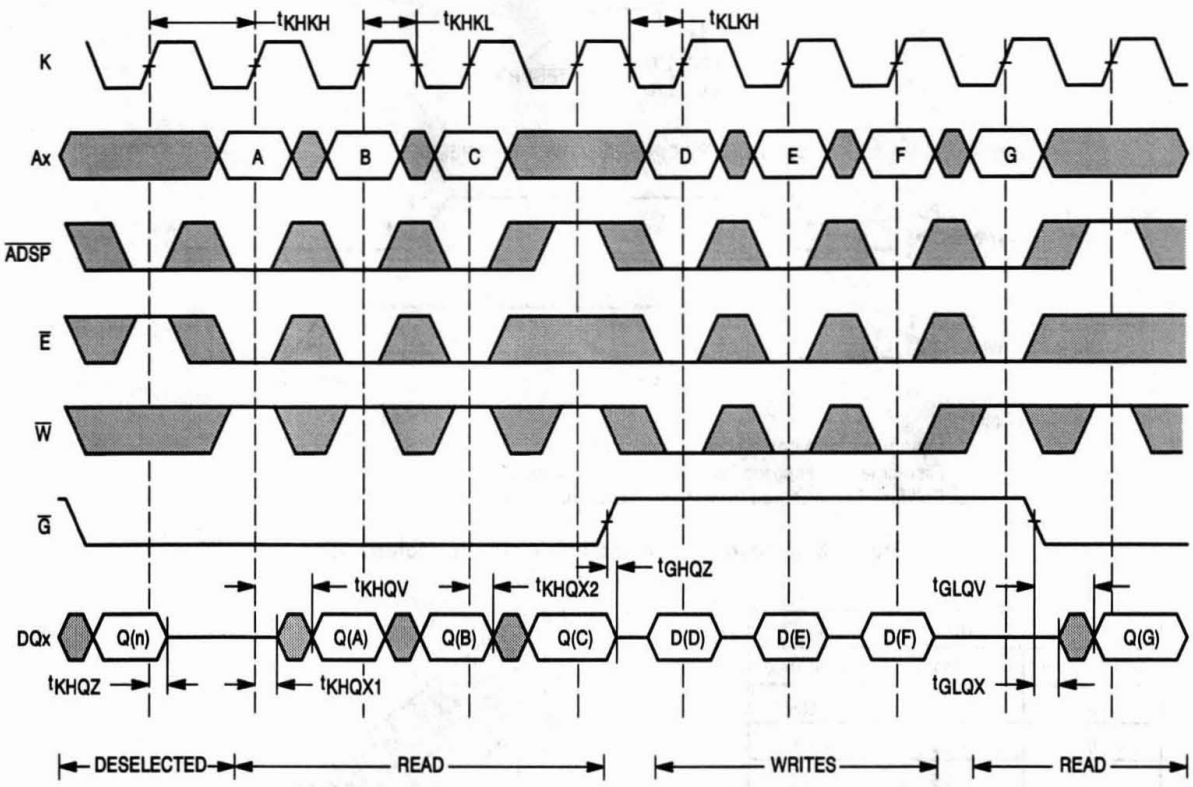
READ/WRITE CYCLES



ORDERING INFORMATION

(Order by Full Part Number)

MCM 72F X XX XX

Motorola Memory Prefix — MCM

Part Number — 72F

Memory Size (10 = 8MB) — X

Package (DG = Gold Pad DIMM) — XX

Speed (8 = 8 ns, 9 = 9 ns, 12 = 12 ns) — XX

Full Part Numbers — MCM72F10DG8 MCM72F10DG9 MCM72F10DG12

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MCM72F8
MCM72F9

Advance Information

2MB and 4MB Synchronous Fast Static RAM Module

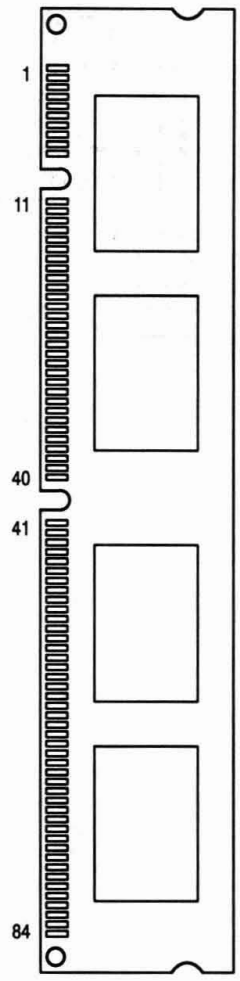
The MCM72F8 (2MB) is configured as 256K x 72 bits and the MCM72F9 (4MB) is configured as 512K x 72 bits. Both are packaged in a 168 pin dual–in–line memory module DIMM. Each module uses Motorola's 3.3 V 256K x 18 bit flow–through BurstRAMs™.

Address (A), data inputs (DQ, DP), and all control signals except output enable ($\overline{G}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

Write cycles are internally self–timed and initiated by the rising edge of the clock (K) input. This feature provides increased timing flexibility for incoming signals. Synchronous byte write ($\overline{W}$) allows writes to either individual bytes or to both bytes.

- Single 3.3 V + 10%, – 5% Power Supply
- Plug and Pin Compatibility with 2MB and 4MB
- Multiple Clock Pins for Reduced Loading
- All Inputs and Outputs are LVTTL Compatible
- Byte Write Capability
- Fast SRAM Access Times: 8/9/12 ns
- Decoupling Capacitors for Each Fast Static RAM
- High Quality Multi–Layer FR4 PWB With Separate Power and Ground Planes
- 168 Pin DIMM Module
- Burndy Connector, Part Number: ELF178KSC–3Z50

168–LEAD DIMM
CASE TBD
TOP VIEW



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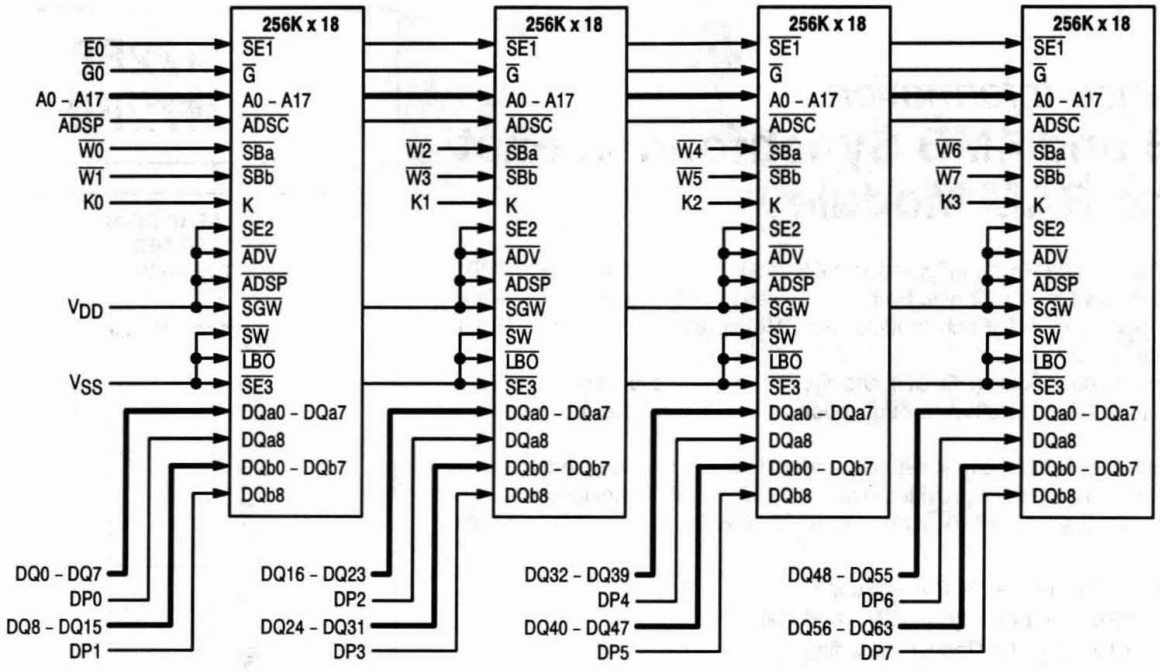
BurstRAM is a trademark of Motorola.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 1
3/17/97

MCM72F8 BLOCK DIAGRAM



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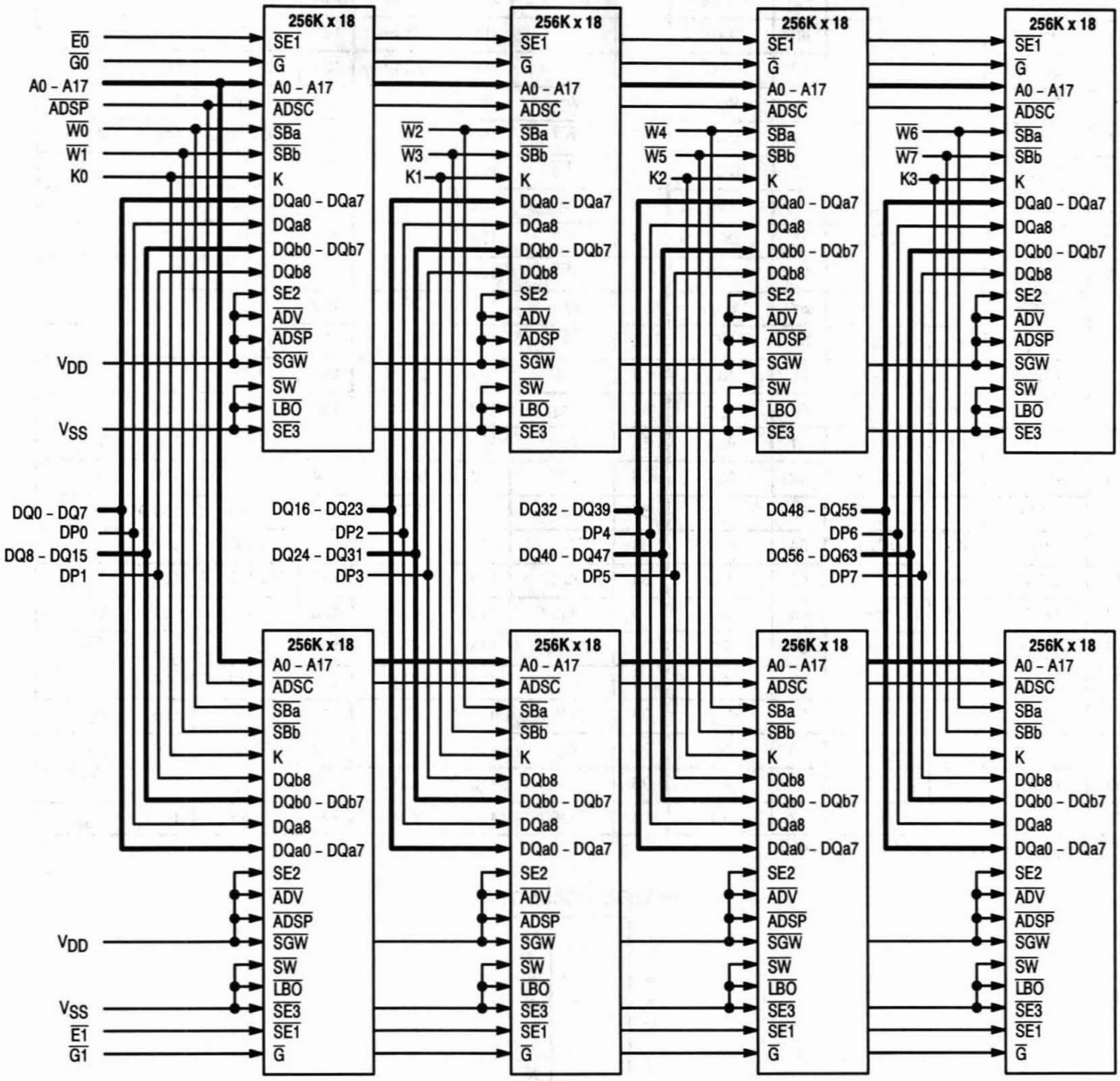
MCM72F9 BLOCK DIAGRAM



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PIN ASSIGNMENT 168–LEAD DIMM

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	25	V_{SS}	49	DQ10	73	V_{SS}	97	V_{SS}	121	DP2	145	A15
2	DQ63	26	DQ35	50	DQ8	74	K1	98	DQ48	122	DQ22	146	A13
3	DQ62	27	DQ33	51	V_{SS}	75	V_{SS}	99	DQ47	123	V_{DD}	147	V_{DD}
4	V_{DD}	28	V_{SS}	52	DQ7	76	$\overline{W7}$	100	V_{SS}	124	DQ20	148	A11
5	DQ60	29	K3	53	DQ5	77	$\overline{W5}$	101	DQ45	125	DQ18	149	A9
6	DQ58	30	V_{SS}	54	V_{SS}	78	V_{SS}	102	DQ43	126	V_{SS}	150	V_{SS}
7	V_{SS}	31	DP3	55	DQ3	79	$\overline{W3}$	103	V_{SS}	127	DQ16	151	A7
8	DQ56	32	DQ30	56	DQ1	80	$\overline{W1}$	104	DQ41	128	DQ15	152	A5
9	DQ55	33	V_{DD}	57	V_{DD}	81	V_{SS}	105	DP4	129	V_{SS}	153	V_{SS}
10	V_{SS}	34	DQ28	58	NC	82	$\overline{G1}$	106	V_{DD}	130	DQ13	154	A3
11	DQ53	35	DQ26	59	NC	83	$\overline{E1}$	107	DQ38	131	DQ11	155	A1
12	DQ51	36	V_{SS}	60	V_{SS}	84	V_{SS}	108	DQ36	132	V_{SS}	156	$\overline{ADSP}$
13	V_{SS}	37	DQ24	61	A16	85	V_{SS}	109	V_{SS}	133	DQ9	157	V_{SS}
14	DQ49	38	DQ23	62	A14	86	DP7	110	DQ34	134	DP0	158	K0
15	DP5	39	V_{SS}	63	V_{SS}	87	DQ61	111	DQ32	135	V_{DD}	159	V_{SS}
16	V_{DD}	40	DQ21	64	A12	88	V_{SS}	112	V_{SS}	136	DQ6	160	$\overline{W6}$
17	DQ46	41	DQ19	65	A10	89	DQ59	113	K2	137	DQ4	161	$\overline{W4}$
18	DQ44	42	V_{SS}	66	V_{SS}	90	DQ57	114	V_{SS}	138	V_{SS}	162	V_{SS}
19	V_{SS}	43	DQ17	67	A8	91	V_{SS}	115	DQ31	139	DQ2	163	$\overline{W2}$
20	DQ42	44	DP1	68	A6	92	DP6	116	DQ29	140	DQ0	164	$\overline{W0}$
21	DQ40	45	V_{DD}	69	V_{DD}	93	DQ54	117	V_{SS}	141	V_{SS}	165	V_{DD}
22	V_{SS}	46	DQ14	70	A4	94	V_{DD}	118	DQ27	142	NC	166	$\overline{G0}$
23	DQ39	47	DQ12	71	A2	95	DQ52	119	DQ25	143	A17	167	$\overline{E0}$
24	DQ37	48	V_{SS}	72	A0	96	DQ50	120	V_{SS}	144	V_{SS}	168	V_{SS}

NOTE: V_{DD} must be connected on all modules.

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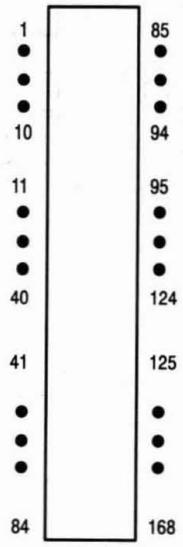
TOP VIEW – CASE TBD



PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
61, 62, 64, 65, 67, 68, 70, 71, 72, 143, 145, 146, 148, 149, 151, 152, 154, 155	A0 – A17	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
156	$\overline{ADSP}$	Input	Synchronous Addresss Status Controller: Initiates read, write, or chip deselect cycle.
15, 31, 44, 86, 92, 105, 121, 134	DP0 – DP7		Synchronous Parity Data Inputs/Outputs
2, 3, 5, 6, 8, 9, 11, 12, 14, 17, 18, 20, 21, 23, 24, 26, 27, 32, 34, 35, 37, 38, 40, 41, 43, 46, 47, 49, 50, 52, 53, 55, 56, 87, 89, 90, 93, 95, 96, 98, 99, 101, 102, 104, 107, 108, 110, 111, 115, 116, 118, 119, 122, 124, 125, 127, 128, 130, 131, 133, 136, 137, 139, 140	DQ0 – DQ63	I/O	Synchronous Data Inputs/Outputs
167, 83	$\overline{E0}$, $\overline{E1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high – blocks $\overline{ADSP}$ or deselcts chip when $\overline{ADSC}$ is asserted. $\overline{E1}$ is only used on 4MB module.
166, 82	$\overline{G0}$, $\overline{G1}$	Input	Asynchronous Output Enable Input: Low – enables output buffer. High – DQx pins are high impedance. $\overline{G1}$ is only used on 4MB module.
29, 74, 113, 158	K0 – K3	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$ and $\overline{LBO}$.
76, 77, 79, 80, 160, 161, 163, 164	$\overline{W0}$ – $\overline{W7}$	Input	Synchronous Byte Write Inputs: x refers to the byte being written (byte a, b). $\overline{SGW}$ overrides $\overline{SBx}$.
4, 16, 33, 45, 57, 69, 94, 106, 123, 135, 147, 165	V_{DD}	Supply	Power Supply: 3.3 V + 10%, – 5%.
1, 7, 10, 13, 19, 22, 25, 28, 30, 36, 39, 42, 48, 51, 54, 60, 63, 66, 73, 75, 78, 81, 84, 85, 88, 91, 97, 100, 103, 109, 112, 114, 117, 120, 126, 129, 132, 138, 141, 144, 150, 153, 157, 159, 162, 168	V_{SS}	Supply	Ground.
58, 59, 142	NC		No Connection: There is no connection to the chip.

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DATA RAM MCM69F618A SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, 3 and 4)

Next Cycle	Address Used	$\overline{E}$	$\overline{ADSP}$	$\overline{G}$	DQx	WRITE
Deselect	None	1	0	X	High–Z	X
Begin Read	External Address	0	0	0	DQ	Read
Read	Current	X	1	1	High–Z	Read
Read	Current	X	1	0	DQ	Read
Begin Write	External	0	0	X	High–Z	Write
Write	Current	X	1	X	High–Z	Write

NOTES:
1. X = don't care, 1 = logic high, 0 = logic low.
2. Write is defined as any $\overline{Wx}$ low.
3. $\overline{G}$ is an asynchronous signal and is not sampled by the clock K. $\overline{G}$ drives the bus immediately (t_{GLQX}) following $\overline{G}$ going low.
4. On write cycles that follow read cycles, $\overline{G}$ must be negated prior to the start of the write cycle to insure proper write data setup times. $\overline{G}$ must also remain negated at the completion of the write cycle to insure proper write data hold times.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{DD}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} (See Note 2)		V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V
Input Voltage Three State I/O (See Note 2)		V_{IT}	– 0.5 to V_{DD} + 0.5	V
Output Current (per I/O)		I_{out}	± 20	mA
Power Dissipation	MCM72F8 MCM72F9	P_D	4.6 9.2	W
Temperature Under Bias		T_{bias}	– 10 to + 85	°C
Operating Temperature		T_J	20 to + 110	°C
Storage Temperature		T_{stg}	– 55 to + 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. This is a steady–state DC parameter that is in effect after the power supply has achieved its nominal operating level. Power sequencing cannot be controlled and is not allowed.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_J = 20 to + 110°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{DD}	3.135	3.3	3.6	V
Input High Voltage	V_{IH}	1.7	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	– 0.3*	—	0.7	V

* $V_{IL} \geq -2.0$ V for $t \leq t_{KHKH}/2$.

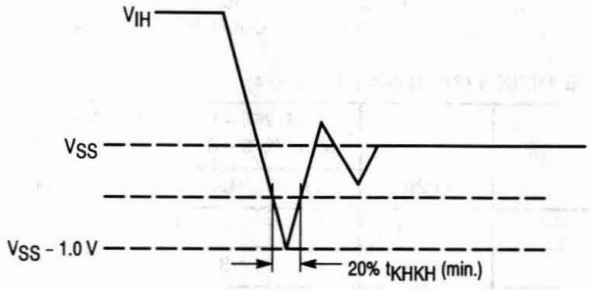


Figure 1. Undershoot Voltage

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (0 V ≤ V_{in} ≤ V_{DD})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current (0 V ≤ V_{in} ≤ V_{DD})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit
AC Supply Current (Device Selected, All Outputs Open, Cycle Time ≥ t_{KHKH} min)	MCM72F8DG8 MCM72F8DG9 MCM72F8DG12 MCM72F9DG8 MCM72F9DG9 MCM72F9DG12	I_{DDA}	—	1300 1200 1120 2600 2400 2240	mA
CMOS Standby Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}	MCM72F8DG MCM72F9DG	I_{SB1}	—	520 1040	mA
Clock Running Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}, All Other Inputs Held to Static CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{DD} – 0.2 V)	MCM72F8DG MCM72F9DG	I_{SB2}	—	120 240	mA

MCM72F8 CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_J = 20 to 110°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	$\overline{W}$, K Other Inputs	C_{in}	— —	15 32	pF
I/O Capacitance		$C_{I/O}$	—	18	pF

MCM72F9 CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_J = 20 to 110 °C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	$\overline{W}$, K $\overline{E}$, $\overline{G}$ Other Inputs	C_{in}	— — —	20 32 52	pF
I/O Capacitance		$C_{I/O}$	—	26	pF

MASS (Periodically Sampled Rather Than 100% Tested)

Parameter	Max	Unit
MCM72F8	16	g
MCM72F9	20	g

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_J = 20 to + 110°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.25 V
Input Pulse Levels ..... 0 to 2.5 V
Input Rise/Fall Time ..... 1 ns

Output Timing Reference Level ..... 1.25 V
Output Load ..... See Figure 2 Unless Otherwise Noted
Output Rise/Fall Time ..... 1.8 ns

DATA RAMs READ/WRITE CYCLE TIMING (See Notes 1, 2, 3 and 4)

Parameter	Symbol	MCM72F8 – 8 MCM72F9 – 8		MCM72F8 – 9 MCM72F9 – 9		MCM72F8 – 12 MCM72F9 – 12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	10	—	11	—	16.6	—	ns	
Clock Access Time	t_{KHQV}	—	8	—	9	—	12	ns	4
Output Enable to Output Valid	t_{GLQV}	—	3.5	—	3.5	—	5	ns	4
Clock High to Output Active	t_{KHQX1}	0	—	0	—	0	—	ns	4, 5, 6
Clock High to Output Change	t_{KHQX2}	2	—	2	—	2	—	ns	4, 6
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4, 5, 6
Output Disable to Q–High–Z	t_{GHQZ}	—	3.5	—	3.5	—	3.5	ns	4, 5, 6
Clock High to Q–High–Z	t_{KHQZ}	2	3.5	2	3.5	2	3.5	ns	4, 5, 6
Clock High Pulse Width	t_{KHKL}	4	—	4.5	—	5	—	ns	
Clock Low Pulse Width	t_{KLKH}	4	—	4.5	—	5	—	ns	
Setup Times: Address	t_{AVKH}	2	—	2	—	2	—	ns	
$\overline{ADSP}$	t_{ADKH}								
Data In	t_{DVKH}								
Write	t_{WVKH}								
Chip Enable	t_{EVKH}								
Hold Times: Address	t_{KHAX}	0.5	—	0.5	—	0.5	—	ns	
$\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$	t_{KHADX}								
Data In	t_{KHDX}								
Write	t_{KHWX}								
Chip Enable	t_{KHEX}								

NOTES:
1. In setup and hold times, write refers to either any $\overline{SBx}$ and $\overline{SW}$ or $\overline{SGW}$ is low.
2. Chip enable is defined as $\overline{SE1}$ low, SE2 high, and $\overline{SE3}$ low whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted.
3. All read and write cycle timings are referenced from K or $\overline{G}$.
4. Tested per AC Test Load (Figure 2).
5. Measured at ± 200 mV from steady state.
6. This parameter is sampled and not 100% tested.

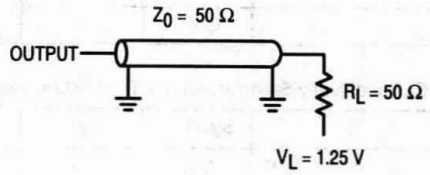
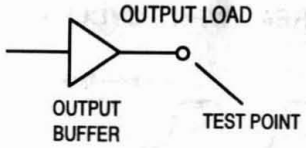


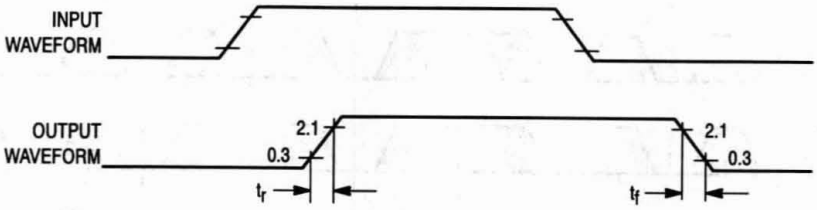
Figure 2. AC Test Load

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.



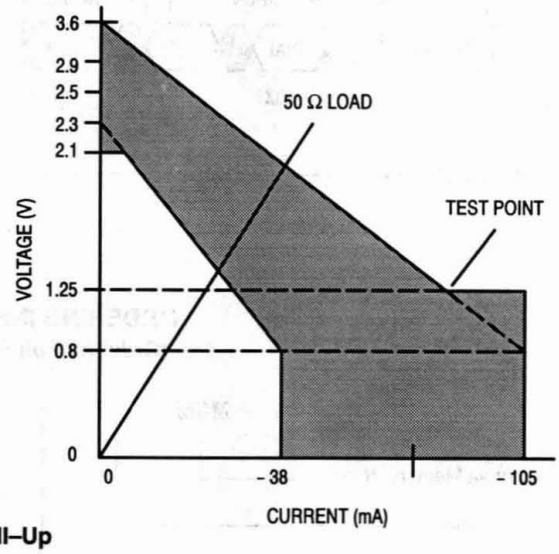
UNLOADED RISE AND FALL TIME MEASUREMENT



NOTES:
1. Input waveform has a slew rate of 1 V/ns.
2. Rise time is measured from 0.3 V to 2.1 V unloaded.
3. Fall time is measured from 2.1 V to 0.3 V unloaded.

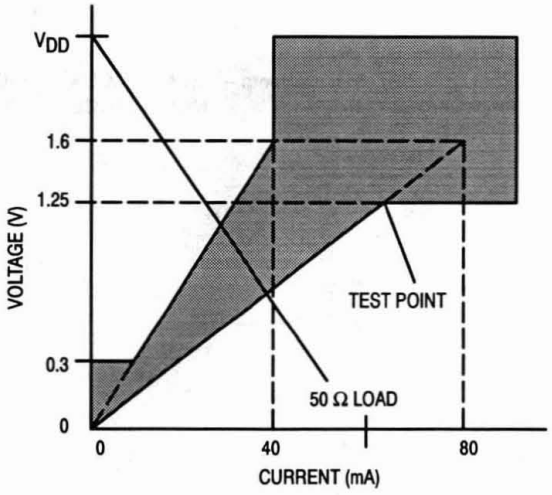
Figure 3. Unloaded Rise and Fall Time Characterization

PULL-UP		
VOLTAGE (V)	I (mA) Min	I (mA) Max
- 0.5	- 38	- 105
0	- 38	- 105
0.8	- 38	- 105
1.25	- 26	- 83
1.5	- 20	- 70
2.3	0	- 30
2.7	0	- 10
2.9	0	0
3.4	0	0
3.6	0	0



(a) Pull–Up

PULL-DOWN		
VOLTAGE (V)	I (mA) Min	I (mA) Max
- 0.5	0	0
0	0	0
0.4	10	20
0.8	20	40
1.25	31	63
1.6	40	80
2.8	40	80
3.2	40	80
3.4	40	80
3.6	40	80

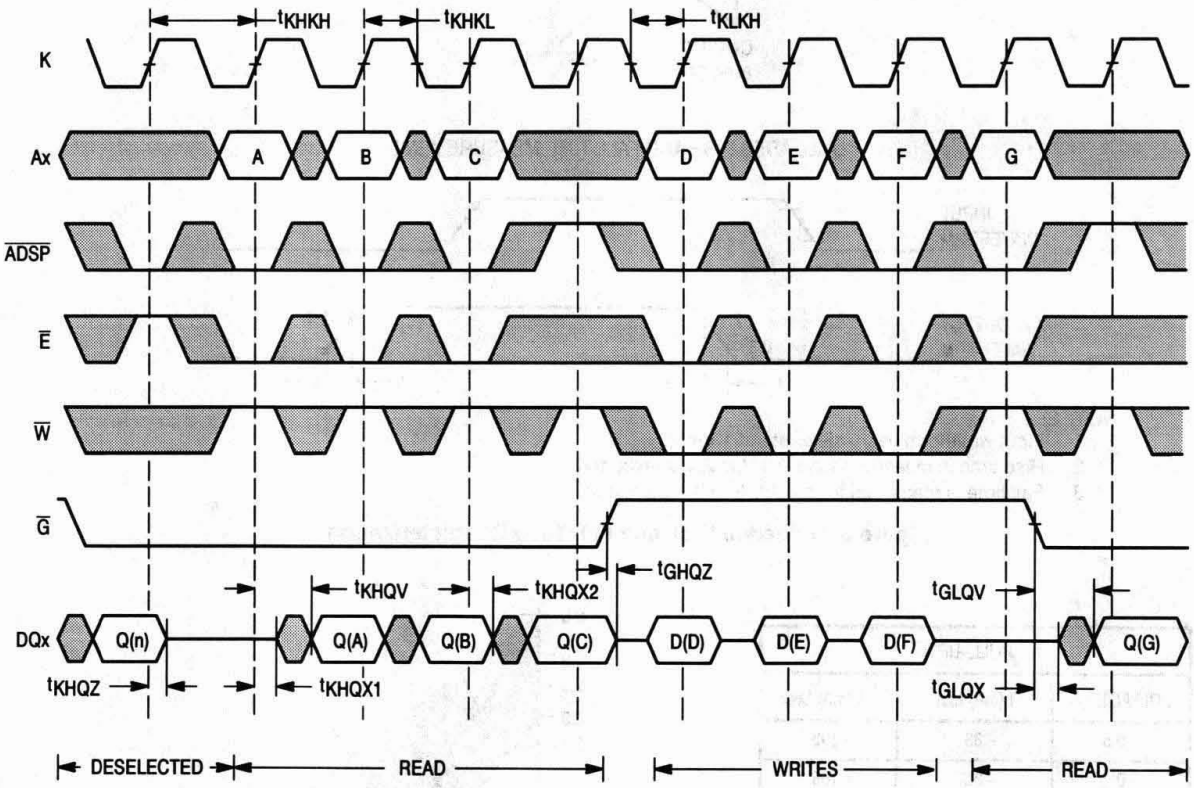


(b) Pull–Down

Figure 4. Output Buffer Characteristics

6

READ/WRITE CYCLES



ORDERING INFORMATION

(Order by Full Part Number)

MCM 72F X XX XX

Motorola Memory Prefix — MCM

Part Number — 72F

Speed (8 = 8 ns, 9 = 9 ns, 12 = 12 ns) — XX

Package (DG = Gold Pad DIMM) — XX

Memory Size (8 = 2MB, 9 = 4MB) — X

Full Part Numbers — MCM72F8DG8, MCM72F8DG9, MCM72F8DG12, MCM72F9DG8, MCM72F9DG9, MCM72F9DG12

MCM72F6
MCM72F7

Advance Information

512KB and 1MB Synchronous Fast Static RAM Module

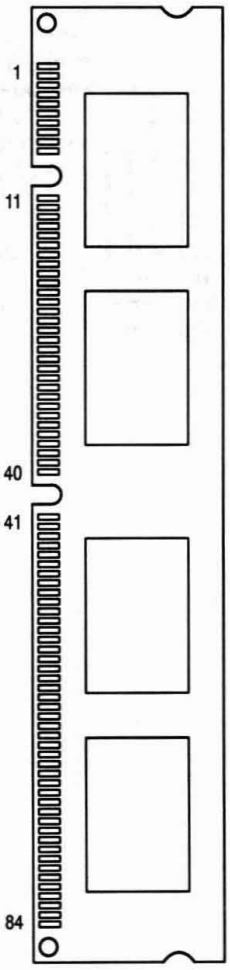
The MCM72F6 (512KB) is configured as 64K x 72 bits and the MCM72F7 (1MB) is configured as 128K x 72 bits. Both are packaged in a 168 pin dual–in–line memory module DIMM. Each module uses Motorola's 3.3 V 64K x 18 bit flow–through BurstRAMs™.

Address (A), data inputs (DQ, DP), and all control signals except output enable ($\overline{G}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

Write cycles are internally self–timed and initiated by the rising edge of the clock (K) input. This feature provides increased timing flexibility for incoming signals. Synchronous byte write ($\overline{W}$) allows writes to either individual bytes or to both bytes.

- Single 3.3 V + 10%, – 5% Power Supply
- Plug and Pin Compatibility with 2MB and 4MB
- Multiple Clock Pins for Reduced Loading
- All Inputs and Outputs are LVTTL Compatible
- Byte Write Capability
- Fast SRAM Access Times: 9/10/12 ns
- Decoupling Capacitors for Each Fast Static RAM
- High Quality Multi–Layer FR4 PWB With Separate Power and Ground Planes
- 168 Pin DIMM Module
- Burndy Connector, Part Number: ELF178KSC–3Z50

168–LEAD DIMM
CASE TBD
TOP VIEW



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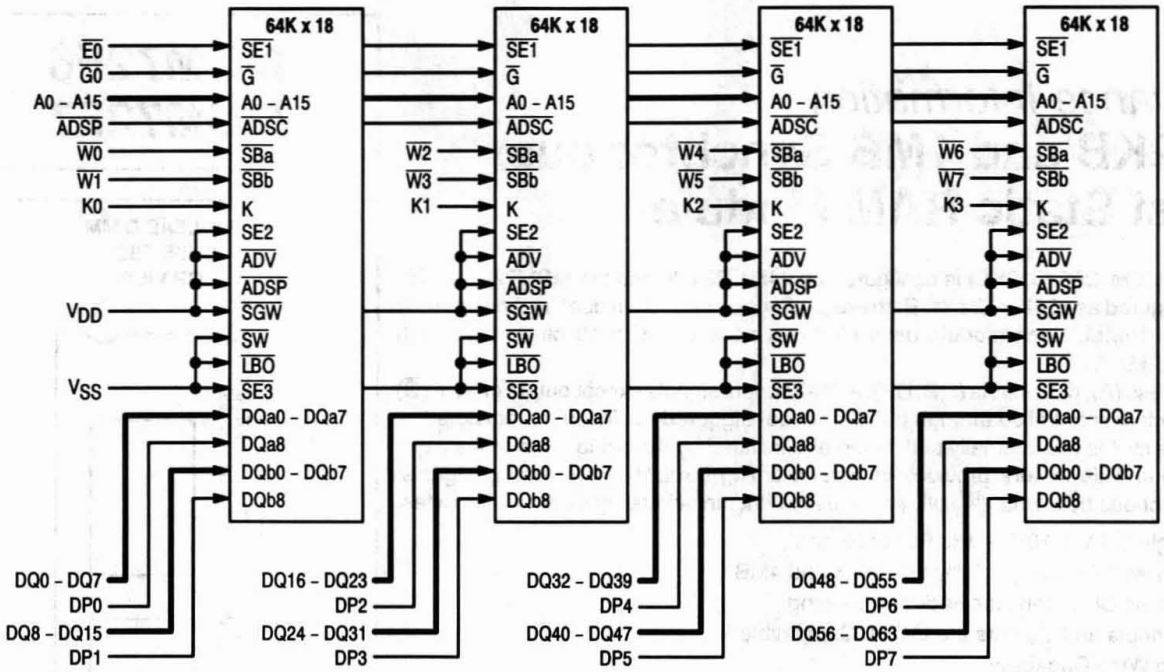
BurstRAM is a trademark of Motorola.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 1
3/17/97

MCM72F6 BLOCK DIAGRAM



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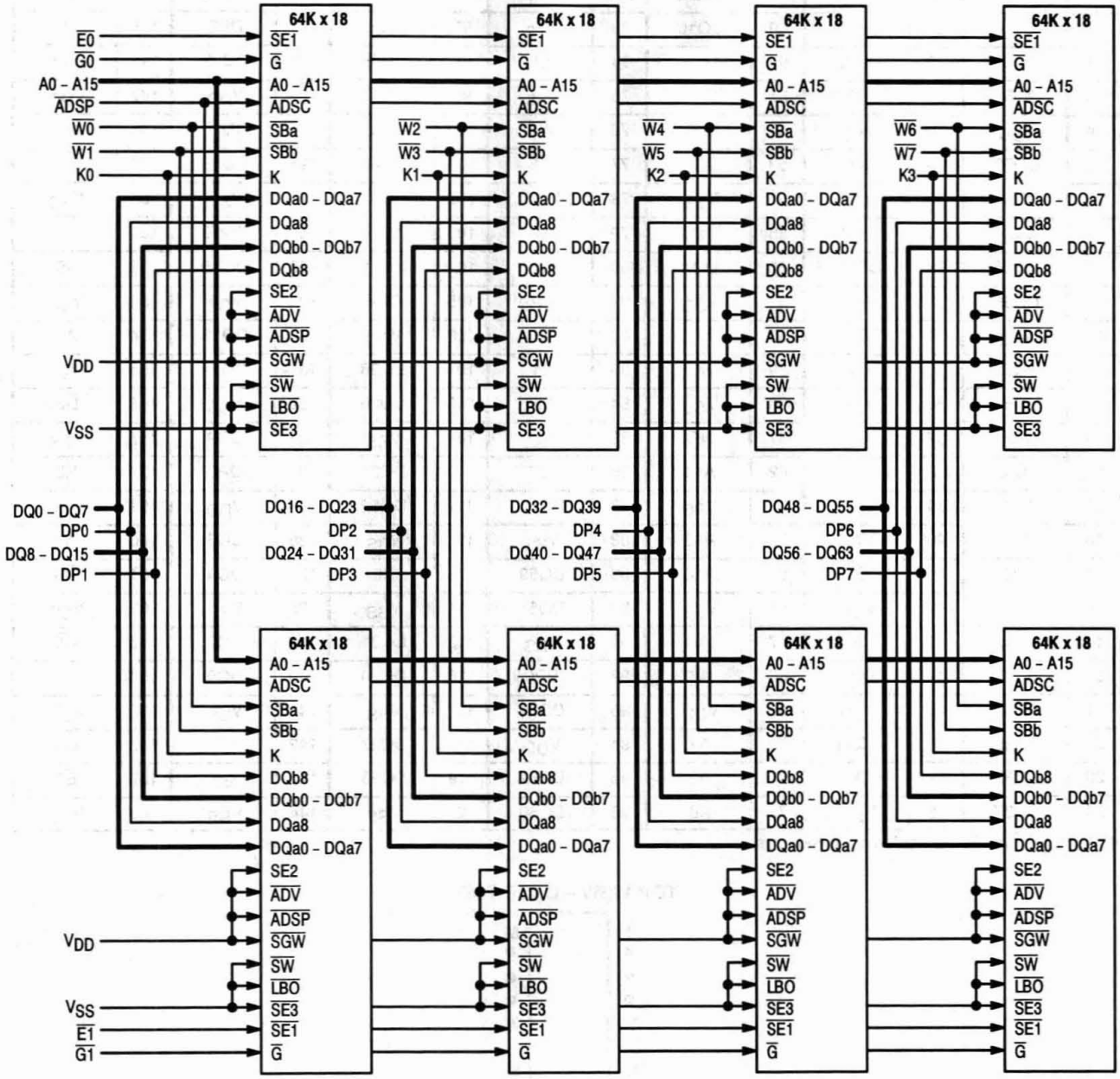
MCM72F7 BLOCK DIAGRAM



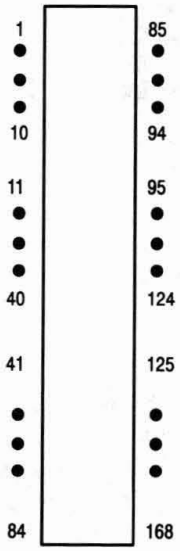
PIN ASSIGNMENT 168–LEAD DIMM

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	25	V_{SS}	49	DQ10	73	V_{SS}	97	V_{SS}	121	DP2	145	A15
2	DQ63	26	DQ35	50	DQ8	74	K1	98	DQ48	122	DQ22	146	A13
3	DQ62	27	DQ33	51	V_{SS}	75	V_{SS}	99	DQ47	123	V_{DD}	147	V_{DD}
4	V_{DD}	28	V_{SS}	52	DQ7	76	$\overline{W7}$	100	V_{SS}	124	DQ20	148	A11
5	DQ60	29	K3	53	DQ5	77	$\overline{W5}$	101	DQ45	125	DQ18	149	A9
6	DQ58	30	V_{SS}	54	V_{SS}	78	V_{SS}	102	DQ43	126	V_{SS}	150	V_{SS}
7	V_{SS}	31	DP3	55	DQ3	79	$\overline{W3}$	103	V_{SS}	127	DQ16	151	A7
8	DQ56	32	DQ30	56	DQ1	80	$\overline{W1}$	104	DQ41	128	DQ15	152	A5
9	DQ55	33	V_{DD}	57	V_{DD}	81	V_{SS}	105	DP4	129	V_{SS}	153	V_{SS}
10	V_{SS}	34	DQ28	58	NC	82	$\overline{G1}$	106	V_{DD}	130	DQ13	154	A3
11	DQ53	35	DQ26	59	NC	83	$\overline{E1}$	107	DQ38	131	DQ11	155	A1
12	DQ51	36	V_{SS}	60	V_{SS}	84	V_{SS}	108	DQ36	132	V_{SS}	156	$\overline{ADSP}$
13	V_{SS}	37	DQ24	61	NC	85	V_{SS}	109	V_{SS}	133	DQ9	157	V_{SS}
14	DQ49	38	DQ23	62	A14	86	DP7	110	DQ34	134	DP0	158	K0
15	DP5	39	V_{SS}	63	V_{SS}	87	DQ61	111	DQ32	135	V_{DD}	159	V_{SS}
16	V_{DD}	40	DQ21	64	A12	88	V_{SS}	112	V_{SS}	136	DQ6	160	$\overline{W6}$
17	DQ46	41	DQ19	65	A10	89	DQ59	113	K2	137	DQ4	161	$\overline{W4}$
18	DQ44	42	V_{SS}	66	V_{SS}	90	DQ57	114	V_{SS}	138	V_{SS}	162	V_{SS}
19	V_{SS}	43	DQ17	67	A8	91	V_{SS}	115	DQ31	139	DQ2	163	$\overline{W2}$
20	DQ42	44	DP1	68	A6	92	DP6	116	DQ29	140	DQ0	164	$\overline{W0}$
21	DQ40	45	V_{DD}	69	V_{DD}	93	DQ54	117	V_{SS}	141	V_{SS}	165	V_{DD}
22	V_{SS}	46	DQ14	70	A4	94	V_{DD}	118	DQ27	142	NC	166	$\overline{G0}$
23	DQ39	47	DQ12	71	A2	95	DQ52	119	DQ25	143	NC	167	$\overline{E0}$
24	DQ37	48	V_{SS}	72	A0	96	DQ50	120	V_{SS}	144	V_{SS}	168	V_{SS}

NOTE: V_{DD} must be connected on all modules.

6

TOP VIEW – CASE TBD



PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
62, 64, 65, 67, 68, 70, 71, 72, 145, 146, 148, 149, 151, 152, 154, 155	A0 – A15	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
156	$\overline{ADSP}$	Input	Synchronous Addresss Status Controller: Initiates read, write, or chip deselect cycle.
15, 31, 44, 86, 92, 105, 121, 134	DP0 – DP7		Synchronous Parity Data Inputs/Outputs
2, 3, 5, 6, 8, 9, 11, 12, 14, 17, 18, 20, 21, 23, 24, 26, 27, 32, 34, 35, 37, 38, 40, 41, 43, 46, 47, 49, 50, 52, 53, 55, 56, 87, 89, 90, 93, 95, 96, 98, 99, 101, 102, 104, 107, 108, 110, 111, 115, 116, 118, 119, 122, 124, 125, 127, 128, 130, 131, 133, 136, 137, 139, 140	DQ0 – DQ63	I/O	Synchronous Data Inputs/Outputs
167, 83	$\overline{E0}$, $\overline{E1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high – blocks $\overline{ADSP}$ or deselcts chip when $\overline{ADSC}$ is asserted. $\overline{E1}$ is only used on 1MB module.
166, 82	$\overline{G0}$, $\overline{G1}$	Input	Asynchronous Output Enable Input: Low – enables output buffer. High – DQx pins are high impedance. $\overline{G1}$ is only used on 1MB module.
29, 74, 113, 158	K0 – K3	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$ and $\overline{LBO}$.
76, 77, 79, 80, 160, 161, 163, 164	$\overline{W0}$ – $\overline{W7}$	Input	Synchronous Byte Write Inputs: x refers to the byte being written (byte a, b). $\overline{SGW}$ overrides $\overline{SBx}$.
4, 16, 33, 45, 57, 69, 94, 106, 123, 135, 147, 165	V_{DD}	Supply	Power Supply: 3.3 V + 10%, – 5%.
1, 7, 10, 13, 19, 22, 25, 28, 30, 36, 39, 42, 48, 51, 54, 60, 63, 66, 73, 75, 78, 81, 84, 85, 88, 91, 97, 100, 103, 109, 112, 114, 117, 120, 126, 129, 132, 138, 141, 144, 150, 153, 157, 159, 162, 168	V_{SS}	Supply	Ground.
58, 59, 61, 142, 143	NC		No Connection: There is no connection to the chip.

DATA RAM MCM69F618A SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, 3 and 4)

Next Cycle	Address Used	$\overline{E}$	$\overline{ADSP}$	$\overline{G}$	DQx	WRITE
Deselect	None	1	0	X	High–Z	X
Begin Read	External Address	0	0	0	DQ	Read
Read	Current	X	1	1	High–Z	Read
Read	Current	X	1	0	DQ	Read
Begin Write	External	0	0	X	High–Z	Write
Write	Current	X	1	X	High–Z	Write

NOTES:
1. X = don't care, 1 = logic high, 0 = logic low.
2. Write is defined as any $\overline{Wx}$ low.
3. $\overline{G}$ is an asynchronous signal and is not sampled by the clock K. $\overline{G}$ drives the bus immediately (t_{GLQX}) following $\overline{G}$ going low.
4. On write cycles that follow read cycles, $\overline{G}$ must be negated prior to the start of the write cycle to insure proper write data setup times. $\overline{G}$ must also remain negated at the completion of the write cycle to insure proper write data hold times.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{DD}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS}		V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V
Output Current (per I/O)		I_{out}	± 20	mA
Power Dissipation	MCM72F6 MCM72F7	P_D	4.6 9.2	W
Temperature Under Bias		T_{bias}	– 10 to + 85	°C
Operating Temperature		T_J	20 to + 110	°C
Storage Temperature		T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

6

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V ± 10%, – 5%, T_J = 20 to + 110°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{DD}	3.135	3.6	V
Input High Voltage	V_{IH}	2.0	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* $V_{IL} \geq -2.0$ V for $t \leq t_{KHKH}/2$.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (0 V ≤ V_{in} ≤ V_{DD})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current (0 V ≤ V_{in} ≤ V_{DD})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit	Notes
AC Supply Current (Device Selected, All Outputs Open, Cycle Time ≥ t_{KHKH} min)	MCM72F6DG9 MCM72F6DG10 MCM72F6DG10 MCM72F7DG9 MCM72F7DG10 MCM72F7DG12	I_{DDA}	—	900 860 840 1800 1720 1680	mA	2, 3, 4
CMOS Standby Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}, All Inputs Toggling at CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{DD} – 0.2 V)	MCM72F6DG9 MCM72F6DG10 MCM72F6DG12 MCM72F7DG9 MCM72F7DG10 MCM72F7DG912	I_{SB1}	—	440 400 380 880 800 760	mA	
Clock Running Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}, All Other Inputs Held to Static CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{DD} – 0.2 V)	MCM72F6DG9 MCM72F6DG10/12 MCM72F7DG9 MCM72F7DG10/12	I_{SB2}	—	160 140 320 280	mA	

MCM72F6 CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_J = 20 to 110°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	$\overline{W}$, K Other Inputs	C_{in}	— —	16 36	pF
I/O Capacitance		$C_{I/O}$	—	19	pF

MCM72F7 CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_J = 20 to 110 °C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	$\overline{W}$, K $\overline{E}$, $\overline{G}$ Other Inputs	C_{in}	— — —	22 36 60	pF
I/O Capacitance		$C_{I/O}$	—	28	pF

MASS (Periodically Sampled Rather Than 100% Tested)

Parameter	Max	Unit
MCM72F6	16	g
MCM72F7	20	g

6

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V ± 10%, – 5%, T_J = 20 to + 110°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1 Unless Otherwise Noted

DATA RAMs READ/WRITE CYCLE TIMING (See Notes 1, 2, 3 and 4)

Parameter	Symbol	MCM72F6 – 9 MCM72F7 – 9		MCM72F6 – 10 MCM72F7 – 10		MCM72F6 – 12 MCM72F7 – 12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	12	—	15	—	16.6	—	ns	
Clock Access Time	t_{KHQV}	—	9	—	10	—	12	ns	5
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	6	ns	5
Clock High to Output Active	t_{KHQX1}	0	—	0	—	0	—	ns	5, 7
Clock High to Output Change	t_{KHQX2}	3	—	3	—	3	—	ns	5, 7
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	5, 7
Output Disable to Q–High–Z	t_{GHQZ}	—	5	—	5	—	6	ns	6, 7
Clock High to Q–High–Z	t_{KHQZ}	3	5	3	5	3	6	ns	6, 7
Clock High Pulse Width	t_{KHKL}	4	—	5	—	6	—	ns	
Clock Low Pulse Width	t_{KLKH}	4	—	5	—	6	—	ns	
Setup Times: Address	t_{AVKH}	2.5	—	2.5	—	2.5	—	ns	
$\overline{ADSP}$	t_{ADKH}								
Data In	t_{DVKH}								
Write	t_{WVKH}								
Chip Enable	t_{EVKH}								
Hold Times: Address	t_{KHAX}	0.5	—	0.5	—	0.5	—	ns	
$\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$	t_{KHADX}								
Data In	t_{KHDX}								
Write	t_{KHWX}								
Chip Enable	t_{KHEX}								

NOTES:
1. In setup and hold times, write refers to either any $\overline{SBx}$ and $\overline{SW}$ or $\overline{SGW}$ is low.
2. Chip Enable is defined as $\overline{SE1}$ low, SE2 high, and $\overline{SE3}$ low whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted.
3. All read and write cycle timings are referenced from K or $\overline{G}$.
4. $\overline{G}$ is a don't care after write cycle begins. To prevent bus contention, $\overline{G}$ should be negated prior to start of write cycle.
5. Tested per AC Test Load (Figure 1).
6. Measured at ± 200 mV from steady state.
7. This parameter is sampled and not 100% tested.

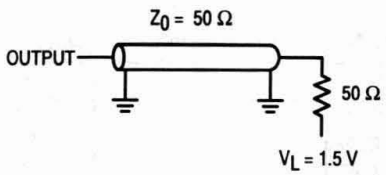
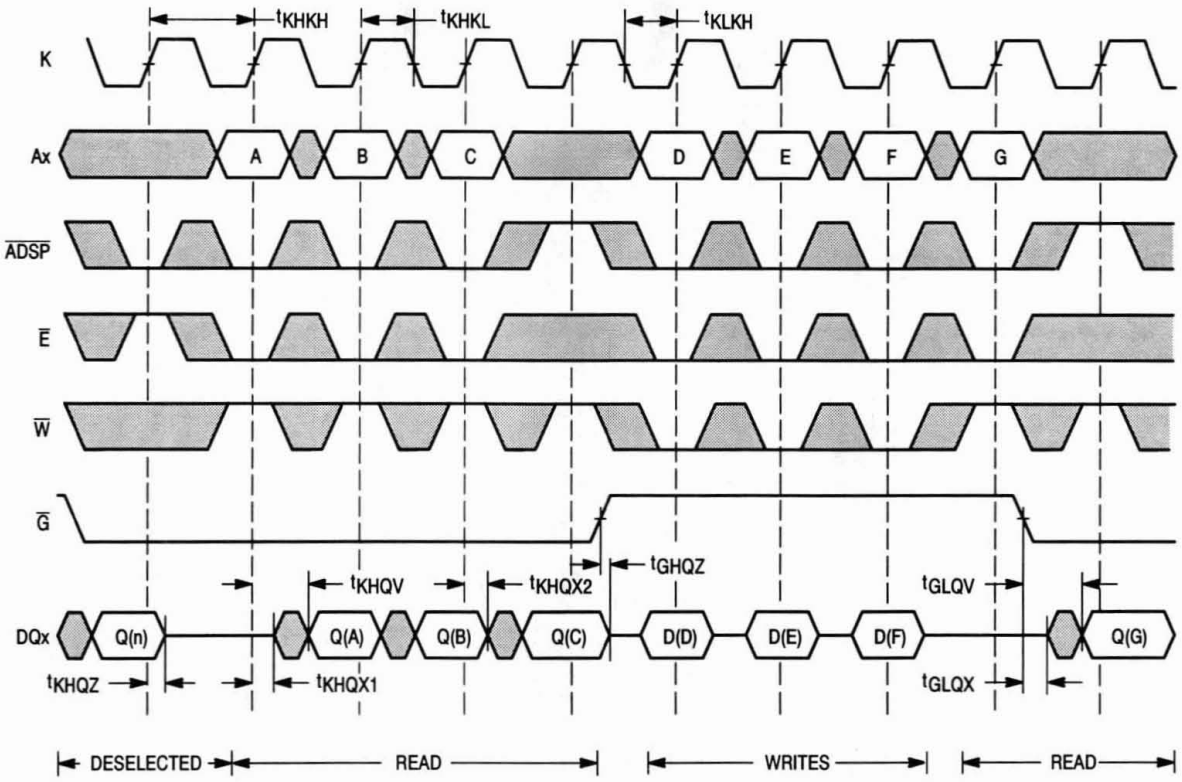


Figure 1. AC Test Load

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ/WRITE CYCLES



ORDERING INFORMATION

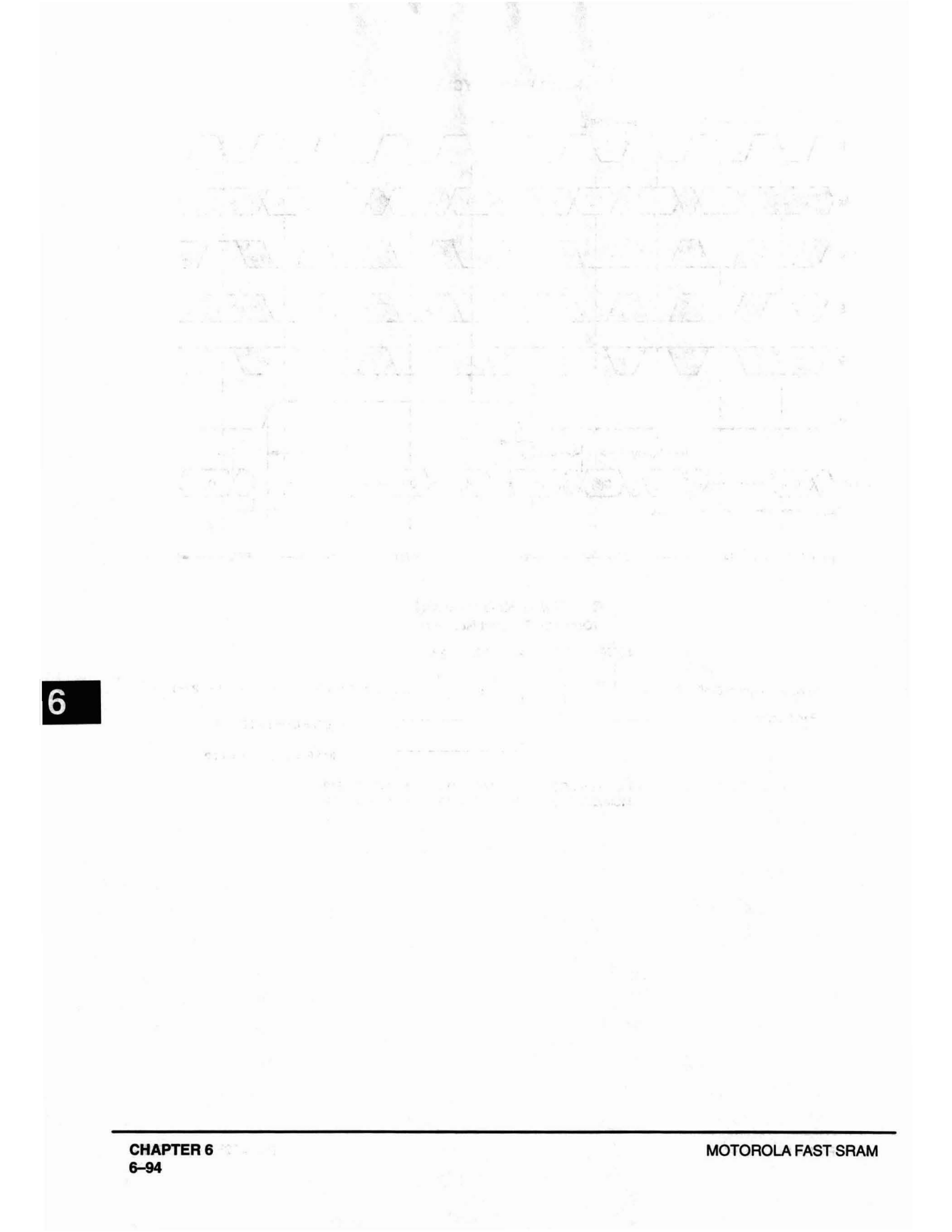
(Order by Full Part Number)

MCM	72F	X	XX	XX

- MCM — Motorola Memory Prefix
- 72F — Part Number
- XX — Speed (9 = 9 ns, 10 = 10 ns, 12 = 12 ns)
- XX — Package (DG = Gold Pad DIMM)
- X — Memory Size (6 = 512KB, 7 = 1 MB)

Full Part Numbers —			
	MCM72F6DG9	MCM72F6DG10	MCM72F6DG12
	MCM72F7DG9	MCM72F7DG10	MXM72F7DG12

6

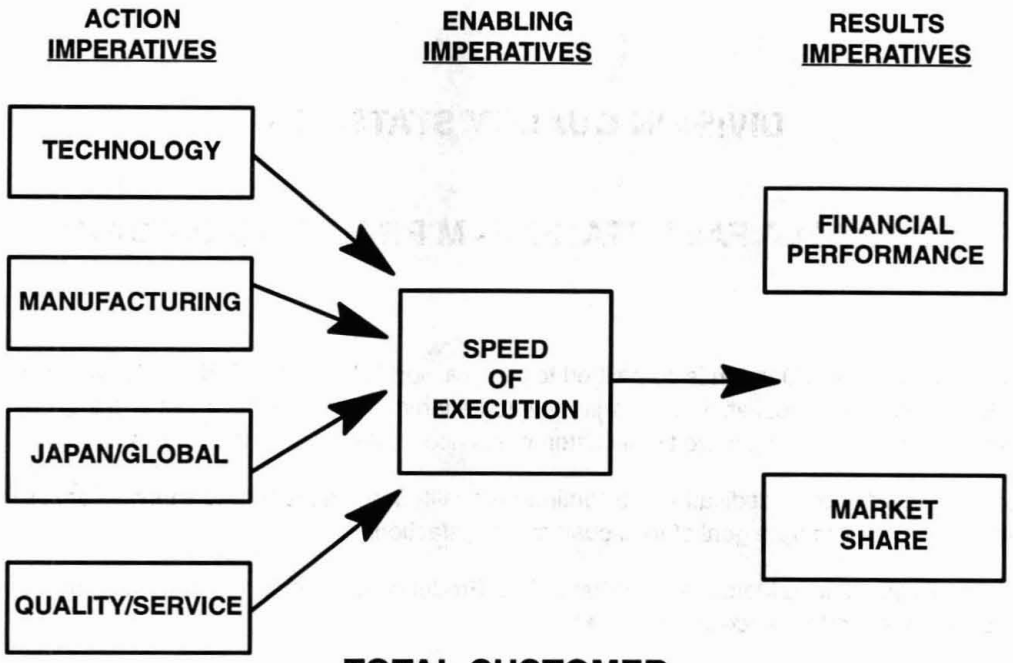


Reliability Information

7

7

MOTOROLA
SEMICONDUCTOR PRODUCTS SECTOR
IMPERATIVES



TOTAL CUSTOMER SATISFACTION

7

FASTATICS

DIVISION QUALITY STATEMENT

MOTOROLA FAST STATIC RAM PRODUCTS DIVISION

The Fast Static RAM Products Division is committed to being a world class CMOS, BiCMOS, Application Specific, and Module Fast Static RAM supplier. This means the integration of outstanding product and technology designs, linked with excellent manufacturing, cycle time, customer service, and engineering analysis.

This will be accomplished through dedication to a continuous quality improvement culture that will ensure our success in reaching the Motorola Corporate goal of total customer satisfaction.

We trust that you will experience Motorola Fast Static RAM Products Division as the best memory supplier through WORLD CLASS product performance and services.

Thomas Conn
Vice–President and General Manager
Fast Static RAM Division
Microprocessor and Memory Technologies Group

Michael Phillips
Director, Reliability and Quality Assurance
MOS Memory Products
Microprocessor and Memory Technologies Group

7

QUALITY SYSTEMS

Motorola Fast Static RAM Products Division maintains a World Wide Quality Assurance system that is second to none. Daily status reports are received from remote locations, and any problems that arise are tackled on a timely basis. The Fast Static RAM Products Division is also a leader in accurate and efficient methods of quality data collection and reporting.

Every unit that the Fast Static Ram Products Division produces is coded so that complete traceability is maintained, including visibility to the wafer and assembly lot level. The Quality System ensures that we can provide any specific processing information to our customers on request.

INTERNAL QUALIFICATION DISCIPLINE

Motorola recognizes the need to establish that all Fast Static RAM devices, both new products as well as existing ones, reach and maintain a level of quality and reliability that is unsurpassed in the electronics marketplace. To ensure this, internal qualification requirements, procedures, and methods as well as vendor qualification specifications have been developed. These activities are intended to provide a consistent, comprehensive, and methodical approach to device qualification and to improve our customer's understanding of Motorola's qualification results and their subsequent application implications.

For qualification results to be valid and acceptable, the collected data must be proven accurate to the highest possible confidence level. Therefore, a complete device history and data log is kept with any lost or missing data potentially leading to test results that are unusable for qualification purposes. Testing conditions and pass/fail criteria are established before stressing begins. Strict adherence to these criteria and the use of control devices ensure that the test results are valid and meaningful.

New Fast Static RAM devices which are under development or in the prototype stage are subject to requirements defined for the three levels of the development cycle. These levels are the alpha, beta, and introductory phases of device development. Each phase contains guidelines and controls concerning issues such as device labeling, number of customers, sample quantities, pricing and stocking levels, and open-order-entry timing. Decisions regarding these items are made jointly by marketing, design, product, and reliability personnel.

JOINT QUALIFICATION

As a result of the rigorous discipline used for internal qualification of Motorola Fast Static RAM products, our customers can benefit from joint qualification activities. Motorola's clearly defined qualification procedures improve the customer's ability to comprehend the qualification results in an effective manner which aides in their qualification decision making process. Through parallel qualification activities between Motorola and its customers, this procedure can cut qualification costs by reducing duplication of effort, improving resource utilization, and shortening introduction cycle time. This helps to ensure competitive edge advantages for our customers.

Joint Qualification activities result in a partnership type of interaction between Motorola and its customers on an engineering level. This assists our customers in two critical areas. First, it allows them to understand more clearly the strengths and weaknesses of Motorola's products. Secondly, our customers can make clear decisions concerning which stresses they need to concentrate on during their internal qualification activities.

QUALITY MONITORING

Average Outgoing Quality (AOQ) refers to the number of devices per million that are outside specification limits at the time of shipment. Motorola has continually improved its outgoing quality, and has established a goal of zero defects. This level of quality will lead to vendor certification programs with many of our customers. The program ensures a certain level of quality, thus allowing a customer to either reduce or eliminate the need for incoming inspections.

By paying strict attention to quality at an early stage, the possibility of failures occurring further down the line is greatly minimized. Motorola's electrical parametric testing eliminates devices that do not conform to electrical specification. Additional parametric testing on a sample basis provides data for continued improvement.

AVERAGE OUTGOING QUALITY CALCULATION

$$\text{AOQ in PPM} = (\text{Process Average}) \bullet (\text{Lot Acceptance Rate}) \bullet (10^6)$$

$$\text{Process Average} = \frac{\text{Total Projected Reject Devices*}}{\text{Total Number of Devices}}$$

$$\text{Projected Reject Devices} = \frac{\text{Defects in Sample}}{\text{Sample Size}} \bullet \text{Lot Size}$$

$$\text{Total Number of Devices} = \text{Sum of all the units in each submitted lot}$$

$$\text{Lot Acceptance Rate} = 1 - \frac{\text{Number of Lots Rejected}}{\text{Number of Lots Tested}}$$

*10^6 = Conversion to parts per million (PPM)

The chart in Figure 1 indicates the product Average Outgoing Quality performance as measured in parts per million.

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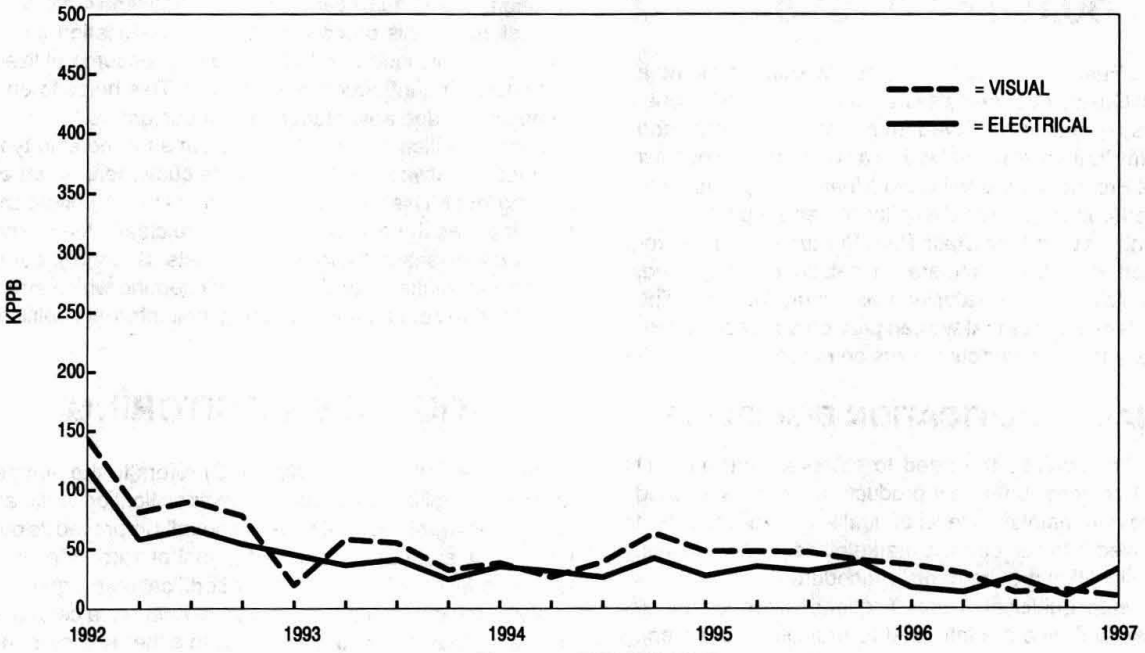

Figure 1. FSRAM AOQ

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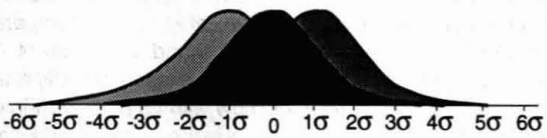
STATISTICAL PROCESS CONTROL

Motorola's Fast Static RAM Products Division is continually pursuing new ways to improve product quality. Initial design improvement is one method that can be used to produce a superior product. Equally important to outgoing product quality is the ability to produce product that consistently conforms to specification. Process variability is the basic enemy of semiconductor manufacturing since it leads to product variability. Used in all phases of Motorola's product manufacturing, STATISTICAL PROCESS CONTROL (SPC) replaces variability with predictability. The traditional philosophy in the semiconductor industry has been adherence to the data sheet specification. Using SPC methods ensures that the product will meet specific process requirements throughout the manufacturing cycle. The emphasis is on defect prevention, not detection. Predictability through SPC methods requires the manufacturing culture to focus on constant and permanent improvements. Usually, these improvements cannot be bought with state-of-the-art equipment or automated factories. With quality in design, process, and material selection, coupled with manufacturing predictability, Motorola produces world class products.

The immediate effect of SPC manufacturing is predictability through process controls. Product centered and distributed well within the product specification benefits Motorola with fewer rejects, improved yields, and lower cost. The direct benefit to Motorola's customers includes better incoming quality levels, less inspection time, and ship-to-stock capability. Circuit performance is often dependent on the cumulative effect of component variability. Tightly controlled component distributions give the customer greater circuit predictability. Many customers are also converting to just-in-time (JIT) delivery programs. These programs require improvements in cycle time and yield predictability achievable only through SPC techniques. The benefit derived from SPC helps the manufacturer meet the customer's expectations of higher quality and lower cost product.

Ultimately, Motorola will have Six Sigma capability on all products. This means parametric distributions will be centered within the specification limits, with a product distribution of plus or minus Six Sigma about mean. Six Sigma capability, shown graphically in Figure 2, details the benefit in terms of yield and outgoing quality levels. This compares a centered distribution versus a 1.5 sigma worst case distribution shift.

New product development at Motorola requires more robust design features that make them less sensitive to minor variations in processing. These features make the implementation of SPC much easier.



Standard Deviations From Mean

Distribution Centered	Distribution Shifted ± 1.5
At ± 3 σ 2700 ppm defective 99.73% yield	66810 ppm defective 93.32% yield
At ± 4 σ 63 ppm defective 99.9937% yield	6210 ppm defective 99.379% yield
At ± 5 σ 0.57 ppm defective 99.999943% yield	233 ppm defective 99.9767% yield
At ± 6 σ 0.002 ppm defective 99.9999998% yield	3.4 ppm defective 99.99966% yield

Figure 2. Percent Defective and Yield from a Normal Distribution of Product with 6σ Capability

MARKING PERMANENCY, HERMETICITY, AND SOLDERABILITY MONITORS

Marking permanency testing is performed per Motorola specification. The procedure involves soaking the device in various solvents, brushing the markings, and then inspecting the markings for legibility.

Hermeticity monitoring includes tests for both fine and gross leaks in the hermetic package seal.

Solderability testing is used to ensure that device leads can be soldered without voids, discoloration, flaking, dewetting, or bridging. Typically, the test specifies steam preconditioning followed by a 235 to 260°C solder dip and microscope inspection of the leads.

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RELIABILITY STRESS TESTS

The following summary briefly describes the various reliability tests included in the Motorola reliability monitor program.

DYNAMIC EARLY FAIL STUDY

This stress is performed to accelerate infant mortality failure mechanisms, which are defects that occur within the first year of normal device operation. Typical stress is a temperature of 125°C, nominal voltage (6.5 V), and a duration of 72 hours. All devices used in this test are sampled directly after the standard production final test flow with no prior burn-in or other prescreening, unless called out in the normal production flow.

DYNAMIC AND STATIC LONG TERM LIFETEST

Both Dynamic and Static Long Term Lifetests are performed to accelerate failure mechanisms and access parametric shifts, which are voltage and thermally activated. This is done through the application of extreme temperatures and the use of biased operating conditions. Typical stress temperature is 125°C with the bias applied being equal to or greater than the data sheet nominal value. All devices used in the long term lifetest are sampled from the Dynamic Early Fail Study. Testing is either performed with dynamic signals applied to the devices or in a static bias configuration for a test duration of 1008 hours.

TEMPERATURE CYCLE

This test accelerates the effects of thermal expansion mismatch among the different components within a specific die and packaging system. This test is typically performed to minimum and maximum temperatures of – 65 to + 150°C for a duration of 500 cycles. During temperature cycle testing, devices are inserted into a cycling system and held at cold dwell temperature for at least ten minutes. Following this cold dwell, the devices are heated to the hot dwell where they remain for another ten minutes. The system employs a circulating air environment to assure rapid stabilization at the specified temperature.

THERMAL SHOCK

The objective of this test is the same as that for Temperature Cycle testing: to emphasize differences in expansion coefficients for components of the packaging system. However, thermal shock provides additional stress because the device is exposed to a sudden change in temperature due to the transfer time of ten seconds maximum as well as the increased thermal conductivity of a liquid ambient. This test is typically performed to minimum and maximum temperatures of – 65 to + 150°C for a duration of 500 cycles. Devices are placed in a fluorocarbon bath and cooled to minimum specified temperature. After being held in the cold chamber for five minutes, the devices are transferred to an adjacent chamber filled with fluorocarbon at the maximum specified temperature for an equivalent time. Two five minute dwells plus two ten second transitions constitute one cycle.

TEMPERATURE HUMIDITY BIAS (THB)

This is an environmental test performed at a temperature of 85°C and a relative humidity of 85%. The test is designed to measure the moisture resistance of plastic encapsulated circuits. A nominal static bias is applied to the device to create the electrolytic cells necessary to accelerate corrosion of the metalization. Typical stress duration is 1008 hours.

PRESSURE TEMPERATURE HUMIDITY BIAS (PTHB)

This test is performed to accelerate the effects of moisture penetration with the dominant effect being corrosion. This test detects similar failure mechanisms as THB but at a greatly accelerated rate. Conditions employed during this test are a temperature of 148°C, humidity of 90%, 44 psig, and a nominal static bias voltage. Typical stress duration is 72 hours.

SMT PRECONDITIONING STRESS

The purpose of this test is to simulate the manufacturing steps involved in mounting and reworking a surface mount device used in customer applications. The test consists of simulating ambient moisture absorption by the device followed by exposure to temperatures typical of solder reflow. Devices are exposed to 85°C/85% relative humidity until saturated (non-moisture sensitive devices) or 30°C/60% relative humidity (moisture sensitive devices) followed by four passes of vapor phase reflow (215°C) for 120 seconds per pass. This test method meets all requirements of Jedec A113.

AUTOCLAVE

Autoclave is an environmental test that measures devices resistance to moisture penetration and the resultant effects of galvanic corrosion. Conditions employed during the test include 121°C, 100% relative humidity, and 15 psig. Corrosion of the die is the expected failure mechanism. Autoclave is a highly accelerated and destructive test. Typical test duration is 96 hours.

SYSTEM SOFT ERROR

System soft error is designed to detect errors caused by impact ionization of silicon by high energy particles. This stress is performed on a system level basis. The system is operated for millions of device hours to obtain an accurate measure of actual system soft error performance.

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THERMAL PERFORMANCE OF FAST STATIC RAM PACKAGES

Test and simulation methodologies that are used to determine thermal performance are explained. Simulations are reported for most of Motorola's Fast Static RAM packages currently in use.

JUNCTION TO AMBIENT THERMAL RESISTANCE

The thermal performance of a surface mount integrated circuit package is normally reported as a junction to ambient thermal resistance. Theta JA, θ_{JA}, and $R_{\theta JA}$ are the normal nomenclature. Theta JA is determined using the methodology of SEMI Standard G38–87. To summarize briefly, the package is built with a thermal test die which has resistors for heating the silicon die within the package and one or more diodes to measure the die temperature. A surface mount package is then soldered to a printed circuit board. Naturally, the size and amount of metallization on the board strongly influence the measured thermal performance. The test boards are designed with "minimum" metallization but with all the leads routed. The printed circuit board with the package is placed horizontally in either the wind tunnel for forced convection measurements or in a closed chamber for natural convection measurements. The test chip is used to heat the package and determine the die temperature within the package. This die temperature is the "junction" temperature. Then the junction to ambient thermal resistance is determined by:

$$\theta_{JA} = \frac{(T_J - T_A)}{P}$$

where T_J is the die temperature, T_A is the ambient temperature, and P is the power dissipated within the package. The ambient temperature is measured below the printed circuit board, one half inch away from the edge of the board and one inch below the plane of the board. This location is a local ambient while avoiding measuring the air temperature after it has been heated by the package. Typically for the SOJ packages, one watt is used for the measurement. The measured value of Theta JA is not a strong function of the measurement power, although the measured value will decrease slightly with increasing power. The slight decrease occurs because higher surface temperatures cause a more effective natural convection.

We had measurements on several packages for this report: 28 lead, 300 mil wide SOJ; 32 lead, 300 mil wide SOJ; two 32 lead, 400 mil wide SOJ; and 44 and 52 lead PLCC. This data was used to validate the thermal simulations listed in Table 1. The simulations are expected to be within 20%. The range in thermal performance between the various devices in a given package are primarily a result of the different die and die paddle sizes.

JUNCTION TO CASE THERMAL RESISTANCE

The junction to case thermal resistance, Theta JC or θ_{JC}, has been used in many different ways. The definition that is used by the JEDEC 15.1 committee is the thermal resistance from the junction to the surface of the package when that surface is heat sunk to achieve an uniform temperature. For the SOJ and PLCC package, that would be the thermal resistance from the junction to top surface of the package. Since heat sinks are rarely employed for SOJ packages, the junction to case thermal resistance is not normally used in determining the junction temperature. Table 1 provides the simulated junction to case thermal resistance. The values will have sufficient accuracy under most circumstances. For a critical application, the junction to case thermal resistance should be measured.

Frequently, however, Theta JC is used for the temperature difference (divided by total package power) between the junction and a thermocouple (or other temperature sensor) attached to top of the case. The JEDEC JC15.1 committee has established a new nomenclature of Ψ_{JT} for the Thermal Characterization Parameter defined by

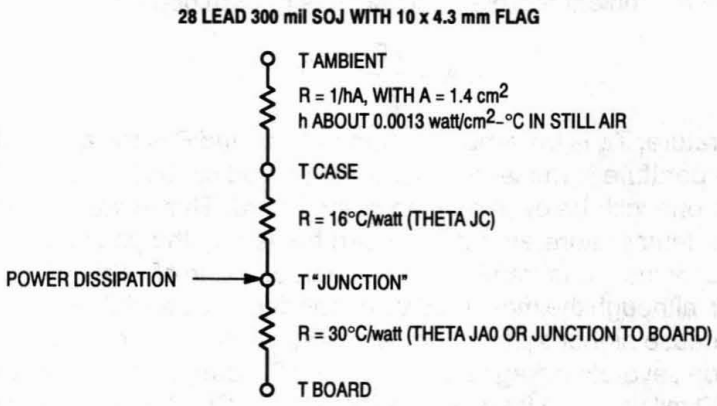
$$\Psi_{JT} = \frac{(T_J - T_T)}{P}$$

where T_J is the junction temperature and T_T is the thermocouple at the top of the package. The measurement method is described in EIA/JESD51–2. Using the temperature on the top of the package in conjunction with Ψ_{JT} is the best method to determine junction temperature in an actual use condition. In natural convection for the memory packages, we recommend using a value of 4°C/watt. In forced convection

above 400 ft/minute, the recommended value is Theta JC. These values will allow estimation of the junction temperature within 5°C for the normal range of applications, provided that the thermocouple is 40 gauge or smaller and is applied correctly.

OVERALL PACKAGE THERMAL MODEL

Theta JC has also been used for a junction to lead thermal resistance. From an experimental point of view, it makes more sense to discuss the junction to board (printed circuit board) thermal resistance. The simulation software calculates a thermal resistance that is similar to the junction to board resistance: namely, θ_{JA0} that is defined to be the thermal resistance with the printed circuit board held at ambient temperature. This is a close approximation to the junction to board thermal resistance since approximately 80% of the heat flows to the board in natural convection. These values can be used to construct a 1–D model of the thermal paths of the package as shown in Figure 1. This model can be used in the 2.5–D thermal model of the printed circuit application, if the spreading resistance of the board is treated correctly. Because the junction temperature is so closely coupled to the board temperature, determining the board temperature in the actual application is extremely important if the junction temperature is to be estimated.


28 LEAD 300 mil SOJ WITH 10 x 4.3 mm FLAG
T AMBIENT
R = 1/hA, WITH A = 1.4 cm2
h ABOUT 0.0013 watt/cm2–°C IN STILL AIR
T CASE
R = 16°C/watt (THETA JC)
POWER DISSIPATION
T "JUNCTION"
R = 30°C/watt (THETA JA0 OR JUNCTION TO BOARD)
T BOARD

NOTE: Theta JA simulated in Natural Convection 67°C/watt.

Figure 1. One Dimensional Thermal Model

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Part No.	Lead Count	Package	Package Width (mils)	Theta JA Simulated	Theta JA 200ft/min Simulated	Theta JC Simulated	Theta JAO, Natural Conv. Simulated
MCM56824A	52	PLCC		43	35	15	17
MCM6206BA	28	SOJ	300	94	82	40	59
MCM6226B	32	SOJ	300	60	51	12	25
MCM6226BB	32	SOJ	300	65	55	16	30
MCM6227B	28	SOJ	400	65	54	14	28
MCM6229B	28	SOJ	300	62	52	11	25
MCM6246	36	SOJ	400	54	40	5	16
MCM6249	32	SOJ	400	56	40	4	14
MCM6249A	32	SOJ	400	56	40	4	14
MCM62990A	52	PLCC		43	35	16	17
MCM62995A	52	PLCC		43	35	16	17
MCM62X308	28	S0J	300	81	69	27	46
MCM6706B	28	SOJ	300	72	61	19	37
MCM6706BR	32	SOJ	300	73	63	23	40
MCM6706CR	32	SOJ	300	73	63	23	40
MCM6709B	28	SOJ	300	72	61	19	37
MCM6709BR	28	SOJ	300	72	61	19	37
MCM6726B	32	SOJ	400	51	41	8	21
MCM6726C	32	SOJ	400	55	44	11	25
MCM6729B	32	SOJ	400	56	45	11	26
MCM6729C	32	SOJ	400	56	45	11	26
MCM67A618A	52	PLCC		39	31	11	13
MCM67B618A	52	PLCC		39	31	11	13
MCM67C618A	52	PLCC		39	31	11	13
MCM67D709A	52	PLCC		39	31	11	13
MCM67Q804	36	SOJ	400	50	40	8	21
MCM6926	32	SOJ	400	56	45	11	26
MCM6929	32	SOJ	400	56	45	11	26

AN971
REV1

Avoiding Bus Contention in Fast Access RAM Designs

INTRODUCTION

When designing a bus oriented system, the possibility of bus contention must be taken into consideration. Bus contention occurs when two or more devices try to output opposite logic levels on the same common bus line.

This application note points out common causes of bus contention when designing with fast static random access memories and describes ways to eliminate or reduce contention.

WHAT CAUSES BUS CONTENTION?

The most common form of bus contention occurs when one device has not completely turned off (output in a high-impedance state) before another device is turned on (output active). Basically, contention is a timing overlap problem that results in large, transient current spikes. These large current spikes not only generate system noise, but can also affect the long term reliability of the devices on the bus (see Figure 1).

BUS CONTENTION AND FAST STATIC RAMs

Since memory devices are primarily used in bus oriented systems, care must be taken to avoid bus contention in memory designs. Fast static RAMs with common I/O data lines (or any high frequency device with common I/O pins) are the most likely candidates to encounter bus contention. This is due to the tight timing requirements that are needed to achieve high-speed operation. If timing control is not well maintained, bus contention will occur. The most common form of bus contention for memories occurs when switching from a read mode to a write mode or vice versa.

SWITCHING FROM A READ TO WRITE MODE

With $\overline{E}$ low (device selected), on the falling edge of $\overline{W}$ (write asserted) the RAM output driver begins to turn off (high-impedance state). Depending on the input and output logic levels, if sufficient time is not allowed for the output to fully turn off before an input driver turns on, bus contention will occur (see Figure 2a).

Figure 2a shows an example of a RAM trying to drive a bus line low while an input driver is trying to drive the line high. If the situation were reversed (RAM output high and the input driver low), bus contention would still exist.

Of course the obvious way to avoid this type of bus contention is to make sure that the input buffer is not enabled until the write low to output high-impedance (t_{WLQZ}) time is satisfied (see Figure 2b). This specification is usually given on most manufacturers' data sheets.

Another method to eliminate bus contention would be to use $\overline{E}$ to deselect the RAM before asserting $\overline{W}$ (low). This allows the RAM output extra time to go into high-impedance state before the input driver is enabled. $\overline{E}$ and $\overline{W}$ are later asserted low to begin a write cycle (see Figure 2c).

SWITCHING FROM A WRITE TO A READ MODE

With $\overline{E}$ set low (device selected), on the rising edge of $\overline{W}$ (write terminated) the address or data-in changes before the device has had a chance to terminate the write mode. If this should occur, and depending on the input and output logic levels, a bus contention situation could exist (see Figure 3). To avoid address changing type bus contention requires that the address not change till the write recovery specification (t_{WHAX}) is satisfied. To avoid bus contention caused by data changing requires that the data-in remains stable for the duration of the data hold specification (t_{WHDX}). Most of

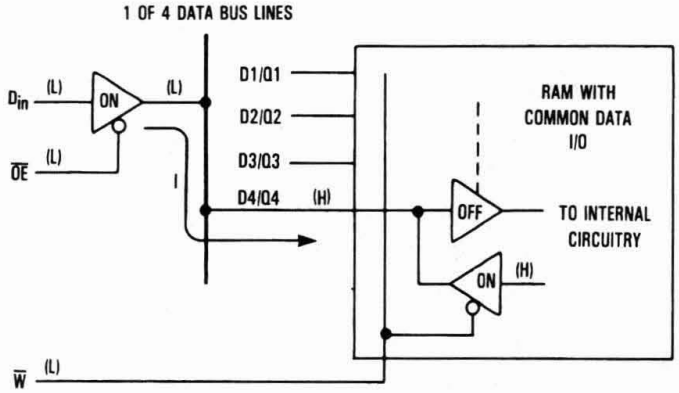

Figure 1. Common I/O Bus Contention

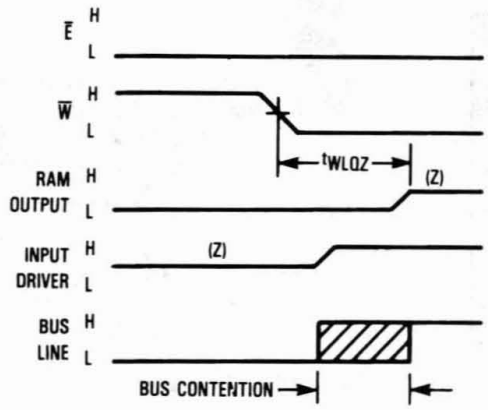

Figure 2a. Input Driver Enabled Prior to Disabling RAM Output

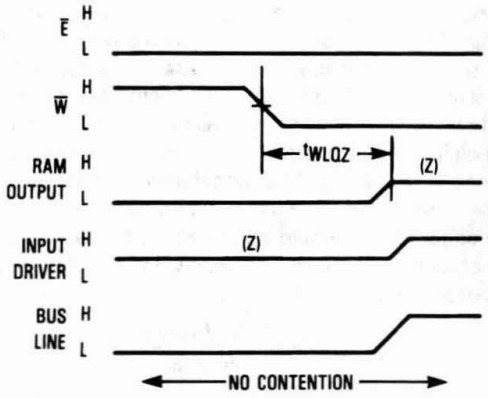

Figure 2b. Input Driver Disabled Prior to Enabling RAM Output

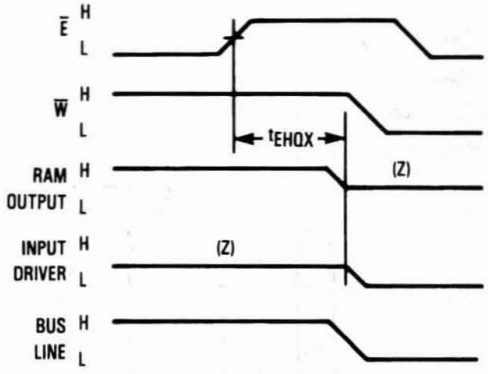

Figure 2c. Using $\overline{E}$ to Avoid Bus Contention

Motorola's fast static RAMs specify write recovery and data hold times of 0 ns. However, it is always a good practice to allow some margin to take care of possible race conditions.

Both of these types of contention could also be avoided by taking $\overline{E}$ high prior to taking $\overline{W}$ high. This will give the RAM output driver time to go to a high-impedance state before $\overline{W}$ goes high. In this case $\overline{E}$ is used to terminate the write cycle instead of $\overline{W}$ (see Figure 3c).

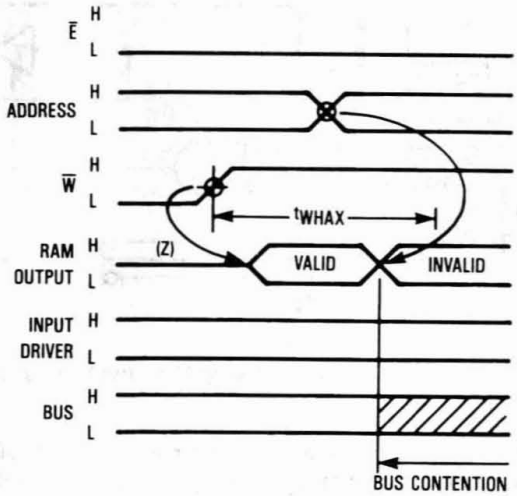

Figure 3a. Data Setup Time Violation

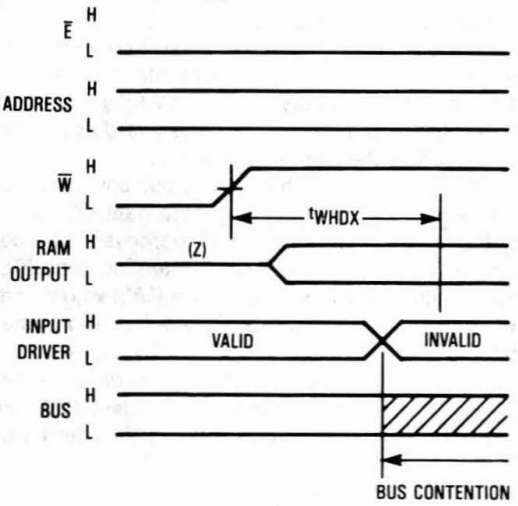

Figure 3b. Data Hold Time Violation

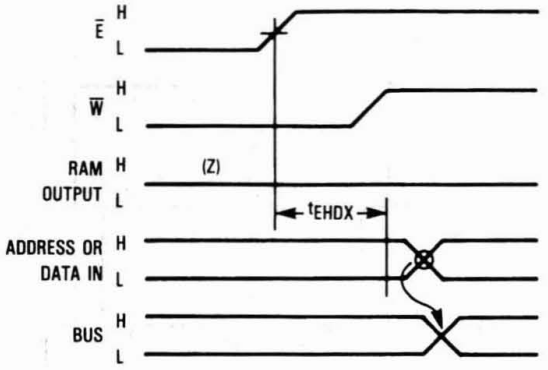

Figure 3c. Using $\overline{E}$ to Avoid Bus Contention

OTHER WAYS TO ELIMINATE BUS CONTENTION

If the RAM has an output enable pin ($\overline{G}$), synchronizing schemes can be incorporated to help eliminate bus contention. Taking $\overline{G}$ high will ensure that even when the RAM is in a read mode the output will be in a high-impedance state. This will allow the input driver to be enabled longer.

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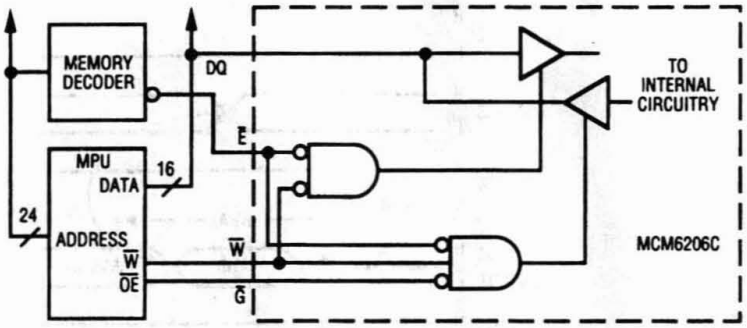

Figure 4a. Using $\overline{G}$ to Avoid Bus Contention

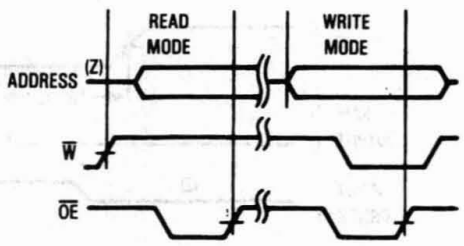

Figure 4b. Timing Diagram of MPU

Most advanced microprocessors have asynchronous bus-control signals that take advantage of fast memory devices with output enable pins. Figure 4 shows one way to avoid bus contention using a microprocessor interfaced to a Motorola 15-ns MCM6206C.

A more obvious way to eliminate bus contention is to use slow memory devices. Slow memories have loose timing requirements that allow devices to fully turn off before another device turns on. Of course this defeats the whole purpose of fast static memory devices.

Another obvious way to eliminate bus contention is to use memory devices that have separate data I/O pins. In this way the $\overline{W}$ signal from the microporcessor can control a buffer device to eliminate bus contention (see Figure 5). However, the industry is demanding RAM with common I/O because these devices cost less and save system real estate.

Common I/O devices reduce package size since fewer pins are needed. Smaller packages result in less PCB space requirement. Common I/O devices also eliminate the need for an extra buffer with its associated expense and space requirement. In general fast static RAMs configured greater than a X1 will have common data I/O pins.

Another popular way to reduce bus contention is to put a current limiting series resistor on each bus line (see Figure 6). The series resistor does not eliminate bus contention, but it helps reduce the large transient currents associated with bus contention. However, series resistors increase access time as well as increasing component count. The added access time depends on the total bus capacitance (including the capacitance of the devices on the bus) and the total bus resistance. The added delay should be added on to the point at which bus contention ceases. The following formulas can be used to determine the added access delay.

$$t_{HL} = R_L \cdot C_L \cdot \ln \frac{V_{in}(\text{initial}) - V_{in}(\text{final})}{V_{IL}(\text{max}) - V_{in}(\text{final})}$$

$$t_{LH} = R_L \cdot C_L \cdot \ln \frac{V_{in}(\text{final}) - V_{in}(\text{initial})}{V_{in}(\text{final}) - V_{IH}(\text{min})}$$

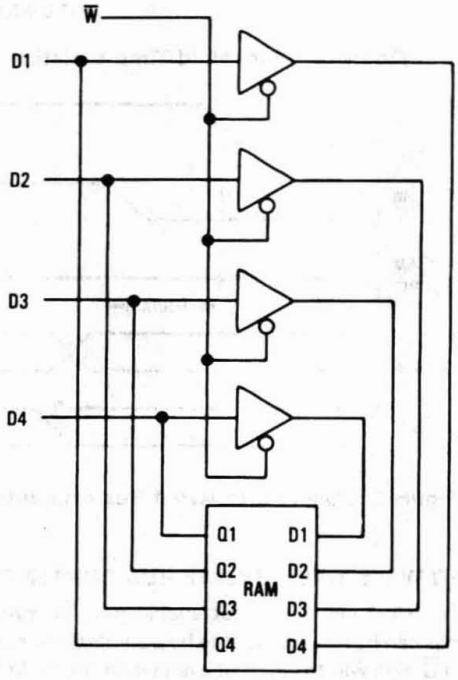

Figure 5. Separate I/O Buffer

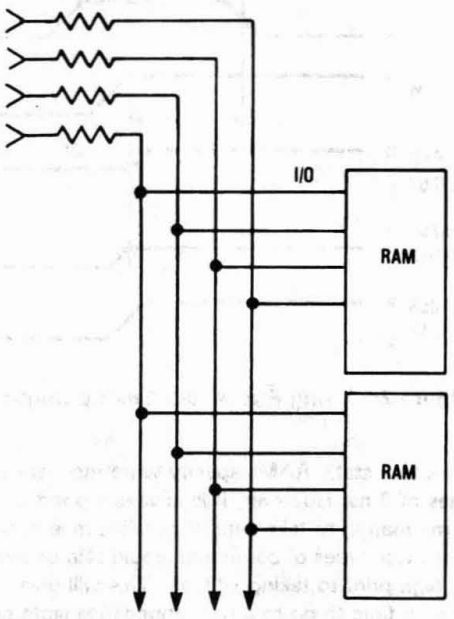

Figure 6. Using Series Terminating Resistors

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Generally the value of the resistor should be around 50 ohms. The larger the resistor the less the transient current generated, but the greater the delay. Using a 150-ohm resistor will limit the current flow to less than 20 milliamperes while adding approximately 3 nanoseconds extra access time. However, note that even the series resistors bus contention duty cycle must be minimized to reduce EMI and bus ringing.

Although it is very important to reduce bus contention, CMOS memories can tolerate more bus noise generated by bus contention than can bipolar memories, due to the excellent noise immunity advantage of CMOS over bipolar technology. However, even when using CMOS memories, large destructive transient currents generated by bus contention can still occur.

CONCLUSION

Bus contention must be taken into consideration in most bus-oriented system design. The occurrence of bus contention generates large transient currents that produce system noise and could also affect the system's long term reliability.

Fast random access memories with common data I/O pins are very susceptible to bus contention due to tight timing requirements. Although it is almost impossible to totally eliminate bus contention, it must be the goal of the system designer to minimize bus contention.

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AN1209

The Motorola BurstRAM™

Prepared by: James Garris

This note introduces the MCM62486 32K x 9 Synchronous BurstRAM. The device was designed to provide a high-performance, secondary cache for the Intel i486™ microprocessor and future microprocessors with burst protocol. Four of these devices can supply a 128K byte direct-mapped bursting cache with parity support.

THE MCM62486

The 62486 is a synchronous device with input registers and address counters surrounding a standard 32K x 9 FSRAM core. The additional circuitry in the periphery enables the memory to uniquely interface with the i486. Like the i486, the timings are referenced to the rising edge of the clock (K). Signals generated by the processor and control logic must be stable during all transitions of clock from low to high. Output enable ($\overline{G}$) on the 62486 is the only asynchronous input.

The 62486 contains three burst-control inputs. They are $\overline{ADV}$, $\overline{ADSC}$, and $\overline{ADSP}$. These inputs are used by the cache controller to control the burst capabilities of the 62486 and to maintain synchronization with the i486 or other logic driving the cache.

USE WITH THE i486 PROCESSOR

The 62486 requires an ASIC or discrete PAL type of cache controller to work with the i486. This cache control logic must also include 8K x 16 of cache-tag comparator RAM and any other buffers needed for system operation.

Control signals are sourced as follows: K is driven by the system clock (CLK); $\overline{ADSP}$ is an output from the microprocessor; and $\overline{ADV}$, $\overline{ADSC}$ are generated from the cache control logic. The data bus and lower address bus may interface directly with the 62486 or the address bus may be buffered to improve its drive to the rest of the system. A simple block diagram of this setup is shown in Figure 2.

INPUT PINS OF THE MCM62486

K is the clock input of the 62486. This should be tied to the system clock.

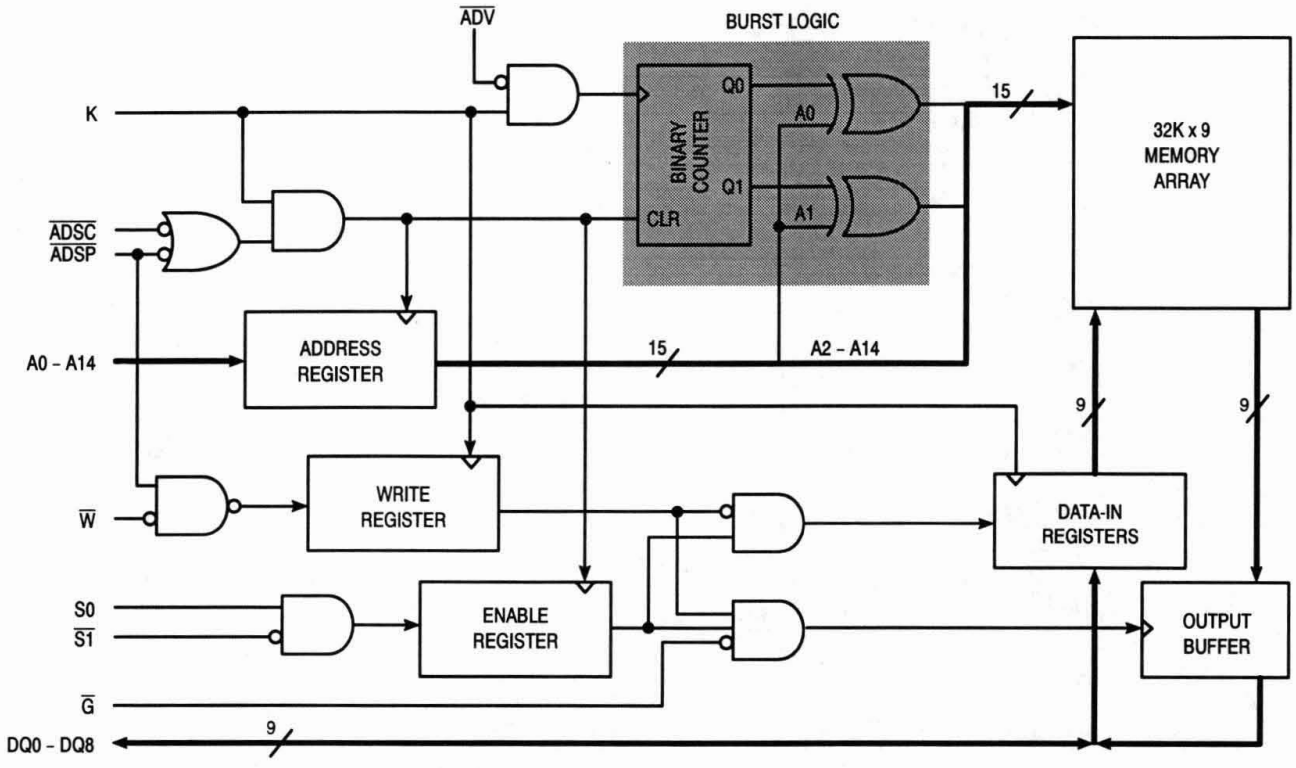

Figure 1. MCM62486 Block Diagram

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i486 is a trademark of Intel Corp.

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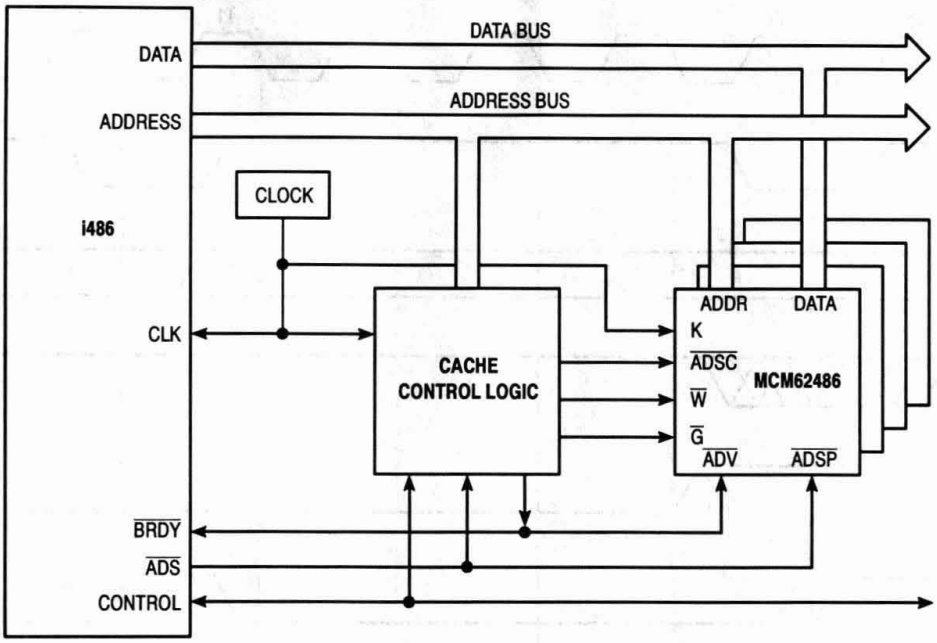

Figure 2. Typical System Block Diagram

ADSP is one of two address status input pins that are supplied on the 62486. This input allows the microprocessor to initiate a cache bus cycle. For every processor access, to or from memory, the i486 will assert ADS for one transition of K from low to high. If ADS from the i486 is tied to ADSP on the 62486, the 62486 will register the correct address from the processor. During all "T2" cycles on the i486, ADS and ADSP should not be asserted as described in the i486 processor user manual.

ADSC is the second of two address status input pins supplied on the 62486. This input allows external logic to initiate or continue cache bus cycles. The purpose of this input is to give the cache controller its own input to regulate cache accesses. This gives the 62486 a good deal of system design flexibility. One use of ADSC is for burst extension. After four burst accesses have been generated by the 62486, the cache controller may supply an additional base address to continue the burst. This method works well with 72 bit data buses. This pin can also be used in a similar manner to facilitate a cache fill from other sources.

ADV is the burst advance input pin supplied on the 62486. The purpose of this pin is to acknowledge a successful read-from or write-to memory as determined by the cache control logic. The 62486 may then proceed to the next address. This input is a function of T2 (T2 cycle as defined by the i486 processor manual), KEN (from the processor), MATCH (from the cache tags), READ (from the processor) and MISS (a cacheable read miss from the control logic).

W is the synchronous write input pin supplied on the 62486. This signal must be valid for every clock cycle ADSP is not asserted.

A0 – A14 are the synchronous address pins supplied on the 62486. These must be valid for the transitions of K from low to high. If neither ADSC or ADSP is negated, or if the chip is deselected, the address inputs do not need to meet the required setup/hold times. For all other read/write operations, the setup/hold times **MUST** be met.

S0 and S1 are the synchronous chip selects supplied on the 62486. These must be valid whenever the addresses are required valid. These inputs can be used for address depth expansion without any external logic.

G is the asynchronous output enable supplied on the 62486. This pin changes the outputs from high impedance to active at any time that the SRAM is selected.

CACHE OPERATION

READ CYCLES

Cache operations of the 62486 are initiated with one of the two Address Status Pins mentioned. Figure 3 shows the read cycle timings when ADSP is tied to ADS. During the first cycle (T1) the i486 supplies an address and asserts ADS low. The 62486 responds to ADSP being asserted by registering the lower 15 addresses. The 62486 begins to perform a read access regardless of the state of its W input.3

During the next cycle (T2), the cache controller determines if the read access was a cache hit. If so, the controller should assert G and ADV on the 62486 as well as BRDY on the i486. The assertion of G will allow the 62486 to drive the data onto the data bus while BRDY will inform the processor that the data is correct. The assertion of ADV will cause the 62486 to begin on the next burst access. Subsequent burst access will be available without wait states in a similar fashion.

Single, non-burst reads behave in a similar manner as the first access of a read burst.

Note for timing diagrams: Q1, Q2, Q3, Q4 represent the data output from the first address (base address), second, third and fourth address. For example, if A in Figure 3 was #000C, Q1 would be the data from #000C, Q2 from #0008, Q3 from #0004 and Q4 from #0000. (This is the same burst sequence as in **Table 7.7. Burst Order** in the *i486 Microprocessor Data Book*).

WRITE CYCLES

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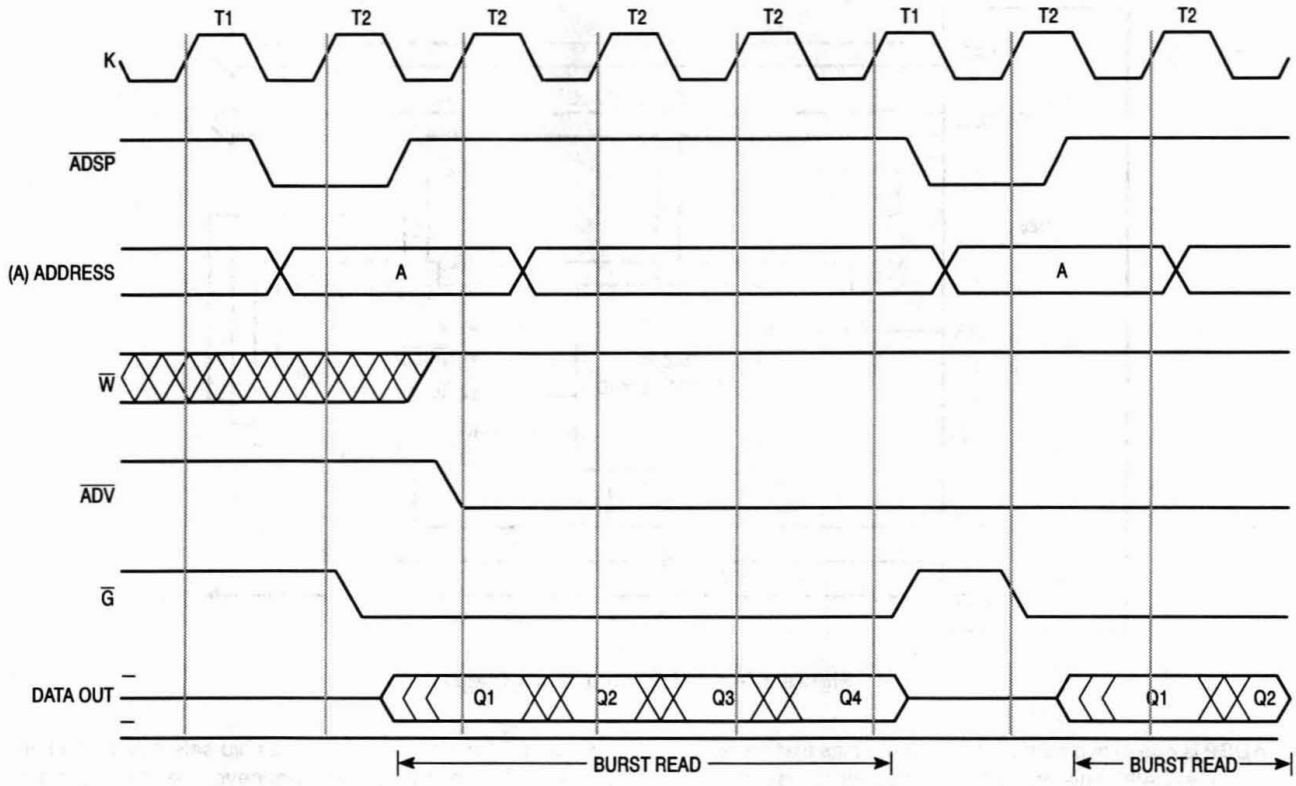


Figure 3. Cache Read Cycles

For a write to cache access, the initial T1 cycle will be the same as above. During the T2 cycle, the cache controller should assert $\overline{W}$ instead of $\overline{G}$. This will allow the 62486 to receive the data from the i486 and write it to memory. The i486 can burst write for 8 and 16 bit operations. The 62486 can support this action as described in the 62486 data sheet and Figure 4.

ADDRESS BUS LOADING

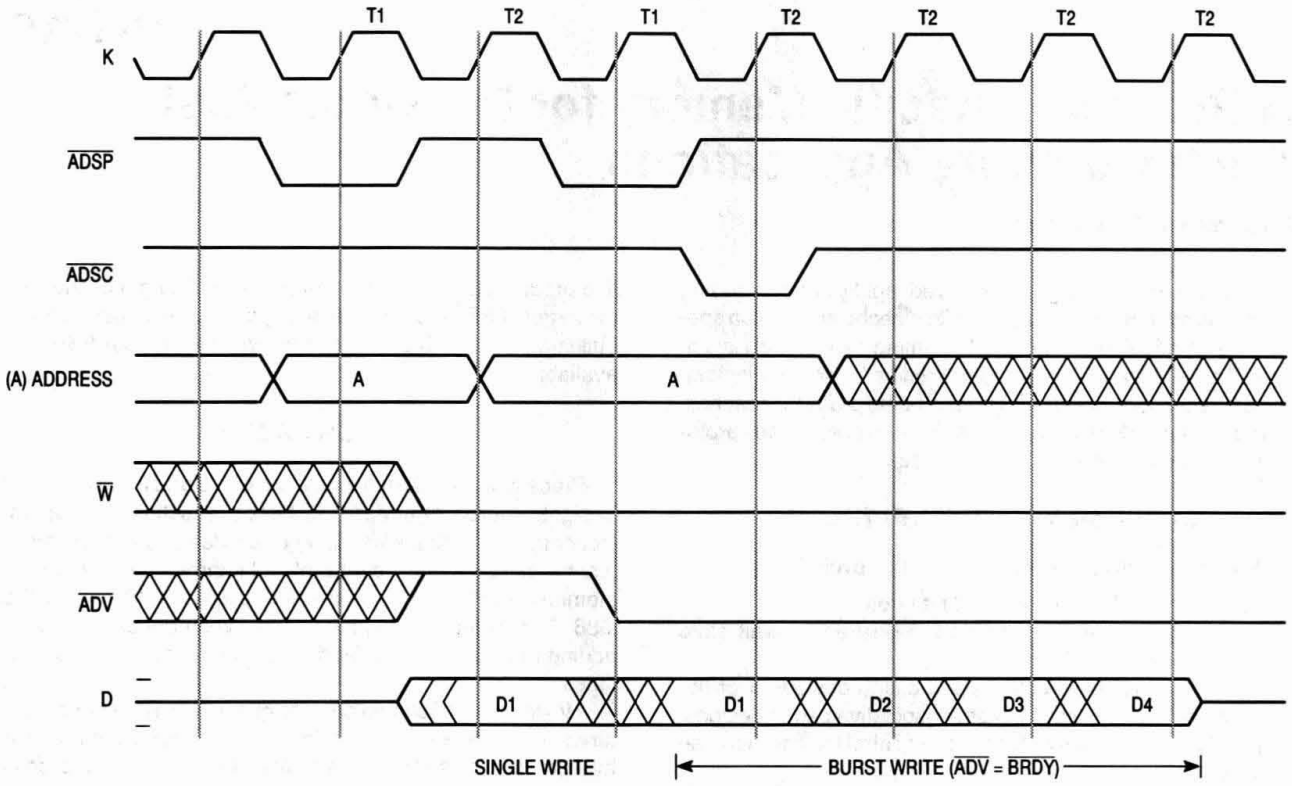
The 62486 has setup and hold timing that allow address buffers to be placed between the SRAM and the processor. The i486 is specified with 50 pF loads. Since the 62486 has a typical input capacitance of 2 pF, the i486 can be run without the buffer assuming the cache tags and other circuitry do not overload the bus.

ADVANTAGES OF THE 62486 OVER OTHER FSRAM SOLUTIONS

The 62486 is meant to replace a standard 32K x 9 FSRAM as well as some external logic. By incorporating this logic and RAM onto one chip, the system designer is given more board space, less power consumption, and most of all, easier design timing requirements. At 33 MHz, a discrete logic/SRAM solution would require a 7 ns PAL (for the burst counter) and an 18 ns SRAM [30 ns (period) – 5 ns (i486 setup) – 7 ns (PAL) = 18 ns].

This timing is even more difficult in write cycles. Closer examination of writes shows that the write signal and data from the processor do not correspond with the requirements of a standard 32K x 9 SRAM. A self-timed write SRAM is essential for high performance systems.

The 62486 represents the JEDEC standard for a 32K x 9 Synchronous SRAM for the i486. This pin-out provides enough power and ground pins to allow these devices to support systems running 50 MHz and faster. Also the 62486 represents the standard functionality descriptions for $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$. These same pins are used in the JEDEC standard 64K x 18 SRAM to be used with the i486 and the "P5".



NOTE: The first T1/T2 cycle is a single write operation. This works the same as the first two cycles of a burst write. In this single write operation, $\overline{ADV}$ goes high for the T2 cycle, while the $\overline{RDY}$ signals on the processor must be asserted low. In this operation, the $\overline{ADV}$ and $\overline{RDY}$ signals behave differently. To match their behavior, examine the second T1/T2 cycles. This second write operation (the burst write) shows how the $\overline{ADV}$ signal may behave like the $\overline{RDY}$ signals. Note that the $\overline{ADSC}$ is asserted for the first T2 cycle, thereby reloading the base address. Had the $\overline{ADSC}$ remained high for this cycle, the data (D1) would have been incorrectly written to the second burst address. This second write operation shows both single and burst write operations with $\overline{ADV}$ and $\overline{RDY}$ both asserted low for all T2 cycles.

Figure 4. Cache Write Cycles

AN1210

A Protocol Specific Memory for Burstable Fast Cache Memory Applications

Prepared by: Ron Hanson

Cache memory design has evolved rapidly in recent years, taking full advantage of the specialized cache application specific fast static RAMs that are becoming increasingly available. These advanced designs are driven by several factors: faster processor clock rates, larger on-chip processor caches, larger and faster FSRAMs, more efficient processor bus protocols, and more efficient DRAM interfaces.

CACHE MEMORY DESIGN TRENDS

Six key trends can be observed in this evolution:

1. Larger caches to improved hit rates.
2. Faster caches to maintain the desired no-wait state response.
3. Dominance of direct-mapped cache designs over the number of multiple-way set associative cache designs.
4. Minimization of external cache control logic to increase speed.
5. Users are developing their own cache solutions, even though vendors are offering more and more integrated solutions.
6. An increasing use of Application Specific Memories (ASMs).

LARGER CACHES

The latest CISC and RISC processors all have ample amounts of no-wait state cache on-chip or included in the processor chip set. Frequently this cache responds a full clock cycle or more faster than an external memory cache could because it is connected to the processor's highly efficient internal bus. In the case of the MC68040, this is a full Harvard Bus architecture that is at least twice as efficient as the fastest external memory system.

The hit rates of these internal caches are very impressive too. The i486™ provides 8K bytes of on-chip four-way set associative cache as does the '040. Though a small amount of cache, these caches have read hit rates greater than 80%. In short, it takes a comparatively large external cache to improve on the performance of the processor alone and this trend will continue. However, FSRAMS are also getting larger. 256K bit FSRAMs are now in abundance and 1 Megabit FSRAMs are in production. As has always been the case with memories, these new larger FSRAMs will replace the older smaller ones at about the same price relative to their respective product life cycles. In other words, building a cache with the largest FSRAMs available today is no more expensive that building a cache three years ago with the largest FSRAMs available then.

FASTER CACHES

Processor speeds continue to increase and there is no end in sight. There are already 50 MHz production processors. Recently the processors have been designed to be more "cache friendly." Significant protocol improvements were implemented on the '040 versus the '030 and the i486 versus the i386. These include implementing synchronous protocols, adding burst addressing, and reducing the data input set-up times.

However, it still comes down to question of raw speed. Fortunately, the increase in density has also been accompanied by increases in FSRAM speed. Now RAMs with 12 ns access times are available to support the 50 MHz processors. It is increasingly apparent that greater integration will be needed to continue to support the fastest processors. The elimination of logic circuits from the critical cache speed path is being vigorously pursued today.

THE DOMINANCE OF DIRECT-MAPPED CACHE DESIGNS

It has been shown that for any given system, as the size of the external cache increases, the performance advantage of a multiple way set associative cache over a direct mapped cache quickly fades to insignificance.[1] Furthermore, a multiple way set associative cache is always more complex to implement.[2] In a discrete design, this translates to either more cost or a loss in response time, which erodes any performance advantage that might be gained. For an integrated solution, it means relying on a vendor for a purchased proprietary solution. Often, if more performance is sought, it is far simpler and less expensive to just enlarge the cache rather than build in multiple way set associativity.

[1] Jeff Leonard, "Clever Cache Designs Required to Pace High-Speed RISCs," *EE Times*, March 19, 1990, pp. 56, 68 – 69.

[2] Mark D. Hill, "A Case for Direct-Mapped Caches," *IEEE*, December 1988, pp. 25 – 40.

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SPARC is a registered trademark of SPARC International, Inc.
i486 is a trademark of Intel Corp.

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MINIMIZATION OF EXTERNAL LOGIC

This point differs from the comment made on the elimination of logic circuits though integration. The Cache Tag RAM is a good example of integration that eliminated the need for a discrete comparator logic device. This did not minimize the logic required. Synchronous or self timed RAMs accomplish this by greatly reducing the complex logic required during write cycles. This is only the beginning; new protocol-specific memories are on the way that will take their cues from the processor itself and perform the needed RAM functions.

USERS ARE DEVELOPING THEIR OWN SOLUTIONS

There are many reasons why computer companies from the lowest performance to the highest are developing their own circuits rather than purchasing the ready-made solutions. One is competitive pressures. PC manufacturers using the same processor, coprocessor, mass storage devices, etc., must find a way to differentiate their products. They can do this by designing their own circuits. Another reason is value added. Many of these companies desire to develop their own chip technology to increase their own share of the revenue received for each computer.

Nevertheless, there is still a high demand for standardized memories. The sheer volume a memory can generate if it is adopted as a standard will drive its cost down far below what an individual custom memory could accomplish. Thus, though cache designs are using more specialty ICs, they still rely on multi-sourced high volume memories for cache data storage.

USE OF APPLICATION SPECIFIC MEMORIES

Referring back to the problem of supporting the very fastest processors, it is clear that the cache designer must attack this problem on all fronts. What is needed is a smart flexible, integrated, high density, very fast SRAM. Such products do exist, and the following is a description of one of the latest under development by several vendors that combines all of these features.

THE SYNCHRONOUS BURST PROTOCOL

In an effort to overcome the limitations of memory bus bandwidth, many of the high performance microprocessors have implemented burst memory protocols. Rather than transferring a single memory word per bus cycle, the microprocessor will transfer (burst) several consecutive memory words in quick succession. The number of words transferred corresponds to the length of a line in the microprocessor's internal cache. Burst transfers have been shown to greatly improve bus utilization. The MC68030, MC68040, PowerPC™, i486, Pentium™, MC88200, and AM29000 all employ burst memory transfers of one type or another.

Though the on-chip cache(s) can be very effective, system performance frequently can be improved by the addition of a secondary cache memory external to the microprocessor. There are three good possible reasons to add a secondary cache: 1) in multiprocessing systems, the time spent arbitrating for control of a global bus can severely degrade performance; 2) the system bus may run at a significantly slower rate than the microprocessor bus; and 3) the nature of the code itself may be better suited for larger caches than are available on-chip.

Burst protocols provide a new challenge for system designers. To achieve no wait state performance, it is necessary for the cache to count through the burst sequence. This in turn creates a problem during cache update cycles when wait states must be added to account for slower DRAM access times. Clearly, the designer would benefit from the integration of as much of this logic as possible onto the FSRAM. This reduces chip count and eliminates the propagation delay from discrete devices. Furthermore, by using inputs directly from the processor, it is possible to actually minimize the amount of logic required to manage the burst cycle. The inclusion of this logic creates an FSRAM that is not only processor specific, but protocol specific as well.

THE 32K x 9 SYNCHRONOUS BURST FSRAM

Not surprisingly, the original specification proposal for this burst FSRAM came from a user, Compaq Computer (Houston, Texas). It is a Synchronous FSRAM with an on-chip burst counter (see Figure 1) and special logic that enables the RAM to interface directly to the i486 processor as well as a cache controller. This device is being developed by several vendors for the i486 market.

The device is similar to existing synchronous FSRAMs in the market today. All of the address and control signal inputs to the RAM are held in registers on the chip, which are triggered by the rising edge the clock input (K) or the clock input gated by another input signal. These other signals include the $\overline{\text{ADSP}}$ and $\overline{\text{ADSC}}$ signals that qualify the address input.

The burst counter on chip is designed to count in the sequence used by the i486; however, the on chip count avoids the wait state inserted by the i486 at the beginning of a burst read cycle, thus improving cache performance. The $\overline{\text{ADV}}$ signal advances the counter of the rising edge of the clock, prior to the next memory access. The device uses a data input register to clock in the data on write cycles. Writes to the RAM are self-timed, requiring the minimal amount of control logic.

This FSRAM has a special built in wait state on write cycles (see Figure 2). This conforms with the i486 write timing. Furthermore, the RAM only advances its internal counter when told to by the controller, which is simultaneously acknowledging the previous transfer to the processor. The RAM can insert wait states whenever needed and, more importantly, it can hold address and count and switch from read to write mode in the event that a cache read miss occurs.

The real value of the BurstRAM™ is its simple processor interface (see Figures 3 and 4). The on-chip Address Register is controlled by the clock input and the processor's valid address signal. Thus, the RAM only registers the address when told to by the processor.

Using inputs from users on Motorola's MC68040 microprocessor, a similar device for '040 has been developed. This version, the MCM62940A, can also interface with the MPC601 (PowerPC), MC88200 and AM29000 RISC processors.

This version of the BurstRAM naturally has a modulo four burst counter to stay in step with the '040 and MPC601. No-wait state Write Burst Cycles at very high clock rates are attainable on both '040 and PowerPC platforms.

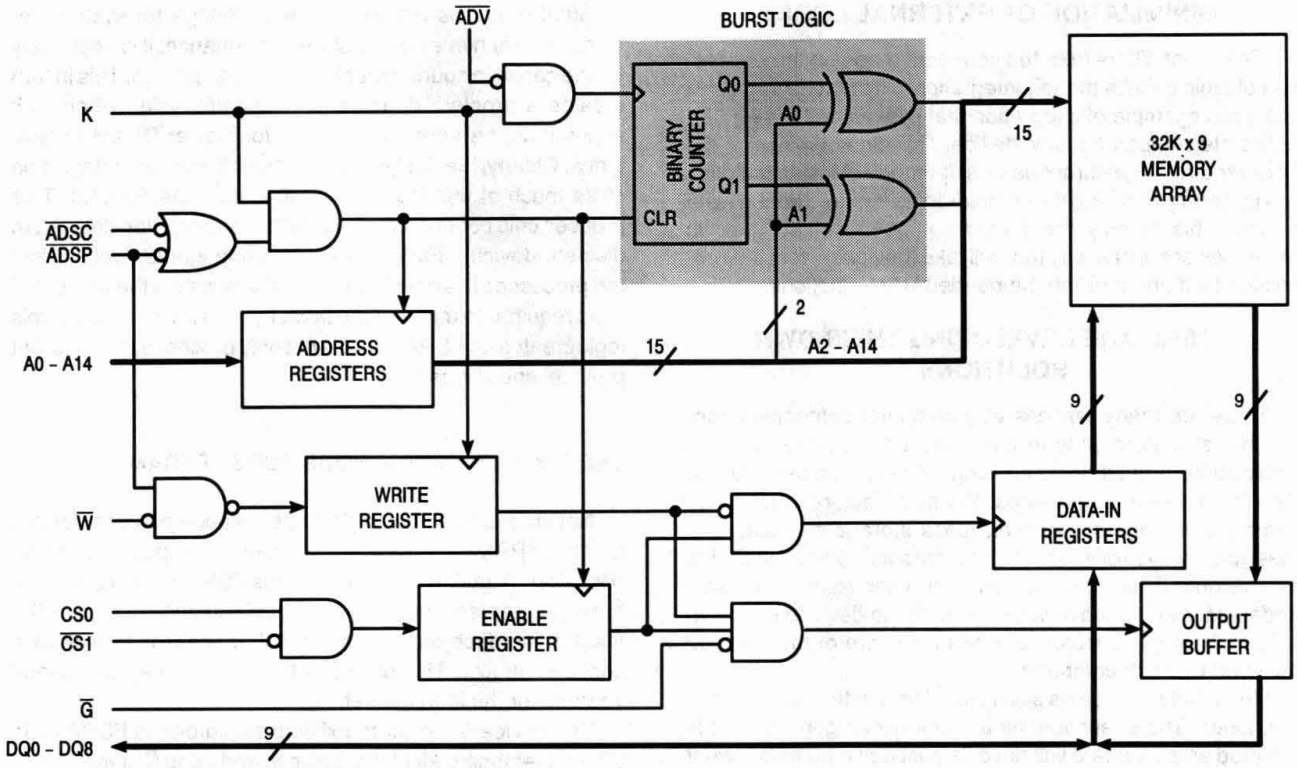

Figure 1. MCM62486A 32K x 9 BurstRAM Block Diagram

The removal of the wait state from the beginning of the write cycle actually simplifies the control logic since the conditions under which the BurstRAMs internal counter is advanced are now identical for both read and write cycles.

The conditional registering of the address input is especially useful when interfacing to a processor with multiplexed address and data buses such as the MC88200 or shared address buses such as the AM29000.

Burst FSRAMs are not a new concept; when the '030 first introduced the burst protocol in a microprocessor environment, a burst protocol FSRAM specification was developed. Unfortunately, the timing constraints of the '030 placed the performance goals of the FSRAM beyond the technology available at the time. The only way to build a no-wait state cache at the higher speeds was to utilize the bus retry cycle to rerun any memory access in the event of a cache miss.[3] To the RAM, this meant having to count backwards in the event of a cache miss and adding pins and logic to control this adjustment. Furthermore, the 15 ns access times needed were not feasible at the time.

THE FUTURE DIRECTION OF PROTOCOL SPECIFIC FSRAMs

Clearly, with the technology being developed today, it will be quite feasible to fully integrate all of the elements of the cache (data storage, address tag storage, and control logic) onto one chip. This will be the least cost approach, and if offered by a vendor, it will represent the least amount of user design resources. However, this approach will severely limit cache options and product differentiation. Furthermore, this approach will never perform as well as on-chip caches, which are growing in size. Thus, discrete FSRAMs of some kind will continue to be used in cache memory design.

Protocol Specific FSRAMs will increase in usage, but they will not completely replace standard products if for no other reasons than the versatility advantage of a standard device and its smaller packages. The densities of both will have to increase, though it appears that wider RAMs will be preferred for the new designs.

[3] Richard Crisp, Brian Branson, and Ron Hanson, "Designing a Cache for a Fast Processor," *Electronic Design*, October 13, 1988, pp. 111 – 118.

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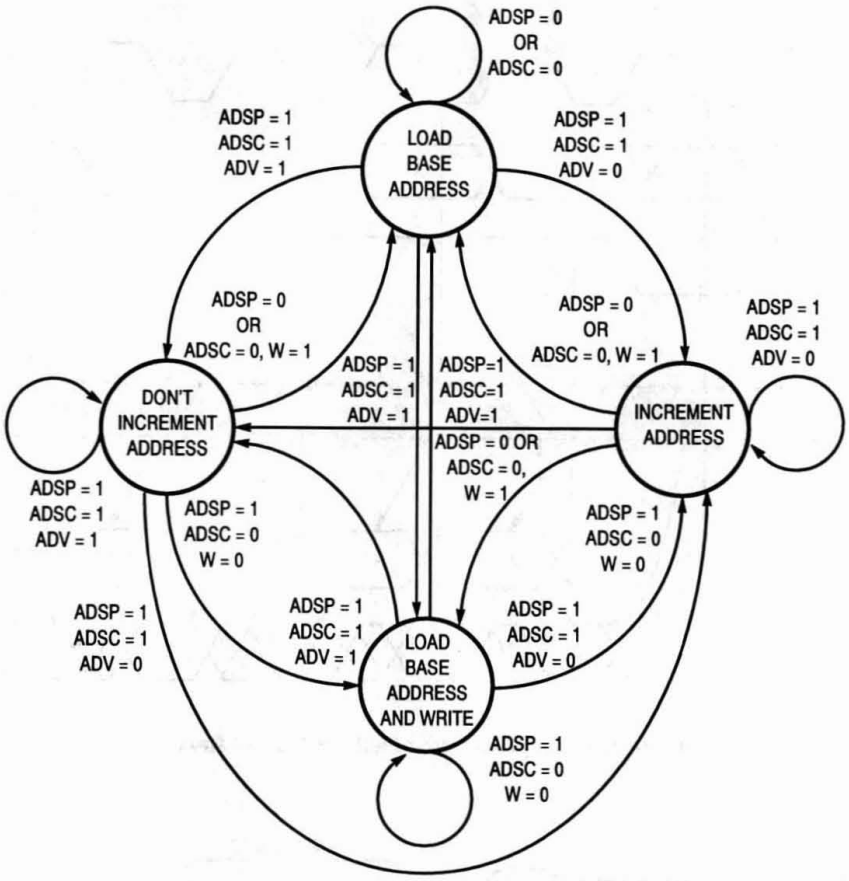

Figure 2. State Diagram for Address Determination on the MCM62486A BurstRAM

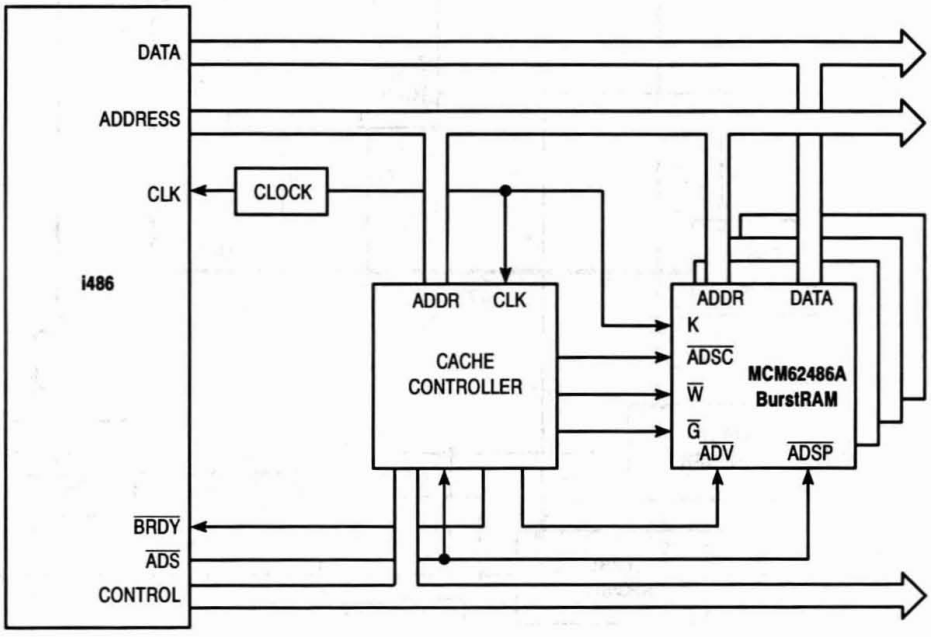

Figure 3. i486 128K Byte Burstable Cache Memory Block Diagram

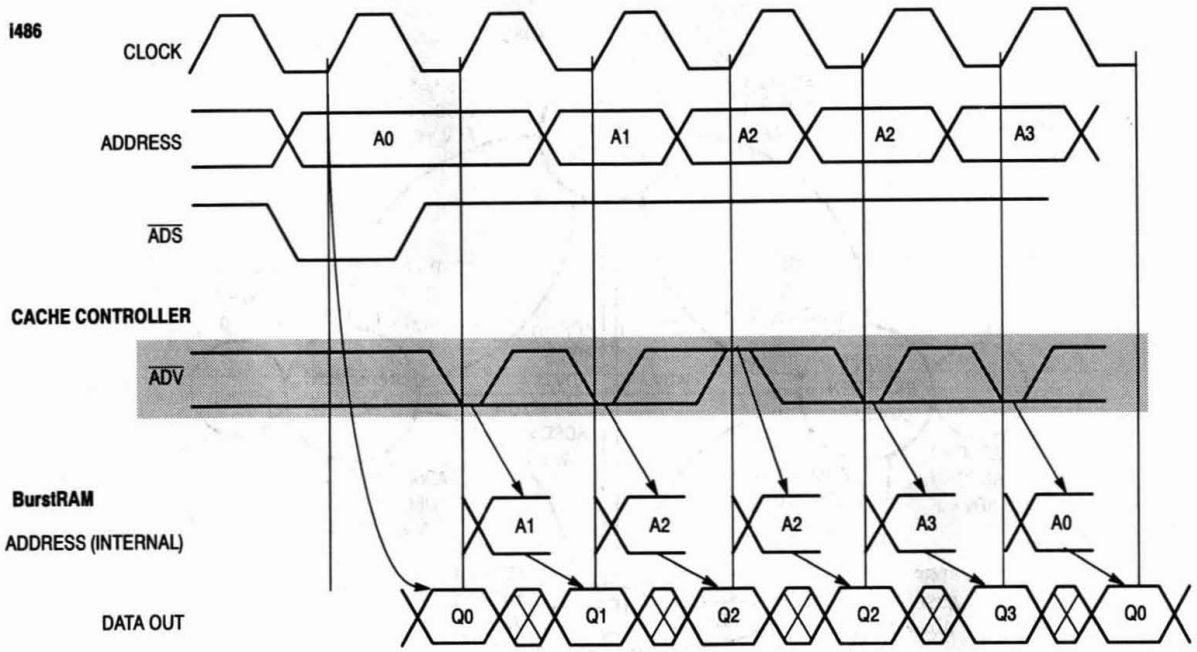

Figure 4. Timing Example of a 2/1/2/1 Burst Read

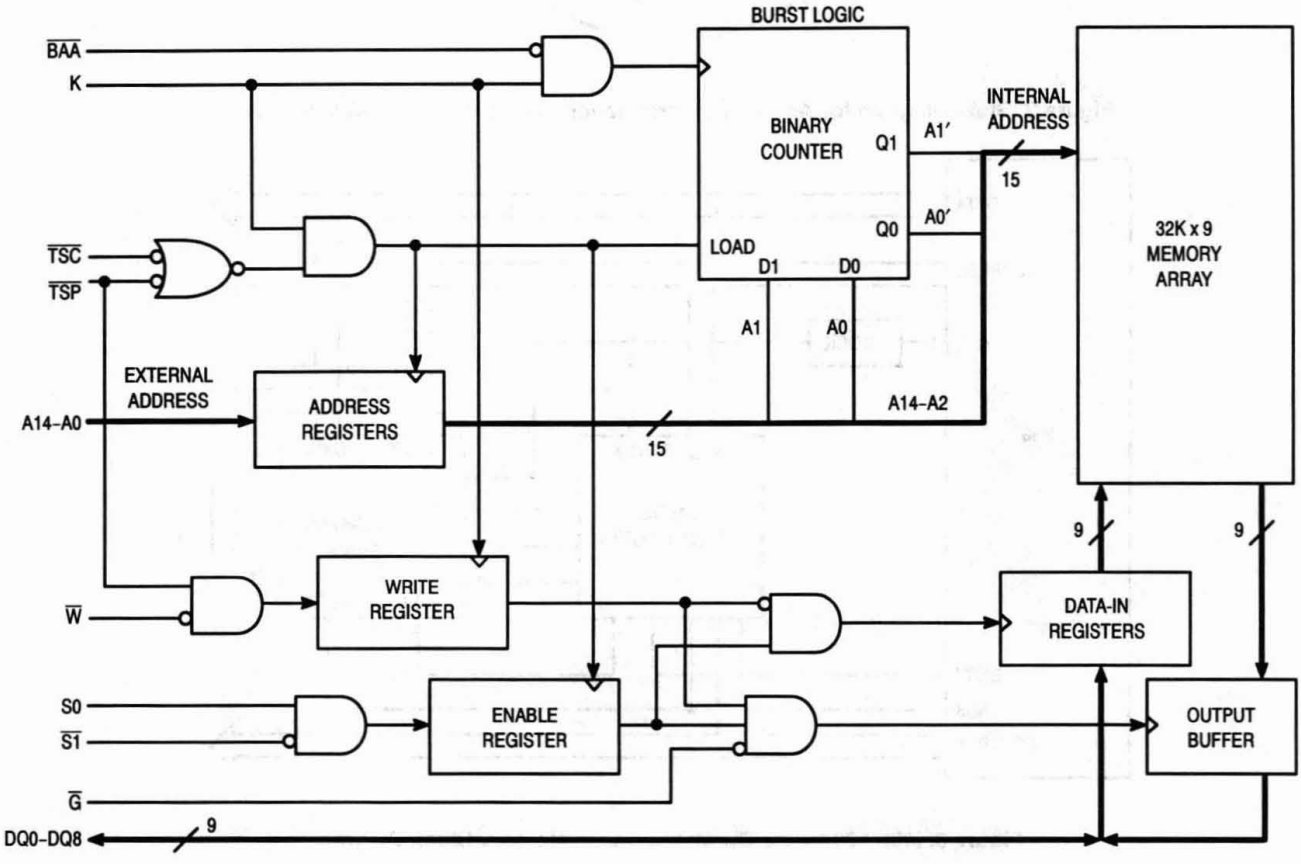

Figure 5. MCM62940A 32K x 9 BurstRAM Block Diagram

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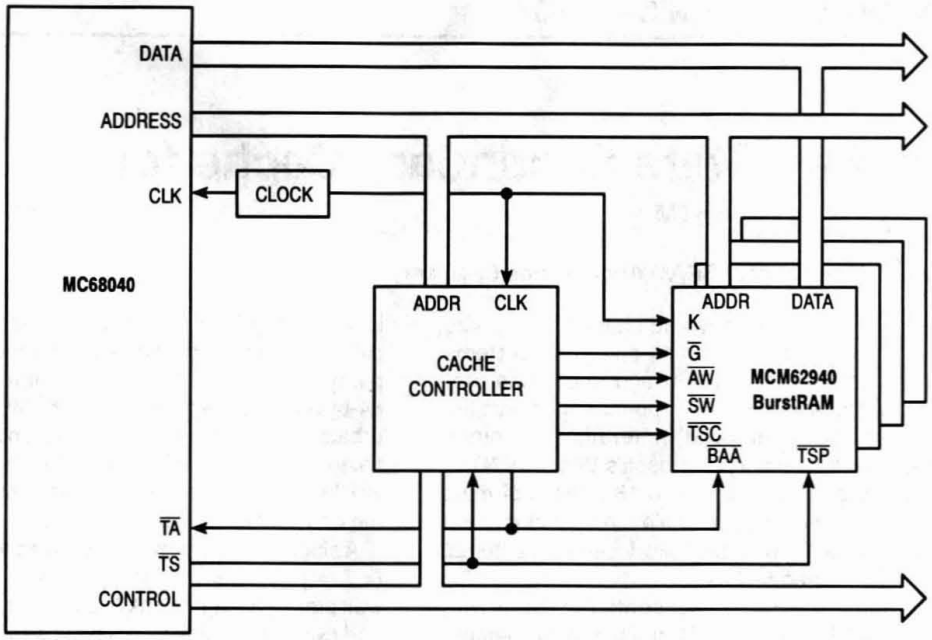

Figure 6. MC68040 128K Byte Burstable Cache Memory Block Diagram

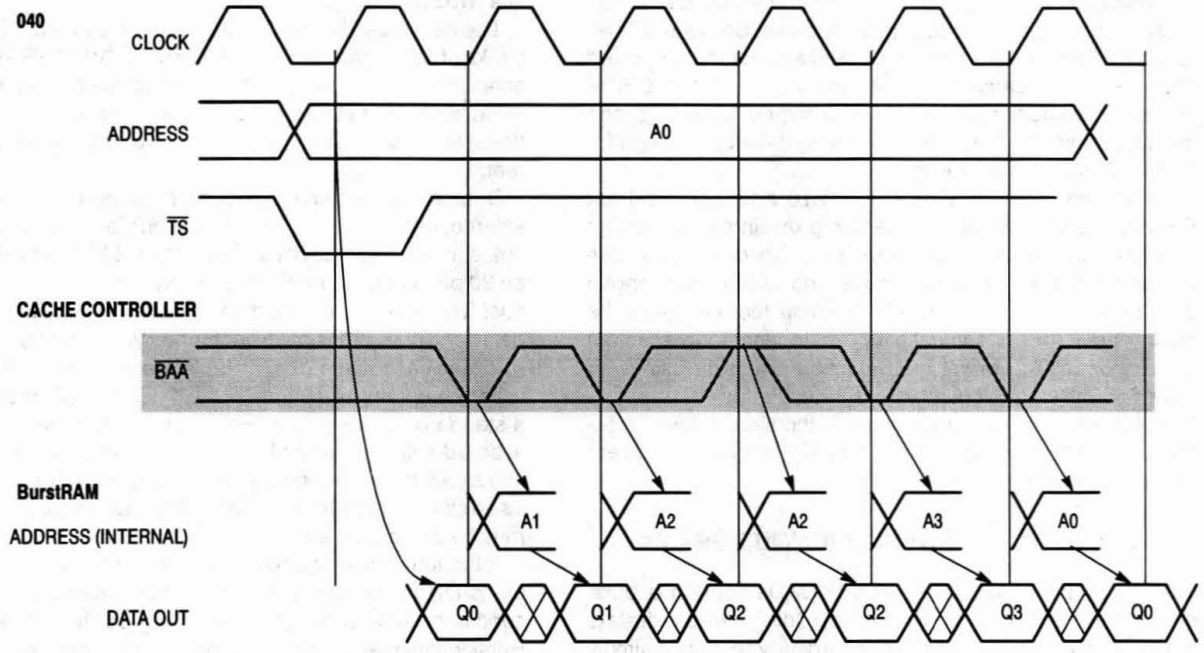

Figure 7. Timing Example of a 2/1/2/1 Burst Read

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AN1223

A Zero Wait State Secondary Cache for Intel's Pentium™

Prepared by: Michael Peters, FSRAM Applications Engineer

Due to the increased complexity and sheer memory size requirements of new and forthcoming operating systems (OS), graphical user interfaces (GUI) and application programs, the demand for ever-increasing performance from the desktop machine continues. Next generation machines require more and faster memory. Microsoft's Windows NT™, for instance, will most likely need 12 to 16 MBytes of main memory. Cache size requirements follow accordingly. And Intel's new Pentium CPU has been introduced with external bus speeds of 60 MHz and 66 MHz.

High performance memory is essential in achieving Pentium's full potential. First level (L1), on-chip cache memory hit rates will suffer as a result of users' migration away from DOS to Windows to Windows NT. It has been shown that L1 cache hit rates decrease mainly due to the increased number and types of references demanded by the newer OS.[1] The CPU designer can only afford relatively small increases in L1 cache size in an effort to keep chip size down. So, second level (L2) cache must make up for the lack of an appropriately sized cache and significantly help to avoid time consuming DRAM accesses. In addition, at 60/66 MHz bus speeds, the L2 cache must be capable of reading and writing data fast enough for Pentium's superscalar design.

Motorola's new families of 64Kx18 and 32Kx18 Fast SRAMs establish a new standard in providing a big enough and fast enough data cache for Pentium designs. These families include five synchronous and two asynchronous devices in each family. All x18 SRAMs feature byte-write capability, 3.3 V I/O compatibility, and asynchronous output enable control. A zero wait state solution is possible using four MCM67B618 (or four MCM67B518) BurstRAMs™. The objective of this note is to explain some of the system level, electrical, and timing issues associated with the design of a zero wait state secondary cache.

BurstRAMs vs. ASYNCHRONOUS SRAMs

Although the i486™ and Pentium CPUs support a burst cache line fill protocol, in most cases building a zero wait state bursting cache with a single bank of ordinary SRAMs is simply not practical. Virtually all cache controllers/chipsets designed to work with the i486 accommodate the burst protocol by using an interleaved scheme of two banks of standard asynchronous SRAMs. The speed requirements for this type of caching arrangement allow the use of 20 ns through 35 ns SRAMs. These speeds accommodate 20 through 33 MHz i486 machines, the bulk of today's IBM-compatible PC market. For the i486's 32-bit bus speeds less than 50 MHz, this hook-up is technically feasible, but somewhat expensive and physically large, and it consumes a good deal of power since as many as eight SRAMs are required. However, Pentium's 64-bit bus and bus cycle rates of 60 MHz and faster only exacerbate the difficulties with single and double bank caches using ordinary asynchronous SRAMs. Most chipset vendors will find that the use of synchronous burstable SRAMs will be the only practical zero wait state solution for Pentium.

A single bank scheme must use either extremely fast RAMs (< 7 ns for a 60 MHz bus) or add wait states. With the added wait states, a single bank 3-2-2-2 (three lead-off clock cycles and two clock cycles for each subsequent read) design might still require 12 ns standard SRAMs.

A double bank scheme can be designed with wait states or for high speed with no wait states. Figure 1 shows the timing for a 3-2-2-2 design using sixteen 15 ns 32Kx8 (or x9) SRAMs in a two bank design.

The cache can be expected to consume about 8.6 W. Two banks of 12 ns standard 32Kx8 (or x9) BiCMOS SRAMs might achieve 3-1-1-1 burst, but at an even greater power premium — nearly 12 W. In two bank schemes, even when one bank is de-selected, it will still draw about 65% of the full operating current.

Double bank designs present other issues that must be considered, including address and data bus loading, physical layout, and socketing devices. Two banks of 32Kx8s will present an 80 pF load (plus routing) to the cache controller's address bus. These heavily loaded lines represent additional signal delay and power dissipation compared to a BurstRAM design. And, one cannot afford a 5 ns buffer delay in the address path. When comparing the BurstRAM's 52-lead PLCC package with a standard 32Kx9 SOJ, direct mounting of these devices on a board will yield roughly four square inches versus eight square inches, respectively. Socketing the SRAMs is ill advised since access time will be pushed out, and signal integrity may be compromised.

Although designing caches with asynchronous SRAMs can be done, the control signal timing is far from easy. Of all timing concerns, write pulse generation may be the biggest issue. Burst writes may be next to impossible to perform since both edges of the write pulse must be positioned precisely to accommodate address set-up and data hold times. One can expect 10 ns minimum write pulse widths for 12 ns asynchronous SRAMs; this does not leave much time for the 15 ns cycle processor bus.

Motorola has developed a series of 256Kbit, 512Kbit, and 1Mbit SRAMs, known collectively as BurstRAMs, to solve these problems.[2]

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i486 and Pentium are trademarks of Intel Corp.
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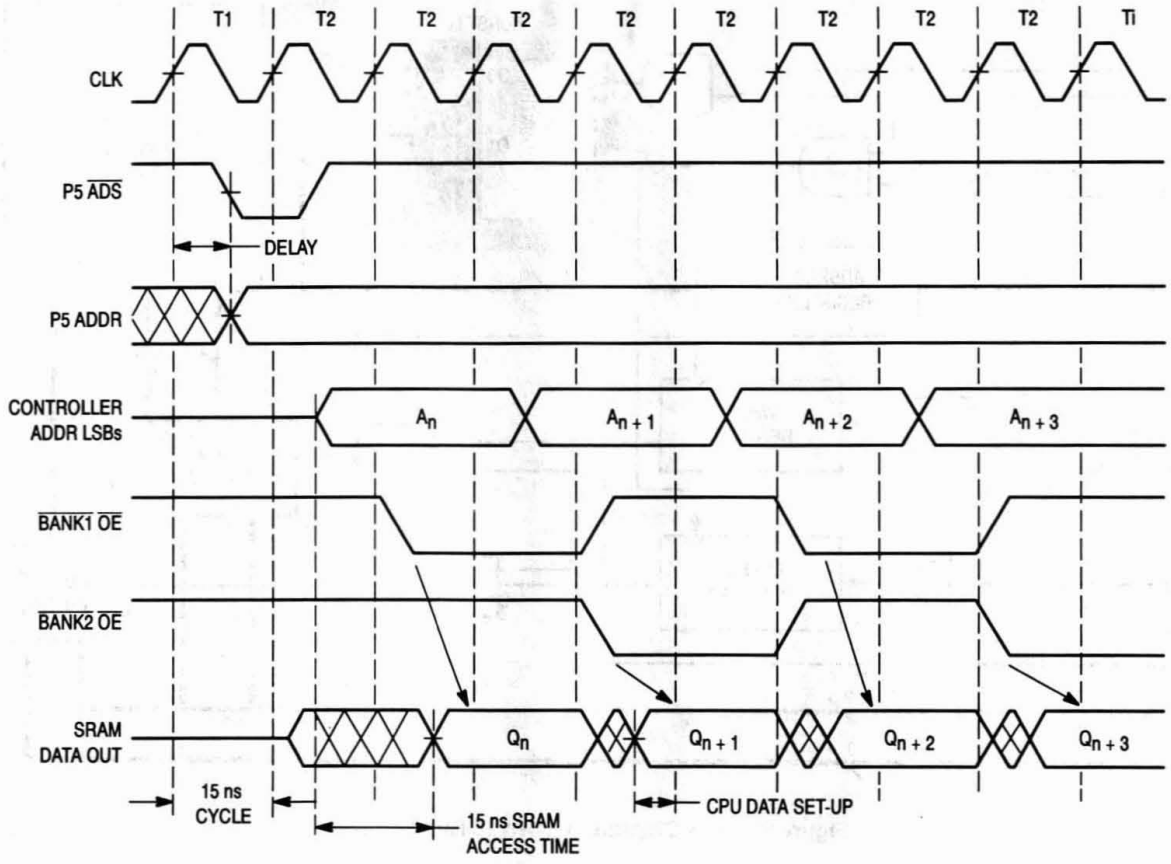

Figure 1. Two Bank Asynchronous SRAMs Performing 3-2-2-2 Burst READ

The MCM62486, a 32Kx9 BurstRAM, was developed for i486 systems. These BurstRAMs are being used in many of the 50 MHz i486 systems built today. The MCM67518, a 32Kx18 device, and the MCM67618, a 64Kx18 device, are the best suited for Pentium-based designs. Key to the success of a zero wait solution is the SRAM's support of Intel's burst protocol. A 2-1-1-1 (zero wait state) burst read cycle can be performed at cycle times of 20 ns and less. Pipelined addressing can further reduce a burst cycle to a 1-1-1-1 count. The MCM67B618 and MCM67B518 are synchronous BiCMOS SRAMs that feature wide x18 data paths, burst reading and writing, byte-write capability, 3.3 V I/O compatibility, and asynchronous output enable control. Note that all BurstRAM operations occur on the rising edge of clock (CLK).

Four (4) MCM67618 devices provide a single bank of 512K byte L2 cache. The interface to the Pentium chip is a direct connection for address and data paths. These new BurstRAMs (MCM67B518, MCM67B618) have been designed to operate at clock rates of up to 66 MHz (15 ns cycle time). They are available in access times of 9/12/18 ns with cycle times of 15/20/30 ns, respectively. The term "access time" is used loosely for synchronous SRAMs and is more accurately, CLK-to-VALID DATA time.

WHAT IS A BurstRAM™ ?

BurstRAMs are synchronous SRAMs that contain input registers for address, write, and enable signals and have an on-chip burst counter that imitates the i486 and Pentium's lower order address burst count. These control signals are registered into the BurstRAM on the rising edge of the CLK input. Three (3) control pins allow complete control of the burst function. $\overline{ADSP}$ (ADS Processor), $\overline{ADSC}$ (ADS Controller), and $\overline{ADV}$ (ADVance) control the burst read/write functions as well as single read/writes. A self-timed write is also provided for the purpose of simpler (and relaxed) write timing. Byte-write capability is provided with the $\overline{UW}$ and $\overline{LW}$ (Upper/Lower byte Write) signals. Note that all control signals are active low. See Figure 2.

THE BURST CYCLE

A burst read cycle is performed as follows (see Figure 3):

1. During the first cycle (T1), the CPU generates ADS and a valid address, and the BurstRAMs register the external address A<18:3> and enable on the rising edge of the system clock (CLK). This address can be considered the base address from which the BurstRAM begins its address counting,

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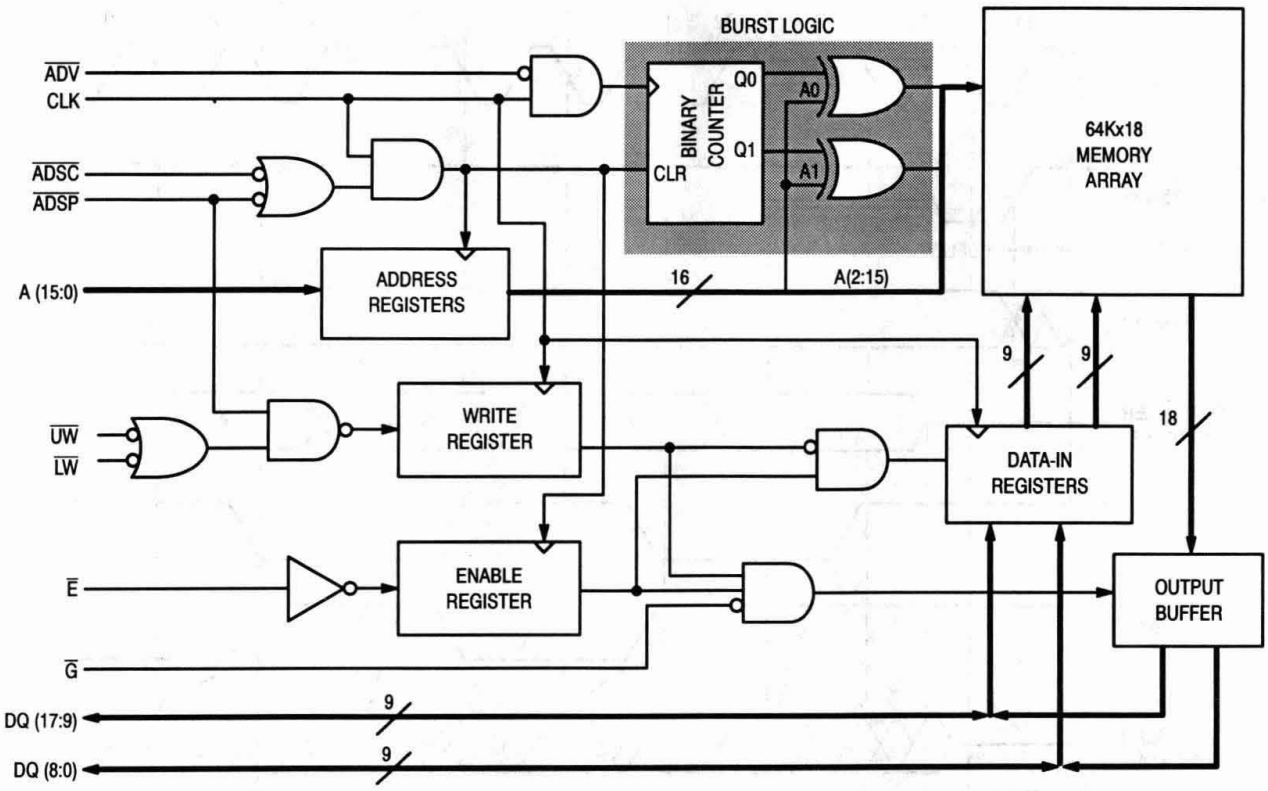


Figure 2. Block Diagram of 64Kx18 BurstRAM

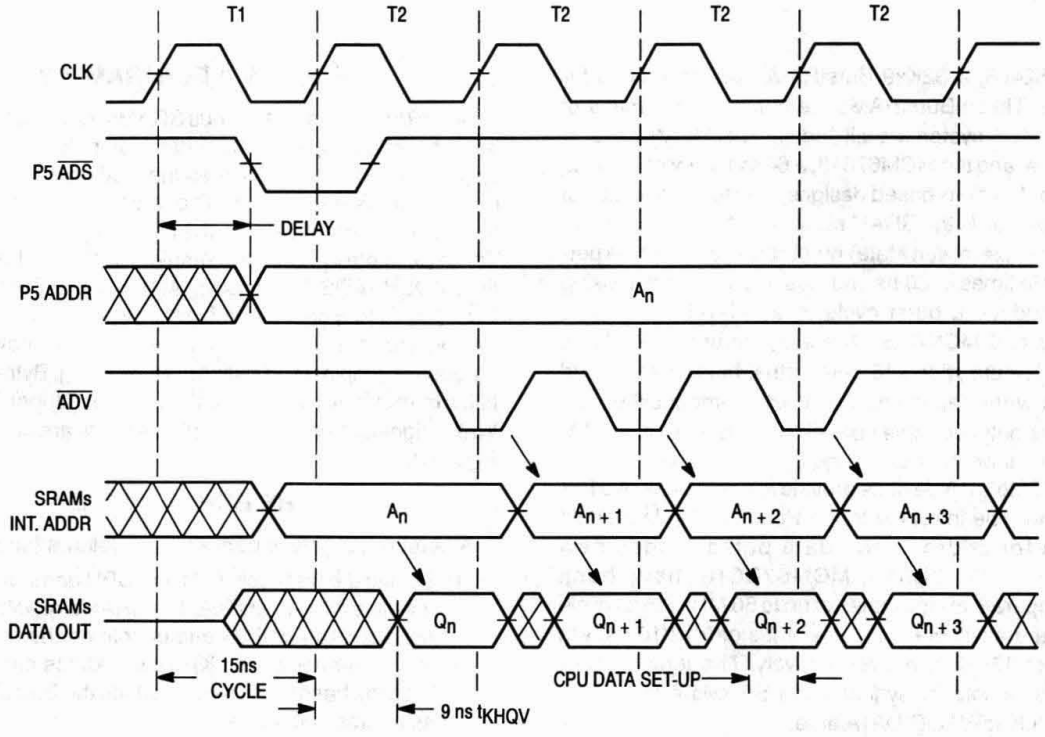


Figure 3. 64Kx18 BurstRAM Performing 2-1-1-1 Burst READ

2. Assuming the cache controller has determined that the cycle is a cache hit, the first 8 bytes of valid data are driven onto the data bus 9 ns after the second rising clock edge,
3. Subsequent cycles present valid data upon the negation of $\overline{ADS}$ and the assertion of $\overline{ADV}$. An entire 32 byte cache line can be supplied to the CPU in just five cycles. The BurstRAM's output enable ($\overline{G}$) can be asserted well into the 2nd cycle since it is asynchronous and represents only 5 ns delay.

Pentium operates with external bus speeds of 60 MHz and 66 MHz. This corresponds to 16.6 ns and 15 ns cycle times, respectively. Standard asynchronous SRAMs are hard pressed for a zero-wait state application. A look at the timing reveals that sub-12 ns SRAMs would be required since Pentium's data set-up time is about 3 to 4 ns. The inclusion of on-chip logic allows the BurstRAM to be directly connected to the CPU, and avoids the timing penalty associated with glue logic.

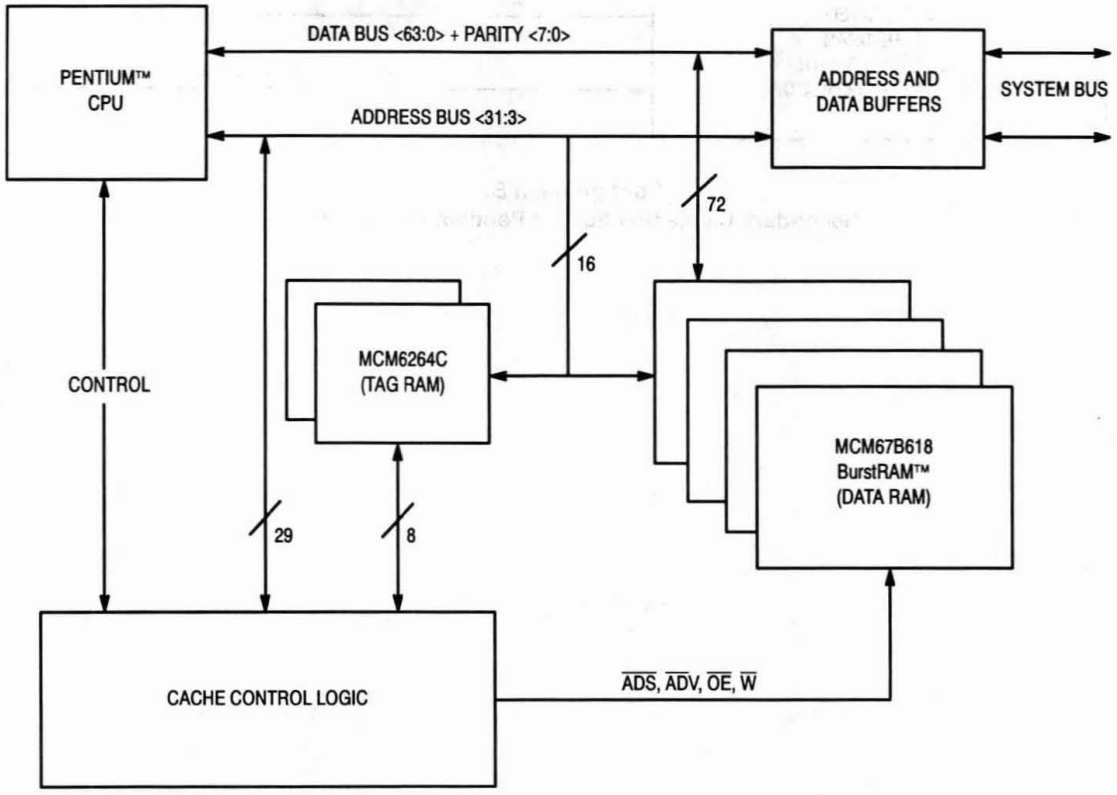
Using the BurstRAM, a zero wait state burst write cycle can be performed as well. Upon the CPU's assertion of $\overline{ADS}$, the BurstRAM begins and completes a burst write cycle with the assertion of $\overline{E}$, $\overline{LW}$, $\overline{UW}$, and $\overline{ADV}$ signals. A burst write cycle can be started using either $\overline{ADSP}$ or $\overline{ADSC}$. If $\overline{ADSC}$ is sampled low (while $\overline{ADSP}$ is high), data can be written immediately to the BurstRAM while $\overline{ADV}$ is asserted on subsequent cycles for the completion of the burst cycle. If $\overline{ADSP}$ is sampled low (while $\overline{ADSC}$ is high), the write register is blocked inside the BurstRAM and consequently only allows A<15:0> and $\overline{E}$ to be registered. On the following cycle ($\overline{ADSP}$ and $\overline{ADSC}$ negated), the burst write operation begins assuming $\overline{LW}$ and $\overline{UW}$ have been asserted. Again, $\overline{ADV}$ must be asserted on subsequent cycles to complete the burst cycle.

The use of a synchronous SRAM makes a design simpler in the sense that address and control signals can have looser timing constraints since they are registered in, and the SRAM does the rest. As long as DQ<17:0>, $\overline{LW}$, and $\overline{UW}$ signals comply with the required set-up (2.5 ns) and hold (0.5 ns) times, complex off-chip write pulse generation can be eliminated. An undue burden will be placed on the controller to provide proper write pulse width and write timing edges relative to address and the CPU's valid data.

SYSTEM CONFIGURATIONS

Pentium's 64-bit data path will require four (4) MCM67B618s (or MCM67B518s) to provide a single bank 512K (256K) byte L2 cache. The interface to the Pentium chip is a direct connection for address and data paths. Control signals must come from the cache controller. See Configurations A/B/C of the System Block Diagrams.

Configuration A is the least integrated solution, one that uses external tag RAM and a PAL or ASIC for the cache controller. The DRAM controller would be yet another component in the system.



Configuration A
Secondary Cache Solution for Pentium — 512KByte

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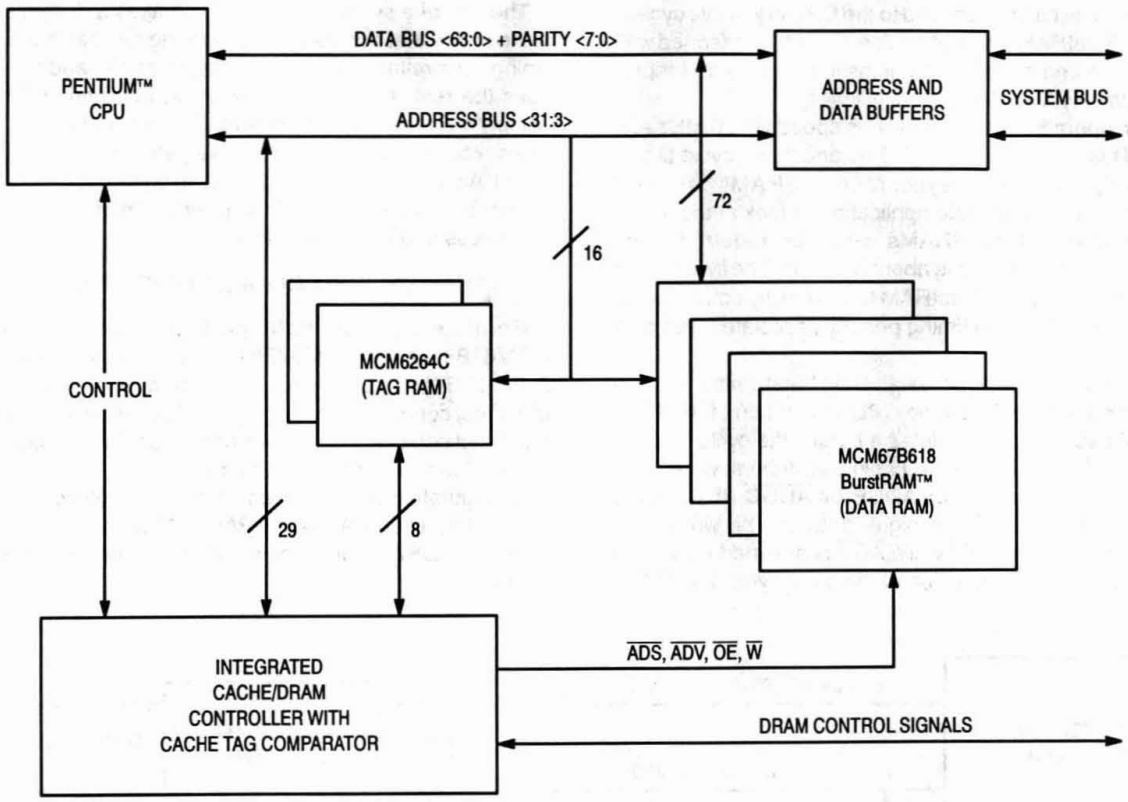
Configurations B and C are the most likely approaches taken by chipset vendors in which the tag RAM may or may not be integrated, but will probably integrate the DRAM control. For direct-mapped caches such as these, tag RAM size depends on the controller's mapping of tags (or sectors) to cache lines. Each sector may consist of 1, 2, 4, or more cache lines. Tag RAM depth is then 16K, 8K, 4K, or so, respectively.



Configuration B
Secondary Cache Solution for Pentium — 512KByte

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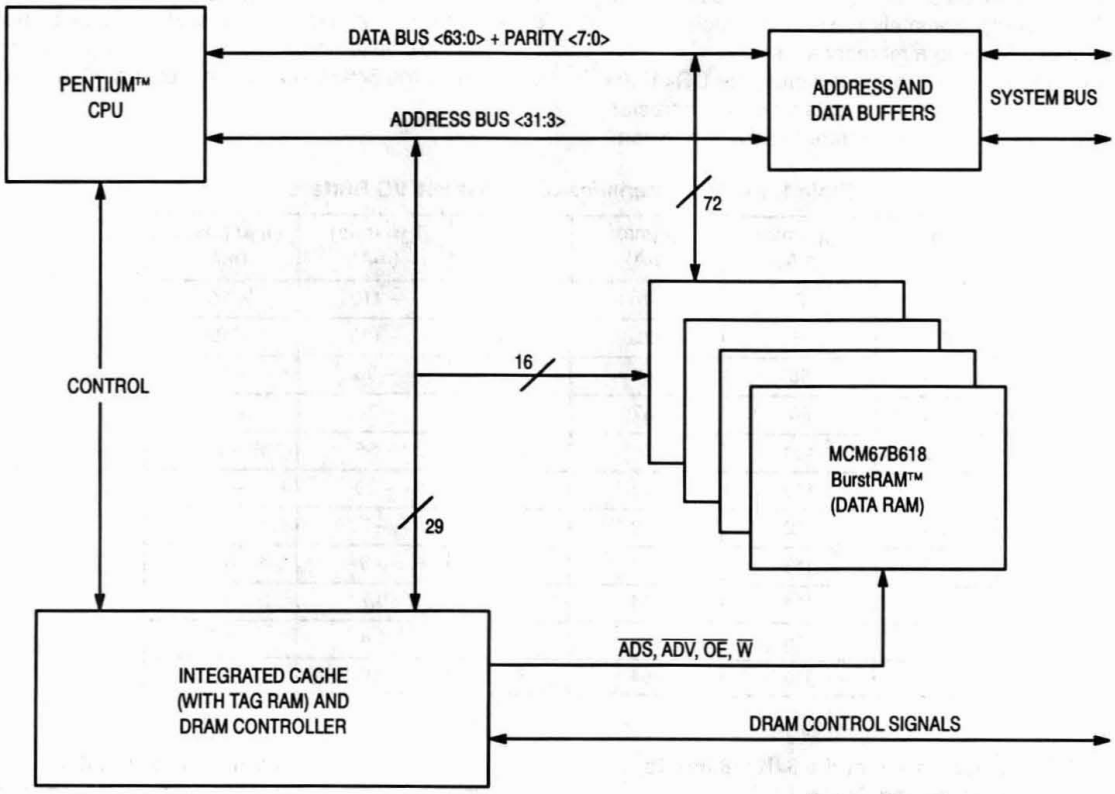
The tag RAM must be at least 10 ns for zero wait state performance; otherwise, a lead-off wait state must be added (3-1-1-1). This is determined by the speed of the controller's tag comparison as well. If the cache line size is 32 bytes and the data RAM depth is 64K, the tag RAM will have to be a 16Kx8/10 or 4Kx8/10 organization. The tag RAM's width (data path) is a function of the system's main memory size. An 8-bit tag will allow a cache size of 512KB to cache 128MB of main memory.



Configuration C
Secondary Cache Solution for Pentium — 512KByte

FEATURES OF 64Kx18

The 64Kx18 SRAMs are fabricated on a BiCMOS process and exhibit less dependence on output loading compared to CMOS devices. These SRAMs are powered on a single 5 V supply (± 5%) and are 3.3 V I/O compatible — no additional power supplies are required. The output buffer is composed of an NPN pull-up and an N-channel MOS pull-down. The pull-up circuitry has been carefully designed to limit the NPN's base drive such that the output pulls up to approximately 3.3 V even under high supply conditions (e.g., 5.25 V). These 3.3 V "friendly" output buffers have controlled 3.3 V output swing and will not overdrive a future 3.3 V controller or processor. This important feature allows one to easily migrate from an all 5 V system to a mixed 5 V – 3.3 V system upon the availability of 3.3 V Pentium and controller chips.

SYSTEM CONSIDERATIONS

The entire 64Kx18 SRAM family makes use of multiple power and ground pins on the 52-lead PLCC package. Five (5) power and five (5) ground pins (6 pairs for the asynchronous devices) have been provided to allow adequate supply decoupling and return current paths for such a fast device. Multiple power and ground pins reduce the effective inductance of theses connections. Since the output buffers swing 3.3 V in 1 to 2 ns (t_r/t_f), significant di/dt currents flow in the V_{CC} and V_{SS} pins. Separate power and ground planes on the printed circuit board are highly recommended and will help improve signal integrity, ground bounce, and in turn the SRAM's access time. The use of a 0.001 µF or 0.01 µF chip capacitor or similar leadless (surface mount) capacitor connected within 0.5 inch or so of each pair of V_{CC}/V_{SS} pins will provide a low impedance path for the fastest transients. A single 1 to 4.7 µF chip or ceramic capacitor per device should be sufficient for dc stability.

The use of standard (asynchronous) SRAMs may prove to be very difficult to use in 50+ MHz systems due to the requirements of carefully controlling the signal integrity, maintaining good noise margins, keeping component count down, and reducing board space. Because the BurstRAM, a synchronous device, registers address and control signals during a very brief moment during the system cycle, noise occurring throughout most of the cycle in the system can be tolerated by the BurstRAM. Component count, and therefore board space, is reduced since these SRAMs integrate the burst counter logic and self-timed write circuitry onto the chip and, in addition, have a wide (x18) data path. Because of the on-chip logic, cache control logic can be simplified and some control signal timing can be relaxed.

In cases that demand detailed timing analysis and a close look at the analog effects of your board design, it is recommended that a board-level (Quad Design/Viewlogic) or SPICE simulator is used. Particularly when PCB routing lengths are about 4 inches or more, transmission line effects become dominant over the lumped circuit equivalent. Since interconnect time-of-flight is approximately 175 to 190 ps/inch, a 4 inch route adds about 0.75 ns to a memory access.

When analyzing the cache data read path, the DQ<17:0> are in their active state and drive the data bus. The characteristics of these output pins are important to know when completing a board's physical layout. Use the information in Table 1 (output buffer I-V data), Table 2 (input I-V data), and Table 3 (package parasitics) to help verify your timing and loading effects. This tabular data may be used directly as input to board level simulators, such as those offered by Quad Design, Integrity Engineering, Quantic Labs, etc. Figure 4 shows how to connect the parasitic package components between the chip (output buffer or input) and package pin. An input pin on the 64Kx18 can be modeled as C die = 4 pF.

Table 1. I-V Characteristics of the 64Kx18 I/O Buffers

V_{OL} (V)	I_{OL} (min) (mA)	I_{OL}(max) (mA)	V_{OH} (V)	I_{OH} (min) (mA)	I_{OH} (max) (mA)
0	0	0	0	–110	– 145
0.5	38	60	0.5	– 106	– 136
1.0	68	107	1.0	– 96	– 124
1.5	90	137	1.5	– 78	– 102
2.0	104	154	2.0	– 55	– 77
2.5	110	160	2.5	– 29	– 45
3.0	112	162	3.0	– 7	– 13
3.5	113	163	3.5	0.3	0.2
4.0	114	164	4.0	0.7	0.6
4.5	115	164	4.5	1.4	1.3
5.0	115	164	5.0	2.0	2.0

Table 2. I-V Characteristics of the 64Kx18 Inputs (Address and Control)

Diode to GND		Diode to V_{CC}	
V_{in} (V)	I_{in} (mA)	V_{in} (V)	I_{in} (mA)
0	0	5.0	0
– 0.4	0	5.4	0
– 0.5	0	5.5	0
– 0.6	0	5.6	0
– 0.7	– 0.1	5.7	0.1
– 0.8	– 2.0	5.8	2.1
– 0.9	– 25	5.9	20
– 1.0	– 70	6.0	50

Table 3. Packaging Characteristics

	Min	Max	Unit
R package	50	200	mΩ
L package	3	6	nH
C package	0.5	1.0	pF
C die	2	7	pF

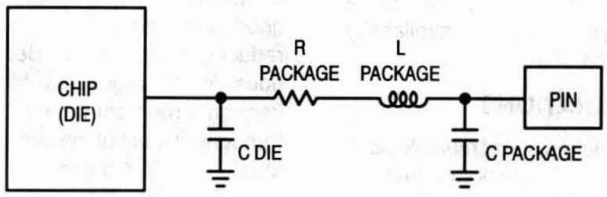


Figure 4. Package Parasitics Schematic

OUTPUT BUFFER CHARACTERISTICS

The access times guaranteed in the datasheet are based on a 50Ω test load and should be derated for unterminated CMOS loads. Refer to the derating curve (Figure 5) for your application. This curve relates the difference in access time between a 50Ω test environment and a lumped capacitive load (no dc load) condition typically found in most applications. The curve is based on worst case conditions, i.e., V_{CC} = 4.75 V and T_A = 70°C. Note that the 50Ω test condition is equivalent to a lumped 10 pF load. For instance, if the BurstRAM outputs see a 30 pF load, derate the access time by about 0.4 ns. So, for a Pentium design that uses the MCM67B618 – 9 ns device, one can expect a worst case access time of 9.4 ns under these conditions.

SUMMARY

For high performance Pentium systems, the use of Motorola's 64Kx18 BurstRAMs provides a straightforward solution to Pentium's secondary cache requirements. Four BiCMOS BurstRAMs support the size and speed required by zero wait state Pentium systems. For equivalent cache size and performance, standard SRAM solutions warrant two bank interleaved approaches that utilize more board space, require more power, and demand a higher performance cache controller.

REFERENCES

1. AP-469: "Cache and Memory Design Considerations for the Intel 486DX2 Microprocessor", Intel Corp.
2. DL156/D: *Fast Static RAM BiCMOS, CMOS, and Module Data*, Motorola, Inc.

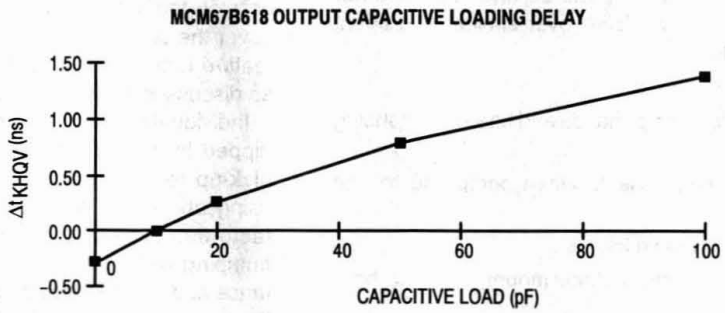


Figure 5. Access Time Derating Curve

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AN1231

Plastic Ball Grid Array (PBGA)

Prepared by: Andrew Mawer
(MMTG Final Manufacturing Operations)

INTRODUCTION TO THE PBGA

The Plastic Ball Grid Array or PBGA package is the industry description of what is sometimes referred to as Motorola's OverMolded Pad Array Carrier or OMPAC package. It was developed by Motorola in the late 1980's for use in Motorola products with space limitations such as radios, pagers and cellular telephones. Since that time it has grown in popularity within the electronic industry and standard body sizes and pin counts have been adopted by JEDEC and soon by EIAJ. The many benefits of using PBGA over similar lead count leaded devices include:

1. Board space efficiency.
2. Thermal and electrical performance and ease of enhancing both.
3. Excellent surface mount yields when compared to fine pitch leaded devices.
4. Lower profile (i.e., overall thickness).
5. Compatibility with existing surface mount, test and handling equipment.
6. Potential lower total cost of ownership compared to leaded devices due to reduced scrap, rework and lack of need for fine pitch assembly equipment.

This application note serves to provide general information about the PBGA package as well as provide information about its implementation into products and surface mount assembly.

PACKAGE CONSTRUCTION

The PBGA package is based on a printed circuit board (PCB) substrate or "leadframe" fabricated of Bismaleimide Triazine (BT) epoxy/glass laminate. This material is used over standard and multi-functional FR4 laminates for its high glass transition temperature of 170 – 215°C and heat resistance (230°C exposure for 30 minutes with no degradation). The standard core thickness of this two layer substrate is typically 0.2 mm with 18 μm (half ounce or 0.7 mil) rolled copper on each side. The core thickness for two layer substrates has also been increased to 0.4 mm for some designs. A two mil or less thick (thickness over BT–epoxy/glass) dry or multiple pass wet film soldermask is currently used to ensure that all the substrate vias will be completely tented. The silicon chip containing an integrated circuit is die bonded to the top side of the substrate using die attach adhesive typical of that found in leaded devices. The chip is then gold wire-bonded to wire bond pads on the circuitized substrate. Traces from the wire bond pads take the signals to vias which carry them to the bottom side of the substrate and then to circular solder pads. The bottomside solder pads are laid out on a square or rectangular grid with either a constant 1.5 mm or 1.27 mm pitch. These two pitches, as well as a 1.0 mm pitch, are prescribed by the JEDEC registration for the square PBGA, which is summarized in Appendix A. Some pre–JEDEC 60.0 mil pitch packages, such as the 86 pin, still exist in Motorola's portfolio. An overmold (or possibly a liquid or "glob-top" encapsulation) is then performed to completely cover the chip, wires and substrate wire bond pads. Typical feature dimensions common to most PBGA configurations, as discussed above, are summarized in Table 1.

Individual preformed 30 mil diameter solder balls are gang dipped in no-clean paste flux using a specially designed pick-up tool then placed on each bottomside solder pad using an internal Motorola developed (by Motorola Manufacturing Systems), but commercially available, robotic bumping cell. To provide somewhat greater fatigue resistance and a finer, more homogeneous solder microstructure, the near-eutectic (62%Sn/36%Pb) solder balls also contain 2% Ag, which results in a solidus temperature of 179°C. Straight eutectic solder balls with a melting temperature of 183°C may also be used. The balls are reflowed onto the solder pads using a conventional forced convection nitrogen reflow oven and a typical surface mount assembly profile with a maximum specified temperature of 230°C. Following reflow, the substrates are centrifugally cleaned in Terpene (CFC-free organic cleaner) to remove flux residue as well as any fibers and particulates from the remainder of the package.

The entire process described above, takes place on a substrate containing several (currently from three to six, or more) PBGA devices. The final step in assembly is the singulation or excise of the individual PBGA devices out of that larger substrate or panel. The resulting device has a body size that now conforms to JEDEC standards, although for the near term some pre-JEDEC devices are included in Motorola's package offerings. The package outline dimensions for several PBGA configurations (86, 119, 169, 225, 313, and 357 pins) currently offered by Motorola are included in Appendix B. The total number of I/Os on the package is obviously determined by the body size and pitch. Additionally, the JEDEC standard allows for any number of balls to be depopulated from a completely populated matrix (i.e, staggered pitch, corner, or center balls depopulated). A cross-sectional rendering of a typical PBGA mounted to a PCB is pictured in Figure 1.

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Table 2 provides nominal room temperature values for the physical properties of all the materials that comprise the PBGA package. It is important to note that the properties of many of the PBGA materials have a temperature-dependence that is not included in the table.

Table 1. Typical Nominal Dimensions of Selected PBGA Substrate Features

Feature	Dimension (mil/mm)	Comment
Substrate Thickness (Two Layer)	7.9/0.20 OR 15.7/0.40 14.1/0.36 21.9/0.56	BT/glass laminate core thickness. Overall (BT/glass + Cu + soldermask).
Substrate Thickness (Four Layer)	17.3/0.44 24.0/0.60	BT/glass laminate core thickness. Overall (BT/glass + Cu + soldermask).
Copper Thickness	0.71/0.018 1.2/0.030	Clad to BT/glass laminate. Plated on (electroless + electrolytic).
Trace/Space Widths	3.5/0.090	Minimum.
Soldermask Thickness	2.0/0.05 1.2/0.03	Over BT/glass. Over copper features.
Via ϕ	9.8/0.25 11.8/0.30	Typical Minimum. Normal.
Solder Pad Cu ϕ	33/0.84 31/0.78	Most 1.5 mm/60 mil pitch devices. Specific 1.27 mm pitch devices.
Soldermask Opening ϕ	25/0.64 23/0.58	Most 1.5 mm/60 mil pitch devices. Specific 1.27 mm pitch devices.

NOTE: ϕ = Diameter. All dimensions are approximate and are for reference only.

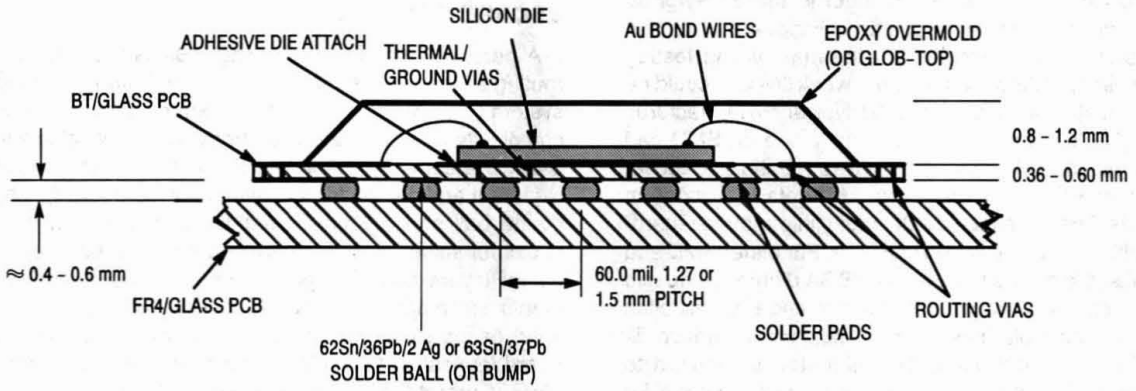

Figure 1. Cross-Sectional View of an PBGA Mounted to a PCB

Table 2. Physical Properties of All Materials Used in the PBGA Package at 23°C

Material	Elastic Modulus (ksi)	Poisson's Ratio (–)	T_g (°C)	CTE – x, y/z < T_g (ppm/°C)	Thermal Cond. (W/m-°K)
Copper (ED/Rolled)	17,500	0.345	1085 (melt)	17	418
62% Sn/36% Pb/2% Ag Solder	4,600	0.4	178 (melt)	21	50
Dry Film soldermask	580	0.40	≈120	35	0.33
BT/Glass Subtrate	2,200	0.195	175	13/57	0.19
Silicon Die	18,900	0.278	1412 (melt)	2.6	83
Mold Compound	2,300	0.25	196	15	0.67
Ag Filled Epoxy Die Attach	1,070	0.3	77	52	1.38

MOTHERBOARD LAYOUT

The PBGA package, with its leads or balls in an array configuration, presents some unique challenges to overcome with respect to motherboard routing when compared to peripherally leaded devices. Additionally, the volume of solder in the joint is relatively large and since all of it is molten during reflow, special considerations must be taken when determining appropriate pad geometries.

SOLDER PAD GEOMETRY

There are two basic types of solder pads commonly used with PBGA: copper or non–soldermask defined (NSMD) and soldermask defined (SMD). The NSMD case is similar to a standard surface mount pad where there is a soldermask clearance around the copper solder pad. The SMD type of pad has a larger copper than soldermask opening diameter. Both pad types have been used successfully by Motorola but the NSMD pad type is recommended for most applications. It has the advantage that copper dimensions can typically be controlled more tightly than soldermask and a hot air solder leveled (HASL or HAL) surface finish with better uniformity and coverage can usually be achieved. An additional advantage may be a lower stress concentration on the PBGA solder joint and accompanying increased solder joint reliability. This advantage can only be realized when NSMD pads are employed on both the PCB and PBGA package. The SMD pad, because of its greater copper area and soldermask overlap, has greater adhesion strength to the epoxy/glass laminate. This extra strength could be important in certain extreme bending and accelerated thermal cycling testing where the pad to PCB adhesion is the weak link and could be the failure location as opposed to the typical solder fracture.

The PBGA itself has traditionally contained an SMD pad for the increased adhesion strength as mentioned above. Some newer PBGA designs from Motorola may contain NSMD pads. The user should ask for pad information regarding a specific design packaged in PBGA. For either SMD and NSMD pads, the goal is to have the PBGA diameter equal to that on the package. In general, 1.5 mm and 60.0 mil pitch designs from Motorola have a 25 mil solderable surface diameter. For 1.27 mm pitch, this diameter is reduced to approximately 23 mils. Once again, the exact diameter for any given PBGA design should be obtained from Motorola prior to the start of layout so that the motherboard can be designed with an equal diameter.

As will be covered in the next section on escape routing, solder pads internal to the PBGA usually contain integral vias. This configuration, which is pictured in NSMD form in Figure 1a, is sometimes referred to as a "dog–bone" or "dumbbell" pad. The pad in Figure 1a is dimensioned as it would be for use with a 1.27 mm pitch PBGA which contained a 23 mil pad. In this figure, the via, via pad, and via soldermask clearance are shown as recommended but some variation is permissible. The copper always be maintained at 23 mils for most 1.27 mm pitch and 25 mils for most 1.5 mm and 60.0 mil pitch designs and there should always be at least 1 mil of soldermask clearance around that. The soldermask opening in the figure is shown at 31 mils which assumes a soldermask to artwork registration of ±3 mils. This 3 mils is typical in the industry for no cost adder PCB technology, although suppliers may range from ±2 to ±5 or higher mils. At ±2 mils only 6 mils would have to be added to the 23 or 25 mil copper diameter to ensure a 1 mil soldermask clearance at worst case registrational tolerance. It is recommended that the width of the trace attached to NSMD pads should be not much greater than the 8 mils shown in Figure 1a. A trace much wider than this will cause the pad to begin to resemble a mixture between NSMD (on the side of the pad away from the trace) and SMD (where the trace is covered with soldermask). Also, a fillet should always be present where the trace joins the solder pad and no more than one trace should joined to any NSMD solder pad.

Figures 1b and 1c show SMD pads with integral vias in dog–bone and tear drop shapes, respectively. For these SMD pads, the soldermask and copper diameters are simply reversed compared to the NSMD pads. The one mil soldermask clearance necessary for SMD pads becomes a minimum overlap and this overlap may be slightly reduced since any overlap greater than 0 mils will result in no changes to the solder joint geometry. Figure 2d is simply the NSMD pad shown without a via as would be used on external rows.

One other consideration that should be taken into account when determining which solder pad to use is the effect on stand–off height. With NSMD pads, the solder wets down the side of the pad and creates an effectively larger solder pad diameter. For a given diameter this results in an effectively lower stand–off for NSMD pads. This is illustrated in Figure 3, where a larger volume of solder is needed in the NSMD pad case to maintain the same stand–off between as the SMD case.

ESCAPE ROUTING

A perceived drawback of using BGA is the challenge of routing all the required signal, power and ground pins to the system board without increasing printed circuit board (PCB) complexity and therefore cost. Fortunately, this challenge is easily overcome by Motorola with thoughtful package pin assignment and device configuration considerations (pitch, ball count, ball depopulation methods) in conjunction with the choice of solder pad geometry and board technology (number of layers and line/space widths). If signal pin assignments are made too deeply within the BGA matrix, board level escape using conventional eight mil printed circuit board fabrication technology becomes difficult for large matrices. Current PCB technology with eight mil lines and eight mil spaces typically does not incur any additional cost. For this reason Motorola attempts to perform signal pin assignment such that the outer four rows of the PBGA contain all the signals that must be escaped. The Motorola 68356 chip is an example of such a properly assigned BGA footprint that provides users with easy board–level escape with no cost adders for sub–eight mil line and space board technology or internal signal layers. The 68356 is a Signal Processing Communications Engine with integrated functions such as a 68000 based microprocessor, RISC communications core, 24 bit DSP and a PCMCIA controller. The device is housed in a 25 mm PBGA, using a 1.27 mm ball pitch. The balls are in a 19x19 array with the four corner balls depopulated to result in 357 pins.

One of the key features that facilitates the routeability of this package is the location of the power and ground assignments to an 11x11 matrix in the center of the package. Within this inner matrix, the centermost 9x9 pins form a ground bus and the remaining 40 pins encircle that with what is called a power ring. Those power and ground pins do not need to be

escaped as they are dropped straight down using dumbbell or teardrop shaped pads with offset vias to the associated power and ground planes on the circuit board. This leaves the outer four rows containing 236 signal pins around the perimeter of the package that need to be escaped. This package itself has 23 mil diameter solder pads on it and the same solderable surface diameter or only slightly larger is recommended for the PCB. Therefore, using a 23 mil non–solder-mask defined pad in conjunction with a 25 mil diameter via pad a board employing eight mil lines and spaces can be used to easily route these four outer rows using two signal layers. The escape routing of the outer two rows can be achieved on the topside of the PCB without using vias and the third and fourth rows from the outside are escaped by dropping down vias and escaping on the bottomside. This example is illustrated in Appendix C, which shows a representative top and bottomside signal layer routing schematic for the 68356.

A similar package design methodology is used on other devices packaged in BGA such as Fast Static RAM devices that utilize a 7x17 and soon a 9x17 array PBGA, the PowerPC 603™, PowerPC 604™ microprocessors as well as the MPC105 PCI Bridge/Memory Controller for PowerPC™ microprocessors that will be available in a ceramic BGA. The fact that this 119 pin FSRAM package only contains seven rows in one direction further simplifies routing since there are a maximum of three buried rows. As can be seen in Table 3, no matter what geometry (diameter and SMD versus NSMD pad configuration) is chosen for 1.5 mm pitch PBGA devices one eight mil trace can always be routed between two solder pads. Only if NSMD pads are used an eight mil trace can be routed between two pads at 1.27 mm pitch. As can be seen in Table 3, a maximum trace width of six mils would be needed to use an SMD pad.

As PBGA pin count and matrix size increase it may be necessary to make signal assignments on more than just the four outer rows. This would require more that one buried row on each of the outer layers to be escaped on a given PCB layer to maintain a two signal layer board. When this becomes the case, trace size will have to decrease further from the standard eight to six. Table 3 also shows how many traces can be routed between two pads for given line and space technologies down to three and three and all the current standard PBGA pad diameters. For example, when and if it becomes necessary to route two signal traces between NSMD pads at 1.27 mm pitch, five mil trace widths will be necessary to avoid adding extra signal layers. If SMD pads were used those traces could only be three mils wide maximum. This example once again underscores the routing advantages of NSMD pads.

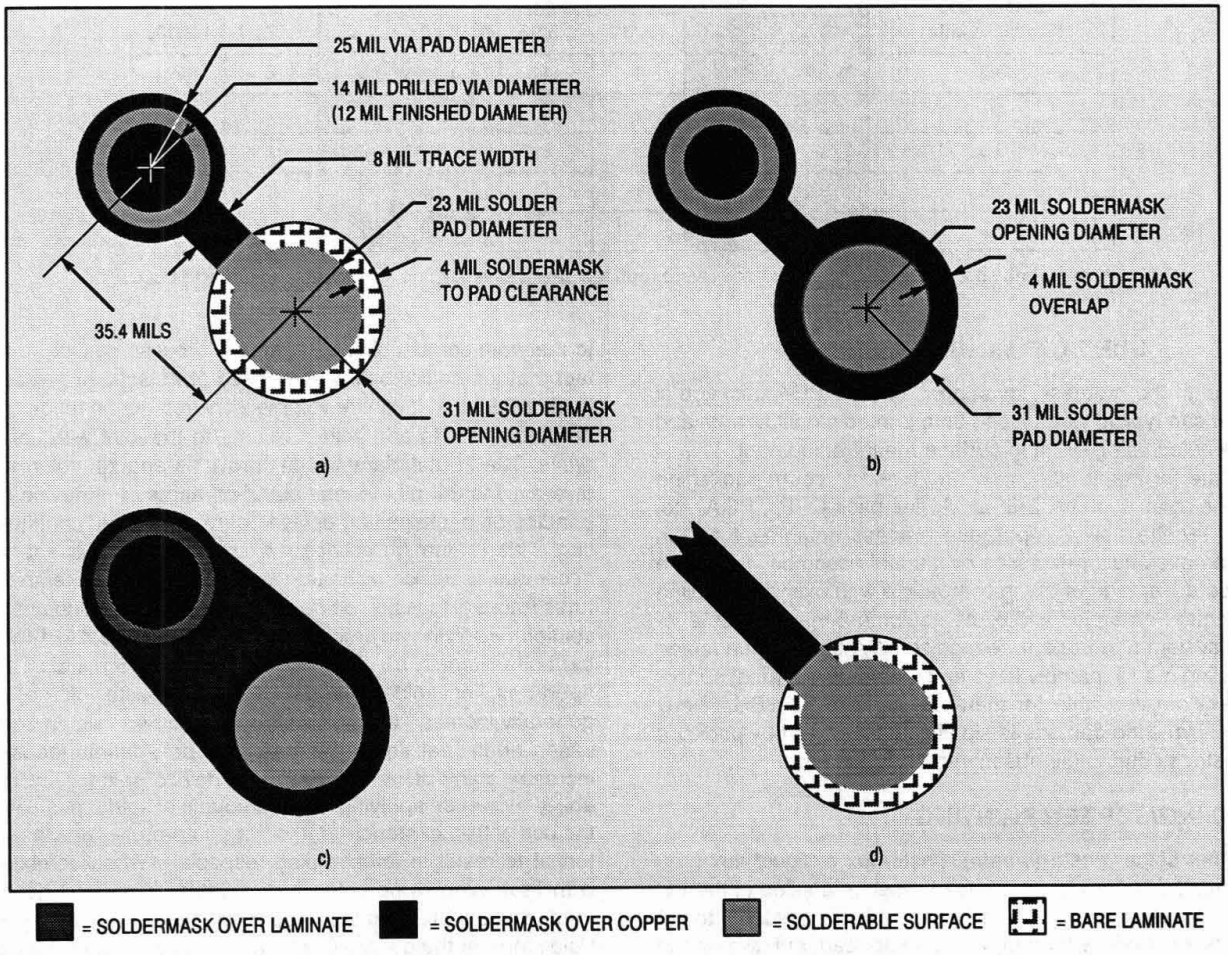

Figure 2. Solder Pad for PBGA: a) recommended NSMD dumbbell pad shown with typical dimensions for most 1.27 mm pitch PBGAs, b) SMD dumbbell pad for most 1.27 mm pitch PBGAs, C) SMD teardrop pad, and d) NSMD pad as would be used for signal routing on the device layer of the motherboard.

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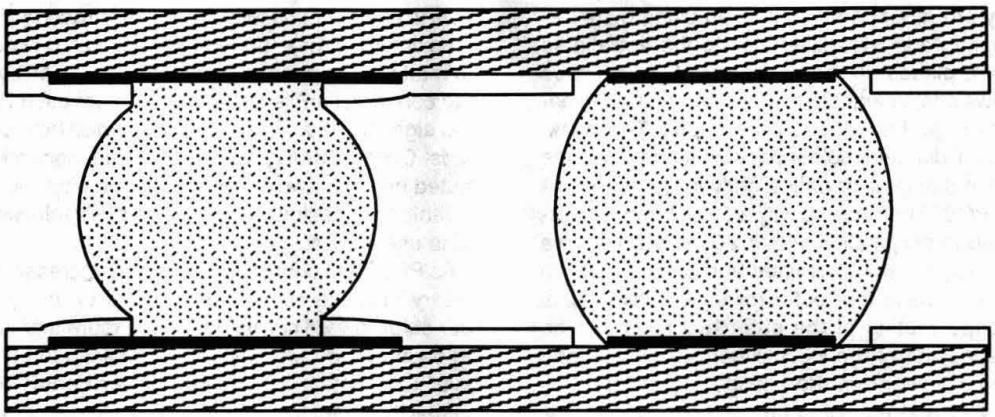

Figure 3. Comparison of PBGA Solder Joints with: a) soldermask-defined pad and b) conventional non-soldermask defined pad. Note the greater volume of solder and greater effective joint diameter for the non-soldermask defined pad to achieve the same stand-off.

Table 3. Number of Escape Traces That Can Be Routed Between PBGA Pads Given Device Pitch, Pad Diameter, and Board Line/Space Widths

Board Technology (Line/Space Widths in Mils)	Number of Escape Traces Routed Between Pads Given Ball Pitch/Pad Diameter (mms/mils). Shaded Columns Represent NSMD Pads.							
	1.5/23	1.5/25	1.5/31	1.5/33	1.27/23	1.5/25	1.27/31	1.27/33
3/3	5	5	4	4	5	3	2	2
4/4	4	3	3	2	2	2	1	1
5/5	3	2	2	2	2	2	1	1
6/6	2	2	1	1	1	1	1	
8/8	1	1	1	1	1	1		

Note: When encountered, fractions of traces were rounded down. Line spacing assumed to be equal to trace width.

SURFACE MOUNT ASSEMBLY

One of the greatest advantages of the PBGA package is that it can typically be placed onto printed circuit boards and assembled using existing surface mount equipment. This is not true for many other new and high pin count packaging technologies such as TAB, DCA, fine pitch QFPs, PGA, etc. Most require new or upgraded process equipment and in some cases new processes or manual assembly. It has the added advantage of being compatible with existing handling systems. Some pick and place equipment may require a vision system updgrade to recognize BGA balls. Open tooled handling media, namely trays and tape and reel (heat seal or C-pak) are available for many of the JEDEC PBGA body sizes. Handling damage is significantly reduced by package robustness due to the absence of fragile leads.

FLUXING/SCREEN PRINTING

Either solder paste (cream), paste flux or liquid flux (i.e., spraying, dispensing, or foaming) must be applied to the PC board solder pads prior to assembly. This is necessary to not only reduce oxides formed on the solder pad, but also on the solder ball. Slight solder ball oxidation may occur during exposure to burn-in, storage, and dry baking in non-inert atmospheres. Typically, the method chosen to apply flux is done to maintain compatibility with current processes. Due to the fact that the solder ball is comprised of eutectic or near-eutectic solder and its entire volume is molten during reflow, it is not necessary to add solder volume to the joint with solder paste. The 30 mil diameter ball provides enough volume to give a 16 to 24 mil average stand-off across the device depending on package and device/board solder pad configuration. This is enough collapse to ensure that no opens will occur due to device or board warpage at elevated temperatures (more discussion on device warpage in the Coplanarity section). Applying an amount of solder paste equal to 14% of the ball volume (i.e., eight mil thick stencil, 25 mil diameter apertures, final solder volume = 1/2 solder paste volume) will generally increase the stand-off by one to two mils. In some cases additional solder volume may be advantageous to increase stand-off and subsequent device solder joint reliability. However, applying larger amounts of solder paste with the use of thicker stencils and/or larger apertures has the potential to result in joint voiding, especially when combined with fast oven ramp rates and volatile fluxes. Voids are formed when flux volatilizes and is entrapped within the joint. Voids form at the bottom (motherboard interface) of the ball, but end up at the joint/package interface due to buoyancy effects. These voids have been shown not to be a reliability risk. Figure 4 shows a pad from an PBGA test board with

eight mils of solder paste screenprinted onto it prior to device placement. Besides screening solder paste and flux, pin transfer and single point dispense of paste flux have also been used successfully on PBGA within Motorola.

DEVICE PLACEMENT

Due to the large pitches involved relative to fine pitch QFPs, pick and place is much simpler and involves lower required machine accuracy. Additionally, due to tight ball pattern to device edge tolerances (better than ± 3 mils) relative to the pitch, placement can be performed off of the body outline. This is the method currently used for much smaller devices in the industry using extremely fast "chip-shooters". Additionally, new equipment with upward looking vision or lasers (dual lasers or better are recommended over a single laser system) that are specifically designed for the ball grid array are widely available. This equipment centers off the ball array itself and can also check for missing balls and in some cases calculate device coplanarity real-time. Sometimes, only balls on the outer or perimeter row are recognized and used for placement. Finally, due to the fact that the PBGA is self-centering in the reflow process, a device can be placed up to 50% off pad and still be expected to align itself. The self-centering feature, which is a result of the surface tension of the molten solder, can be easily observed by placing devices deliberately off pad and reflowing.

REFLOW

Surface mount reflow of the PBGA device is similar to that of leaded devices. The process of reflowing a PBGA is sometimes referred to as a Controlled Chip Carrier Collapse Connection or C5 since the solder ball starts with an approximate height of 25 mils (plus paste if any) and collapses down one to nine mils during reflow due to the weight of the package, solder paste collapse, and wetting of the motherboard pad. PBGA devices can easily be reflowed in IR, convection and mixed heating ovens, as well as with vapor phase. Care must obviously be taken that each solder joint is exposed to the solder liquidus temperature immediately following a flux-dependent high temperature soak period in which the flux is mobile and active. An example of an IR reflow profile (somewhat optimized) obtained by placing thermocouples under two different devices at the middle and corner of a 4.5″ x 7.5″ four layer test board is presented in Figure 5. The main difference in reflowing the PBGA lies in the fact that the joints are heated more from the package and board as opposed to direct air impingement or IR exposure onto the leads. Due to low mass of the PBGA. It is relatively easy to obtain a suitable profile with boards containing a variety of surface mount and through-hole device types along with the PBGA.

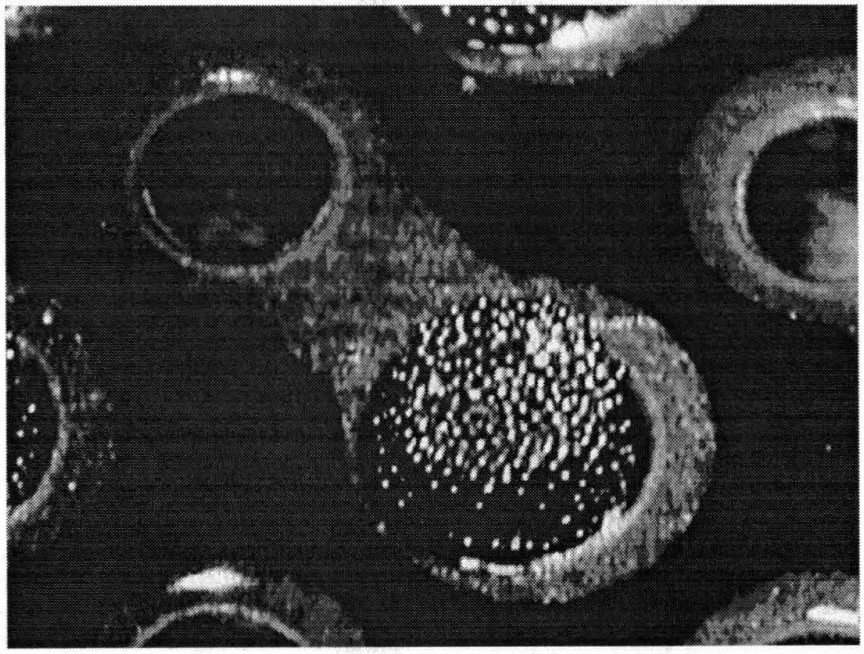

Figure 4. Micrograph of an PBGA Test Board Pad with Eight Mils of Screenprinted Solder Paste (Magnification of Approximately 40X, 45°)

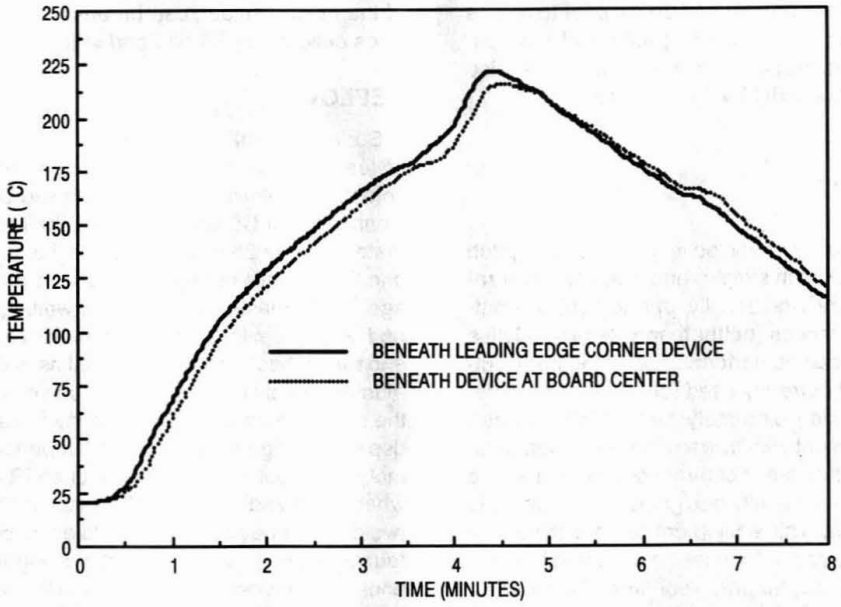

Figure 5. PBGA IR Reflow Profile Obtained by Placing TCs Underneath Devices

Another difference between PBGA and typical leaded devices is in profiling. The profiling thermocouple(s) (TC) must be placed underneath the package and preferably within an actual solder joint. This requires using thinner TC wire (30 or 36 gauge recommended) than may typically be used as to allow the device to solder to the board almost normally with minimal tilt or non-contacting balls. A suggested procedure for making a profile board is to solder the TC bead to a ball under the device. The center ball is recommended since it is likely to exhibit the minimum peak temperature and is therefore the worst-case position for a cold solder joint. It is advantageous to also TC the outermost ball on the leading edge of the device to obtain worst case maximum temperatures. The device is then hand placed onto a prefluxed board footprint, secured with the minimal amount of polyimide (i.e., Kapton™) tape possible and reflowed. The tape is then removed and the board can be used for repeated profiles, assuming the TC did not break free and that the device reflowed somewhat normally onto the board. An alternate way of more securely fastening a TC is to remove a PBGA ball with a solder sucker or wick and to attach the bead to the site using high-temperature solder or thermally conductive epoxy. Drilling a hole through either the top of the device or the bottom of the board for subsequent thermocouple placement can also be done successfully. Also, inserting a TC with thermal grease on the bead under an already mounted package can sometimes yield sufficient results.

8

COPLANARITY

The JEDEC standard for maximum allowable non-coplanarity is currently 0.15 mm (5.91 mils), regardless of package size or pin count. This coplanarity is defined in the standard as the maximum distance from the highest ball to a seating plane formed by the three balls that the package would rest on if placed on a perfectly flat surface. Any lack of PBGA coplanarity is a result of two elements, the warpage of the overmolded substrate and differential substrate pad to-solder ball tip heights. The substrate warpage is typically the major contributor to any lack of coplanarity, while the solder ball heights are relatively uniform. At room temperature, the typical PBGA has a slight upward curvature, such that 225 pin PBGAs with a 27 mm body size have been measured to have a worst case coplanarity of around four mils.

Motorola determines the coplanarity per the JEDEC standard, scanning all the PBGA bumps and determining the relative positions of their tips in space. Software that takes into account the center of mass of the part then determines which three or more balls the device would rest on and the distance from the remaining ball tips to a plane formed by these three seating balls. An automated system, the Model 830B, to do this has been developed by View Engineering and is available now (priced in the mid-$100K range). The system also has the capability to determine the coplanarity to a best fit plane, ball volumes, the absence of balls and the deviation of ball tips from the expected x-y grid. A more expensive and flexible system that also performs printed solder paste height inspection is also available from Synthetic Vision Systems, who are affiliated with View. Among others, RVSI is also a potential equipment supplier.

SOLDER JOINT INSPECTION

One of the perceived drawbacks to using PBGA technology is the fact that, as with any array package, the interior joints are not visible to be readily inspected. Perimeter joints, can be readily inspected. High volume users have presented data showing that the 169 and 225 pin PBGA has one to two orders of magnitude fewer solder-related defects than the 208 PQFP.

X–ray inspection can be used during assembly process development and for failure analysis. Due to the atomic density of the lead in the solder joints, standard resolution real-time x-ray systems may only be useful in determining shorts and missing or double balls, which are readily observable (see Figure 6). More subtle joint assembly defects like voids, total wetting of the motherboard pad (i.e., full or partial opens) and solder splattering/balling require more sophisticated systems to detect. Very costly x-ray laminography systems (i.e., Four Pi Systems) can detect such features,

although their current cost and image acquisition cycle time may be prohibitive for some users. Fein Focus and Imaging Systems International (affiliated with Nicolet) have both developed lower cost systems with the resolution to identify voids and in some cases non-contact failures. Examples imaged with the Fein Focus Model FXS-160.32 and Nicolet Model NXR-1400, are presented in Figures 7 and 8, respectively. Other systems with similar capabilities are available from Lixi, I.R.T. and others.

A pad geometry design change that can allow detection of non-contact failures or opens involves modifying the motherboard pad footprint. A tab or ear is placed in the soldermask defined pad as in Figure 9. During reflow, solder fills the pad and is readily observed by using even inexpensive x-ray systems. If solder plated or HASL motherboards are used or solder paste is screened on prior to reflow, this ear would already be filled with some solder. In these cases, the x-ray would have to be of sufficient resolution to distinguish between an ear filled by solder from the ball and one already filled by plated, HASL'd or stenciled on solder.

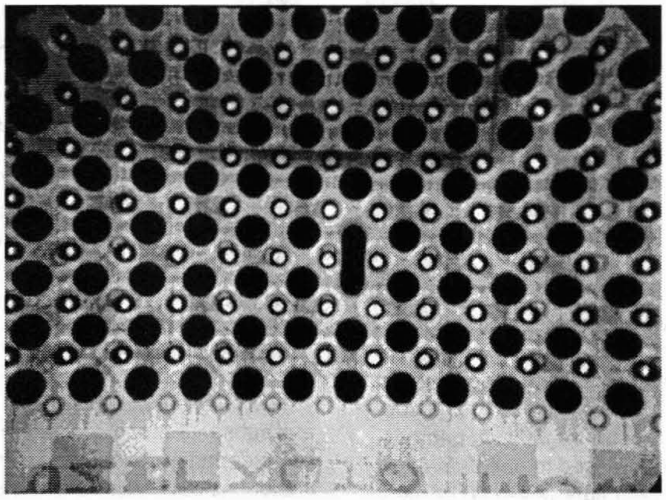

Figure 6. X-ray Micrograph of a Mounted PBGA Showing Solder Shorting

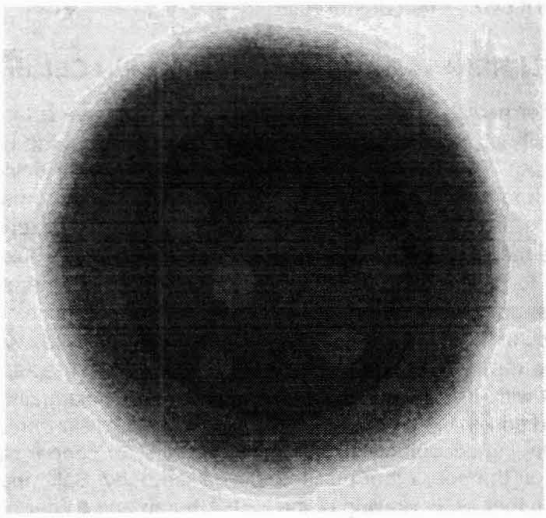

Figure 7. X-ray Micrograph of a Mounted PBGA Showing Voiding in the Solder Joints

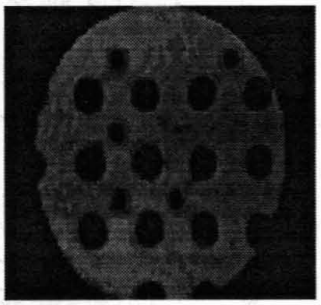

Figure 8. X-ray Micrograph of a Mounted PBGA Showing Solder Splattering/Balling

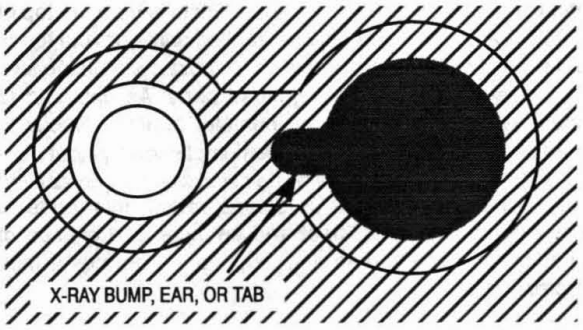

Figure 9. PBGA Pad with Bump to Facilitate X-ray Inspection

REWORK AND REPAIR

The main point that should be stressed when discussing PBGA rework is that since the assembly process gives so much better yields than high pin count, fine pitch leaded devices, that the frequency of rework is greatly reduced. Unfortunately, when one joint is defective the entire package must be replaced since there is no touchup. However, methods and equipment do exist to successfully remove and replace PBGA devices that are found to have assembly or device-related defects.

DEVICE REMOVAL

Typically, PBGA device removal involves simply heating above the liquidus temperature of the solder. As opposed to the original surface mount assembly process, no special considerations (assuming the device will be scrapped) need to be taken with respect to ramp-up rates and time over solidus as long as all joints are molten upon device lifting. It may be beneficial to apply a liquid flux beneath the device prior to heating and removal. This flux will facilitate uniform heating and reduce device and board oxidation for subsequent soldering processes. Joints which were not quite molten will appear as "candy kisses" on the board and PBGA after removal. This is an indication that the device was removed at the earliest possible time, such that the board is being subjected to a minimal amount of temperature-induced damage. If the assembled board has been exposed to out of dry-pack conditions for an extended period of time (24 to 96 or more hours depending on PBGA configuration and ambient conditions) and removal is performed, "popcorning" or die attach delamination may occur. To avoid this, the entire assembly must be baked at 125°C for 12 hours. Since the saturation/bake-out curves for PBGA are quite steep, baking for a half to two-thirds of this time will go a long way in preventing popcorning as long as care is taken not to use an excessive ramp-up rate (i.e., > 3°C/min) or maximum temperature (≈ 240 – 250°C).

If other known good PBGAs (or other surface mount devices) are proximate to the device being removed, care must be taken not to overheat them and cause collateral delamination damage. Studies performed by an equipment division of Motorola who are a high volume PBGA user on devices which have body sizes of 19 mm or less indicate that neighboring devices should not exceed 185°C to prevent popcorn at any reasonable saturation level. Also, to minimize temperatures on adjacent devices the nozzle on the rework station should be maintained around 100 mils from the top of the PBGA and heating should be applied only from the top of the device. Additionally, the size of the nozzle should be less than or equal to the device molded body. As opposed to leaded devices which require perimeter heating directly to the leads, reflow of the PBGA is accomplished by heat conducting through the body of the device. Heat can be applied from the bottom also, but as stated earlier, this leads to greater spreading of the heat and an increased chance of damaging or partially reflowing neighboring devices if they are present.

EQUIPMENT

The cost of rework equipment for PBGA, as with leaded devices, varies greatly with features. Some of the features that may be useful to include in rework stations for PBGA are as follows: selectable top and/or bottom heating, selectable IR and/or forced air heating, nitrogen capability, auto-profiling capabilities, split-prism optics manual placement, automated vision placement, and a device removal head or vacuum tool. For the production rework of its smaller PBGA devices, Motorola uses a simple, inexpensive (< $4K) portable rework station made by A.P.E that provides top heating only and has no device placement capabilities. Other PBGA users are known to use the same industry-standard equipment they use for their leaded device rework made by Conceptronics, S.R.T., Air-Vac, Manix, and many others. Prices for these latter machines are ≈ $40K and up without post-removal vision placement capabilities. Of course, special PBGA-specific nozzles need to be bought or made for each of these pieces of equipment. Due to their position as a supplier of rework equipment to Motorola, A.P.E. has nozzles that correspond to most current PBGA body sizes. As PBGA popularity increases, similar nozzles and related tooling will undoubtedly be available from all rework equipment suppliers.

PRE- AND POST-REWORK BOARD CONSIDERATIONS

The principal board consideration during device removal and subsequent replacement lies in the fact that the pad may be soldermask defined and as such damage can occur if the soldermask is subjected to extreme heat and/or has poor initial adhesion to the copper pad. This situation is magnified if the board technology is soldermask over solder (SMOS) which is not recommended. If there are offset vias integral to the tear-drop shaped PBGA pad and they are not filled or tented with soldermask, the web between the usable pad and via pad will be subjected to lifting due to its potential sub 10 mil width. Also, as with reworking all SMT device types, the motherboard itself is subject to other modes of failure such as blistering, delamination and copper/PCB adhesion lifting if overheated or subjected to repeated heat cycles.

SITE PREPARATION AND DEVICE REPLACEMENT

After device removal the pads will typically have a large quantity of solder remaining (approximately half of the ball volume). This solder needs to be removed to allow device placement and facilitate self aligning of the replacement device. Removal can be performed with a solder sucker or more manually with a solder wick. The site should be fluxed prior to replacement with another PBGA device. Generally, solder paste cannot be reapplied due to the interference of a stencil and accompanying fixturing with other devices close to the removal/replacement site. Short of machine replacement with vision, the new device can be placed manually. A board design consideration to aid in this can be a silk-screen (assuming acceptable registration tolerance) or copper pattern on the board that outlines the device body. Split prism optics that allow viewing of the PBGA bump and solder pad patterns simultaneously for alignment prior to device placement are inexpensive and have been used very successfully. The profile that is used to reflow the device should match the initial reflow profile as much as possible, although it is subject to the constraints previously discussed with regard to damaging neighboring devices.

DEVICE REBUMPING TEST AND POSSIBLE REUSE AFTER REMOVAL

Much discussion has taken place within the industry on the subject of rebumping and reusing BGAs which have been removed from an assembly for a variety of reasons. After a BGA is de–soldered or removed from a motherboard with heat, the resulting solder balls are typically non–uniform at best and in some cases the pad is completely void of solder. Methods, supplies, and a variety of equipment currently exist to successfully remove the remaining solder residue from the pads and replace the solder with new preform spheres to make the device suitable for reuse. Motorola does, in fact, rebump packages that are returned from the field to allow them to be tested. However, Motorola does not recommend this process be used to allow re–assembly of the BGA into actual product. BGAs that are shipped by Motorola are typically qualified to withstand from two to four reflows depending on the intended application and the specific Motorola product group involved. That is to say, the packaged devices are subjected to from two to four reflows of preconditioning prior to any reliability stressing as part of qualification testing. When a BGA is removed from a board, rebumped, and reflowed back onto a board it has potentially seen from a minimum of four up to six reflows and may have exceeded the number for which it was qualified. Additionally, there is no traceability to discern a BGA that has been rebumped versus one that has not. Any questions in this area should be directed to the reliability and quality assurance group dealing with the particular BGA in question.

SOLDER JOINT RELIABILITY

The decreased compliance of PBGA solder joints as compared to conventional leads has raised concern about its suitability for certain applications where environments are severe (i.e., automotive), required lifetime is long (i.e., telecommunications) or device power is substantial (i.e., microprocessors). This lead compliance is important when a mounted PBGA is subjected to any thermal excursions since the joint typically absorbs the relative device/board expansion and contraction caused by thermal mismatch or temperature gradients. The materials that are used to construct the PBGA, as outlined in the earlier section on package construction, have thermal expansion coefficients that for the most part match that of the FR4/glass PCB to which they are typically mounted. The largest exception to this, for materials which are structurally significant to the package, is the silicon die. It has an expansion coefficient of 2.6 ppm/°C compared to 15 to 17 ppm/°C for other structural materials (see Table 2).

THERMAL CYCLING METHODOLOGY

Assembly-level accelerated thermal cycling is generally used to compare the performance of PBGAs relative to conventional leaded as well as other technologies. It is also used to detect any latent process defects that may be manifested in the first few cycles and to determine a wear-out (i.e., fatigue) failure distribution for the given device and environment. These test conditions are typically accelerated in cycle time as well as temperature extremes when compared to the actual application use environment. This is necessary since, by definition, an accelerated test is meant to decrease time to failure so that the failure characteristics and mechanisms may be known before the prohibitive amount of time it would take for something to fail in an actual application. Temperature extremes chosen could be the worst case expected application conditions or an expansion of that excursion to further accelerate the test. In either situation, the test will be accelerated because the cycle times chosen will probably be less than the application cycle time. A field cycle length depends on the particular application. For example, desktops personal computers are usually considered to cycle one or two times per day, while laptops cycle three to five or more cycles per day. A network server or high-end workstation may only cycle once every month on average to basically never.

The sample size in thermal cycling is generally much smaller than the ultimate population in the field. Therefore, accelerated reliability test results must be statistically analyzed and extrapolated to determine application cycles to fail a small percentage of the population. Also, these differences between cycle duration, form of excitation (i.e., internal device power versus ambient temperature swings) and temperature extremes between the accelerated test and the application field environment may need to be resolved before accurate predictions of field solder joint reliability can be made. These three differences result in a different failure distribution, namely the scale (time to 50% device failure) of that distribution, determined from accelerated testing than would be obtained by cycling to the actual application conditions. Everything involved with accounting for and resolving those differences is beyond the scope of this document, but some basic discussion to that end is included.

TESTING CONFIGURATION

Thermal cycling involves assembling PBGA devices using standard production processes to test boards that approximate the actual application board configuration in thickness, number of layers and pad geometry/layout. Some way of determining when a PBGA has failed must be used in order to gather failure data. The standard way is to use daisy-chain devices where adjacent pads are simply shorted on the PBGA substrate. Motorola has daisy-chain versions of all the PBGA designs that are currently available expressly for this purpose as well as for process studies. Traces directly connecting adjacent pads on the test board complete the chain such that there are one or more independent nets that go through all joints. An entire device can be covered with one net or several nets can be used to determine, for example, how rows fail relative to one another. Figure 10 provides an example of a routing scheme that was used on the 361 pin PBGA with 1.27 mm pitch and a 25 mm body. The rows on the device were divided into four sets: outer, middle, die perimeter, and inner.

The continuity of each net or device is measured either in-situ or every few (50 to 100 recommended) cycles to determine if it has failed. Monitoring in-situ is the preferred method and specialized equipment can be used to automate or simplify the monitoring process. Event detectors made by Anatech are especially made for monitoring solder joints, logging the data to a computer file and calculating the statistical failure parameters (discussed later) in real time. Data loggers with resistance capability may also be used.

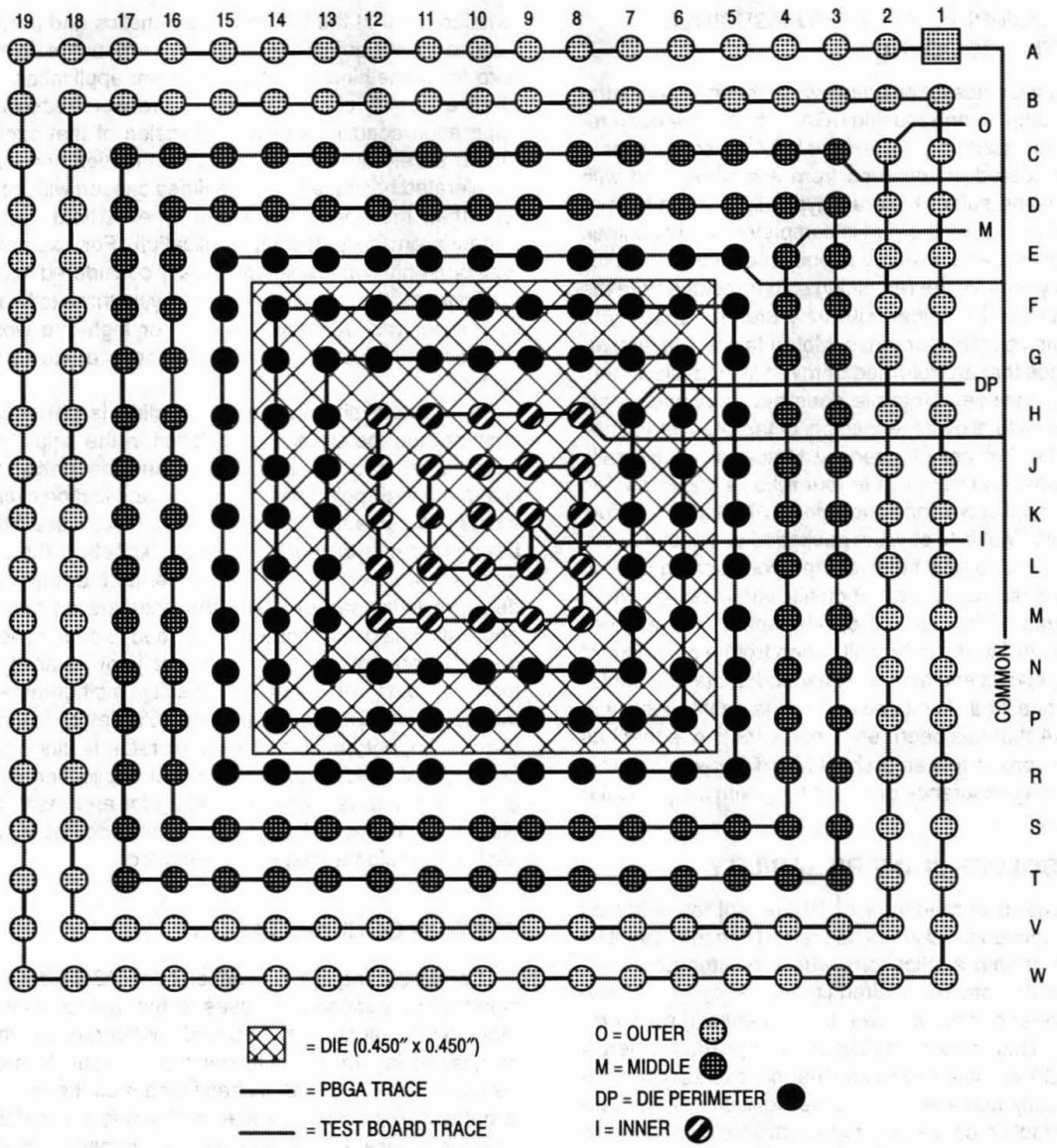
19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
A B C D E F G H J K L M N P R S T V W
O
M
DP
I
COMMON
= DIE (0.450″ x 0.450″)
= PBGA TRACE
= TEST BOARD TRACE
O = OUTER
M = MIDDLE
DP = DIE PERIMETER
I = INNER

Figure 10. Example of an PBGA/Test Board Daisy-Chain Configuration to Allow Monitoring of Individual Groups of Rows (361 Pin, 19 x 19 Array, 1.27 mm Pitch, Device Bottom View)

Motorola uses two basic thermal cycle conditions. The most severe is a one hour – 40 to 125°C cycle that is mainly used to determine suitability to automotive under the hood applications. The other, more commonly used cycle is tyically 20 minutes in duration and goes from 0 to 100°C. The 20 minutes is made up of five minute ramps where possible and five minute dwell times at each temperature. The ramp time is limited by chamber heating and cooling capacity and sometimes has to be extended to allow the boards to reach the prescribed temperature. It is very important to know what temperature the boards and devices are actually experiencing as opposed to what was programmed or what the chamber air temperature is. This is accomplished through profiling the boards directly by placing thermocouples beneath several devices under which temperatures are expected to show differences. The air and board temperatures for a typical 0 to 100°C profile are shown in Figure 11. The ramp times for this profile had to be extended beyond five minutes to achieve the prescribed endpoint temperatures such that the total cycle time was 25 minutes. Examples of devices that would be expected to see the closest and furthest temperatures from the ambient air are the corner device on the board the most upstream of chamber airflow versus the middle device on the center board, respectively. To minimize these board to board thermal gradients, it is advisable to place boards parallel to the prevailing chamber air flow direction.

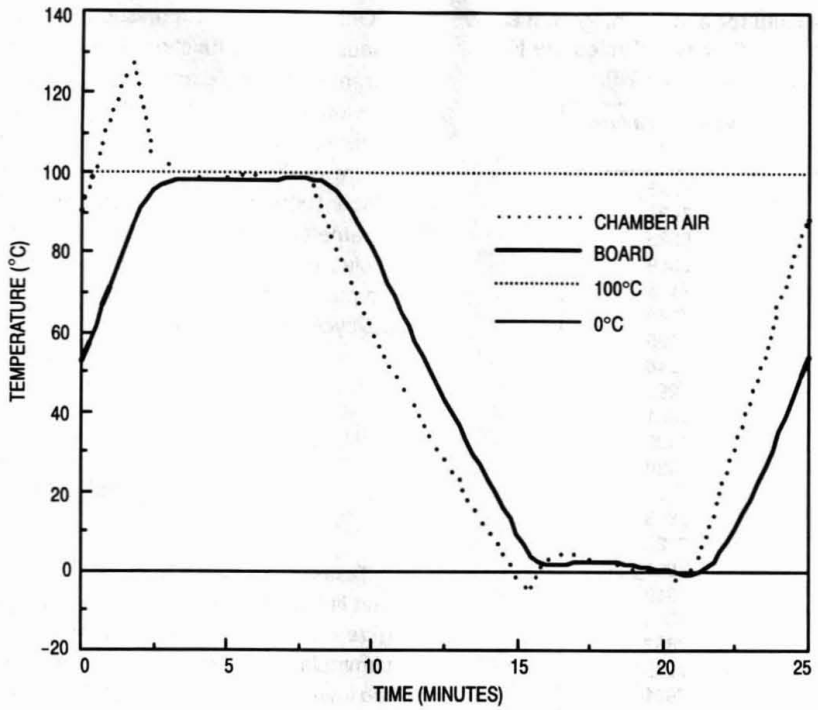

Figure 11. Typical 0 to 100°C Thermal Cycling Profile Showing the Difference Between Chamber Air Temperature and Temperature Seen by the Test Board

FAILURE DATA STATISTICAL ANALYSIS

After the thermal cycling has resulted in a substantial number of PBGA device failures (typically at least 50%, greater than 75% is preferred), the data can be fit to a statistical failure distribution. The two most commonly used for fatigue are the Weibull and the Log Normal distributions. The reliability function that describes failure in the Weibull distribution is as follows:

$$R(t) = e^{-\left(\frac{t}{\alpha}\right)^{\beta}} \quad (1)$$

In the above equation R is the fraction of devices that have survived and α and β are called the scale and shape parameters, respectively. The scale parameter, α, corresponds to the time at which 63.2% of all devices fail. Time, t, is usually expressed in cycles.

After testing is complete the data consists of a number of data pairs that is equal to the number of devices that failed. Each pair will contain the failure number and the cycles to failure for that specific device. An example of some actual data for a 225 pin PBGA that was subjected to 30 minute thermal cycles from 0 to 100°C is presented in Table 4 on the next page. In this example the sample size was 28 and cycling continued until all devices failed (100% device failure or R = 0). Larger sample sizes such as these on the order of 30 or greater are recommended. The α and β are determined by doing a best fit curve of equation (1). Statistical software packages with Weibull capability can automate the process of determining α and β. One powerful tool to do this is WeibullSmith™ (written by Fulton's Findings) and another is the software that comes with the previously mentioned Anatech event detectors. The Anatech software presents the data in terms of cycles to 50% failure as opposed to 63.2% (α). For the case of the data in Table 4, $N_{50\%}$ was determined to be 7737, α was determined to be 7958 cycles and β, which is dimensionless, was 13.0.

The data can then be plotted on Weibull axes as it is in Figure 12. Note that also plotted on this graph is the 95% lower confidence limit of the data. It is also important to note that each set of data has a correlation coefficient or a measure of its goodness of fit to the particular failure distribution. In this case, the correlation coefficient (R^2 on the graph) was an adequate 0.965.

The Log Normal distribution is similar to the Normal distribution but it operates on the logarithm of the failure data. In other words, if the distribution of the log of the cycles to failure data is normal, the data is Log Normally distributed. The reliability function for the Log Normal distribution cannot be written in closed form and is closely approximated by the following:

$$R(t) = \frac{1}{2}\left\{1 - \text{erf}\left(\frac{\ln(t) - \ln(N_{50\%})}{\sqrt{2}\sigma}\right)\right\} \quad (2)$$

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Table 4. Sample Failure Data for a 225 Pin, 27 mm Body PBGA Cycled from 0 to 100°C at Two Cycles per Hour (Starting Sample Size, n = 28).

Failure Number	Cycles to Failure (t)
1	6253
2	6438
3	6536
4	6869
5	7105
6	7148
7	7195
8	7246
9	7291
10	7361
11	7405
12	7430
13	7521
14	7698
15	7720
16	7807
17	7819
18	7886
19	7887
20	7945
21	7991
22	8163
23	8197
24	8272
25	8497
26	8772
27	8874
28	9143

Once again, t is expressed in cycles and erf refers to the (Gaussian) error function. The Log Normal scale and shape parameters, $N_{50\%}$ and σ, may be calculated as mentioned previously using a best fit procedure or preferably with a statistical software package. $N_{50\%}$ is simply the mean time to failure or the time at which 50% of the sample has failed. Since 100% of the samples have failed, the Log Normal parameters can be calculated directly as follows from the cycles to failure data, with n being the sample size (Log Normal standard deviation is actually calculated on the log of the cycles to failure data):

$$N_{50\%} = \frac{\Sigma t_i}{n} \quad (3)$$

and

$$\sigma = \sqrt{\frac{\Sigma (t_i - N_{50\%})^2}{n-1}} \quad (4)$$

Taking the same 225 pin PBGA failure data from Table 4 and fitting it to the Log Normal distribution reliability function gives an $N_{50\%}$ of 7628 cycles and a σ of 0.042. The cummulative failure 95% plot is represented in Figure 13 with the lower confidence interval shown once again. Note that for this data set the correlation coefficient (R^2) was 0.985 in the Log Normal distribution, which is better than was achieved with the Weibull distribution. Which failure distribution is used ultimately depends on how it fits the majority of the collected data as well as the availability of statistical software and familiarity with a particular distribution.

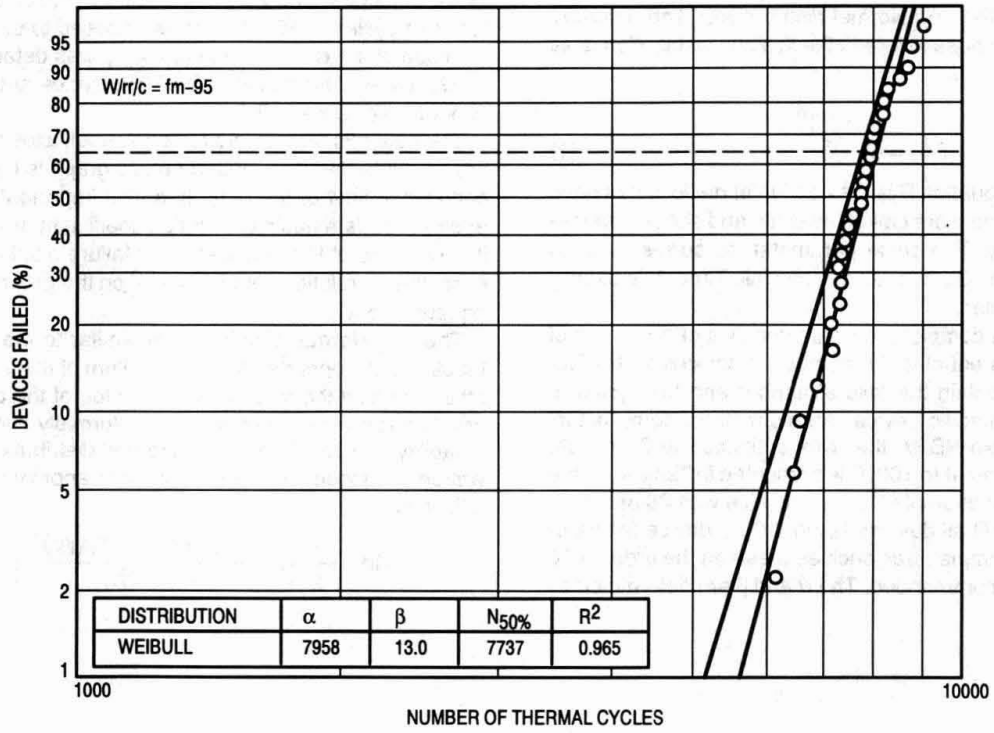

Figure 12. Weibull Failure Distribution of the Data in Table 4

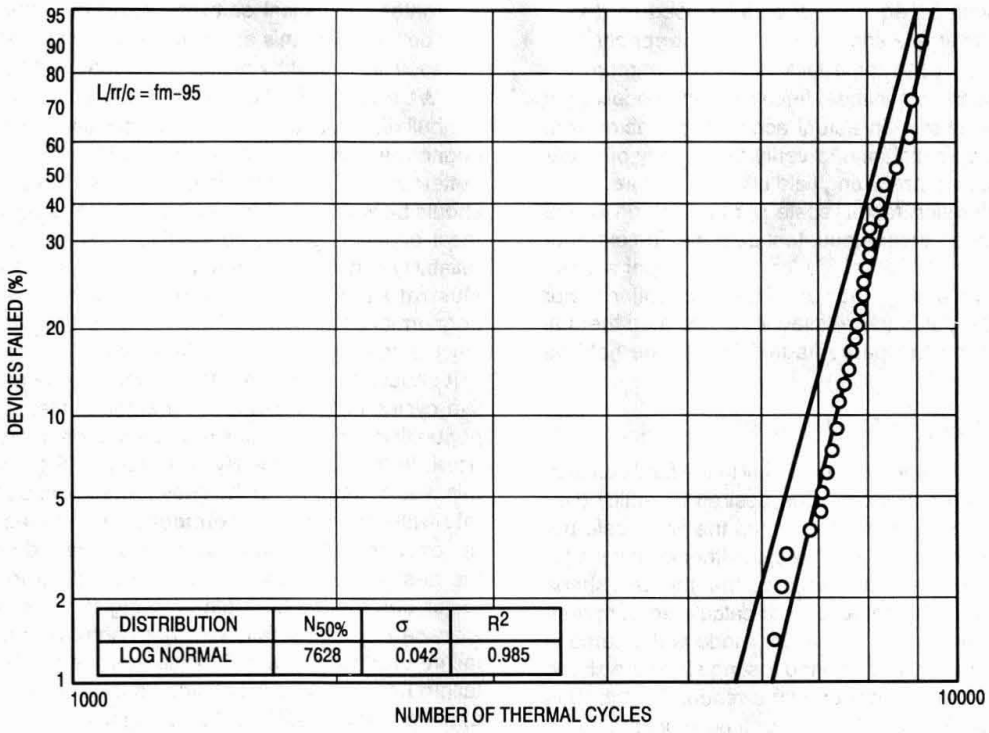

Figure 13. Log Normal Failure Distribution of the Data in Table 4

Extrapolation to Application Failure Data

As mentioned previously, PBGA accelerated reliability data and field failure data are usually different in three ways: 1) the sample size is much smaller in accelerated testing, 2) the cycle duration is greater in the actual application and 3) typical thermal excursions are usually less severe in the application. Additionally, the isothermal temperature excursions associated with thermal cycling are somewhat different than the thermal gradients found in the mounted PBGA in an actual application. The difference in the size of the population (sample size) can generally be accounted for by extrapolating data from the previously mentioned statistical distributions. Due to the highly nonlinear dependence of PBGA solder joint fatigue life on cycle time and severity, these differences generally cannot be accounted for as simply. Typically, nonlinear finite element models employing the viscoplastic temperature–dependent behavior of the solder as it undergoes creep and plastic deformation must be used. The finite element model is provided with accelerated testing and field temperature distributions for a cycle and the solder joint stress and inelastic strain or damage is determined. Crack growth and S–N correlations may then be used to determine the joint and subsequently the device life. The ratio formed by dividing the percentage of the population failing ($N_{xx\%}$) in the field (f) by the accelerated thermal cycling (ATC) testing cycles to failure is called the acceleration factor (AF):

$$AF = \frac{N_{xx\%,f}}{N_{xx\%,ATC}} \quad (5)$$

It has been proposed that a joint's, and therefore the entire package's, mean cycles to failure or $N_{50\%}$ follow a power law of the inelastic strain range seen by a joint during a thermal or application cycle (assuming inelastic strain is dominated by creep as opposed to plastic deformation):

$$N_{50\%} \propto (\Delta\varepsilon_{joint,inelastic})^n \quad (6)$$

The strain exponent (n) has been proposed by Solomon (see reference to Solomon in last section) to be approximately –2 for eutectic or near–eutectic solder. For long cycle dwell times, as would be found in typical field applications, this creep strain range is proportional to the cycle temperature range (ΔT). This temperature range raised to the strain exponent can then also be said to be proportional to the cycles to failure. For accelerated reliability testing, this is not the case unless the dwell times are sufficiently long to allow complete stress relaxation in the joint as stresses are converted to creep deformation. Substituting ΔT for $\Delta\varepsilon$ in equation (6) for both field and accelerated testing, substituting the resulting equations into equation (5) and simplifying results yields an equation of the form:

$$AF \approx \left(\frac{\Delta T_f}{\Delta T_{ATC}}\right)^{-2} \quad (7)$$

This equation has been further modified in an attempt to account for the field and ATC cyclic frequencies and maximum temperature seen during a cycle:

$$AF \approx \left(\frac{\Delta T_f}{\Delta T_{ATC}}\right)^{-1.9} \left(\frac{f_f}{f_{ATC}}\right)^{1/3} \exp\left(1414\left(\frac{1}{T_{max,f}} - \frac{1}{T_{max,ATC}}\right)\right) \quad (8)$$

Where: f, ATC = Subscripts to indicate field and accelerated thermal cycling testing.

ΔT = Difference in minimum and maximum cyclic extremes (°C).

f = Cyclic frequency (Note: For purposes of the above equation, f_f minimum is 6 cycles per day).

T_{max} = Maximum temperature during a cycle (°K).

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Once again, such an equation should be used as a very rough first–order estimate and could give very erroneous results, but it may be used for a lack of any other more in–depth analysis (such as nonlinear finite element modeling). It is also prudent to obtain an actual acceleration factor from two different testing conditions to verify the validity of equation 8 before its use in predicting field cycles to failure.

After the acceleration factor, scale parameter and shape parameter have been determined, test data may be extrapolated to determine cycles to failure for a much larger sample size such as a population in the field. The acceleration factor is multiplied by the percentage failed in accelerated thermal cycling to determine the percentage failed in the field as follows:

$$N_{xx\%,f} = AF \bullet N_{xx\%,ATC} \quad (9)$$

Then the time for any percentage to fail in the field can simply be calculated by substituting the desired reliability (i.e., fraction failed), the shape parameter and the field scale parameter and solving for time (in cycles) in either equations (1) or (2) above. It also has to be assumed that the field shape parameter (β or σ) is the same as that calculated from testing. This then assumes that the failure mode is the same in both the field and during accelerated testing since the shape parameter is also an indicator of failure mode. For the Weibull distribution, solving equation (1) for time yields:

$$t = \alpha \bullet \{-1n\,[R(t)]\}^{(1/\beta)} \quad (10)$$

It must be determined to what reliability cycles to failure are desired. It is commonly desirable to know the time at which 1,000 devices per million (ppm) would be predicted to fail. This 1,000 ppm corresponds to an R of 0.999 (R = 1 – 1,000/1,000,000=1 – fraction failed). Substituting this R as well as a previously calculated value of α ($N_{63.2\%}$) and known β into equation (10) yields a time to fail 1,000 ppm or $N_{0.1\%}$ of 4685 cycles. Since the Lognormal equation (2) cannot readily be solved for time due to its complexity, an iterative process (with the aid of a spreadsheet that has the erf function) can be performed to determine the $N_{0.1\%}$. Alternately, statistical software with Lognormal capabilities may be used. For this example it was determined to be 5659 cycles. This is slightly higher than what was predicted using the Weibull distribution. This is usually the case, as the Weibull distribution is a more conservative predictor than the Lognormal. However, the Lognormal traditionally results in a better correlation coefficient. The distribution that is used should be whatever the user is most comfortable and has the most experience or history using. Predictions to any given reliability can likewise be made from the two distributions. To illustrate this and to further compare the Weibull and Lognormal distributions, Table 5 shows a range of reliabilities calculated from using the data in Table 4.

It should be noted that to extrapolate the most conservative cycles to failure values for small percentages of a total population, data to a desired confidence interval should be used. In the two reliability plots above (Figures 12 and 13) this would mean using the lines forming the 90% confidence interval (or whatever confidence level was desired) as opposed the scale and shape parameters determined from the best fit of the data. It is only practical to consider the lower confidence limit since using the upper limit of the expected cycles to failure is not useful or prudent for field failure prediction. Table 6 compares the predicted cycles to failure from the best fit line versus those predicted using the upper and lower 95% confidence limits.

PBGA Thermal Cycling Data

Motorola has thermal cycled several configurations of 72, 119, 225, and 361 pin PBGAs while testing of other configurations is ongoing. Additionally, several other companies have thermal cycling testing either underway or completed. Two of those companies are AT&T and Compaq and their published data, along with a sampling of Motorola data are presented in Table 7. Also listed are Motorola data on two leaded devices, the 68 PLCC and the 208 PQFP, both with copper leadframes. The Motorola PBGA data shown shaded in Table 7 represents data that was used as example data for thermal cycling statistics in the previous section.

Table 5. 225 Pin PBGA Reliability Predictions Using the Weibull and Log Normal Distributions (0 to 100°C Thermal Cycling, 20 Minute Cycle)

Reliability (R)	Percentage Failed (%)	Devices Failed Per Million	Predicted Cycles to Failure Using:	
			Weibull	Log Normal
0.999999	0.0001	1	2758	4794
0.99999	0.001	10	3291	5035
0.9999	0.01	100	3926	5317
0.999	0.1	1000	4685	5659
0.99	1.0	10,000	5592	6098
0.9	10.0	100,000	6696	6739
0.84	16.0	160,000	6960	6925
0.5	50.0	500,000	7737	7628
0.368	63.2	632,121	7958	7878

Table 6. Reliability Predictions Using the Lower 95% Confidence Limits for the Weibull and Lognormal Distributions

	Predicted $N_{0.1\%}$ (in Cycles) Using:	
	Weibull	Log Normal
From Best Fit Line	4685	5659
95% Lower Confidence Limit	4121	5239

Table 7. PBGA Accelerated Thermal Cycling Data from Motorola and Others(with Comparisons to PQFP/PLCC)

Company	Device (Die in mils)	Cycle (°C)	$N_{0.1\%}$	$N_{1\%}$	$N_{50\%}$	α ($N_{63\%}$)	β	Source
Motorola	72 PBGA (270x270)	– 40 to 125, 1cph	1058	1363	2171	2260	9.1	Internal
Motorola	72 PBGA (270x270)	0 to 100, 3cph	3013	4034	6895	7222	7.9	Internal
Motorola	119 PBGA (280x437)	0 to 100, 2cph	4459	5848	9683	10113	8.4	Internal
Motorola	225 PBGA (400x400)	0 to 100, 2cph	4685	5592	7737	7958	13.0	Internal
Motorola	361 PBGA (450x450)	0 to 100, 2cph	6319	7804	11495	11886	10.9	Internal
Motorola	68 **PLCC**, Cu Leadframe	– 40 to 125, 1cph	904	1818	6561	7332	3.3	Internal
Motorola	208 **PQFP**, Cu Leadframe	– 40 to 125, 1cph	639	1553	7912	9111	2.6	Internal
AT&T	169 PBGA (364x359)	0 to 100, 2cph	2103	2741	4459	4651	8.7	Semi/HDP-10/93
AT&T	225 PBGA (389x398)	0 to 100, 2cph	1412	1993	3749	3960	6.7	Semi/HDP-10/93
Compaq	72 PBGA (270x270)	– 25 to 100, 2cph	1734	2194	3379	3508	9.8	1993 IEPS
Compaq	165 PBGA (437x437)	– 25 to 100, 2cph	1010	1309	2106	2195	8.9	1993 IEPS
Compaq	225 PBGA (389x398)	– 25 to 100, 2cph	1252	1664	2807	2937	8.1	1993 IEPS

Comparing the cycles to 50% failure for the PBGA and leaded devices reveals that the PQFP and PLCC tend to last longer. For example, $N_{50\%}$ for the 68 PLCC is a factor of three greater (6561 versus 2171 cycles) than the 72 PBGA for identical cycling conditions. But, it can be seen in Table 7 that the β's associated with leaded device data are significantly lower, on average, than those of the PBGA. This greater spread in the leaded device data can be attributed to a greater variation in the factors that influence solder joint reliability such as solder volume and device coplanarity. This β disparity means that there is a greater spread in the leaded data and when subsequent extrapolations are made down to $N_{0.1\%}$ or lower, they tend to become comparable to the same estimates for PBGA. Extrapolating $N_{0.1\%}$ for the 72 PBGA and 68 PLCC mentioned above, yields 1058 and 904 cycles, respectively. The same thing can be done when comparing the 225 PBGA to the 208 PQFP although the thermal cycle on the leaded device was the more severe – 40 to 125°C. The 208 PQFP had a higher α and $N_{50\%}$, but when $N_{0.1\%}$'s are compared there is a much different situation (4685 cycles PBGA versus 639 cycles PQFP).

Another observation from Motorola testing is that rows under and proximate to the die perimeter tend to fail first. This can be seen in Figure 14 which compares the outer, die perimeter, middle, and inner rows of the standard 361 pin PBGA. This gets back to the previously mentioned mismatch between silicon and the other PBGA and FR4 PCB materials. To further prove this point, tests on 72 pin packages without die went for many more cycles without failure than identical packages with die. Another conclusion drawn from Motorola testing is that there is a relative cycle basis acceleration factor of about 3.5 between 0 to 100°C and – 40 to 125°C PBGA testing. This actually results in no relative acceleration on a time basis since the more severe cycle is approximately three times longer than the 0 to 100°C cycle. Also observed from the testing was that underfill (although it causes the devices to be unreworkable) can give up to a 4X increase in cycles to failure and that increased device standoff (obtained through using larger diameter solder balls) improves the fatigue life as would be expected.

Failure Analysis

Analysis of devices that have failed in accelerated thermal cycling or in an application can provide extremely useful information with regard to determining the failure characteristics and mode. Generally, the failure analysis of PBGA devices consists of resistance probing to locate specific failed joints when possible, cross-sectioning and also die penetrant analysis of fractures. Probing of individual joints (actually joint pairs) usually only pertains to daisy-chain devices on test boards that have vias integral to each solder pad which drop down to the bottomside of the board and can be probed. Knowing the schematic of the daisy-chain net, specific via pairs can be probed until a failing pair with atypical or infinite resistance is found.

Care must be taken when preparing cross-sections of PBGAs with solder joint failures. Vibrations and flexure caused by the cutting of a failed device out of a test board, if not performed properly, can further propagate or initiate fractures. High speed diamond blades, abrasive wheels or routers are recommended over band saws. Once the device is removed, setting of the potting compound should optimally take place in a vacuum. Slower curing potting epoxies are also usually better than the quick setting variety to ensure that the PBGA is completely underfilled. After grinding, polishing and etching to reveal the solder structure, fractures

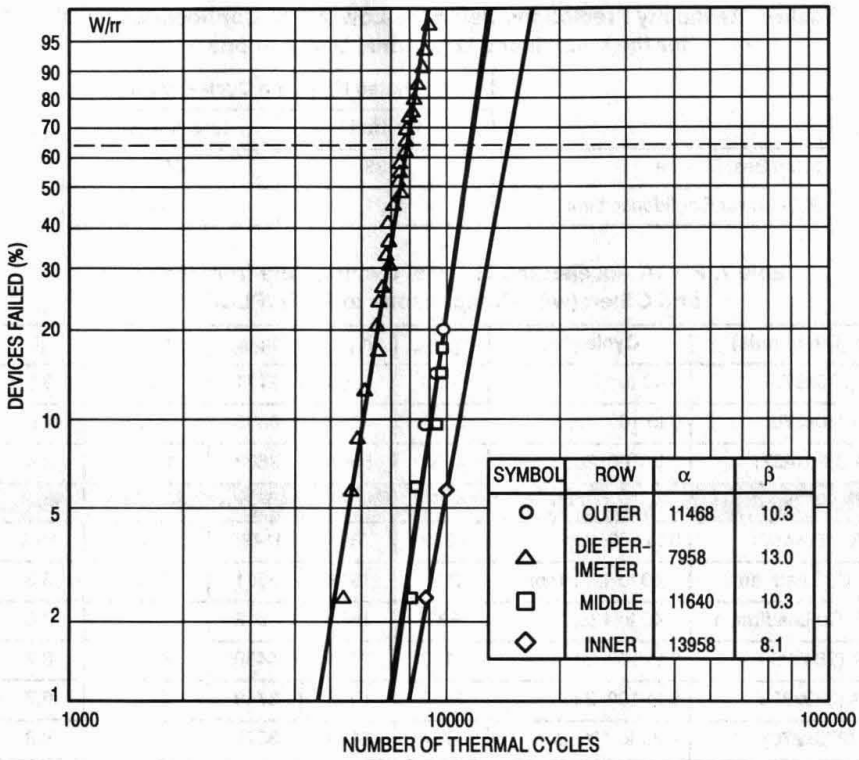


Figure 14. Weibull Failure Distribution by Device Row for a 361 Pin PBGA Cycled from 0 to 100°C at Two Cycles per Hour

can be readily observed. It should be noted that fracture length measurements taken from perpendicular PBGA cross-sections can be erroneous, depending on the row being sectioned, due to the fact that fractures generally propagate in a direction radially from the device center.

A very useful technique in analyzing devices with a multitude of fractured joints is dye penetrant analysis. Dye penetrant analysis can be used to visualize an overall distribution of fractures on all joints. For this procedure to work the best, the mounted device should be cleaned with a solvent prior to the application of a dye penetrant. This cleaning removes any flux residues, soldermask and other particles which are mobile during thermal cycling and may inhibit the flow of the dye into the fracture. There are many dyes available for the specific purpose of penetrating fractures (such as Ardrox Tracer-Tech), however, a machinist's layout dye made by ITW and called Dykem (Steel Red is typically the most visible) has shown excellent results at Motorola and elsewhere. After cleaning, a dropper is used to repeatedly flush the dye underneath the mounted device. The excess dye is then allowed to drain and the remainder is dried. This drying is accelerated by baking at 100°C for 10 to 30 minutes depending on the amount of dye under and around the device. Placing the assembly in a vacuum chamber prior to baking may increase dye penetration into small fracture openings. Following removal from the bake oven and cooling, the PBGA is mechanically removed. It can be pried off with a screwdriver or similar, which may damage joints on the outer one or two rows, or the board repeatedly flexed until the device "pops" off. After removal, the board and device can be readily inspected. Fracture surfaces which are dyed were obviously present prior to device removal and presumably caused by the accelerated testing. An example with a fracture approximately one quarter of the way through the joint is presented in Figure 15.

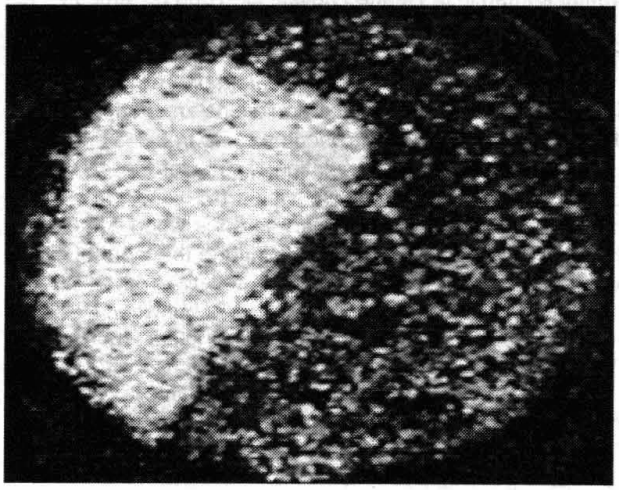


Figure 15. Micrograph of a 361 Pin PBGA Solder Joint Partial Fracture Surface After Application of Dye Penetrant Following 1885 –40 to 125°C Thermal Cycles (Magnification approximately 120X)

8

MOISTURE AND POPCORNING

As with all plastic surface mount packages, the PBGA is currently susceptible to moisture induced delamination or popcorning if it is heated to reflow temperatures with excessive moisture content. The moisture weight percentage at which damage can occur is typically 0.15%. The PBGA is currently specified to meet Level 5 of the JEDEC classifications for moisture sensitivity in Test Method A112 (JESD22–A112). Level 5 in this test method, states that the PBGA will not exhibit delamination after exposure to 30°C/60%RH for 30 hours. The accompanying user handling requirements are a 24 hour out or drypack life. Any exposure over this 24 hours will require baking at 125°C for 24 hours. It is recommended, where possible, that this bake be performed in an inert atmosphere such as nitrogen to minimize potential solder ball oxidation.

The mode of moisture-induced failure in the PBGA package is delamination of the die attach from the die flag. This delamination, caused by the vaporization of the trapped moisture, is clearly visible in the form of a bubble in the BT substrate immediately under the die location. If the moisture content is high enough this delamination occurs violently (i.e., popcorning) and the delamination will propagate along the mold compound/BT interface until it is visible around the perimeter of the package. When this occurs, it is likely that an accompanying shorting of solder balls will occur in the area under the die. For this reason, it is advised to bake and dry pack even mechanical samples or daisy-chain devices prior to process assembly experiments.

RELIABILITY STRESS TESTS

The following summary briefly describes the various reliability tests included in the packaging reliability program. This program includes the PBGA.

SMT Preconditioning Stress

The purpose of this test is to simulate the shipping, storage, and solder attach steps involved in mounting and reworking a surface mount device. The preconditioning flow begins with ten temperature cycles at –65 to 150°C, dehydration bake at 125°C for 24 hours and is followed by a moisture soak. The moisture soak may involve simulating a worst case "no dry pack" condition in an 85°C/85% RH environment, a worst case dry pack condition of 85°C/60% RH, or a typical manufacturing environment condition of 30°C/60% RH. The duration of the moisture condition will vary depending on the moisture level tested. Moisture exposure is followed by two passes of infrared reflow (230°C) for 20 seconds per pass. Infrared reflow equipment is capable of heating the top side package body to 230°C with a ramp rate of 2–10°C per second.

Temperature Cycle

This test accelerates the effects of thermal expansion mismatch among the different components within a specific die and packaging system. This test is typically performed to minimum and maximum temperatures of –65 to 150°C for a duration of 500 or 1000 cycles. During temperature cycle testing, devices are inserted into a cycling system and held at a cold dwell system for at least ten minutes. Following this cold dwell, the devices are heated to the hot dwell where they remain for another ten minutes. the system employs a circulating air environment to assure rapid stabilization at the specified temperature.

Thermal Shock

The objective of this test is the same as that for temperature cycle testing: to emphasize differences in expansion coefficients for components of the packaging system. However, thermal shock provides additional stress because the device is exposed to a sudden change in temperature due to the transfer time of ten seconds maximum as well as the increased thermal conductivity of a liquid ambient. This test is typically performed to a minimum and maximum temperatures of –65 to 150°C for a duration 500 or 1000 cycles. Devices are placed in a fluorocarbon bath and cooled to minimum specified temperature. After being held in the cold chamber for five minutes, the devices are transferred to an adjacent chamber filled with fluorocarbon at the maximum specified temperature for an equivalent time. Two five minute dwells plus two ten second transitions constitute one cycle.

Temperature Humidity Bias (THB)

This is an environmental test performed at a temperature of 85°C. The test is designed to measure the moisture resistance of plastic encapsulated circuits. A nominal static bias is applied to the device to create the electrolytic cells necessary to accelerate corrosion of the metallization. Typical stress duration is 1008 hours.

Autoclave

Autoclave is an environmental test that measures devices resistance to moisture penetration and the resultant effects of galvanic corrosion. Conditions employed during the test include 121°C, 100% relative humidity, and 15 psig. Corrosion of the die is the expected failure mechanism. Autoclave is a highly accelerated and destructive test. Typical test duration is 96 hours.

Results from a qualification of an 86 pin PBGA are included in Appendix D.

RELATED TECHNICAL ARTICLES AND PAPERS

This section provides only a partial listing of articles that have appeared in trade journals and have been published in conference proceedings that discuss issues related to PBGA. All articles are listed alphabetically by principal author/editor last name. Articles for which there is no copyright may be available informally through Motorola.

R. Boyd-Merritt, "Moto Fields New Package Technology", *Electronic Engineering Times*, March 1, 1993, p. 70.

T. Costlow, "Moto Pact Big for BGAs?", *Electronic Engineering Times*, August 2, 1993, p. 16.

R. Darveaux and K. Banjeri, "Fatigue Analysis of Flip Chip Assemblies Using Thermal Stress Simulations and a Coffin-Manson Relation", Proceedings of ECTC, 1991.

R. Darveaux and K. Banjeri, "Constitutive Relations for Tin Based Solder Joints," IEEE Trans on CHMT, Vol. 15, No. 6, December 1992, pp. 1013 – 1024.

R. Darveaux, "Crack Initiation and Growth in Surface Mount Solder Joints," Proceedings ISHM 25th International Symposium on Microelectronics, Dallas, TX, 1993.

M. Donlin, "Packaging Innovations Help Engineers Break Free from Design Constraints", *Computer Design*, June 1993, pp. 65 – 68.

B. Freyman and R. Pennisi, "Overmolded Plastic Pad Array Carriers (OMPAC): A Low Cost, High Interconnect Density IC Packaging Solution for Consumer and Industrial Electronics", Proceedings of the Technical Conference, 1991 ECTC, pp. 176 – 182.

A. Fukuda, Feature Article on BGAs (in Japanese), *Nikkei Electronics*, February 14, 1994, pp. 59 – 73.

D. Hattas, "BGAs Face Production Testing", *Advanced Packaging*, Summer 1993, pp. 44 – 46.

J. Houghten, "New Package Takes on QFP's", *Advanced Packaging*, Winter 1993, pp. 38 – 39.

R. Johnson, A. Mawer et al., "A Feasibility Study of Ball Grid Array Packaging", NEPCON East Proceedings, 1993, pp. 413 – 425.

R. Johnson and D. Cawthon, "Thermal Characterization of 140 and 225 Pin Ball Grid Array Packages", NEPCON East Proceedings, 1993.

J. Lau et al., "No Clean Mass Reflow of Large Over Molded Plastic Pad Array Carriers (OMPAC)", 1993 IEEE/CHMT International Electronics Manufacturing Technology Symposium Proceedings, pp. 63 – 75.

D. Maliniak, "BGAs Make Transition to Memory Packages", *Electronic Design*, October 14, 1993, pp. 34 – 35.

H. Markstein, "Pad Array Improves Density", *Electronic Packaging & Production*, May 1992, pp. 25 – 26.

F. Martin, "C-5 Solder Sphere Robotic Placement Cell for Overmolded Pad Array Carrier", 1993 International Electronics Packaging (IEPS) Conference Proceedings, pp. 740 – 748.

A. Mawer, R. Darveaux and M. Petrucci, "Calculation of Thermal Cycling and Application Fatigue Life of the Plastic Ball Grid Array (BGA) Package", 1993 International Electronics Packaging (IEPS) Conference, 1993, pp. 718 – 730.

B. Miles and B. Freyman, "The Elimination of the Popcorn Phenomenon in Overmolded Plastic Pad Array Carriers (OMPAC)", 1992 International Electronics Packaging (IEPS) Conference Proceedings, pp. 605 – 614.

K. O'Brien, "Will BGA Live Up to Its Billing", *Surface Mount Technology*, August 1993, p. 40.

B. Nagaraj and M. Mahalingam, "OMPAC Package — Creep Analyses of C5 Solder Pads Using FEM Simulation," APDC Technical Report 15-92, 1992.

J. Shimizu, "Plastic Ball Grid Array Coplanarity", Proceedings of the 1993 Surface Mount International Conference, pp. 86 – 90.

H. Solomon, "Strain-Life Behavior in 60/40 Solder", GE Report #88CRD261, 1988.

C. Trigas, "The OMPAC Package — Assembly to Printed Circuit Board", Proceedings of the 1994 EuPAC Conference, Feb 1 – 3, 1994, Essen, Germany.

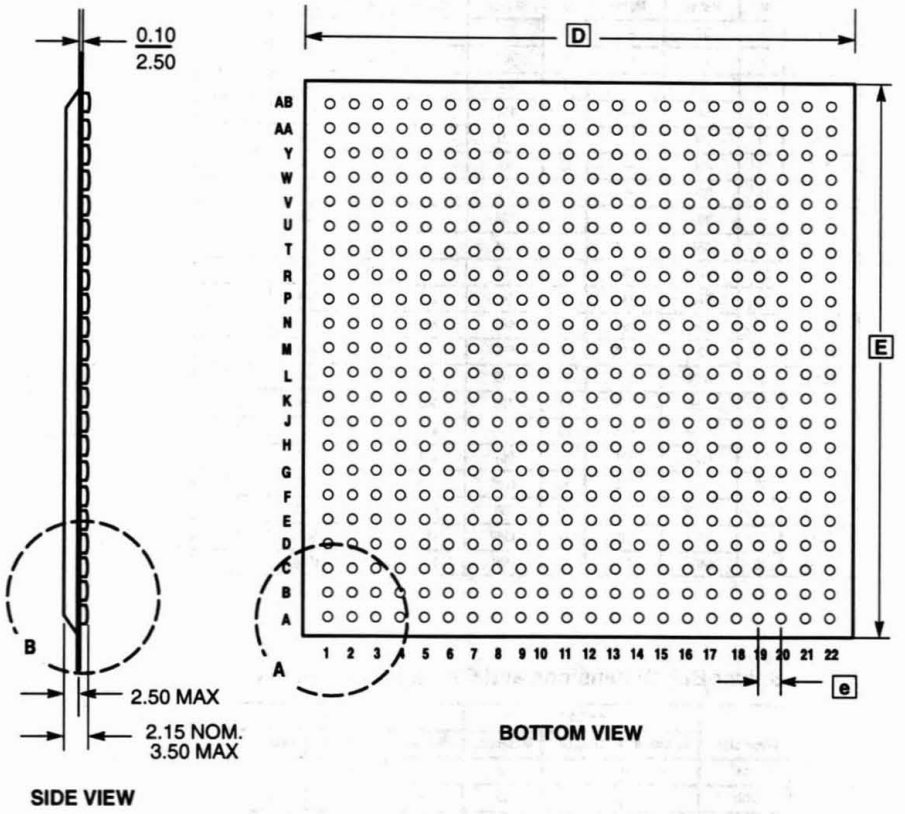
J. Tuck, "BGAs: A Trend in the Making", *Circuits Assembly*, December 1993, pp. 20 – 21.

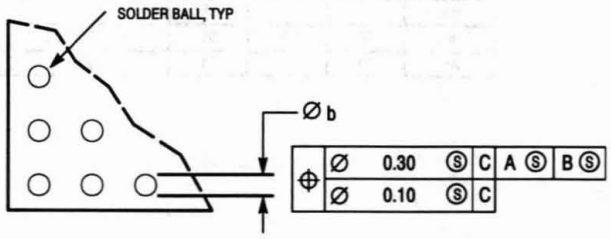
J. Tuck, "BGAs: The Next Chapter", *Circuits Assembly*, August 1993, pp. 24 – 27.

J. Vardaman, "Ball Grid Array Packaging", TechSearch International, Inc. Consulting Report, January, 1993.

W. Yip and C. Tsai, "Electrical Performance of an Overmolded Pad Array Carrier (OMPAC), 1993 International Electronics Packaging (IEPS) Conference Proceedings, pp. 731 – 739.

APPENDIX A
SUMMARY OF JEDEC PLASTIC BALL GRID ARRAY FAMILY REGISTRATION
(Note: All Dimensions in mms)





DETAIL A

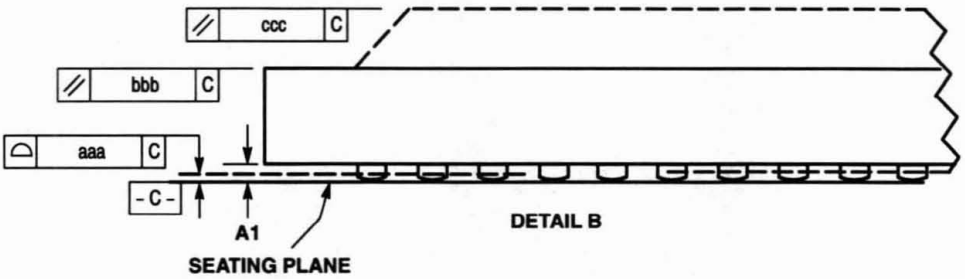


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Table of JEDEC Square PBGA Array Configurations (MxM) for a Given Body Size (D/E) and Pitch (e) (Fully Populated Ball Count Given in Full Matrix Column)

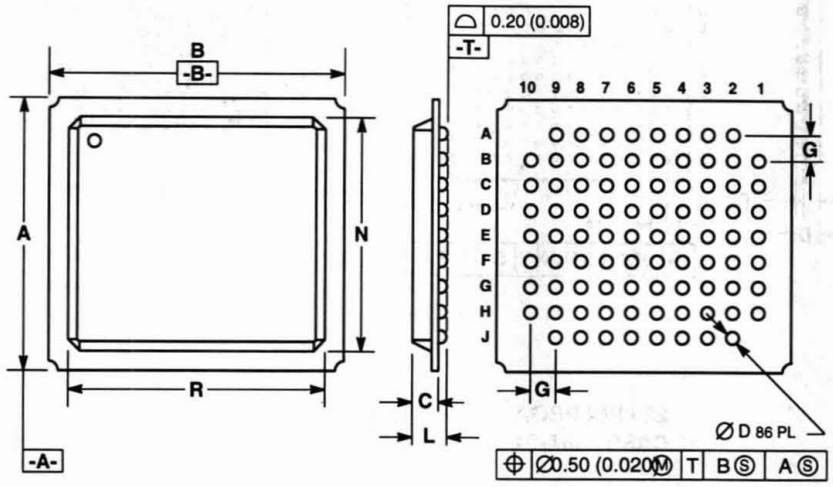
	e = 1.00			e = 1.27			e = 1.50		
		N			N			N	
D / E	M	Full Matrix	Stagger Matrix	M	Full Matrix	Stagger Matrix	M	Full Matrix	Stagger Matrix
7.00	6	36	—	5	25	—	4	16	—
9.00	8	64	—	7	49	—	6	36	—
11.00	10	100	—	8	64	—	7	49	—
13.00	12	144	—	10	100	—	8	64	—
15.00	14	196	—	11	121	—	10	100	—
17.00	16	256	—	13	169	—	11	121	—
19.00	18	324	—	15	225	—	12	144	—
21.00	20	400	—	16	256	—	14	196	—
23.00	22	484	242	18	324	—	15	225	—
25.00	24	576	288	19	361	—	16	256	—
27.00	26	676	338	21	441	221	18	324	—
29.00	28	784	392	22	484	242	19	361	—
31.00	30	900	450	24	576	288	20	400	—
33.00	32	1024	512	26	676	338	22	484	242
35.00	34	1156	578	27	729	365	23	529	265
37.50	37	1369	685	29	841	421	25	625	313
40.00	39	1521	761	31	961	481	26	676	338
42.50	42	1764	882	33	1089	545	28	784	392
45.00	44	1936	968	35	1225	613	30	900	450
47.50	47	2209	1105	37	1369	685	31	961	481
50.00	49	2401	1201	39	1521	761	33	1089	545

Solder Ball Dimensions and Package Coplanarity

	e = 1.27			e = 1.50		
Dimension	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
aaa	—	—	.15	—	—	.15
bbb	—	—	.25	—	—	.25
ccc	—	—	.35	—	—	.35
b	.60	.75	.90	.60	.75	.90
A1	.50	.60	.70	.50	.60	.70

APPENDIX B
PACKAGE MECHANICAL OUTLINES FOR THE 86, 119, 169, 225, 313, and 357 PIN PBGA

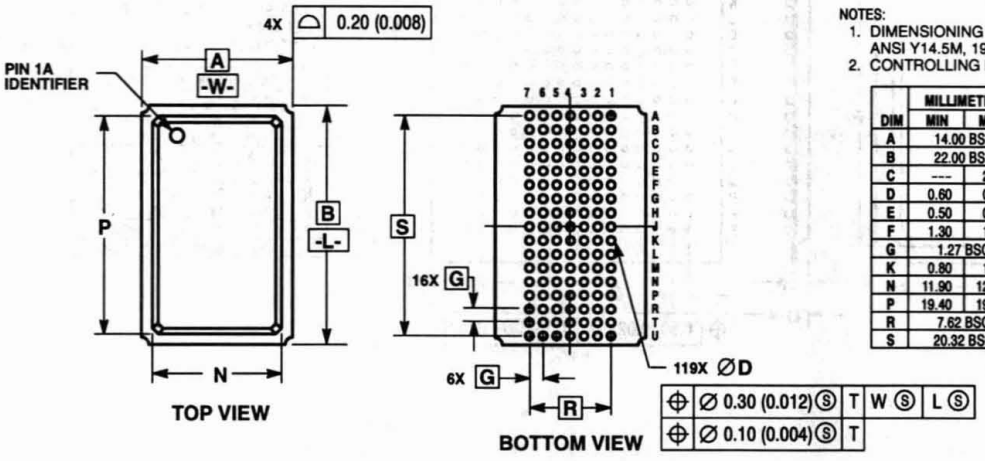
86 PIN PBGA
CASE 896A-01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

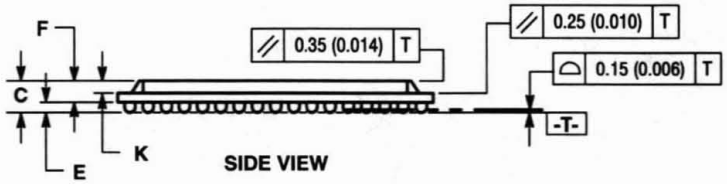
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	16.16	16.36	0.637	0.644
B	17.68	17.88	0.697	0.703
C	1.33	1.73	0.053	0.068
D	0.69	0.81	0.028	0.031
G	1.524 BSC		0.060 BSC	
L	1.84	2.44	0.073	0.096
N	13.80	14.20	0.544	0.559
R	15.29	15.69	0.602	0.617

119 PIN PBGA
CASE 999-01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.00 BSC		0.551 BSC	
B	22.00 BSC		0.866 BSC	
C	---	2.40	---	0.094
D	0.60	0.90	0.024	0.035
E	0.50	0.70	0.020	0.028
F	1.30	1.70	0.051	0.067
G	1.27 BSC		0.050 BSC	
K	0.80	1.00	0.031	0.039
N	11.90	12.10	0.469	0.476
P	19.40	19.60	0.764	0.772
R	7.62 BSC		0.300 BSC	
S	20.32 BSC		0.800 BSC	



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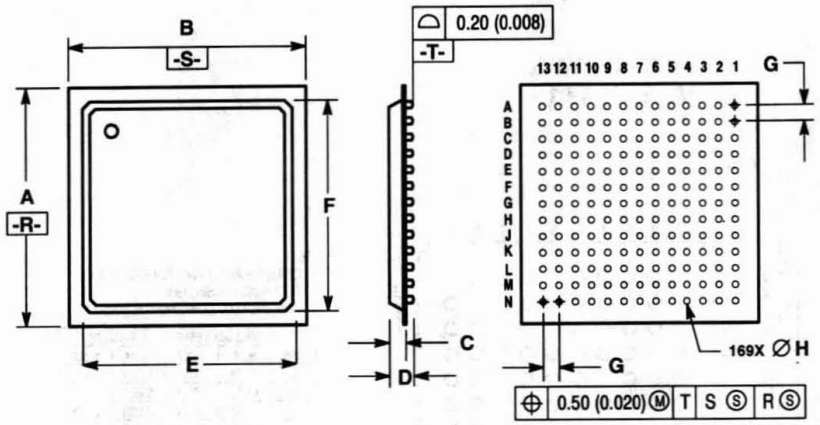
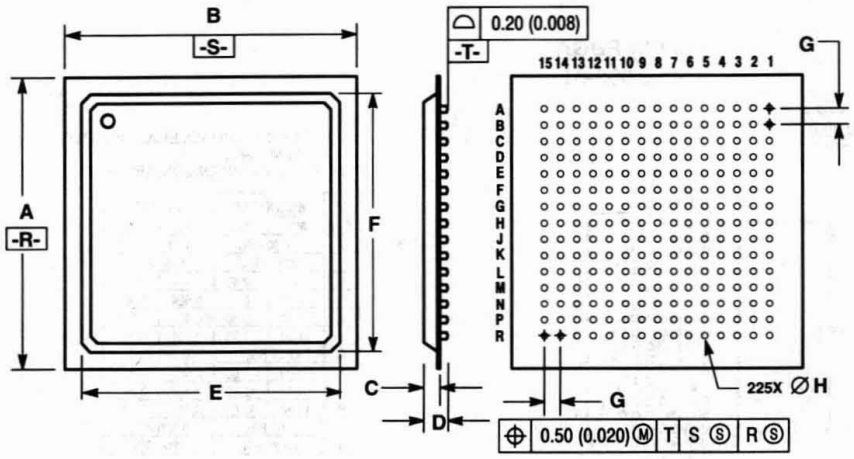
169 PIN PBGA
CASE 938-01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	21.90	22.10	0.8622	0.8700
B	21.90	22.10	0.8622	0.8700
C	1.33	1.73	0.0523	0.0681
D	1.83	2.43	0.0720	0.0956
E	19.30	19.70	0.7598	0.7755
F	19.30	19.70	0.7598	0.7755
G	1.50 BSC		0.0590 BSC	
H	0.690	0.810	0.0271	0.0318

225 PIN PBGA
CASE 938A-01

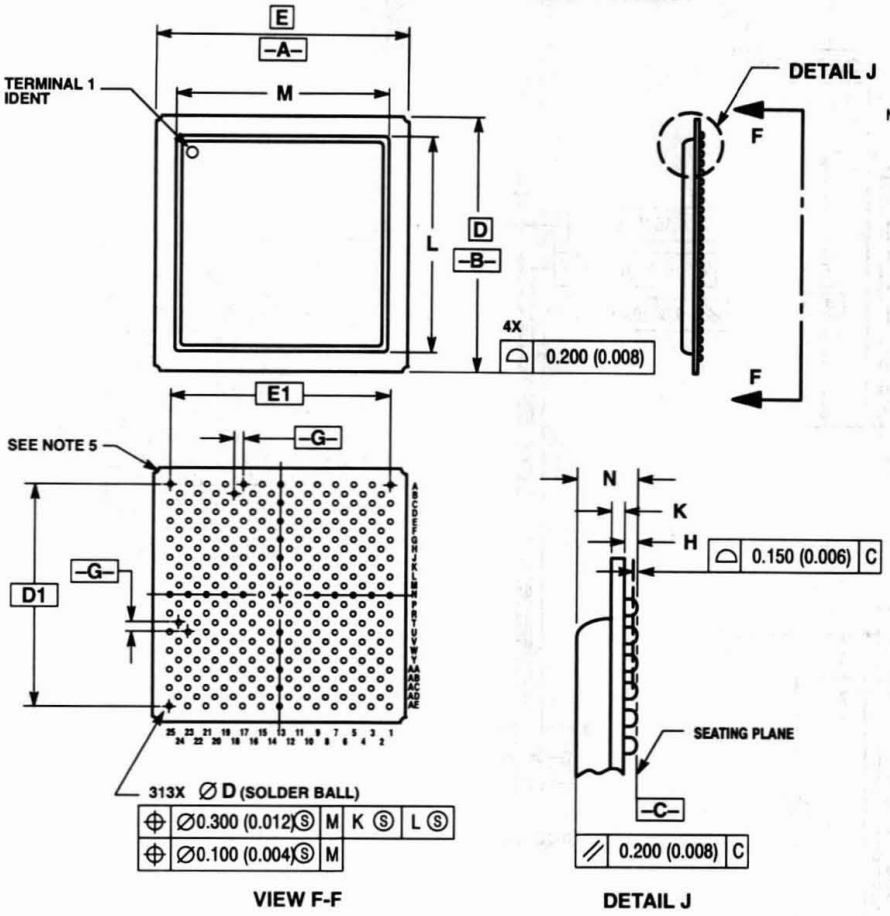


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	26.90	27.10	1.0590	1.0669
B	26.90	27.10	1.0590	1.0669
C	1.33	1.73	0.0523	0.0681
D	1.83	2.43	0.0720	0.0956
E	23.80	24.20	0.9370	0.9527
F	23.80	24.20	0.9370	0.9527
G	1.50 BSC		0.0590 BSC	
H	0.690	0.810	0.0271	0.0318

8

313 PIN PBGA
CASE 969A-01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -D-.
4. DATUM -C- (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
D	35.000 BSC		1.378 BSC	
D1	30.480 BSC		1.200 BSC	
E	35.000 BSC		1.378 BSC	
E1	30.480 BSC		1.200 BSC	
G	1.270 BSC		0.050 BSC	
H	0.500	0.700	0.020	0.028
K	0.510	0.610	0.020	0.024
L	25.500	29.500	1.004	1.161
M	25.500	29.500	1.004	1.161
N	2.026	2.834	0.079	0.111

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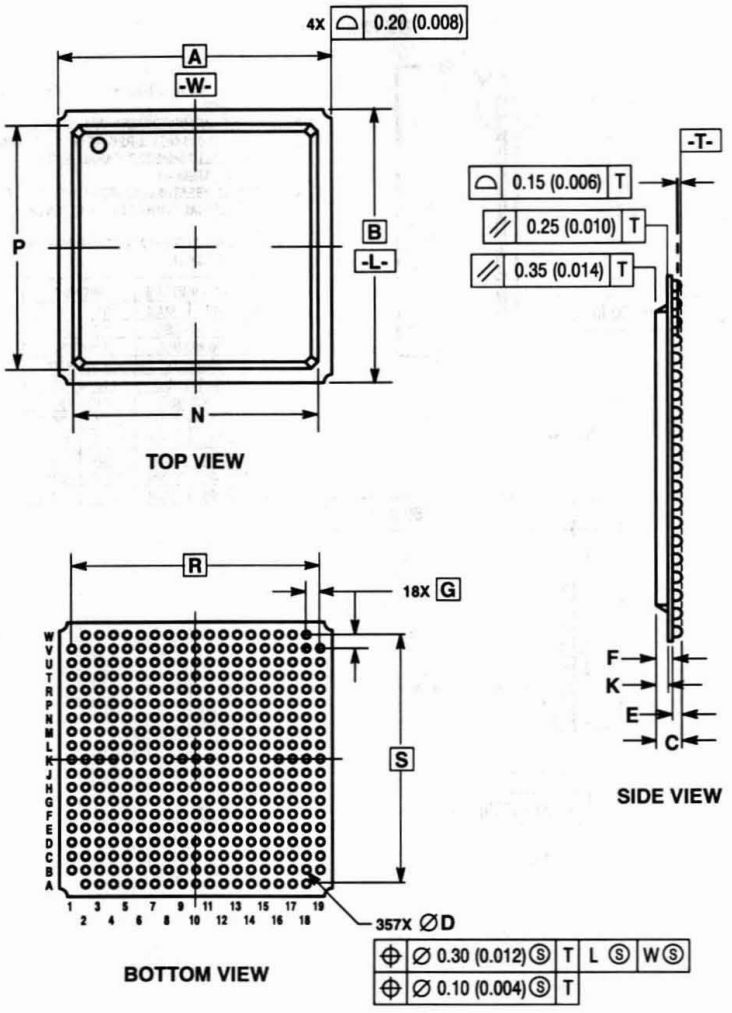
357 PIN PBGA
CASE 1103-01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

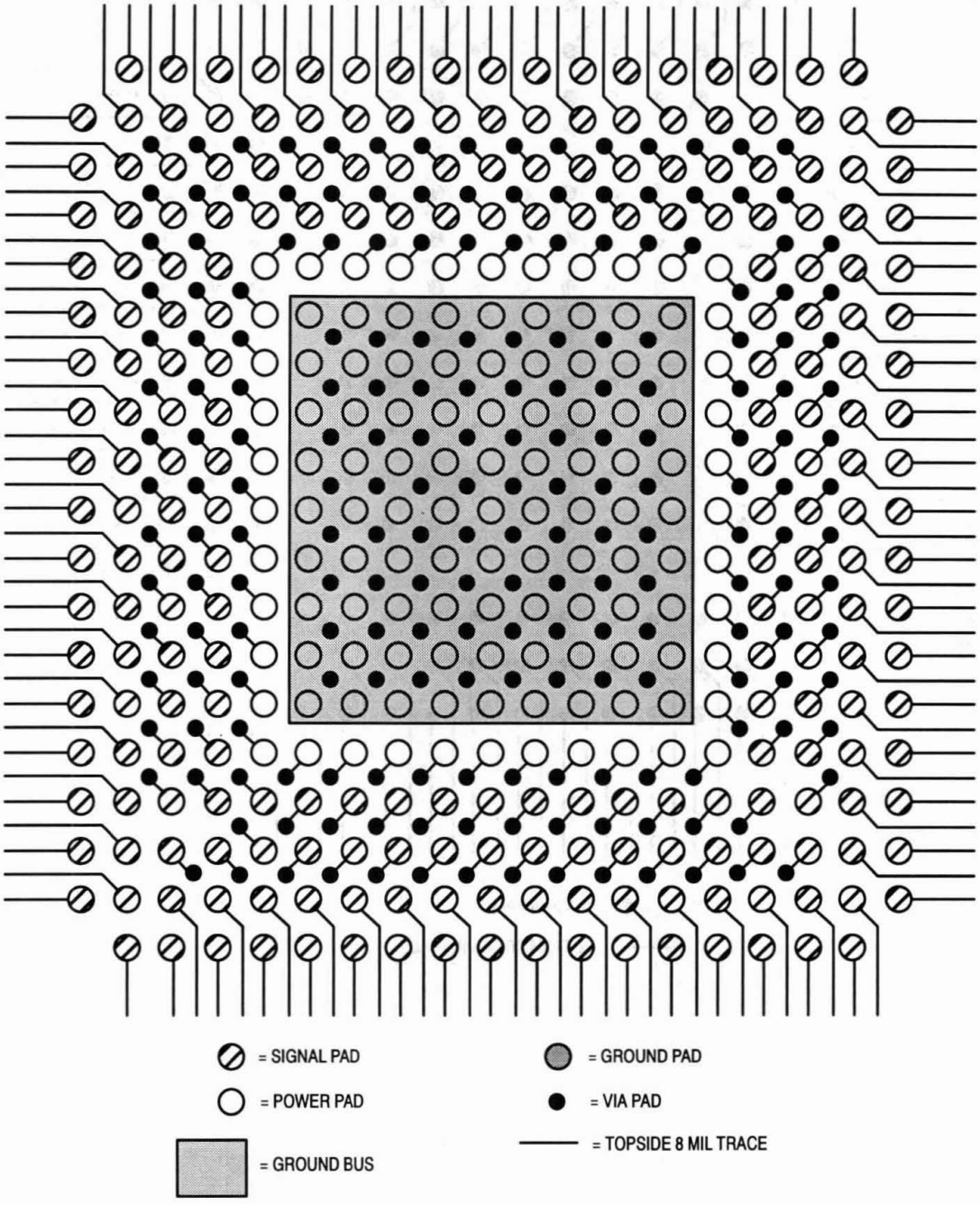
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	25.00 BSC		0.984 BSC	
B	25.00 BSC		0.984 BSC	
C	---	2.05	---	0.081
D	0.60	0.90	0.024	0.035
E	0.50	0.70	0.020	0.028
F	0.95	1.35	0.037	0.053
G	1.27 BSC		0.50 BSC	
K	0.70	0.90	0.028	0.035
N	22.40	22.60	0.882	0.890
P	22.40	22.60	0.882	0.890
R	22.86 BSC		0.900 BSC	
S	22.86 BSC		0.900 BSC	

8

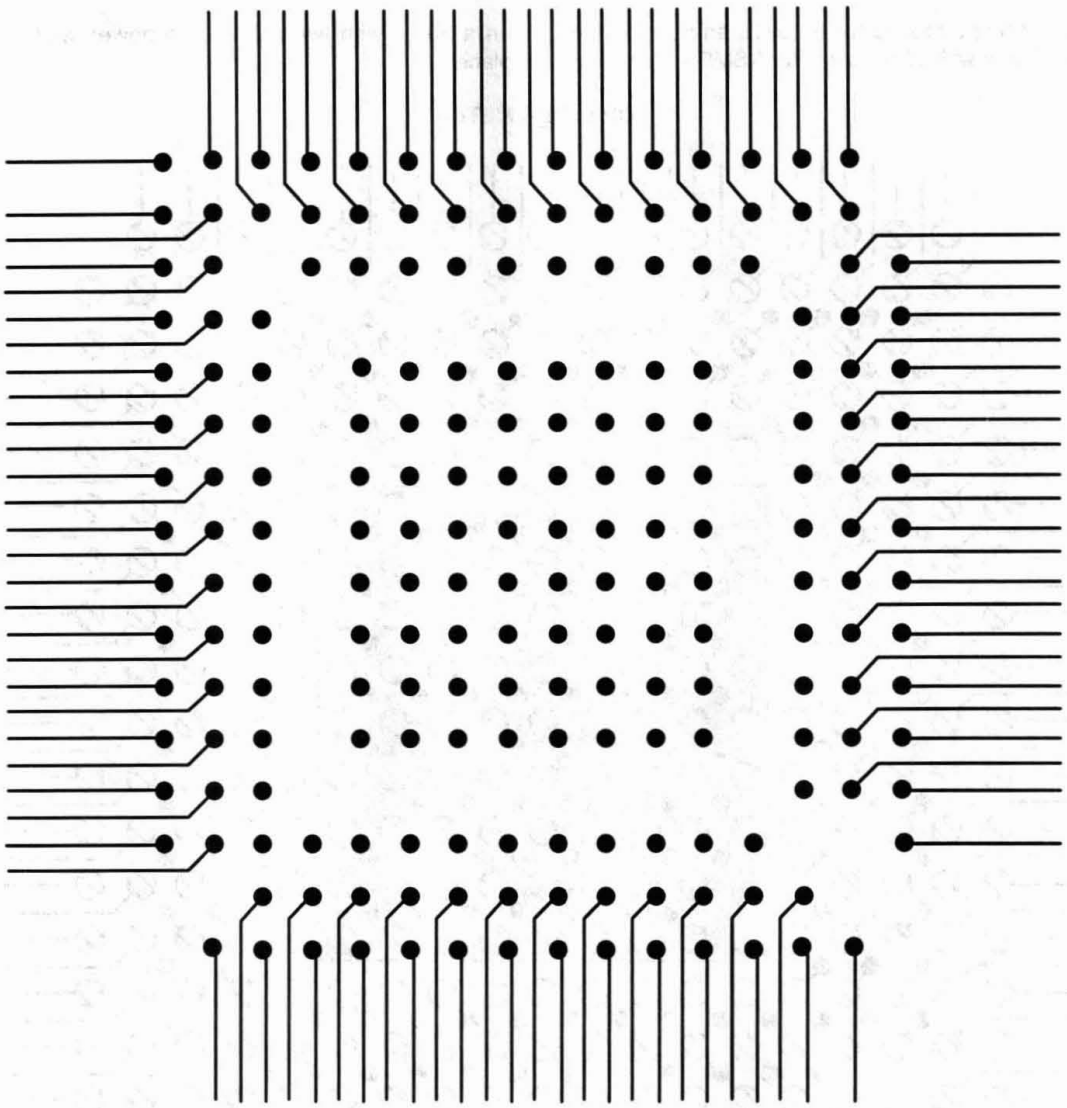
APPENDIX C

Example of escape routing for a 19x19 array, 1.27 mm pitch 357 pin PBGA with 23 mil diameter NSMD solder pads on a board with two signal, one power, and one ground plane.

TOP LAYER METAL



BOTTOM LAYER METAL



● = 25 MIL VIA PAD

——— = BOTTOMSIDE 8 MIL TRACE

APPENDIX D

86 PIN PBGA PACKAGE QUALIFICATION SUMMARY SHEET

SOURCE DEVICE:	MCM62C416ZP21	TECHNOLOGY:	0.8 µ CMOS	FABRICATION:	MOS8
SOURCE DEVICE:	MCM56824ZP25	TECHNOLOGY:	0.8 µ CMOS	FABRICATION:	MOS8
		PACKAGE:	9X10 PBGA		
		LEAD COUNT:	86 BUMP	JOINT QUAL SPEC REV:	I
PURPOSE:	QUALIFICATION OF 86 BUMP PBGA				

PACKAGE RELIABILITY (Preconditioning Temperature Cycle (–65 to +150°C + bake (125°C, 24 hours) + (30°C, 60% RH 48 hours) + infrared reflow (230°C, 20 seconds, two passes)

Stress	Conditions	Results	Hours/Cycle	Next Readout	Pass/Fail
		Actual Data			
Preconditioning	As Above	0/225	2 Passes	Complete	P
Temperature Humidity Bias	85°C/85% RH/5 V	0/45	1008 Hours	Complete	P
Temperature Cycle	–65 to 150°C Air/Air	0/90	500 Cycles	Complete	P
Autoclave	121°C/100% RH 15 PSIG	0/90	96 Hours	Complete	P

8

AN1232

Thermal Performance of Plastic Ball Grid Array (PBGA) Packages for Next Generation FSRAM Devices

Prepared by: Shailesh Mulgaonker (APDC, Phoenix, AZ) and Bennett Joiner (APDPL, Austin, TX)

ABSTRACT

Describing the thermal performance of Plastic Ball Grid Array (PBGA) packages by the traditional Theta JA obscures the performance characteristics of the package. When the package is designed with thermal vias and "thermal balls," the package is closely coupled thermally to the printed circuit board to which it is attached. The thermal performance of the package is dominated by the thermal performance, i.e. the temperature, of the printed circuit board. Since the thermal performance of the package is so closely coupled to the board, the thermal performance, $R_{\theta JA}$, should be expressed as a function of the temperature of the board. The thermal performance of the package is modeled as the junction to board and junction to case thermal resistances. Measured data is provided to validate the techniques. Measurements were taken on the 119 lead PBGA package on single component single and 4 layer printed circuit boards and on a simulated system daughter board with 8 or 16 packages in natural and forced convection environments.

INTRODUCTION

The use of wider bus structures for the static memories used for caches is driving the need for higher lead count packages for memory devices. Additionally, the faster clock and associated rise times highlight the need for multiple power and ground leads. As a result, the memory devices used for cache memories are being packaged into the higher lead count packages such as PLCC, QFP, and PBGA packages. For the range of devices that are being considered here, the PLCC package is physically too large to be acceptable. Hence, the packages of choice are the QFP and the PBGA.

The thermal performance of a 100 lead 14 x 14 mm plastic QFP package is compared to a 119 lead 14 x 22 mm PBGA package in Figure 1. Theta JA, $R_{\theta JA}$, is measured using the procedures of SEMI[1] G38–87 using a single layer printed circuit board (76 x 114 mm) as specified in SEMI G42–88 at natural convection. Normally this value is supplemented by the thermal resistance measurements over a range of forced convection. For illustration of the differences between the two parts consider the bar chart in Figure 1 of the thermal resistance at natural convection for the parts mounted on the standard single layer printed circuit board and parts mounted on a four layer printed circuit board which is included as an extension of the SEMI specification. While the two packages have very similar thermal performance as measured on the standard single layer printed circuit board, there is a substantial difference in the performance on the four layer boards. The higher thermal conductivity of the four layer board with two solid 1 oz. planes causes more of the board to act as a heat sink. The effect is enhanced for the PBGA packages because there is metal conduction path from the die pad to the ground plane of the printed circuit board. This path has much lower thermal resistance than the equivalent path for the QFP. Hence, the PBGA package is much more closely coupled to the printed circuit board and is more sensitive to its temperature and to power dissipation in other components on the board.[2,3]

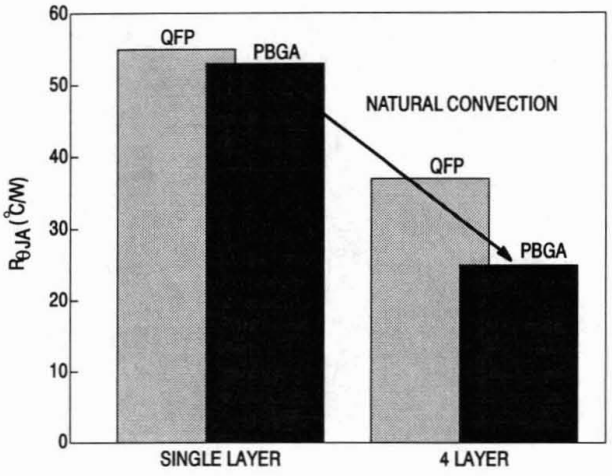


Figure 1. Type of Board on which Package is Mounted

The specific package being considered here is a 119 lead 14 x 22 mm PBGA package which is sketched in Figure 2. The thermal test vehicle packages tested for this characterization activity used a thermal die size of 4.37 x 7.32 mm (172 x 288 mil) mounted on a 7.5 x 11.1 mm die pad. There are 32 vias from the die paddle to the array of 21 thermal balls. The thermal balls are soldered to an array of pads that are connected to the ground plane in the printed circuit board with 32 vias. The planes in the circuit board are solid 1 oz. copper. Allowing the planes to be solid makes simulation easier and reflects the performance of the application boards which will have more than one ground plane.

8

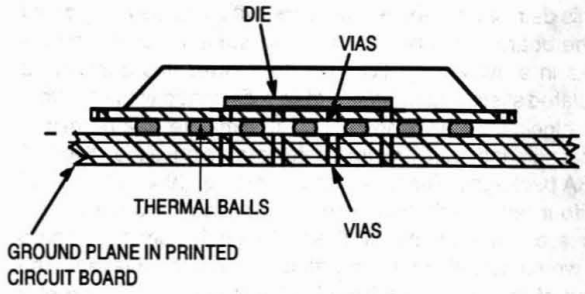


Figure 2.

This paper will address the following questions:
(1) How useful is $R_{\theta JA}$?
(2) Can the customer use the $R_{\theta JA}$ measured on a four layer-board to estimate performance on his multilayer board?
(3) How should the performance of the package be modeled?

Simplified Thermal Models for the PBGA

The heat flow in any package is actually a complicated three dimensional flow in which the path that the heat flow takes is dependent on how each of the surfaces of the package are cooled or heated by adjacent components. There are several approaches to deal with this difficulty including full finite element or finite difference models or the junction to case thermal resistance model of Bar–Cohen.[4] This paper will argue that the additional simplification of the multiple internal resistance models to only the two major thermal paths is valid based on measurement data that fits such a model. The proposed thermal model for a single component on a board is shown in Figure 3.

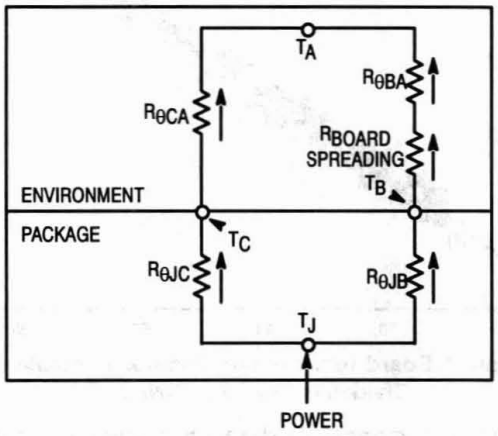


Figure 3.

In this model, the package is modeled as a junction to board thermal resistance, $R_{\theta JB}$, and a junction to case (top of package), $R_{\theta JC}$. These are the two major thermal paths from the package. The heat loss from the package to the environment is represented by the case to ambient thermal resistance, $R_{\theta CA}$; heat loss from the board is represented by a spreading resistance within the board and the board to ambient thermal resistance. For this model, the junction to ambient thermal resistance, $R_{\theta JA}$, can be calculated by series and parallel combinations of the resistance values of the model:

$$\frac{1}{R_{\theta JA}} = \frac{1}{R_{\theta JC} + R_{\theta CA}} + \frac{1}{R_{\theta JB} + R_{BS} + R_{BA}}$$

In most cases, there is not a clear separation between the spreading resistance in the board and the board to ambient thermal resistance. Usually, this equation will just be written in terms of an effective board to ambient thermal resistance.

$$\frac{1}{R_{\theta JA}} = \frac{1}{R_{\theta JC} + R_{\theta CA}} + \frac{1}{R_{\theta JB} + R_{BA}}$$

This analysis works for the single component on the board. If there are other heat sources on the board, the board temperature is not a function of only this one package. For the more general case, the effect of the other components can be represented as the temperature difference, T_{BA}, between the board and the ambient. This term, T_{BA}, is normally referred to as the board temperature rise above ambient. With this addition, the model of the package and board becomes:

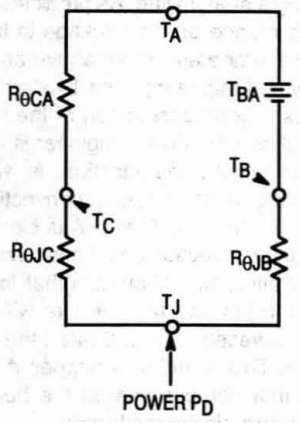


Figure 4.

This model is a simplified version of the model used by Andrews[4] with the junction to header thermal resistance neglected. If one uses this model to solve for the junction to ambient thermal resistance in terms of the thermal resistance values, board to ambient temperature rise, T_{BA}, and power P_d, then the following linear relationship is obtained:

$$R_{\theta JA} = \frac{(R_{\theta JC} + R_{\theta CA})\, R_{\theta JB}}{(R_{\theta JC} + R_{\theta CA}) + R_{\theta JB}} + \frac{(R_{\theta JC} + R_{\theta CA})}{(R_{\theta JC} + R_{\theta CA}) + R_{\theta JB}} \bullet \frac{T_{BA}}{P_D}$$

$$R_{\theta JA} = R_{\theta JA0} + S \bullet \frac{T_{BA}}{P_D}$$

This model predicts that the junction to ambient thermal resistance will be a linear function of the board temperature rise above ambient divided by the power dissipated in the component. The usefulness of the model can be verified by measuring the component thermal performance as function of the board temperature. Experimentally, this is easily accomplished using a silicone rubber heating pad under the printed circuit board. The results are shown in Figure 5.

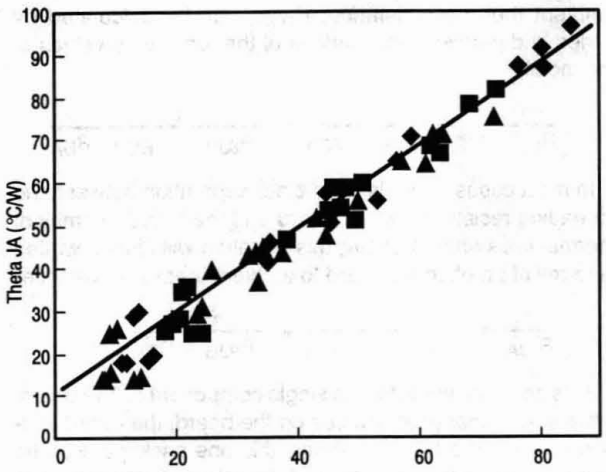


Figure 5. Board Temperature Rise Above Ambient Divided by Package Power

Measurements taken at natural convection, 1 m/s, and 2 m/sec forced convection are shown on the graph with all the data fitted to a single straight line. As predicted by our model, the thermal performance of this package is linearly dependent on the board temperature rise above ambient (divided by package power dissipation). The two resistor model of Figure 4 provides a good description of the thermal performance of the package. When an engineer is first introduced to this concept, one of the first questions is "why is the thermal performance the same at natural convection as at 2 m/s forced convection?" Actually, Theta JA is significantly different between natural convection and 2 m/s because the board temperature is significantly different. What is shown in the Figure 5 is that the junction temperature will be nearly the same at natural convection and at 2 m/s if the board temperature is the same. This would only happen if the power dissipation of the other components on the board forced the additional temperature rise in the board.

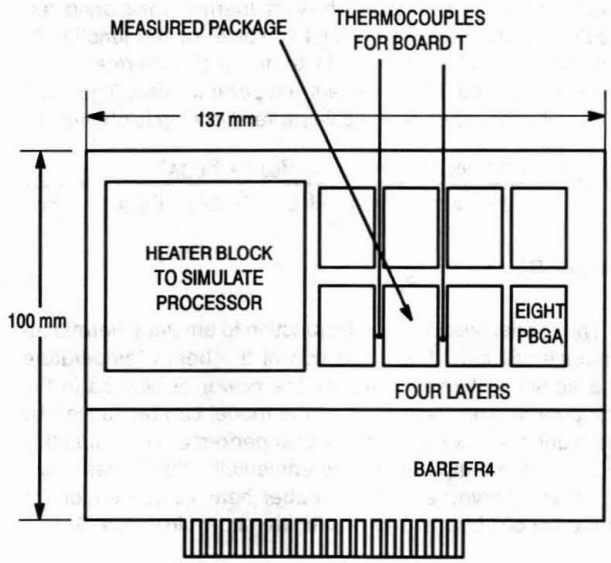


Figure 6.

This data shown above was taken with a single component on the board. The obvious question is: How well this model works in a system application? To answer this question, a simulated system daughter card was designed with an aluminum block with cartridge heaters to simulate a large microprocessor and with provisions for mounting either 8 or 16 PBGA packages. The board has an area of 69 x 137 mm that has four layers with two solid 1 oz planes. Two solid 1 oz. planes are approximately thermally equivalent to a board that would actually be used with perhaps 8 to 12 layers. The layout of the board is shown in Figure 6 with an array of 8 PBGA on one side of the board. The other 8 packages are mounted on the bottom of the board directly under the other ones. The package indicated by the arrow is the one for which data is reported; a package in the "middle" of the array of devices was chosen because it would be representative of a typical package in middle of such an array. Junction temperatures were also measured for the other three devices in that row. The board temperature is measured with a thermocouple on each side of the package soldered into plated through holes which are connected to the ground plane. The thermal balls of the PBGA are connected to the one ground plane.

Results obtained from this board at natural convection, 0.5, 1, and 2 m/s with either 8 PBGA or 16 PBGA packages on the board powered at 1 or 2 watts each are combined with the earlier data taken on single and 4 layer boards and shown in Figure 7.

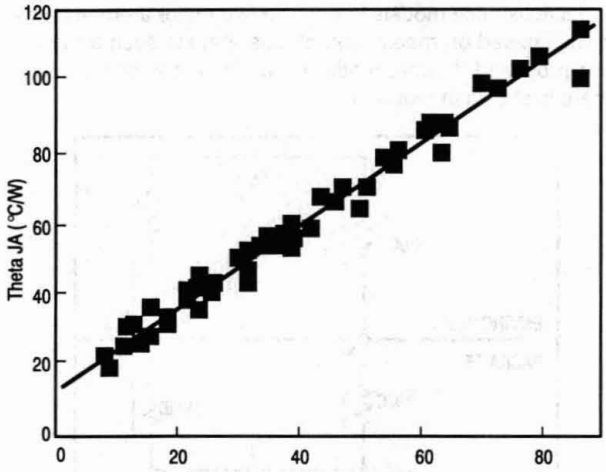


Figure 7. Board Temperature Rise Above Ambient Divided by Package Power

Again, the measured data on a wide variety of environmental conditions fit the linear relationship predicted by the two resistor model. As an example, suppose there is one watt being dissipated in the PBGA package and the board temperature has risen to 30°C above ambient. Then, one could determine from the graph that the Theta JA of the package in that environment would be 40°C/watt. As another example, suppose that the package was dissipating 2 watts and that the board temperature was 60°C above the ambient temperature. Then the board temperature rise divided by the package power would be 30 and the Theta JA would also be 40°C/watt. For an ambient temperature of 25°C, this would result in junction temperatures of 65°C and 105°C for the one and two watt examples, respectively. From this

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discussion, it is evident that good thermal performance will require thermal management of the printed circuit board temperature.

While, the measured Theta JA can be plotted on the same curve for both natural convection and forced convection, a purist would point out that the percentage of heat lost between convection to the air from the package and conducted to the board will change with forced convection. In fact, if the data at natural convection and 1 m/s are separately fitted to a straight line, there will be small differences in the slope and intercept. As an example, the curve fits determined from the results with single component board are given in the following table:

	Intercept	Slope
Natural Convection	9.8	0.997
1 m/s	10.7	0.971
2 m/s	10.7	0.954

As the forced convection increases or a heat sink is placed on the package, a lower percentage of the heat is dissipated to the printed circuit board, and the junction temperature is slightly less coupled to the board temperature. For the typical range of forced convection used in desktop computers, reasonable accuracy for this package is achieved using the simplified expressions combining the results for the various conditions into a single relationship.

A more traditional way to examine the data is to use a table of Theta JA determined by a variety of techniques:

	Theta JA (°C/watt)	
Board Type	Natural Convection	1 m/s Forced Convection
Single Layer Board	52	41
4 Layer Board	24	19
8 Parts at 1 watt (System Board)	56 to 62	46 to 49
8 Parts at 2 watts (System Board)		45 to 49
16 Parts at 1 watt (System Board)	104	84

The junction temperature depends on the environment which includes the conductivity of the board and the power dissipation of surrounding components. The single component on a multilayer board represents one extreme with the other extreme represented by packages mounted closely together on both sides of the board.

The values obtained from the single component on a multilayer board would predict a lower value of the junction temperatures for most applications than would be observed in the typical case with substantial power dissipation in other devices on the board.

The doubling of the observed Theta JA when the packages are mounted on both sides of the board compared to the single sided mounting is a graphic example of the effect of the power density on the board and the resulting board temperature on the junction temperature. Mounting the packages on both sides of the board effectively halves the area available for power dissipation for each package. Incidentally, packages on the bottom of the board had very similar junction temperatures to the packages on top of the board. In natural convection at 1 watt, the package on the top of the board had a junction temperature of 121°C and the bottom package had a junction temperature of 120°C. For all practical purposes, those are identical values. This is explained by the close coupling of the junction temperatures to the board temperature which will be the same for the two packages mounted on opposite sides of the board.

The traditional Theta JA is useful for comparing package performance and as a preliminary estimate to determine whether further analysis is needed. It gives no information to account for the range of thermal performance given as examples in the table above.

The other frequently asked question about this formalism is: How is the board temperature determined? The effective doubling of the Theta JA when the packages are mounted on opposite sides of the board clearly indicates that historical board temperatures could be wrong. The answer to the determination of the board temperature is that a full board level thermal simulation will be required to determine both the thermal performance of the printed circuit board and the performance of each of the packages. There are a number of commercial software codes[6–8] that perform a board level thermal solution with varying degrees of sophistication. These range in sophistication from the 2 1/2 dimensional finite difference or finite element codes to the computational fluid dynamics codes that simultaneously solve the conduction and the fluid flow convection. For all these simulation codes, a simplified thermal model for the package is required. From a component manufacturer's viewpoint, a simple, general purpose model which could be broadly applied would be most helpful. It is our contention that the reduction of the measured data to a single straight line as predicted by the model demonstrates that the two resistor model meets the need for a reasonably accurate description of thermal performance. A proposed method for obtaining that model will be described in the following section.

CONDUCTION MEASUREMENTS TO DETERMINE PACKAGE MODELS

Having determined that the two resistor model will adequately describe the thermal performance, a method for obtaining the values in those models will be discussed. One of the basic premises is that the package model should describe the package behavior. As an example, the package model should not provide a case to ambient thermal resistance because it is not a package characteristic. The case to ambient thermal resistance is a function of whether natural convection can occur in a closed environment, degree of turbulence in forced convection, whether a heat sink is used, etc. Instead, the package model will provide a junction to case thermal resistance. The next level modeling tool can work from that junction to case thermal resistance to determine the total thermal resistance through the top of the case whether a heat sink is used or normal convection environments.

Unfortunately, there are several junction to case formalisms in use. The most confusing is the junction to all surfaces of the case thermal resistance as determined by the junction to a liquid bath measurement which is described in SEMI specification G43–87. One of the board level modeling tools uses this value coupled with the lead resistance as the junction to board measurement. Our position is that this definition is not extensible to the ceramic packages or thermally

enhanced packages on which a heat sink is likely to be used. Instead, the definition taken from the JEDEC[9] committee is used: The junction to case thermal resistance of a package is defined to be "the thermal resistance from the operating portion of a semiconductor device to outside surface of the package (case) closest to the chip mounting area when that same surface is properly heat sunk so as to minimize temperature variation across that surface." Hence, the junction to case thermal resistance is the thermal resistance of the path from the junction to the surface on which a heat sink might be placed. As a result, the junction to case thermal resistance is the thermal resistance from the junction to the top surface of the PBGA. It is determined using a cold plate (infinite heat sink) to force "all" the heat to travel from the junction to the case of the package. The methods for making this measurement are described in the industry specifications: MIL–STD 883D, Method 1012.1 and SEMI G30–88. We deviate from the industry specifications in that the temperature of the cold plate is used instead of the case temperature. All of the techniques to put a thermocouple on the surface of the case using holes or slots in the cold plate or in the case itself will yield a warmer measurement and hence a more optimistic measure of the thermal resistance. Using the cold plate temperature as the "case" temperature creates a slightly conservative result.

A method for determining a junction to board thermal resistance is not defined in the industry. Of the suggestions that have been proposed, the most direct and simple method is the following: The package is soldered to a multilayer printed circuit board with solid power and ground planes to achieve a high thermal conductivity in the x–y plane. The higher thermal conductivity improves the accuracy of the measurement by minimizing the temperature gradients in the vicinity of the package while it is being tested. Any "thermal balls" are connected with vias to the ground plane within the printed circuit board. The printed circuit board is needed for the measurement to provide an easy method to make the necessary electrical connections to the package for the test. The component and printed circuit board are placed on the cold plate as shown in Figure 8 using thermal grease to minimize the thermal resistance between the board and the cold plate.

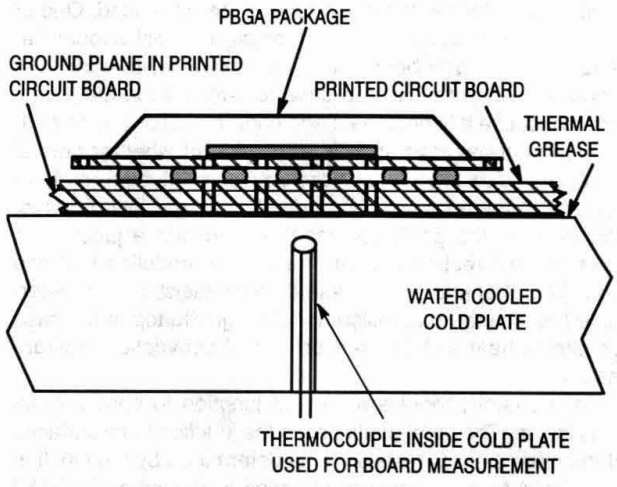
PBGA PACKAGE
GROUND PLANE IN PRINTED CIRCUIT BOARD
PRINTED CIRCUIT BOARD
THERMAL GREASE
WATER COOLED COLD PLATE
THERMOCOUPLE INSIDE COLD PLATE USED FOR BOARD MEASUREMENT

Figure 8.

The junction to board thermal resistance, $R_{\theta JB}$, is then determined by

$$R_{\theta JB} = \frac{(T_J - T_B)}{P}$$

where T_J and T_B are the junction and board temperatures respectively, and P is the power dissipated in the package. Again, a more consistent measurement is obtained by using the cold plate temperature as the board temperature.

The usefulness of the technique can be judged by comparing the junction to board thermal resistance results obtained by the slope and intercept of that data fitted to the two resistor model to the junction to board thermal resistance determined by the cold plate technique. For the two resistor model, the junction to board thermal resistance is determined from the data obtained by the straight line fitted to the data in Figure 7 by the relationship:

$$R_{\theta JB} = \frac{R_{\theta JA0}}{S}$$

To make the judgment easier, the results were compared for the 119 lead 14 x 22 mm, 225 lead 27 x 27mm, and the 357 lead 25 x 25 mm PBGA. The following table gives the junction to board thermal resistance as determined by the two methods for the three different PBGA packages:

Package	Two ResistorModel	Cold Plate
119 Lead	9.8	10.8
225 Lead	8.3	7.4
357 Lead	6.6	7.3

As can be seen, the two methods give a result that is within 1°C/watt. Hence, the choice of techniques should be determined by ease of use except for those cases where testing under the actual heat flow paths is necessary. Testing using actual application environments is appropriate for cases at the conditions of extreme power dissipation or unusual heat sink and convection configurations.

The cold plate method for determining the junction to board thermal resistance is quicker and easier since it is a relatively quick single point measurement instead of requiring some 4 to 8 wind tunnel measurements per sample tested. If it was necessary to test all parts using the two resistor model in the wind tunnel, more wind tunnels would be required within Motorola to meet the package test needs. More importantly, the cold plate technique represents a relatively easy environment to duplicate in simulation to verify the accuracy of simplified models being used in board level simulations. It is also a much easier test environment to explain to a customer.

CONCLUSION

Theta JA determined by the traditional methods provides a comparison of the thermal performance of a package. To be useful to calculate junction temperature, it must be referenced to the board temperature on which the package is mounted. Especially with the PBGA packages, the thermal performance is largely determined by the board temperature to which the package is mounted.

The two resistor thermal model is a simplification of the actual thermal performance of the package, but has been shown to provide an adequate description of the performance of the package over a wide range of environments. The components of the two resistor model can be measured or simulated using the cold plate environment to force essentially all of the heat flow along the path being measured. We are proposing that this two resistor model be made available to designers for use in board level modeling tools for their determination of the board temperatures, Theta JA, and junction temperatures in their application environment.

ACKNOWLEDGEMENTS

The authors would like to thank Jim Andrews, Howard Berg, and Mali Mahalingam for their valuable suggestions during the course of this study. Terry Burnette, Glenn Dody, Vern Hause, R.W. Lawson (APDAC), Gary Lewis, Jay Liu, Brian Miller, Vic Nomi, John Pastore, Ruth Reinhardt, and Y–T Wen are acknowledged for their support in manufacturing the packages and test boards, and during testing.

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9. JEDEC JC15.1 committee is currently writing specification for thermal characterization of surface mount integrated circuits.

AN1243

Output Loading Effects on Fast Static RAMs

Prepared by: Allan Klaus

INTRODUCTION

This review describes the ac loading used for testing. Component test engineers should pay careful attention to the test conditions and derating curves for deviations from the specified load. This information is also applicable for system engineers calculating required device speed for a given environment. This information will help the user make the appropriate choice of device performance for their needs.

As device access times decrease, so do output transition times. With faster rise and fall times come additional problems associated with output and signal path impedances. In any system running at frequencies where the propagation delay of a signal path (t_{pd}) is greater than 1/2 of the total signal transition time, transmission line effects will be seen on the signal. This results in overshoot and undershoot at the load end of a conductor, which can cause problems in testing, or in actual use of the device. This discussion gives a brief overview of the factors contributing to these effects, and the measures that can be used to predict or eliminate them. For a detailed discussion of both PC board layout considerations and applicable transmission line theory, consult the *MECL System Design Handbook*, publication HB205/D, Motorola, Inc., 1983.

DEFINITION OF TERMS

t_{pd} — Propagation delay in seconds
L_0 — Inductance in henries/meter
C_0 — Capacitance in farads/meter
R_L — Load resistance in ohms
$R_{DS(on)}$ — Resistance from drain to source of a FET device when on
R_O — Output resistance in ohms. For CMOS devices, this is the $R_{DS(on)}$ resistance of the output devices.
R_{OH} — Output resistance for a high, or 1, signal from the device
R_{OL} — Output resistance for a low, or 0, signal from the device
ρ_L — Reflection coefficient of the load end of a signal
ρ_S — Reflection coefficient of the source end of a signal, the device output
V_L — Termination voltage of the load resistor in a transmission line termination network

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TRANSMISSION LINE OVERVIEW

What is a transmission line and how does it affect output waveforms? In simple terms, a transmission line is a signal path that exhibits a characteristic impedance. The type of lines discussed in this paper are primarily microstrip (Figure 1) and stripline signal paths (Figure 2) found in most PC boards today. The inductance and capacitance of these lines are a function of the line thickness and width in combination with the dielectric properties of the PC board material and the distance of the line from the ground plane. The impedance of the line is determined by these characteristics and the additional distributed capacitance from other devices on the line.

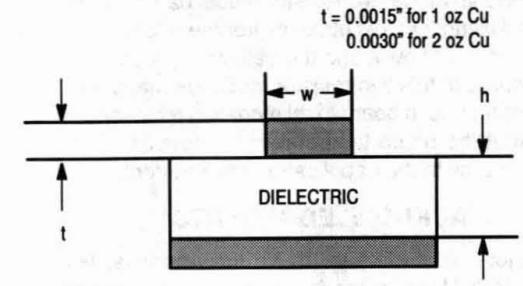

Figure 1. Microstrip Signal Path

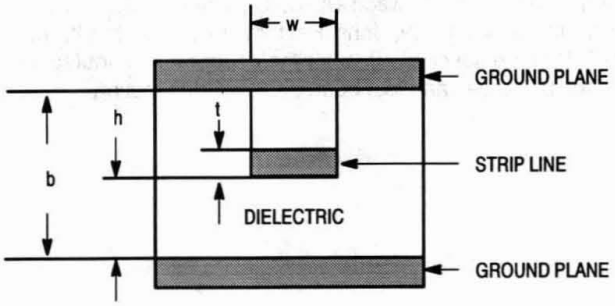

Figure 2. Stripline Signal Path

The characteristic impedance of a microstrip or stripline path is given by the formula $Z_0 = \sqrt{L_0 / C_0}$. The propagation delay of the path, t_{pd}, is $t_{pd} = \sqrt{L_0 / C_0}$ x length = Z_0 C_0 x length. For example, the propagation delay of a microstrip line on G10 epoxy/glass material is approximately 1.76 ns/ft, while the delay for a stripline is about 2.27 ns/ft.

The effect of a transmission line on a device output depends on the electrical length of the line. In all cases, a signal traveling down the line will be affected at the end of the line if it is not terminated with a resistor of the characteristic impedance of the line. The amount of effect is determined by the reflection coefficient of the load, ρ_L, where:

$$\rho_L = \left(\frac{R_L - Z_0}{R_L + Z_0}\right) \quad (1)$$

This reflection occurs at a time t_{pd} after a change at the source of the signal. A similar reflection occurs at $2t_{pd}$ after this new signal has returned from the load to the source, and is determined by the source reflection coefficient, ρ_S, where:

$$\rho_S = \left(\frac{R_O - Z_0}{R_O + Z_0}\right) \quad (2)$$

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R_O is the output resistance of the device. In the case of an electrical line length with t_{pd} less than 1/2 of the rise/fall time of the output signal, the transmission line effects are seen as a delay of the signal transition times. This is caused by the load reflection returning to the source during the actual signal transition and being included in the duration of the signal. For the case of an electrical length with t_{pd} greater than 1/2 of the rise/fall time of the output signal, the reflection effects may be seen directly. In severe cases, signal overshoot or undershoot can cause an invalid level to be seen at the load end at $3t_{pd}$.

The formulas for determining reflection coefficients require knowledge of the output impedance of the device, the characteristic impedance of the signal path, and the termination resistance. The goal of termination is to guarantee that the output signal at the receiving end (load) has enough margin to keep reflection effects from causing a false level to be detected. In an ideal case, the termination resistance is equal to the characteristic impedance of the line, and therefore, no reflection is generated at the load. In that one case, the impedance mismatch at the source is of importance only for signal rise time, V_{OH} and V_{OL} considerations.

The effect of additional distributed capacitance on a transmission line is a reduction in impedance resulting in little change to t_{pd}. This additional capacitance does, however, change the signal transition times resulting in a longer rise and fall time.

OUTPUT BUFFERS

The schematic drawing for a typical CMOS TTL output buffer is shown in Figure 3. Figure 4 shows the equivalent circuit as actually implemented in many devices. The actual values for R_{OH} and R_{OL} vary from design to design but the range of values is similar.

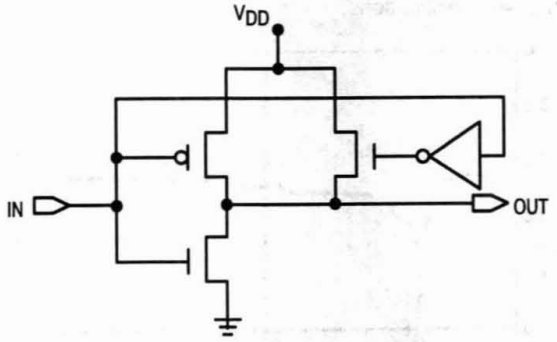

Figure 3. Typical Output Buffer

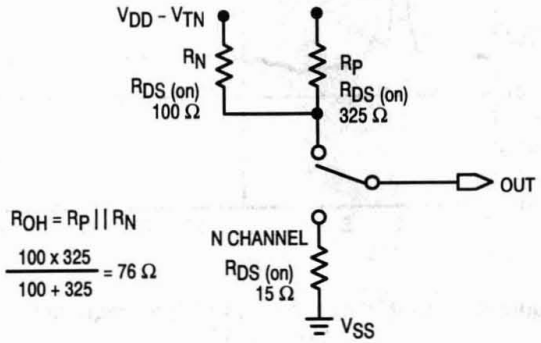

Figure 4. Effective Circuit

As can be seen from Figures 3 and 4, the output impedance of a TTL output buffer is different for high and low output signals. This relation, along with the choice of V_{DD} level, termination resistance, and voltage determine the output high and low levels the part will produce in the system. In a dc condition with $R_L = 50\ \Omega$ = and $V_L = 1.5$ V, the output voltages would be:

$$V_{OL} = V_{SS} + (V_L - V_{SS})\left(\frac{R_{OL}}{R_{OL} + R_L}\right)$$

$$V_{OL} = 0\text{ V} + (1.5\text{ V} - 0\text{ V})\left(\frac{15\ \Omega}{15\ \Omega + 50\ \Omega}\right)$$

$$V_{OL} = 0.35\text{ V} \qquad (3)$$

$$V_{OH} = V_L + \left(V_{DD} - V_L - V_{TN}\ \frac{R_P}{R_P + R_N}\right)\left(\frac{R_L}{R_L + R_{OH}}\right)$$

$$V_{OH} = 1.5\text{ V} + \left(4.4\text{ V} - 1.5\text{ V} - 1.2\text{ V})\ \frac{325\ \Omega}{100\ \Omega + 325\ \Omega}\right)$$

$$\left(\frac{50\ \Omega}{50\ \Omega + 76\ \Omega}\right)$$

$$V_{OH} = 2.33\text{ V} \qquad (4)$$

TRADITIONAL TTL OUTPUT LOAD SPECIFICATIONS

The output loading typically specified in the industry until now is shown in Figure 5. The load consists of a resistor network and capacitance. The values for the network were chosen to present a dc load of 8 mA during an output low condition ($V_{OL} \leq 0.4$ V) and – 4 mA for an output high ($V_{OH} \geq 2.4$ V). A 5 V supply was chosen as the termination supply and a divider network was calculated to provide the specified currents. In addition, a lumped capacitive load of 30 pF was added to the output to represent input loading from other devices. In actual practice during testing, the load used is a Thevenin equivalent as shown in Figure 6, with capacitance being provided by the 50 Ω transmission line connection to the test head and the test fixture capacitance.

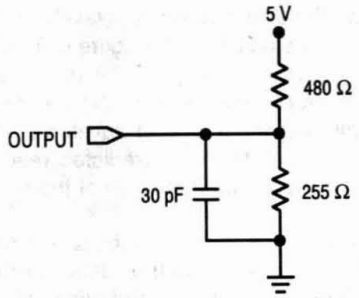

Figure 5. Typical TTL Load

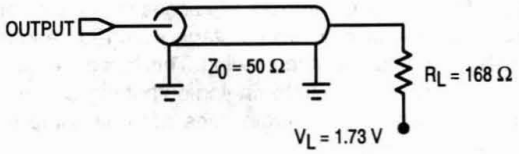

Figure 6. Thevenin Equivalent Test Load

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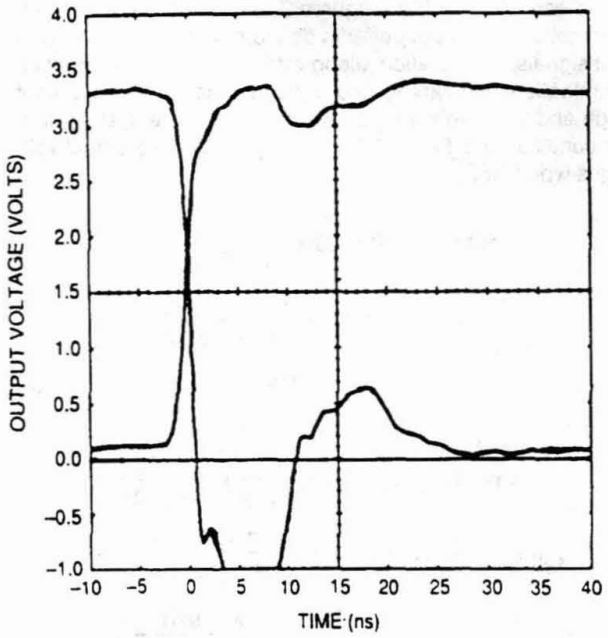

Figure 7. Output Waveforms with Thevenin Equivalent Test Load

The calculated performance of the setup would be that of a transmission line with a Z_0 of 50 Ω terminated to an R_L of 168 Ω at a V_L of 1.73 V. This would be $\rho_L = (168\ \Omega - 50\ \Omega) / (168\ \Omega + 50\ \Omega) = 0.54$. This means that the ΔV at the load would be 154% of the source ΔV. Using the example output buffer with V_{DD} = 5.0 V, the dc V_{OL} would be 0.14 V and the incident V_{OH}, using the 50 Ω from Z_0 in place of R_L, would be 2.67 V, giving a ΔV of 2.53 V. The means that for a low to high going signal at the source, at time t_{pd} later, the load would go to V_{OL} + ΔV + (ΔV x 0.54), or 4.01 V.

Figure 7 shows the actual measured waveform at the load end of a test fixture as described in Figure 6. The t_{pd} of the signal path is measured using a TDR (time domain reflectometer) to be approximately 4 ns. Notice the reflection effects at each multiple of t_{pd} on both waveforms. The actual measured waveforms differ from predicted results due to inductance in the ground and V_{DD} path of the device being tested.

In a testing environment, the t_{pd} is subtracted from the time measured to give the actual output delay of the device (access time). Because of this, the distortions at the device output are of no concern. The ringing at the load end, however, can cause severe problems when trying to accurately test the speed of the parts. In the past, the access time has been measured from some mid–level voltage which is centered between the high and low output swing. This has the effect of giving the most noise margin to ringing output signals. However, this maximum noise margin does not guarantee that problems will not arise.

NEW HIGH FREQUENCY AC TEST LOAD

In order to properly test and guarantee the ac performance of these fast static RAMs, it is necessary to change the conditions for ac loading to a load that will allow accurate evaluation of the device parameters. Because of this, the specified ac load is now a transmission line terminated with a resistor of the characteristic impedance of the line to a load voltage (see Figure 8).

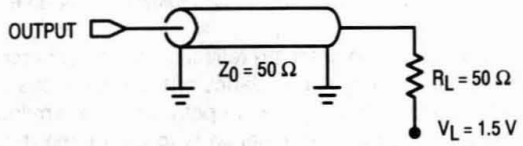

Figure 8. New High Frequency AC Test Load

The calculated performance of this load in a normal test environment would be $\rho_L = (50\ \Omega - 50\ \Omega) / (50\ \Omega - 50\ \Omega) = 0.0$. This means that the ΔV at the load would be the same as the source ΔV with no signal reflection.

As seen in Figure 9, using a transmission line terminated to a load supply through a resistor equal to the characteristic impedance of the line produces a load waveform that matches the source signal. Additionally, under ideal conditions, no reflection effects are produced with this load. This results in the maximum possible noise margin for both test and system environments. In this test setup, power supply inductance causes some output noise which is seen at the load.

Figures 10 and 11 are derating curves for calculating the effects of varying C_0 and R_L. These curves are based on typical device performance and are not intended to be absolute worst case specifications.

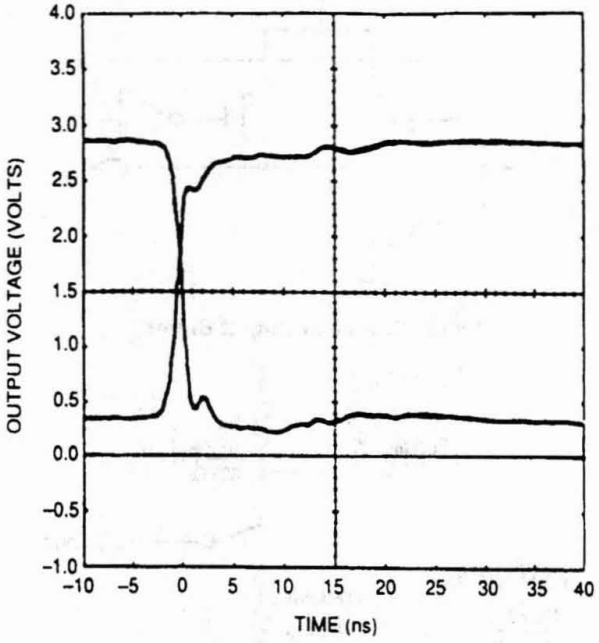

Figure 9. Output Waveforms with High Frequency AC Test Load

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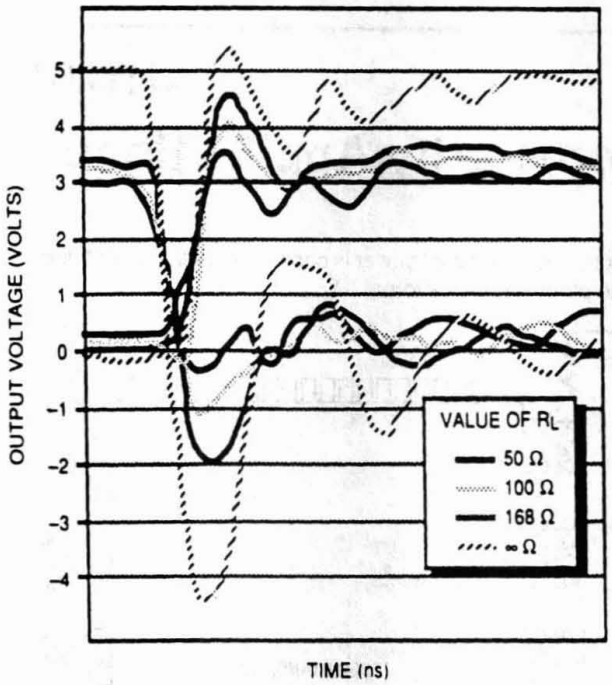

Figure 10. Output Voltage as a Function of R_L

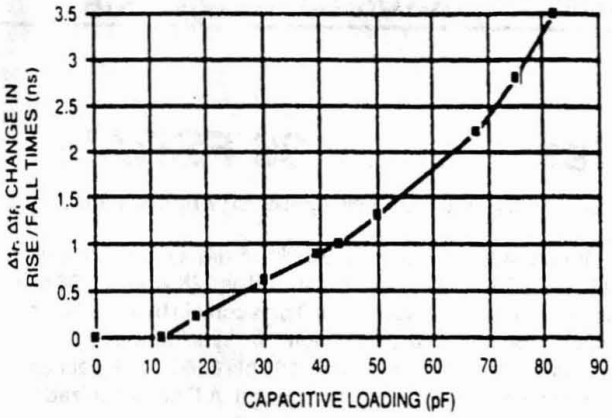

Figure 11. Change in Output Rise and Fall Times for Lumped Capacitive Loads

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AN1261

Use of 32K x 36 FSRAM in Non–Parity Applications

Prepared by: Michael Peters, FSRAM Applications Engineer

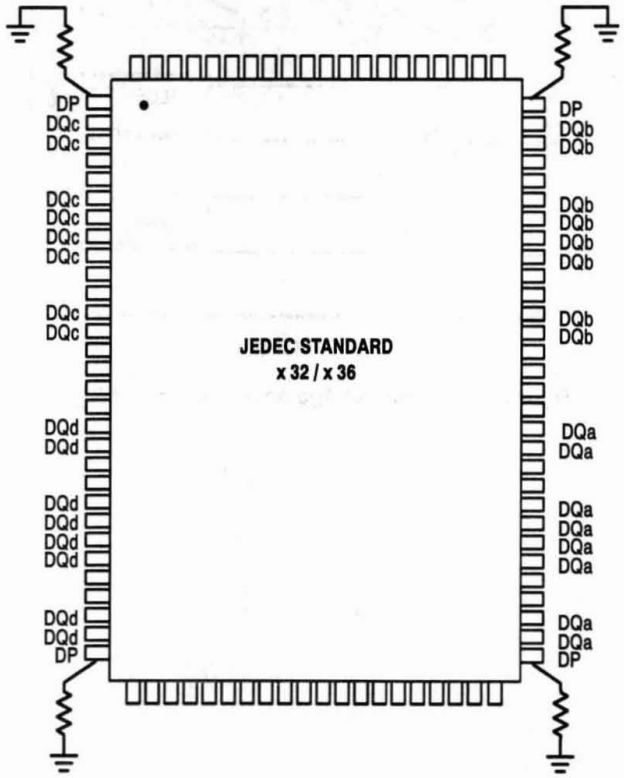
The MCM69F536 and MCM69P536 are synchronous fast static BurstRAMs™ that are organized as 32K words of 36 bits (or four bytes wide) each. The I/O pins contain byte parity. The JEDEC standard pin assignment for synchronous SRAMs defines the corner I/O pins of the 100 pin QFP/TQFP package as either a parity I/O or as a no connect. A RAM organized as 32 bits wide is achieved by making the corner I/O pins no connect.

Motorola's MCM69F536, MCM69P536, and future x36 BurstRAMs can be used in non–parity applications by simply making one of the following two design choices.

1. Connect pulldown (or pullup to 3.3 V V_{CC}) resistors to V_{SS} on the parity I/O pins. The recommended resistor value should be within the 1 kΩ to 10 kΩ range. This is the recommended design choice.

2. Allow the parity I/O pins to be left open circuit. This is not the recommended design choice. One might experience problems associated with floating I/O pins, such as an increase in I_{CC} current.

In general, the use of pulldown/pullup (strap) resistor values closer to 1 kΩ are preferred, since they provide a lower impedance to ac ground (V_{SS} or V_{CC}) and therefore less susceptible to its neighboring pin's noise. The drawback is slightly increased power consumption. However, this additional power is consumed only during the initial read/write cycles after power–up. The array bit pattern upon power–up will be random, so the resistor straps draw current only during read cycles in which the output drives to the opposite state of the strap voltage. During write cycles, the resistor straps insure the parity bits are written with a binary 0 or 1 dependent upon the strap voltage chosen. Subsequent read cycles will return the same binary value that was previously written by the resistor strap. After the entire 32K memory words have been written, no additional power is consumed by the SRAM due to the parity strap resistors.



JEDEC Standard Pin Assignment and Parity Bit Resistors Connected to Ground

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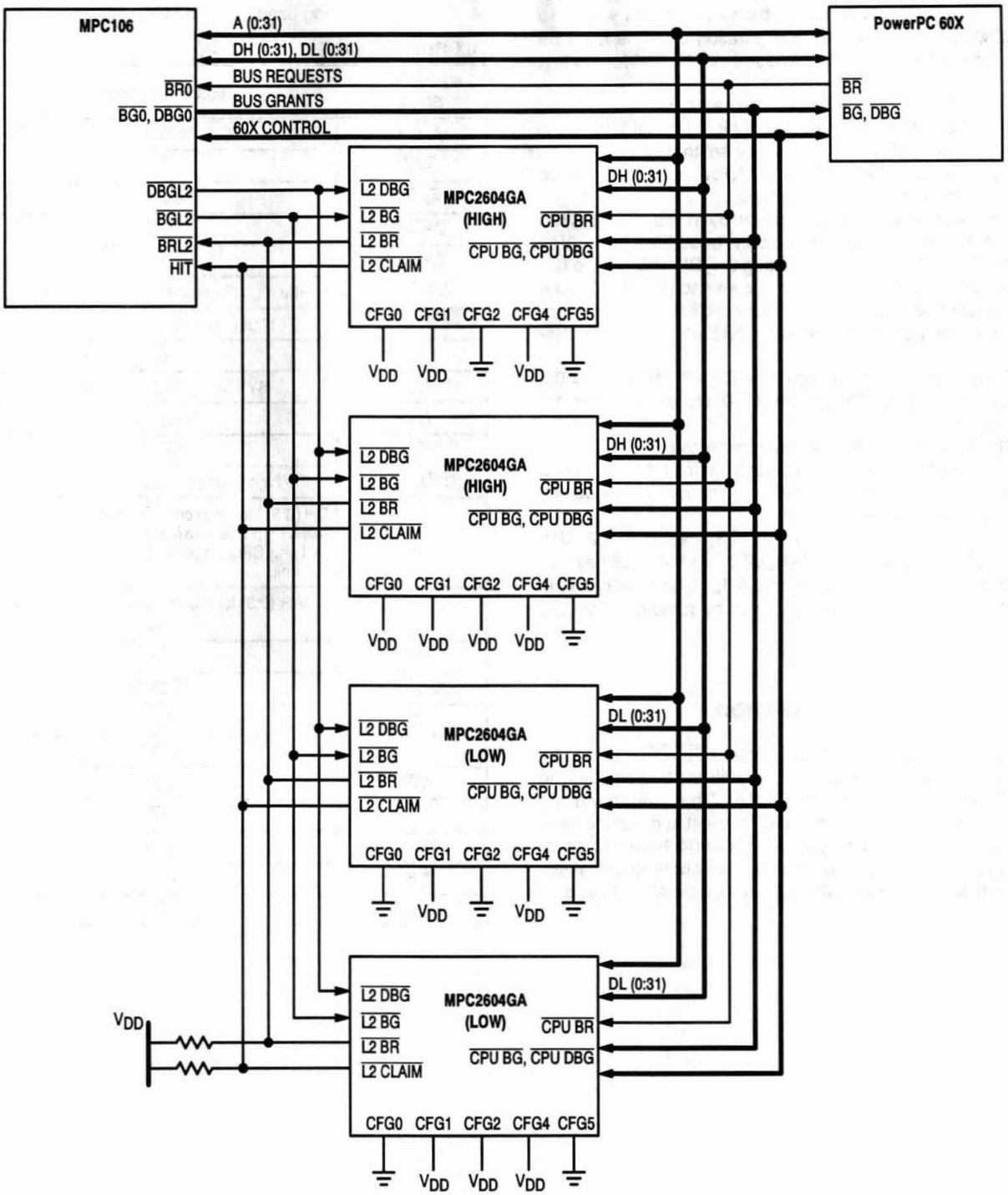
BurstRAM is a trademark of Motorola, Inc.

3/27/96

SYSTEM BLOCK DIAGRAM FOR A 512KB MPC2604GA SOLUTION IN 2–1–1–1 MODE



CONFIGURATION REGISTER BITS

Certain bits in the processor interface configuration register in the MPC106 have to be set to work with the MPC2604GA. Note: These configuration changes must be made before the MPC2604GA asserts $\overline{\text{L2 CLAIM}}$ for the first time.

1. CF_APHASE_WS (1..0) must be set to 00.
2. CF_LOOP_SNOOP must be set high. (default)
3. CF_L2_HIT_DELAY (1..0) must be set to 01.
4. The setting of CF_FAST_L2_MODE should be set to match the processor after a reset.
5. The best performance is achieved by having the MPC106 park the data bus. This can be done by setting CF_APARK and CF_DPARK to 1 and setting CF_BREAD_WS to 0.
6. Since the MPC2604GA has its own cache controller, the controller on the MPC106 must be disabled. This is accomplished by setting bit CF_EXTERNAL_L2 = 1. (default)
7. For a uniprocessor system, bits CF_L2_MP (1..0) = 00. For MP systems, CF_L2_MP (1..0) should be set to 11. (default)
8. CF_CBA_MASK (31..24) must be set to 0xFF.
9. In a system using a 603 running in 1:1 bus mode, CF_BREAD_WS must be set to 1 in normal bus mode or 2 in no-$\overline{\text{DRTRY}}$ mode.

The registers L2_CACHE_MISS_INHIBIT, L2_UPDATE_INHIBIT, and CF_FLUSH_L2 in the MPC106 have no effect on the MPC2604GA. To obtain this functionality on the MPC2604GA, they must be generated by some other device.

INITIALIZATION

To ensure proper initialization, the $\overline{\text{HRESET}}$ pin on the MPC2604GA should be tied to the same line that connects to the $\overline{\text{HRESET}}$ pin on the processor. This will cause the MPC2604GA and the processor to be reset at the same time. Once $\overline{\text{HRESET}}$ is pulled high, the MPC2604GA begins an internal configuration sequence that lasts about 4000 cycles. During this time, the MPC2604GA will ignore all bus transactions.

CONNECTION LIST

The following MPC2604GA signals must be connected to the 60x bus as shown regardless of whether the MPC2604GA is being used with the MPC106.

60X BUS SIGNALS

MPC2604GA Signals	60X Bus Signals
A (0:31)	A (0:31)
$\overline{\text{AACK}}$	$\overline{\text{AACK}}$
$\overline{\text{ARTRY}}$	$\overline{\text{ARTRY}}$
$\overline{\text{CPU BG}}$	$\overline{\text{BG0}}$
$\overline{\text{CPU BR}}$	$\overline{\text{BR0}}$
$\overline{\text{CPU2 BG}}$	Tie high (if uniprocessor), $\overline{\text{BG1}}$ (if MP)
$\overline{\text{CPU2 BR}}$	Tie high (if uniprocessor), $\overline{\text{BR1}}$ (if MP)
$\overline{\text{CI}}$	$\overline{\text{CI}}$
CLK	SYSCLK (the 60X bus clock)
$\overline{\text{DBB}}$	10K pullup
$\overline{\text{CPU DBG}}$	$\overline{\text{DBG0}}$
$\overline{\text{CPU2 DBG}}$	Tie high (if uniprocessor), $\overline{\text{DBG1}}$ (if MP)
D (0:31)	DH (0:31) for high chip, DL (0:31) for low chip. Note, high chip and low chip are differentiated by tying CFG0 high for high chip and low for low chip.
DP (0:3)	PAR (0:3) for high chip, PAR (4:7) for low chip
$\overline{\text{HRESET}}$	$\overline{\text{HRESET}}$
$\overline{\text{SRESET}}$	$\overline{\text{SRESET}}$
$\overline{\text{TA}}$	$\overline{\text{TA}}$
$\overline{\text{TBST}}$	$\overline{\text{TBST}}$
$\overline{\text{TEA}}$	$\overline{\text{TEA}}$
$\overline{\text{TS}}$	$\overline{\text{TS}}$
TSIZ (0:2)	TSIZ (0:2)
TT (0:4)	TT (0:4)
$\overline{\text{WT}}$	$\overline{\text{WT}}$

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MPC2604GA TO MPC106 INTERFACE

The following is a list of MPC2604GA pins and how they should be connected when used with the MPC106.

MPC2604GA Signals	Connect to:
Arbitration Sideband Signals	
$\overline{\text{L2 BR}}$	$\overline{\text{BRL2}}$ (MPC106)
$\overline{\text{L2 BG}}$	$\overline{\text{BGL2}}$ (MPC106)
$\overline{\text{L2 CLAIM}}$	$\overline{\text{HIT}}$ (MPC106)
$\overline{\text{L2 DBG}}$	$\overline{\text{DBGL2}}$ (MPC106)
ASYNCHRONOUS SIGNALS Not Supplied By The MPC106. If these are not supplied by any other chip in the system, they should be tied in the following manner.	
$\overline{\text{L2 MISS INH}}$	Tie High
$\overline{\text{L2 TAG CLR}}$	Tie High
$\overline{\text{L2 UPDATE INH}}$	Tie High
$\overline{\text{L2 FLUSH}}$	Tie High
PWRDN	Tie Low
Configuration and Testability Pins	
CFG0	High for high chip, low for low chip.
CFG1	Low for 256KB, high for 512KB
CFG2	Only used for 512KB solution: tie low for one pair high/low chips, tie high for the other pair
CFG4	Tie High
CFG5	Tie Low
TCK	JTAG
TDI	JTAG
TDO	JTAG
TMS	JTAG
$\overline{\text{TRST}}$	JTAG
Interchip Communication	
$\overline{\text{FDN}}$	Tie between all MPC2604GA chips and to pullup

8

AN1268

DSP5630x FSRAM Interfacing

Prepared by: Ian Forsyth, FSRAM Applications,
Motorola Ltd., East Kilbride, Scotland

INTRODUCTION

Due to ever increasing complexity of executable code, several applications based on Digital Signal Processors are requiring higher and higher performance in terms of execution speed. To accommodate these requirements, Motorola has developed a 24–bit DSP family and several memory support chips to provide cost effective, high performance solutions.

This document describes several options of interfacing different Asynchronous Fast Static RAMs to the Motorola 24–bit DSP5630x family.

DSP56300 CORE DESCRIPTION

The DSP56300 is the powerful New DSP Engine (NDE) core capable of executing an instruction on every clock cycle, thus yielding a twofold performance increase compared to the 56K core while maintaining 100% object code compatibility with it.

The DSP56300 CMOS core is composed of the Expansion Port and DRAM Controller, Data ALU, Address Generation Unit, Instruction Cache Controller, Program Control Unit, DMA Controller, PLL Clock Oscillator, On–Chip Emulator, and the Peripheral and Memory Expansion Bus.

To minimize the total system cost, the DSP56300 core incorporates a versatile external memory interface that provides glueless interface to a variety of memories such as Dynamic RAMs (DRAMs), Static RAMs (SRAMs), and Synchronous Static RAMs (SSRAMs).

PORT A INTRODUCTION

Port A of the DSP56301 core is the memory expansion port that can be used either for memory expansion or for memory–mapped I/O. A number of features make port A versatile and easy to use. These features provide a low part–count connection with fast static memories, dynamic memories, I/O devices, and multiple bus master systems.

PORT A PIN DESCRIPTION

Details of the main pins and their functions, which are appropriate for connection to external FSRAM memories, are listed below.

A0 – A23	(Address Bus) — Specifies the address for external program and data memory accesses. To minimize power dissipation, A0 – A23 do not change state when external memory spaces are not being accessed. A0 – A23 are three–stated during reset.
D0 – D23	(Data Bus) — These pins provide the directional data bus for external program and data memory accesses. D0 – D23 are in the high impedance state when there is no external bus activity.
AA(3:0)/ $\overline{\text{RAS}}$(3:0)	(Address Attribute or ROW Address Strobe) — When addressed as Address Attribute, these signals can be used as chip selects or additional address lines. When defined as $\overline{\text{RAS}}$, these signals can be used as Row Address Strobe for DRAM access.
$\overline{\text{RD}}$	(Read Enable) — $\overline{\text{RD}}$ is asserted to read external memory on the data bus (D0 – D23).
$\overline{\text{WR}}$	(Write Enable) — $\overline{\text{WR}}$ is asserted to write external memory on the data bus (D0 – D23).
$\overline{\text{BS}}$	(Bus Strobe) — Active low output when a bus master, three–stated when not a bus master. Asserted at the start of a bus cycle (for half of a clock cycle), providing an "early bus start" signal for a bus controller. If the external bus is not used during an instruction cycle, $\overline{\text{BS}}$ remains negated until the next external bus cycle. $\overline{\text{BS}}$ is three–stated during hardware reset.
CLKOUT	(Clock Output) — This output pin provides an output clock synchronized to the internal clock phase.

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PORT A OPERATION

The port A data bus is 24 bits wide with a separate 24–bit wide address bus capable of sustained rate of one memory access per clock cycle for data space accesses (using synchronous static memory). External memory is divided into 16M x 24 bit space which can be configured as X, Y, and P; or any combination of these. An internal wait state generator can be programmed to insert up to 31 wait states if access to slower memory or I/O device is required. A bus wait signal allows an external device to control the number of wait states inserted in a bus access operation. Bus arbitration signals allow an external device use of the bus while internal operations continue using the internal memory.

The external bus timing is defined by the operation of the Address Bus, Data Bus, and Bus Control pins described in the **Expansion Port Control** section.

EXTERNAL STATIC RAM CONTROL

External bus timing is controlled by the $\overline{TA}$ control signal and by the Bus Control Register (BCR) that is described in the **Port A Control** section. Insertion of wait states is controlled by the BCR to provide constant bus access timing, and by $\overline{TA}$ to provide dynamic bus access timing. The number of wait states for each external access is determined by the input $\overline{TA}$, or by the BCR; whichever is the longer.

The external memory address is defined by the Address Bus A0 – A23 and the Memory Address Attribute signal AA(3:0). The Address Attribute signals have the same timing as the Address Bus and may be used as additional address lines. The Address Attribute signals are also used to generate chip select signals for the appropriate memory chips. These chip select signals change the memory chips from low power standby mode to active mode and begin the access time. This allows slower memories to be used since the Address Attribute signals are addressed–based rather than read or write enable based.

EXPANSION PORT (PORT A) CONTROL

The expansion port control consist of four Address Attribute Registers, the DRAM Control Register, and the Bus Control Register. The Address Attribute Registers and the Bus Control Register will be described in this section.

AA CONTROL REGISTERS (ONE FOR EACH AA PIN)

The four control registers (AAR3, AAR2, AAR1, and AAR0) are 24–bit read/write registers used to control the activity of the AA3 – AA0/$\overline{RAS3}$ – $\overline{RAS0}$ pins. An AA/$\overline{RAS}$ pin is asserted if the address in the appropriate AAR register (BAC bits) matches the external address (the exact number of address bits that are compared is determined by BNC bits, shown in Table 2), and if the external access is aimed to a space (X, Y, or P) that is enabled in the appropriate AAR register. All AAR registers are disabled (all the AAR bits are cleared) during hardware reset. The AAR bits are shown in Figure 1 and described in the following paragraphs.

A priority mechanism exists among the four AAR control registers in order to resolve selection conflicts. AAR3 has the highest priority and AAR0 has the lowest priority (e.g., if the external address matches the address and the space that is specified in both AAR1 and AAR2, the external access type will be selected according to the AAR2 register). The priority mechanism allows continuous partition of the external address space.

When the AA/$\overline{RAS}$ pin functions as AA pin, it is negated at the start of the next clock cycle only if there is no external access that uses the same AA pin (i.e., the AA pin will be kept asserted in a sequence of two consecutive external accesses that access the same memory bank). This method enables the use of low power standby mode in the external memories (these memories should be accessed first by a dummy access).

The programmer should guarantee an AAR register is not changed while accessing the memory selected by this AAR; otherwise, improper operation may result.

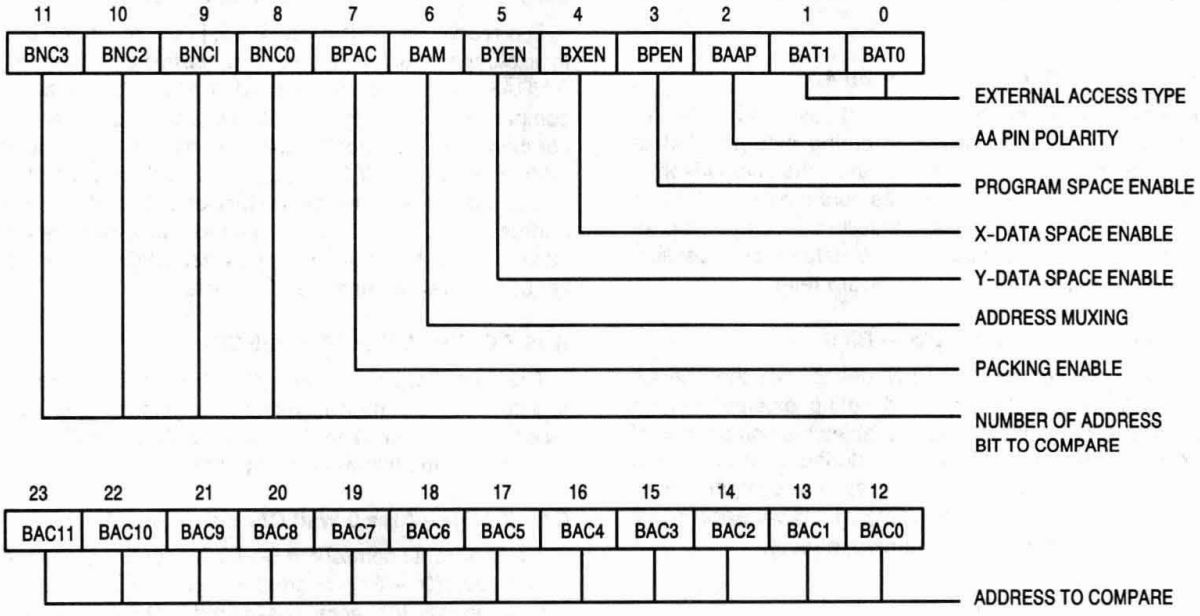
11 10 9 8 7 6 5 4 3 2 1 0
BNC3 BNC2 BNCI BNC0 BPAC BAM BYEN BXEN BPEN BAAP BAT1 BAT0
EXTERNAL ACCESS TYPE
AA PIN POLARITY
PROGRAM SPACE ENABLE
X-DATA SPACE ENABLE
Y-DATA SPACE ENABLE
ADDRESS MUXING
PACKING ENABLE
NUMBER OF ADDRESS BIT TO COMPARE
23 22 21 20 19 18 17 16 15 14 13 12
BAC11 BAC10 BAC9 BAC8 BAC7 BAC6 BAC5 BAC4 BAC3 BAC2 BAC1 BAC0
ADDRESS TO COMPARE

Figure 1. Address Attribute Registers (AAR3 – AAR0)

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BAT(1:0) — External Access Type and Pin Definition — Bits 1 – 0

The read/write control bits BAT(1:0) define the external access type (DRAM, SRAM, or SSRAM) to the area defined by BAC(11:0), BYEN, BXEN, and BPEN bits. The encoding of BAT1 – BAT0 is described in Table 1.

When the external access type is defined as DRAM access (BAT(1:0) = 10) the AA/$\overline{RAS}$ pin will act as an $\overline{RAS}$ pin; otherwise, it will act as an AA pin. External accesses to the default area will always be executed as if they are SRAM accesses; i.e., BAT(1:0) of the default area equals 01 (i.e., static RAM access).

Table 1. External Access Selection

BAT1	BAT0	External Access Type
0	0	Synchronous SRAM access
0	1	Static RAM access
1	0	DRAM access
1	1	Reserved

BAAP — AA Pin Polarity — Bit 2

The read/write control bit, BAAP, defines whether the AA/$\overline{RAS}$ pin is active low or active high. When BAAP is cleared, the AA/$\overline{RAS}$ pin is active low (useful for enabling memory modules, or for DRAM row address strobe). If BAAP is set, the appropriate AA/$\overline{RAS}$ pin is active high (useful as additional address bit). The BAAP bit is cleared during hardware reset.

BPEN — Program Space Enable — Bit 3

The read/write control bit, BPEN, defines whether the AA/$\overline{RAS}$ pin and logic should be activated during external program space accesses. When set, BPEN enables the comparison of the external address to the BAC bits during external program space accesses. If BPEN is cleared, no comparison of address is performed during external program space accesses. The BPEN bit is cleared during hardware reset.

BXEN — X–Data Space Enable — Bit 4

The read/write control bit, BXEN, defines whether the AA pin and logic should be activated during external X–data space accesses. BXEN when set enables the comparison of the external address to the BAC bits during external X–data space accesses. If BXEN is cleared, no comparison of address is performed during external X–data space accesses. The BXEN bit is cleared during hardware reset.

BYEN — Y–Data Space Enable — Bit 5

The read/write control bit, BYEN, defines whether the AA pin and logic should be activated during external Y–data space accesses. BYEN when set enables the comparison of the external address to the BAC bits during external Y–data space accesses. If BYEN is cleared, no comparison of address is performed during external Y–data space accesses. The BYEN bit is cleared during hardware reset.

BAM — Address Muxing — Bit 6

The read/write control bit, BAM, defines whether the eight least significant (LS) bits of the address will appear on A7 – A0 pins (LS portion of the external address bus), or on A23 – A16 pins (MS portion of the external address bus). When BAM is set, the eight LS bits will appear on A23 – A16 pins. When BAM is cleared, the address will appear normally and will occupy the entire external address bus (A23 – A0). This feature enables connection to an external peripheral to the most significant bits of the address, thus decreasing the load on the LSP of the external address and enabling more efficient interface to external memories. BAM is ignored during DRAM access (BAT1=1). The BAM bit is cleared during hardware reset.

BPAC — Packing Enable — Bit 7

The read/write control bit, BPAC, enables (when set) the internal packing/unpacking logic. In this mode, each DMA external access will initiate three external accesses to an 8–bit wide external memory (the address of these accesses will be the original DMA address — the DAB, then DAB+1, and then DAB+2). The packing to a 24–bit word (or the unpacking from 24–bit word to three 8–bit words) is done automatically by the expansion port control hardware. The external memory should reside in the eight least significant bits of the external data bus, and the packing (or unpacking for external write accesses) is done least significant byte first (i.e., the first data byte is the LS byte, the second is the middle byte, and the last is the MS byte). When this bit is cleared, the expansion port control logic assumes a 24–bit wide external memory.

BNC(3:0) — Number of Address Bits to Compare — Bits 11 – 8

The read/write control bits, BNC(3:0), defines the number of bits (from the BAC bits) that are compared to the external address. If no bits are compared (BNC(3:0) = 0000) the AA pin is activated only according to the space enable bits (BPEN, BXEN, and BYEN). The combinations BNC(3:0) = 1111, 1110, 1101 are reserved. The BCN(3:0) bits are cleared during hardware reset.

BAC(11:0) — Address to Compare — Bits 23 – 12

The read/write control bits, BAC(11:0), define the address to be compared to the external address in order to decide if the AA/$\overline{RAS}$ pin should be asserted. The number of bits to be compared is defined by the BNC(3:0) bits; BAC bits are always compared to the most significant portion of the external address bus (e.g., if BNC(3:0) = 0011, then BAC(11:9) are compared to the three most significant bits of the external address). BAC(11:0) bits are cleared during hardware reset. Table 2 details the relationship between BNC bits and the consequential BAC compare address bits.

BUS CONTROL REGISTER (BCR)

The Bus Control Register (BCR) is a 24–bit read/write register used to control the external bus activity and Bus Interface Unit operation. The BCR bits are shown in Figure 2 and described in the following paragraphs.

BA0W(4:0) — Area 0 Wait Control — Bits 4 – 0

The read/write control bits BA0W(4:0) define the number of wait states (0 – 31) inserted in each external SRAM or synchronous SRAM accesses to area 0 (DRAM accesses are not affected by these bits). Area 0 is the area defined by the AAR0 register. For SRAM accesses only, the value of these

Table 2. Address to Compare

	Compare Address											
	Add Bit 23	Add Bit 22	Add Bit 21	Add Bit 20	Add Bit 19	Add Bit 18	Add Bit 17	Add Bit 16	Add Bit 15	Add Bit 14	Add Bit 13	Add Bit 12
BNC3:0	BAC11	BAC10	BAC9	BAC8	BAC7	BAC6	BAC5	BAC4	BAC3	BAC2	BAC1	BAC0
1111	RESERVED											
1110	RESERVED											
1101	RESERVED											
1100	C	C	C	C	C	C	C	C	C	C	C	C
1011	C	C	C	C	C	C	C	C	C	C	C	
1010	C	C	C	C	C	C	C	C	C	C		
1001	C	C	C	C	C	C	C	C	C			
1000	C	C	C	C	C	C	C	C				
0111	C	C	C	C	C	C	C					
0110	C	C	C	C	C	C						
0101	C	C	C	C	C							
0100	C	C	C	C								
0011	C	C	C									
0010	C	C										
0001	C											
0000												

NOTE: A "C" in the table represents a compare is made with this BAC bit. Refer to Figure 1.

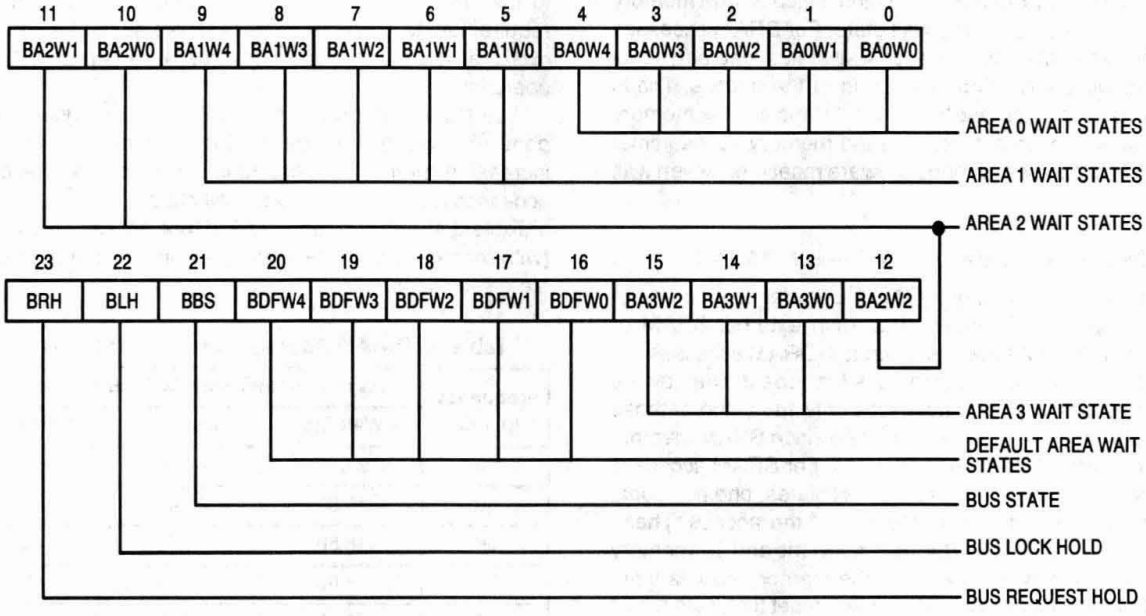
11 10 9 8 7 6 5 4 3 2 1 0
BA2W1 BA2W0 BA1W4 BA1W3 BA1W2 BA1W1 BA1W0 BA0W4 BA0W3 BA0W2 BA0W1 BA0W0
AREA 0 WAIT STATES
AREA 1 WAIT STATES
AREA 2 WAIT STATES
23 22 21 20 19 18 17 16 15 14 13 12
BRH BLH BBS BDFW4 BDFW3 BDFW2 BDFW1 BDFW0 BA3W2 BA3W1 BA3W0 BA2W2
AREA 3 WAIT STATE
DEFAULT AREA WAIT STATES
BUS STATE
BUS LOCK HOLD
BUS REQUEST HOLD

Figure 2. Bus Control Register (BCR)

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bits should not be programmed as zero since SRAM memory access requires at least one wait state. In addition, when selecting four to seven wait states, one additional wait state will be inserted at the end of the access. When selecting eight or more wait states, two additional wait states will be inserted at the end of the access. These trailing wait states increase the data hold time and the memory release time, but do not increase the memory access time. BA0W(4:0) bits are set during hardware reset (i.e., 31 wait states).

BA1W(4:0) — Area 1 Wait Control — Bits 9 – 5

The read/write control bits, BA1W(4:0), define the number of wait states (0 – 31) inserted in each external SRAM or synchronous SRAM accesses to area 1 (DRAM accesses are not affected by these bits). Area 1 is the area defined by the AAR1 register. For SRAM accesses only, the value of these bits should not be programmed as zero since SRAM memory access requires at least one wait state. For SRAM accesses only, when selecting four to seven wait states, one additional wait state will be inserted at the end of the access. When selecting eight or more wait states, two additional wait states will be inserted at the end of the access. These trailing wait states increase the data hold time and the memory release time and do not increase the memory access time. BA1W(4:0) bits are set during hardware reset (i.e., 31 wait states).

BA2W(2:0) — Area 2 Wait Control — Bits 12 – 10

The read/write control bits, BA2W(2:0), define the number of wait states (0 – 7) inserted in each external SRAM or synchronous SRAM accesses to area 2 (DRAM accesses are not affected by these bits). Area 2 is the area defined by the AAR2 register. For SRAM accesses only, the value of these bits should not be programmed as zero since SRAM memory access requires at least one wait state. For SRAM accesses only, when selecting four to seven wait states, one additional wait state will be inserted at the end of the access. These trailing wait states increase the data hold time and the memory release time and do not increase the memory access time. BA2W(2:0) bits are set during hardware reset (i.e., seven wait states).

BA3W(2:0) — Area 3 Wait Control — Bits 15 – 13

The read/write control bits, BA3W(2:0), define the number of wait states (0 – 7) inserted in each external SRAM or synchronous SRAM accesses to area 3 (DRAM accesses are not affected by these bits). Area 3 is the area defined by the AAR3 register. For SRAM accesses only, the value of these bits should not be programmed as zero since SRAM memory access requires at least one wait state. For SRAM accesses only, when selecting four to seven wait states, one additional wait state will be inserted at the end of the access. These trailing wait states increase the data hold time and the memory release time and do not increase the memory access time. BA3W(2:0) bits are set during hardware reset (i.e., seven wait states).

BDFW(4:0) — Default Area Wait Control — Bits 20 – 16

The read/write control bits, BDFW(3:0), define the number of wait states (0 – 31) inserted in each external accesses to an area which is not defined by any of the BAAR registers. The access type to this area is SRAM only. The value of these bits should not be programmed as zero since SRAM memory access requires at least one wait state. When selecting four to seven wait states, one additional wait state will be inserted at the end of the access. When selecting eight or more wait states, two additional wait states will be inserted at the end of the access. These trailing wait states increase the data hold time and the memory release time and do not increase the memory access time. BDFW(4:0) bits are set during hardware reset (e.g., 31 wait states).

BBS — Bus State — Bit 21

The read only Bus State status bit (BBS) is set when the DSP is the bus master, and is cleared otherwise. The BBS bit is cleared during hardware reset.

BLH — Bus Lock Hold — Bit 22

The read/write control bit Bus Lock Hold (BLH) is used to assert the BL pin even if no read–modify–write access is occurring. When BLH is set, the BL pin is always asserted. If the BLH bit is cleared, the BL pin is asserted only if a read–modify–write external access is attempted. The BLH bit is cleared during hardware reset.

BRH — Bus Request Hold — Bit 23

The read/write control bit Bus Request Hold (BRH) is used to assert the BR pin even if no external access is needed. When BRH is set, the BR pin is always asserted. If the BRH bit is cleared, the BR pin is asserted only if external access is attempted or pending. The BRH bit is cleared during hardware reset.

ASYNCHRONOUS STATIC RAM INTERFACING

Asynchronous Static RAM devices can be easily interfaced to the DSP56300 core bus timing. Due to the Static RAM requirement to keep the address stable during the entire bus cycle, at least one wait state must be instead to the bus operation.

Wait states controlled from BCR or by $\overline{TA}$ signal will postpone the disappearance of the external address, thus increasing memory access time. In all cases, static RAM accesses require at least one wait state.

Table 3 shows the required FSRAM access time required (with respect to DSP frequency) for one, two, and three wait state selections.

Table 3. FSRAM Access Time versus Cycle Time

Frequency in MHz	Asynchronous FSRAM Access Time in ns		
	1 Wait State	2 Wait State	3 Wait State
50	24.40	44.40	64.40
60	18.80	35.40	52.00
66	16.50	31.60	46.80
70	15.00	29.30	43.60
80	12.40	24.80	44.00
90	10.30	21.40	37.30
100	8.70	18.70	27.50

It should be noted that faster access times will be required depending on board layout, buffering, and bus loading. For example, for a typical 66 MHz DSP operation with FSRAMs in close proximity and no buffering, the access time selection is

16.52 ns. Allowing for flight time and skew, the standard RAM speed of 15 ns should meet the requirements. Indeed many applications use this combination successfully.

Typical Static RAM access is composed from the steps listed in Table 4.

Table 4. FSRAM Access

1.	The address A(23:0), address attributes AA(3:0), and bus strobe $\overline{BS}$ are asserted in the middle of CLKOUT high phase.
2.	Write Enable $\overline{WR}$ is asserted when the falling edge of CLKOUT (for a single wait access). Read Enable $\overline{RD}$ is asserted in the middle of CLKOUT low phase.
3.	For write operation: Data driven in the middle of CLKOUT high phase. For read operation: Data is sampled in the middle of the CLKOUT last low phase of the external access.

When the external access type is defined as SRAM, the assertion of the $\overline{WR}$ signal depends on the number of wait states programmed in the BCR. If a single wait state is programmed in the BCR, the $\overline{WR}$ signal is asserted with the falling edge of CLKOUT. If the number of wait states programmed is two or three, $\overline{WR}$ assertion is delayed by half of a clock cycle (half CLKOUT cycle). If the number of wait states programmed is four or more, $\overline{WR}$ assertion is delayed by a full clock cycle. This feature enables the connection of slow external devices that require long address setup times before write assertion in order to prevent false write.

BCLK is negated during asynchronous SRAM access; therefore, all signal timing are related to CLKOUT as depicted in the read and write timing diagrams (Figures 3 and 4).

FSRAM SUPPORT CHIP OPTIONS

Motorola FSRAM group have defined several options suitable for the DSP5630x family of devices. Three options are detailed below. The first option (Figure 5) is to use three FSRAM 1 Megabit memories of the configuration of 128K x 8. This provides a memory block of 128K x 24, using the recommended FSRAMs MCM6926WJ or MCM6326YJ. The MCM6926WJ is built in Advanced CMOS technology, providing high–speed solutions, while the MCM6326J utilizes CMOS technology and more cost–effective solutions.

The second option (Figure 6) incorporates two 64K x 16 CMOS devices (MCM6323BWJ) with the UB (upper byte enable) disabled on the second device by connecting this pin to V_{CC} via a resistor. The data bus is 24 bits wide, consequently the upper bits of the second devices are not required. Both byte enables on the first device and the lower byte enable (LB) on the second device are asserted by connecting these pins to a low level via resistors.

The third option (Figure 7) is to use a single chip solution based on the forthcoming MCM6321TQ. This has the advantage of reducing real estate on motherboards and further reduces the load/drive requirements of the DSP.

TYPICAL EXAMPLE

In order to clarify the many options available, a typical example is detailed below. It is assumed that the external memory comprises of three asynchronous 128K x 8 FSRAMs giving a memory block of 128K x 24 with one wait state access.

The FSRAM option is not critical as the address and control inputs of a FSRAM are 6 pF, with I/O having 8 pF input capacitance, and the DSP5630x can drive 50 pF load.

Assuming a DSP cycle time of 66 MHz and using Table 2, the selection would be 16.52 ns. Typically, available memories are 15 ns and these could be used in this example. The FSRAM memory is partitioned to split the upper 64K between external X– and Y–data memory while the lower 64K is reserved for external program memory as can be seen in Figure 8.

The external memory type (X,Y, or P) accesses are enabled by the AA pins and controlled by the AA registers. DSP AA3 and AA2 pins are connected to address pins A16 and A15 respectively of the FSRAMs. Therefore, the AA pins are used for address partitioning of the external FSRAM memories. The top priority is AAR3, which defines the external data memory and is restricted to the top half of the external FSRAM memory block. The associated AA register (AAR3) is configured to the conditions in Figure 9. This defines the external access type as an asynchronous FSRAM to (X or Y) data memory with no address multiplexing or packaging. The number of address bits to be compared is A23:16, where A16 defines the high order addressing of the FSRAMS. If the AAR3 address compare is unsuccessful, then program memory is being accessed and the AA3/A16 will be in a low state defining the lower half of external memory. The remaining addresses are outwith the addressing range of the memories used and are consequently compared to zero.

The second priority is AAR2, defined as the external Y–data memory, assuming a matched compare, and is restricted to the upper quartile of the top half of the external FSRAM memory block. The associated AA register (AAR2) is configured to the conditions in Figure 10. This defines the external access type as an asynchronous FSRAM, Y–data memory with no address multiplexing or packaging. The number of address bits to be compared is A23:15. A16 is compared to a one to confirm the upper half while A15 is compared to a one defining the upper quartile (Y–data) within the upper half of the FSRAM block (i.e., between 96K and 128K addressing range). If the compare is unsuccessful then the X–data block will be accessed as defined in the 64K to 96K addressing range when A16 is a high and A15 is at a low value. The remaining addresses are outwith the addressing range of the memories used and are consequently compared to zero.

The Bus Control register is programmed as in Figure 11. As asynchronous FSRAMS are used, then one wait state is programmed in for all areas. The bus state, bus lock hold, and bus request hold are all programmed to zero.

The connections for the DSP and FSRAMs are detailed in Figure 12. AA3 is connected to A16, while AA2 is connected to A15 for each of the FRAMs. Therefore, different polarity of these pins enables different blocks of the 128K x 24 external memory.

This is by no means the only method of connection or usage of the control pins but is merely supplied as an example. Many different variants have and will be used successfully.

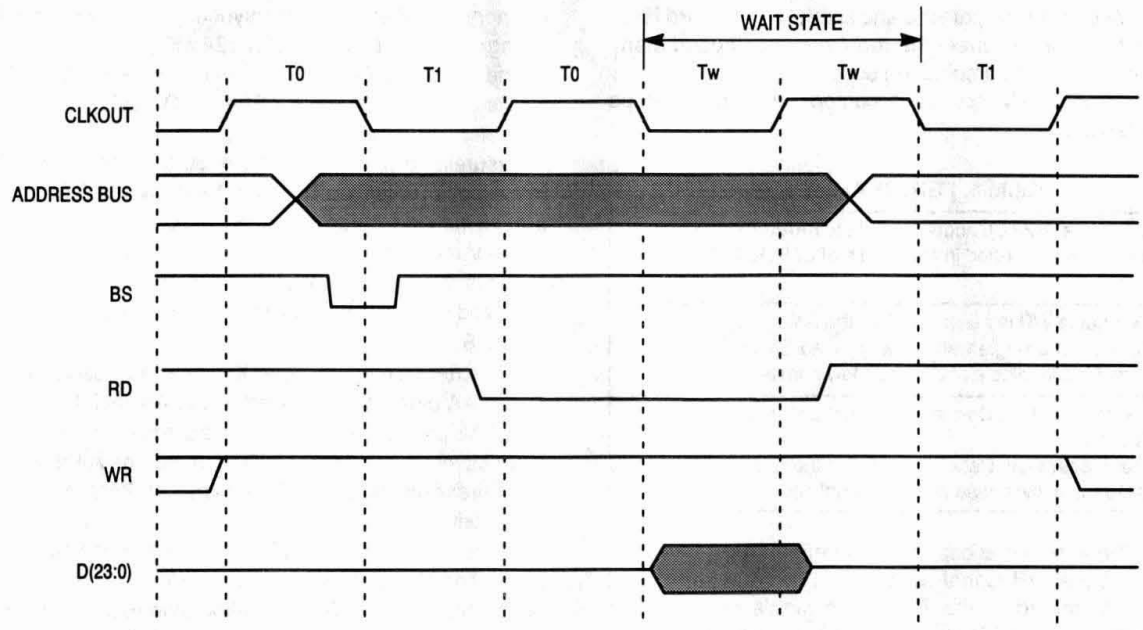

Figure 3. Read Cycle

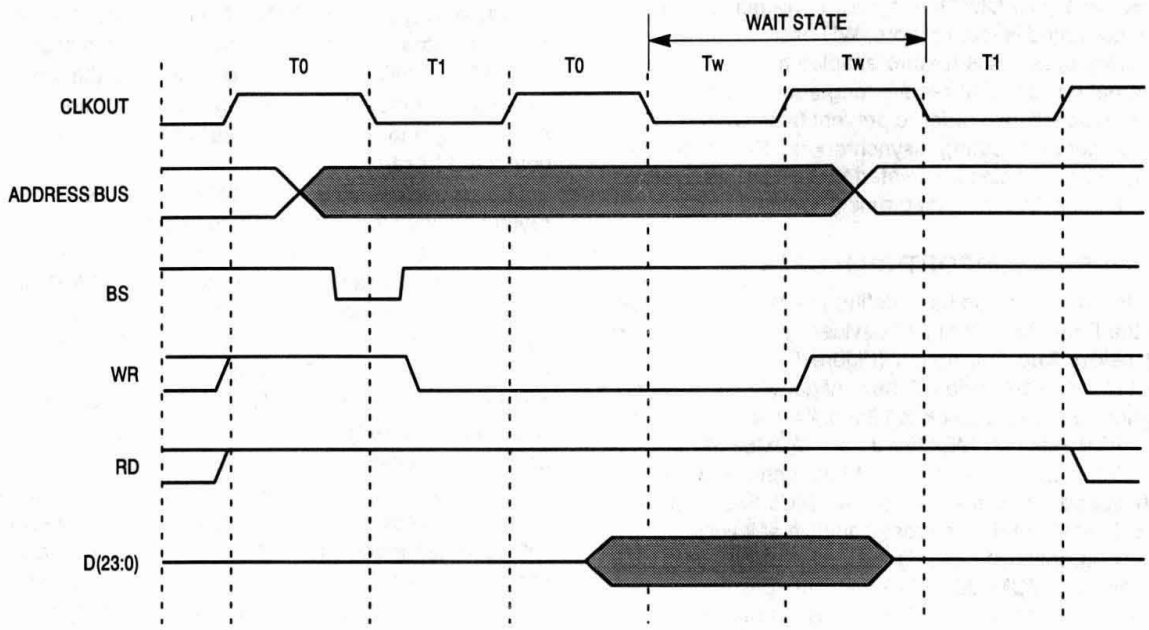

Figure 4. Write Access

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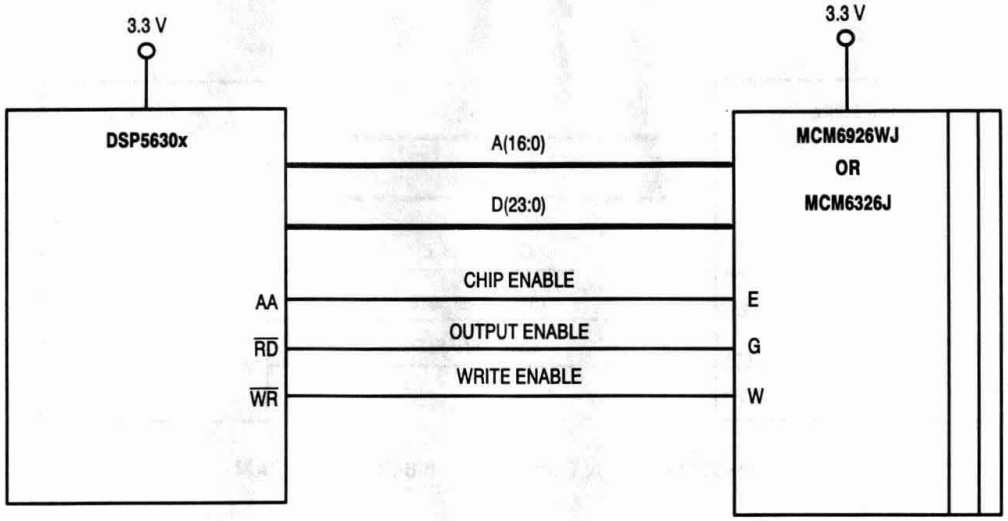

Figure 5. DSP5630x Connection to Three Off (128K x 8) FSRAMs

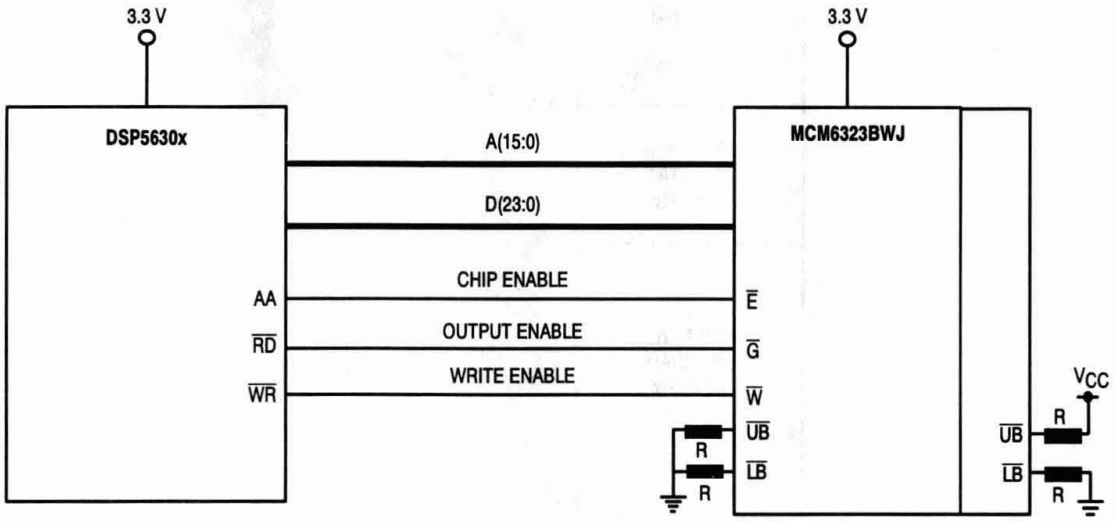

Figure 6. DSP5630x Connection to Two Off (64K x 16) FSRAMs

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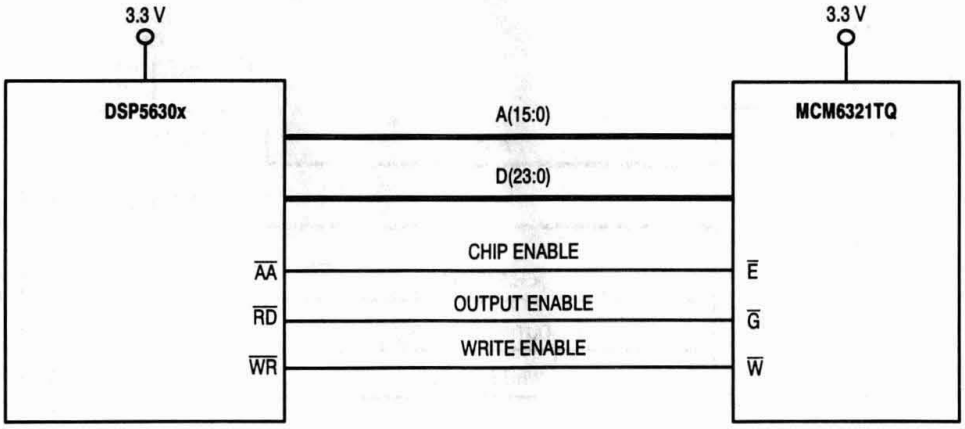

Figure 7. DSP5630x Connection to 64K x 24 FSRAM

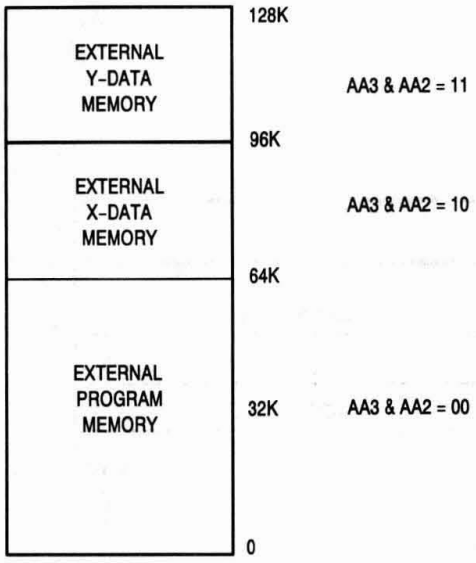

Figure 8. FSRAM Memory Partitioning

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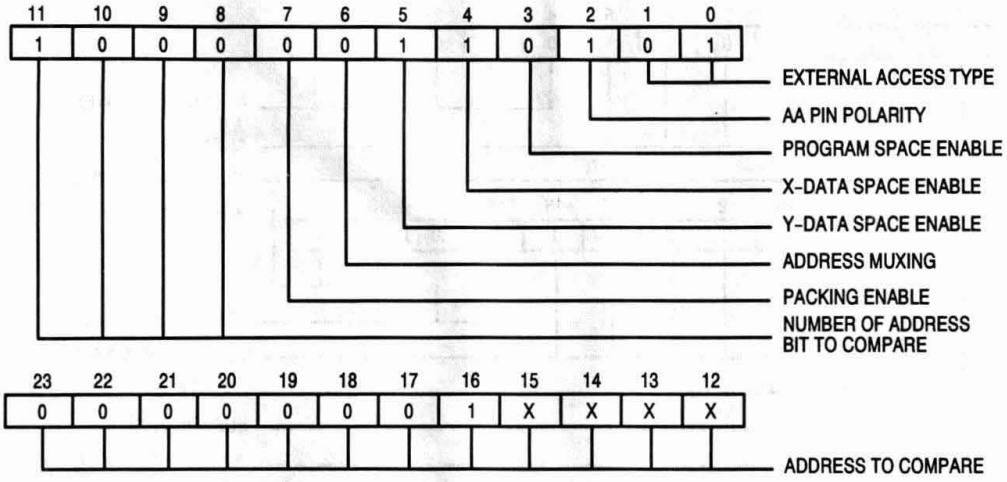
11 10 9 8 7 6 5 4 3 2 1 0
1 0 0 0 0 0 1 1 0 1 0 1
EXTERNAL ACCESS TYPE
AA PIN POLARITY
PROGRAM SPACE ENABLE
X-DATA SPACE ENABLE
Y-DATA SPACE ENABLE
ADDRESS MUXING
PACKING ENABLE
NUMBER OF ADDRESS BIT TO COMPARE
23 22 21 20 19 18 17 16 15 14 13 12
0 0 0 0 0 0 0 1 X X X X
ADDRESS TO COMPARE

Figure 9. AAR3 Register Programming for External X– or Y–Data Memory

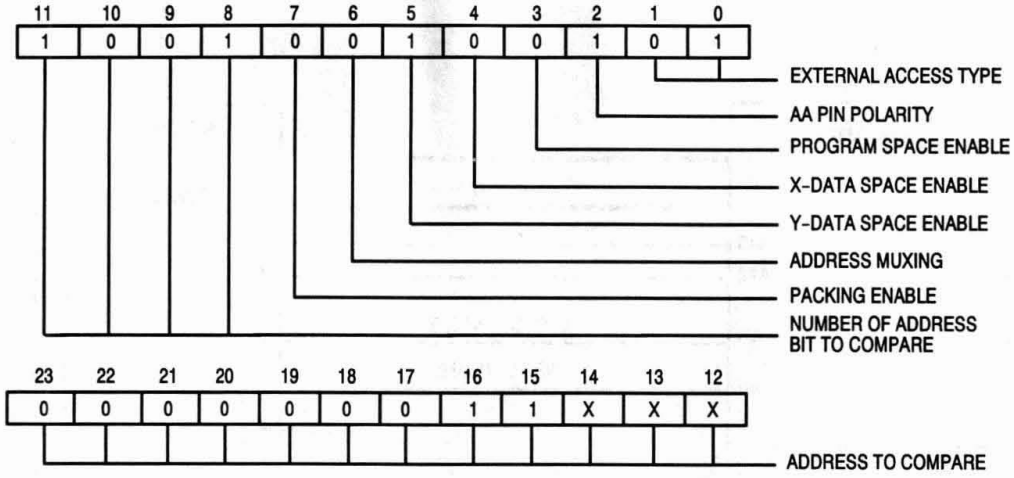
11 10 9 8 7 6 5 4 3 2 1 0
1 0 0 1 0 0 1 0 0 1 0 1
EXTERNAL ACCESS TYPE
AA PIN POLARITY
PROGRAM SPACE ENABLE
X-DATA SPACE ENABLE
Y-DATA SPACE ENABLE
ADDRESS MUXING
PACKING ENABLE
NUMBER OF ADDRESS BIT TO COMPARE
23 22 21 20 19 18 17 16 15 14 13 12
0 0 0 0 0 0 0 1 1 X X X
ADDRESS TO COMPARE

Figure 10. AAR2 Register Programming for External Y–Data Memory

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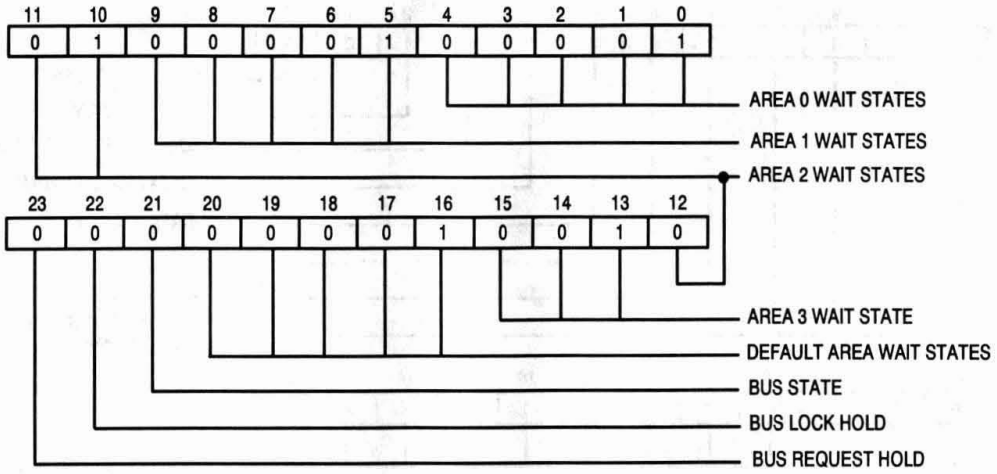
11 10 9 8 7 6 5 4 3 2 1 0
0 1 0 0 0 0 1 0 0 0 0 1
AREA 0 WAIT STATES
AREA 1 WAIT STATES
AREA 2 WAIT STATES
23 22 21 20 19 18 17 16 15 14 13 12
0 0 0 0 0 0 0 1 0 0 1 0
AREA 3 WAIT STATE
DEFAULT AREA WAIT STATES
BUS STATE
BUS LOCK HOLD
BUS REQUEST HOLD

Figure 11. Bus Control Register Programming for Asynchronous FSRAM

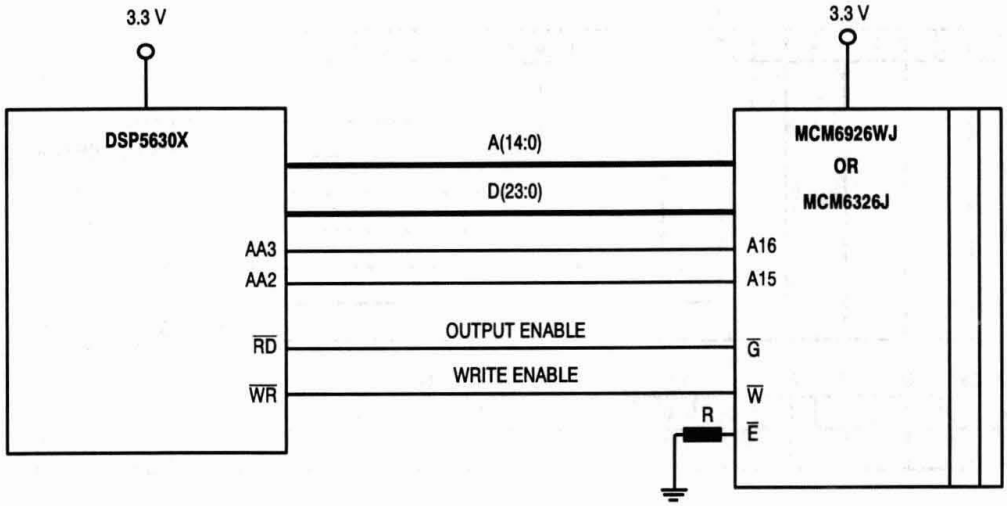

Figure 12. DSP5630x Connection to Three Off (128K x 8) FSRAMs

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AN1289

DSP5630x FSRAM Module Interfacing

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Motorola Ltd.
East Kilbride, Scotland

INTRODUCTION

Due to ever increasing complexity of executable code, several applications based on digital signal processors (DSPs) are requiring higher and higher performance in terms of execution speed. To accommodate these requirements, Motorola has developed a 24–bit DSP family and several memory support chips to provide cost–effective, high–performance solutions.

This document describes several options of interfacing different asynchronous fast static RAM modules to the Motorola 24–bit DSP5630x family.

DSP56300 CORE DESCRIPTION

The DSP56300 is a powerful new DSP engine (NDE) core capable of executing an instruction on every clock cycle, thus yielding a twofold performance increase compared to the 56K core while maintaining 100% object code compatibility with it.

The DSP56300 CMOS core is composed of an expansion port and DRAM controller, data ALU, address generation unit, instruction cache controller, program control unit, DMA controller, PLL clock oscillator, On–Chip Emulation Port (OnCE™), and the peripheral and memory expansion bus.

To minimize the total system cost, the DSP56300 core incorporates a versatile external memory interface that provides glueless interface to a variety of memories such as dynamic RAMs (DRAMs), static RAMs (SRAMs), and synchronous static RAMs (SSRAMs).

PORT A INTRODUCTION

Port A of the DSP56301 core is the memory expansion port that can be used either for memory expansion or for memory–mapped I/O. A number of features make port A versatile and easy to use. These features provide a low part–count connection with fast static memories, dynamic memories, I/O devices, and multiple bus master systems.

PORT A OPERATION

The port A data bus is 24 bits wide with a separate 24–bit wide address bus capable of a sustained rate of 1 memory access per clock cycle for data space accesses (using synchronous static memory). External memory is divided into three 16M x 24 bit spaces — X, Y, and P. An internal wait state generator can be programmed to insert up to 31 wait states, if access to slower memory or I/O devices is required. A bus wait signal allows an external device to control the number of wait states inserted in a bus access operation. Bus arbitration signals allow an external device to use the bus while internal operations continue using the internal memory.

EXTERNAL STATIC RAM CONTROL

External bus timing is controlled by the $\overline{TA}$ control signal and by the bus control register (BCR) (see Table 1). Insertion of wait states is controlled by BCR to provide constant bus access timing, and by the $\overline{TA}$ control signal to provide dynamic bus access timing. The number of wait states for each external access is determined by input $\overline{TA}$ or by BCR, whichever is longest.

Table 1. BCR Register Programming

BCR Bits 23 – 0	Configuration
01X000010010010000100001	Areas 3, 2, 1, and the default area = 1 wait state. BLH and BRH are cleared.

Using the configuration in Table 1, all external memory areas (3, 2, 1, and default) are programmed to 1 wait state. Using the suggested modules shown in Figure 1, areas 3, 2, and 1 are used depending on the configuration. If other types of memory or external devices are required, the relevent areas should be programmed for the required wait states. The external memory address is defined by the address bus A23 – A0 and the memory address attribute signals AA3 – AA0. The AA signals have the same timing as the address bus and may be used as additional address lines. The AA signals are also used to generate chip select signals for the appropriate memory chips. These chip select signals change the memory chips from low power standby mode to active mode and begin the access time. This allows slower memories to be used since the AA signals are address based rather than read or write enable based.

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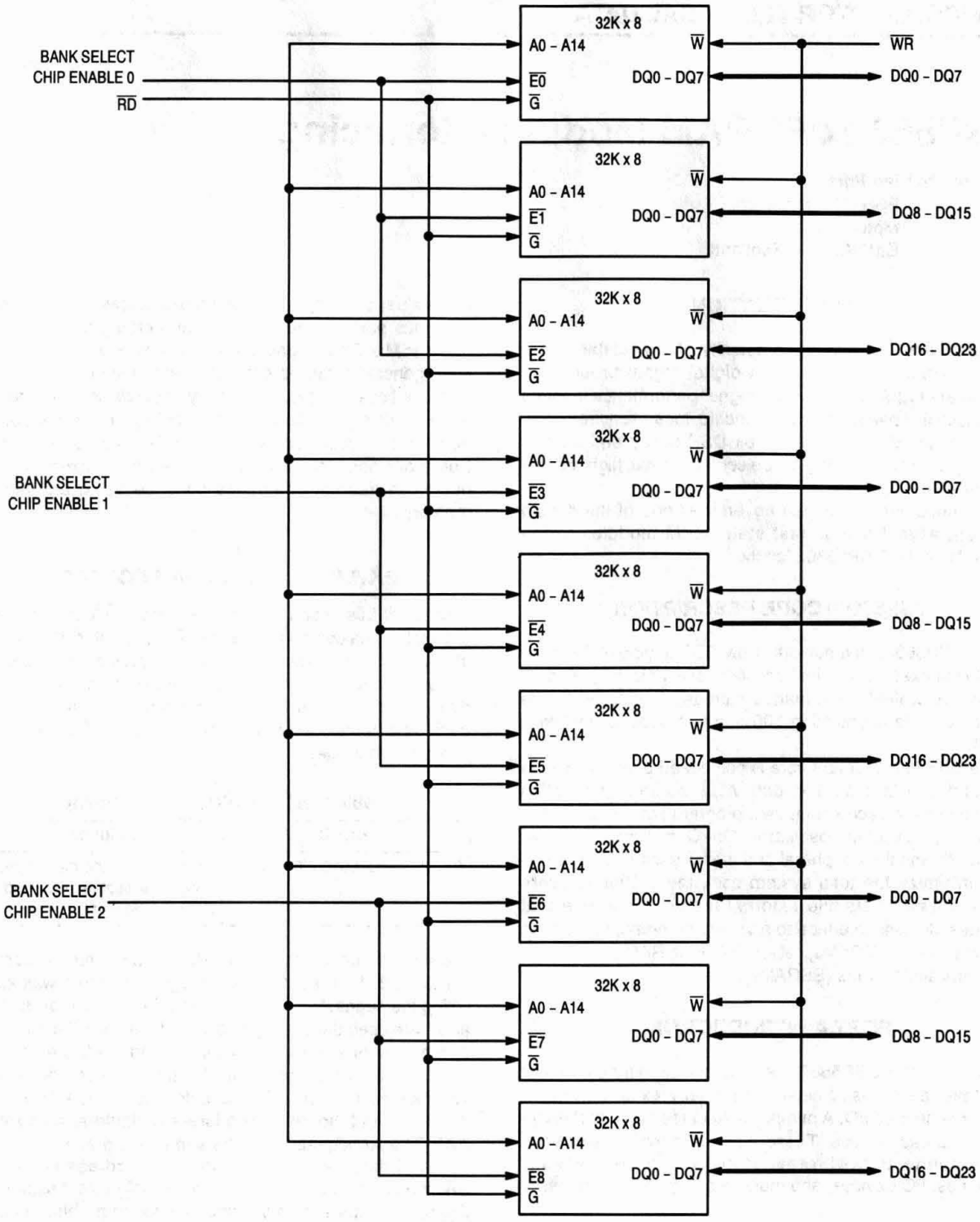

NOTE: The chip enables are connected to the AA pins of the DSP.

Figure 1. Proposed Module Solution Using 32K x 8 FSRAMs

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ADDRESS ATTRIBUTE CONTROL REGISTERS (AAR) (ONE FOR EACH AA PIN)

The four control registers (AAR3, AAR2, AAR1, and AAR0) are 24–bit read write registers used to control the activity of the AA3 – AA0/RAS3 – RAS0 pins. An AA/RAS pin is asserted if the address in its appropriate AAR (BAC bits) matches the external address where the exact number of address bits that are compared is determined by the BNC bits, and if the external access is aimed to a space X, Y, or P, enabled in the appropriate AAR. All AARs are disabled (all AAR bits cleared) during hardware reset. The AAR bits are shown in Figure 2 and described in the following paragraphs.

A priority mechanism exists among the four AARs in order to resolve selection conflicts. AAR3 has the highest priority and AAR0 has the lowest (e.g., if the external address matches the address and the space that is specified in both AAR1 and AAR2, the external access type will be selected according to the AAR2 register). The priority mechanism allows continued partition of the external address space.

When the AA/RAS pin functions as the AA pin, it is negated at the start of the next clock cycle only if there is no external access that uses the same AA pin (i.e., the AA pin will be kept asserted in a sequence of two consecutive external accesses that access the same memory bank). This method enables the use of low power standby mode in the external memories (these memories should be accessed first by a dummy access).

The programmer should guarantee that an AAR is not changed while accessing the memory selected by this AAR, otherwise improper operation may result.

MODULE SOLUTIONS

The proposed module in Figure 1 is composed of nine 3.3 V, 32K x 8 based FRAMS. The RAMs are used in groups of 3 to accommodate the 24–bit bus architecture of the DSP. Selection is segmented into 3 banks, providing a total memory depth of 96K. Bank selection for use of X data space, Y data space, and program memory is facilitated by means of DSP56301 AA control pins. Three AA control lines define which banks (memory type) are selected (see Figure 3). The address pins are directly connected to the address bus partitioned among the nine FSRAMs. The DSP output enable ($\overline{RD}$) is directly connected to each FSRAM output enable, while the DSP write enable is connected to the nine FSRAM write enables. The data bus is connected sequentially across each bank of memory.

If the components are 5 V, the data bus can be clamped to 3.3 V using a voltage regulator (see Figure 4). The voltage regulator circuit uses a 3.3 V EZDropper shunt regulator device (EZ5Z3L–S3.3V), depicted in Figure 5. This voltage regulator circuit is incorporated and supplied on the module and does not impact the user's design.

If one particular memory type (X, Y, or P) needs greater allocation of available external memory, it can be accomplished by using AA control pins and partitioning the external memory by means of one or two extra address bits.

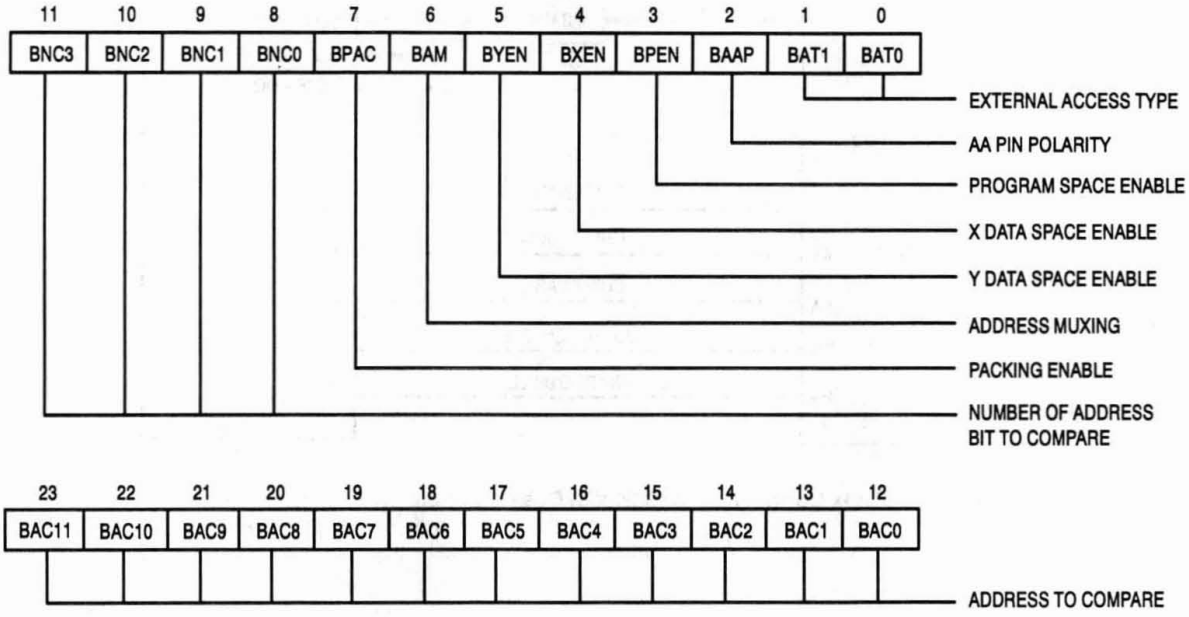
11 10 9 8 7 6 5 4 3 2 1 0
BNC3 BNC2 BNC1 BNC0 BPAC BAM BYEN BXEN BPEN BAAP BAT1 BAT0
EXTERNAL ACCESS TYPE
AA PIN POLARITY
PROGRAM SPACE ENABLE
X DATA SPACE ENABLE
Y DATA SPACE ENABLE
ADDRESS MUXING
PACKING ENABLE
NUMBER OF ADDRESS BIT TO COMPARE
23 22 21 20 19 18 17 16 15 14 13 12
BAC11 BAC10 BAC9 BAC8 BAC7 BAC6 BAC5 BAC4 BAC3 BAC2 BAC1 BAC0
ADDRESS TO COMPARE

Figure 2. Address Attribute Registers (AAR3 – AAR0)

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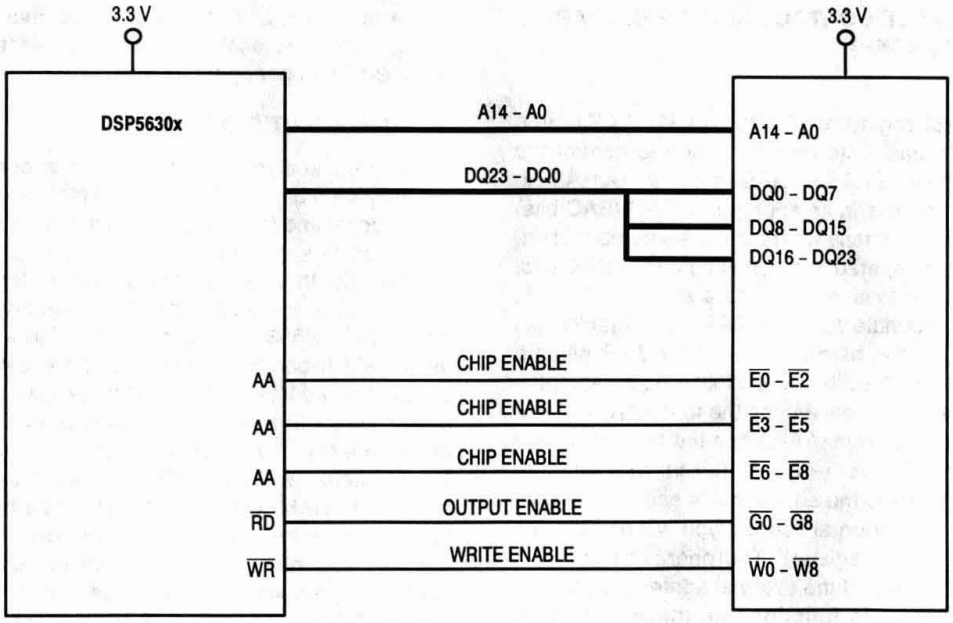

Figure 3. DSP5630x Connection to (32K x 8) Based Module on X, Y, and P Memory

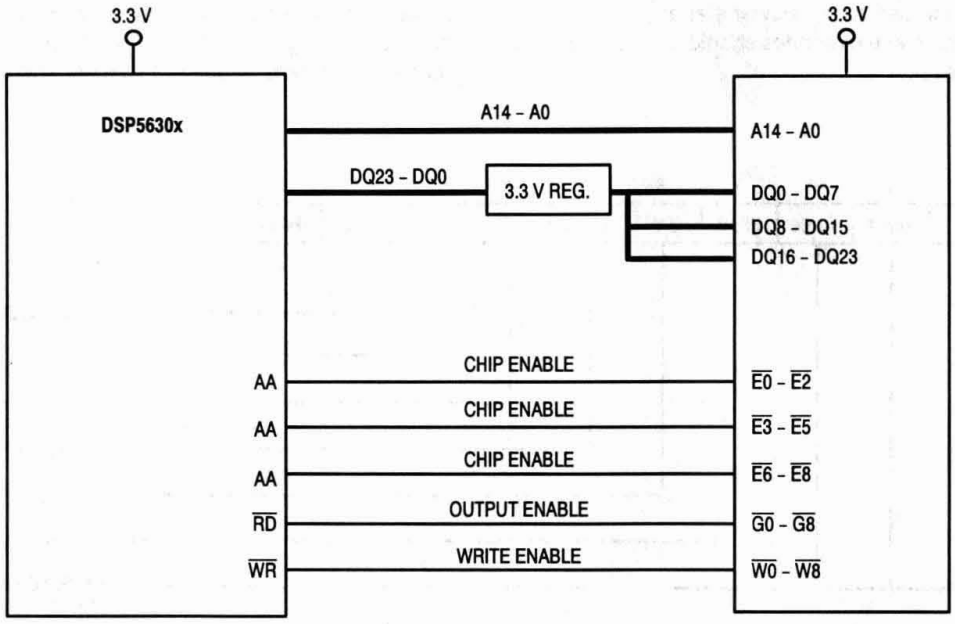

Figure 4. DSP5630x Connection to (32K x 8) Based Module on X, Y, or P Memory

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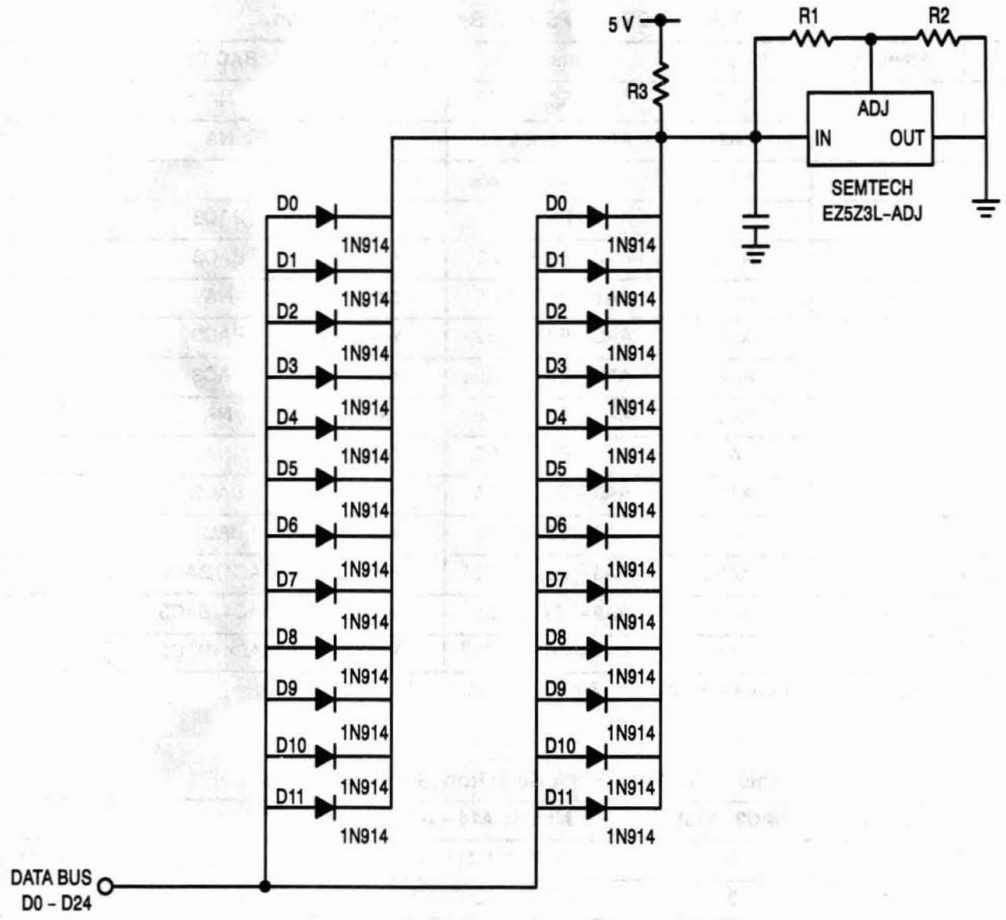

Figure 5. 5 V to 3.3 V Regulator Circuit

Here, the AARs would be configured for the required external memory types; X data space, Y data space, or program memory, and addresses A15, A16 for bank selection by incorporating the address to compare capability. Table 2 details the bank's selection configuration. If only two types of memory are required as in options 2, 3, and 4, the banks can be split in a ratio of two to one. Taking option 2 as an example, the Y memory selects two banks and program memory selects the remaining bank. The program memory does not require comparing the address, and the AA1 pin is connected to chip enables E6, E7, and E8. Y memory selects two banks by means of two AA pins. The high order Y memory bank is selected using AA3 and comparing for a set or 1 value of bit 15 (or BAC3) in AAR3. If this bit is set, the AA3 pin activates the high order Y memory bank. If this bit is not set, a comparison is performed on bit 15 (or BAC3) of AAR2. If this bit is not set or has a 0 value, the low order Y memory bank is selected by the AA2 pin. This process is also valid for options 3 and 4.

Option 5 is unique in that only one type of external memory is selected. In this case, the memory is sequential and the partitioning (bank selection) is selected by means of comparing address bits A16 and A15 (BAC4 and BAC3). The high order addressing is compared using the highest priority AAR3. If the address bits 16 (BAC4) and 15 (BAC3) are set to 10, the highest order bank is selected. If this is not true, address comparison will be made in AAR2 for bits 16 and 15 to be equal to 01. Validation will select the middle addressing bank, otherwise a comparison will be made of bits 16 and 15 (BAC4 and BAC3) of AAR1 (the lowest address bank) being equal to 00. Confirmation selects the low address bank. In this way, the full external 96K memory map can be utilized.

Consequently, programming the AARs for async FSRAM modules with one wait state and the AA pin active low is configured as shown in Table 4. Table 4 depicts examples of different options of compare and no compare addressing for external memory segregation.

Table 2. DSP to FSRAM Bank Configuration

Option	Memory	AA Pin	Connect	Compare	BAC Bit	Address Bit
1	X	AA3	AA3 – E0, E1, E2	No	NA	NA
	Y	AA2	AA2 – E3, E4, E5	No	NA	NA
	P	AA1	AA1 – E6, E7, E8	No	NA	NA
2	Y	AA3	AA3 – E0, E1, E2	Yes	BAC3	15
	Y	AA2	AA2 – E3, E4, E5	Yes	BAC3	15
	P	AA1	AA1 – E6, E7, E8	No	NA	NA
3	X	AA3	AA3 – E0, E1, E2	Yes	BAC3	15
	X	AA2	AA2 – E3, E4, E5	Yes	BAC3	15
	P	AA1	AA1 – E6, E7, E8	No	NA	NA
4	X	AA1	AA1 – E0, E1, E2	No	NA	NA
	P	AA3	AA3 – E3, E4, E5	Yes	BAC3	15
	P	AA2	AA2 – E6, E7, E8	Yes	BAC3	15
5* Refer to Table 3 for compares	P	AA3	AA3 – E0, E1, E2	Yes	BAC4, BAC3	16, 15
	P	AA2	AA2 – E3, E4, E5	Yes	BAC4, BAC3	16, 15
	P	AA1	AA1 – E6, E7, E8	Yes	BAC4, BAC3	16, 15

* This option is also applicable for X or Y data memory as a single selection.

Table 3. Address Bank Selection (See Option 5 in Table 2)

AA Bit	BAC4 (A16)	BAC3 (A15)	Module A14 – A0	Address	Bank Selection
AA3	1	0	111111111111111	Max Address	3 (Highest Addressing)
AA3	1	0	000000000000000	Min Address	3 (Highest Addressing)
AA2	0	1	111111111111111	Max Address	2 (Middle Addressing)
AA2	0	1	000000000000000	Min Address	2 (Middle Addressing)
AA1	0	0	111111111111111	Max Address	1 (Lowest Addressing)
AA1	0	0	000000000000000	Min Address	1 (Lowest Addressing)

Table 4. AAR Programming Options

A23 – A12	A11 – A0	Configuration
000000000000	000000001010	No Addr Compare, Pack or Mux. Program Memory, Active Low, Async SRAM.
000000000000	000000010010	No Addr Compare, Pack or Mux. X Data Space, Active Low, Async SRAM.
000000000000	000000100010	No Addr Compare, Pack or Mux. Y Data Space, Active Low, Async SRAM.
000000000000	100100001010	No Pack or Mux. A15 Compare, Program Memory, Active Low, Async SRAM.
000000000000	100100010010	No Pack or Mux. A15 Compare, X Data Space, Active Low, Async SRAM.
000000000000	100100100010	No Pack or Mux. A15 Compare, Y Data Space, Active Low, Async SRAM.
000000001000	100100001010	No Pack or Mux. A15 Compare, High Order Address, Program Memory, Active Low, Async SRAM.
000000001000	100100010010	No Pack or Mux. A15 Compare, High Order Address, X Data Space, Active Low, Async SRAM.
000000001000	100100100010	No Pack or Mux. A15 Compare, High Order Address, Y Data Space, Active Low, Async SRAM.
000000000000	100100001010	No Pack or Mux. A16, A15 Compare, Lowest Order Address, Program Memory, Active Low, Async SRAM.
000000000000	100100010010	No Pack or Mux. A16, A15 Compare, Lowest Order Address, X Data Space, Active Low, Async SRAM.
000000000000	100100100010	No Pack or Mux. A16, A15 Compare, Lowest Order Address, Y Data Space, Active Low, Async SRAM.
000000001000	100100001010	No Pack or Mux. A16, A15 Compare, Middle Order Address, Program Memory, Active Low, Async SRAM.
000000001000	100100010010	No Pack or Mux. A16, A15 Compare, Middle Order Address, X Data Space, Active Low, Async SRAM.
000000001000	100100100010	No Pack or Mux. A16, A15 Compare, Middle Order Address, Y Data Space, Active Low, Async SRAM.
000000010000	100100001010	No Pack or Mux. A16, A15 Compare, Highest Order Address, Program Memory, Active Low, Async SRAM.
000000010000	100100010010	No Pack or Mux. A16, A15 Compare, Highest Order Address, X Data Space, active Low, Async SRAM.
000000010000	100100100010	No Pack or Mux. A16, A15 Compare, Highest Order Address, Y Data Space, Active Low, Async SRAM.

AN1296

Using the MCM69C232/MCM69C432 Content–Addressable Memory on an ATM Line Card

Prepared by: Mike Parks

Asynchronous Transfer Mode (ATM) switches, due to their connection–based protocol, must translate each cell's address at every point along the routing path. The cell's address information is carried in two fields within the five byte header. The Virtual Path Identifier (VPI) is an 8 or 12 bit value, depending on the protocol being run, while the Virtual Circuit Identifier (VCI) is a 16 bit value. Figure 1 shows a small network of switches (S1 – S5) connecting six computers (C1 – C6).

A connection has been established between C1 and C6, through switches S1, S3, and S5. Conceptually, the connection consists of a list of VPI/VCI translation pairs. For example, C1 sends cells to S1 using a VPI of $7AC_{16}$ (hexadecimal notation) and a VCI of $5AB0_{16}$. When S1 receives a cell on port 1 with those values, it changes the VPI to 902_{16} and the VCI to $A77F_{16}$. The cell is then transmitted to S3 by outputting it on port 3. Similarly, when S3 received the cell, it translates the VPI/VCI and forwards the cell to S5. Switch S5 performs a final VPI/VCI translation and forwards the cell to its end point, C6. This type of connection, in which both the VPI and the VCI are examined and (usually) modified, is known as a Virtual Circuit Connection (VCC). A second connection type, the Virtual Path Connection (VPC) only requires that the VPI be translated. The VPC is used when many connections follow the same path through a sequence of switches.

The speed at which VPI/VCI pairs must be translated is a function of several variables, including the line speed, the number of lines connected to a single line card, and the speed of the other circuitry on the line card. ATM switch designers typically require that a VPI/VCI translation is completed within one quarter to one half the time it takes to receive a cell. For OC12 rates (622 megabits/second) this corresponds to 160 to 320 ns. Note that the translation must be completed in this interval whether the cell belongs to a VPC or a VCC.

Switch designers use one of several approaches to solve the VPI/VCI translation problem. The simplest approach simply restricts the address space. While the 28 bits of the VPI/VCI define a space of 26.8 billion possible values, typically only a few thousand are active in a switch at a time. By assigning an invariant value to most of the VPI/VCI bits and only considering 12 – 14 bits when creating new connections, the switch can maintain a table in memory of the outbound VPI, VCI, and port values that correspond to an incoming cell's address. See Figure 2 for an example. This approach is somewhat risky due to its inflexibility and various regional standards that are still in a state of flux.

Other designers use a hashing technique to translate the VPI/VCI into an appropriately sized table offset. For example, if a switch needs to maintain 4096 connections, i.e., 2^{12}, a logic network can be designed with 28 inputs and 12 outputs. The logic will reduce the VPI/VCI value so that it addresses a table of manageable size. However, the output of the logic network can be duplicated for more than one active connection. Thus, the output values of VPI, VCI, and port number must be maintained in a data structure such as a linked list that allows them to be accessed sequentially until the correct one is found. Figure 3 shows an example of this approach.

The maximum time required to translate a VPI/VCI pair increases with the length of the linked list. In a worst case scenario, the allowable time can be exceeded, unless the switch's processor devotes resources to modification of the hashing function in response to changing active VPI/VCI values.

In yet another approach, the connections can be kept in a table that is sorted by VPI/VCI value. Then, when a cell arrives, a binary search can be performed to find a matching value of VPI/VCI in the table. This approach has the advantage of a deterministic upper bound on search time. For example, a 4K table can be searched in 12 steps. However, the stringent translation time specifications necessitate a high performance hardware implementation.

The best approach uses a Content–Addressable Memory (CAM). The CAM turns the normal memory access "inside out". A *datum* is applied to the CAM, and it outputs the *address* where a matching value is stored. Therefore, if 4K connections need to be active in a switch, their VPI/VCI values can be stored in a 4K x 28 CAM. The 12 bit address output can be used as an index into a RAM table where the translated VPI/VCIs are stored. While the CAM–based solution is simple, deterministic, and unrestricted, it has been relatively expensive. In mid–1995, a CAM with 1024 entries sold for approximately $40.

Motorola's introduction of the 4K MCM69C232 and the 16K MCM69C432 CAMs has changed the balance of the competing VPI/VCI translation methods. Due to the use of a standard 4–transistor bit cell, the Motorola products are both higher capacity and lower cost than past solutions. Like competing CAMs, they are very well suited to this application.

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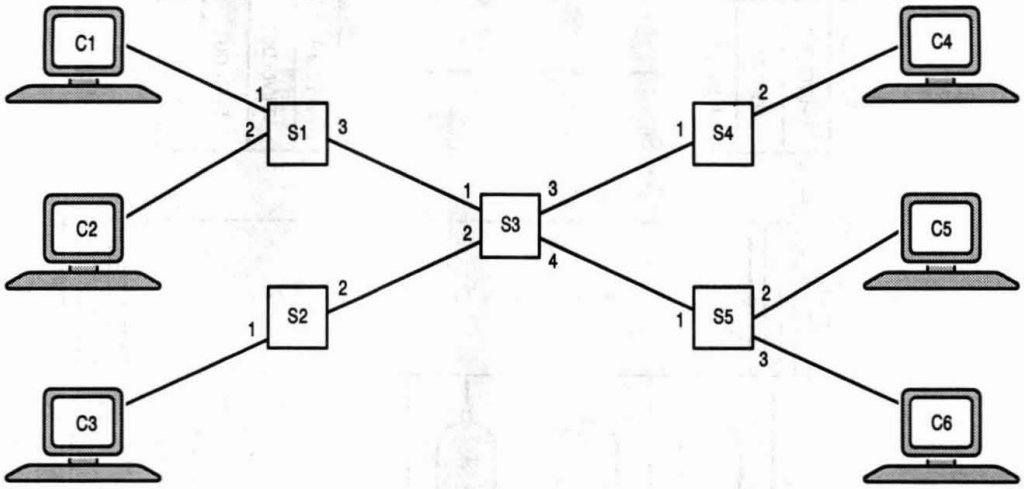

Figure 1.

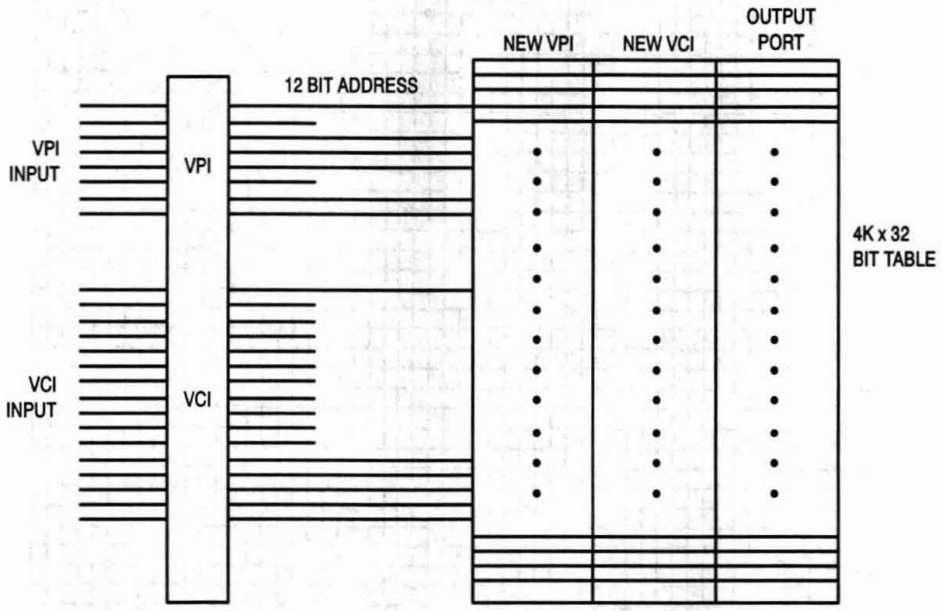

Figure 2. "Brute Force" VPI/VCI Compression

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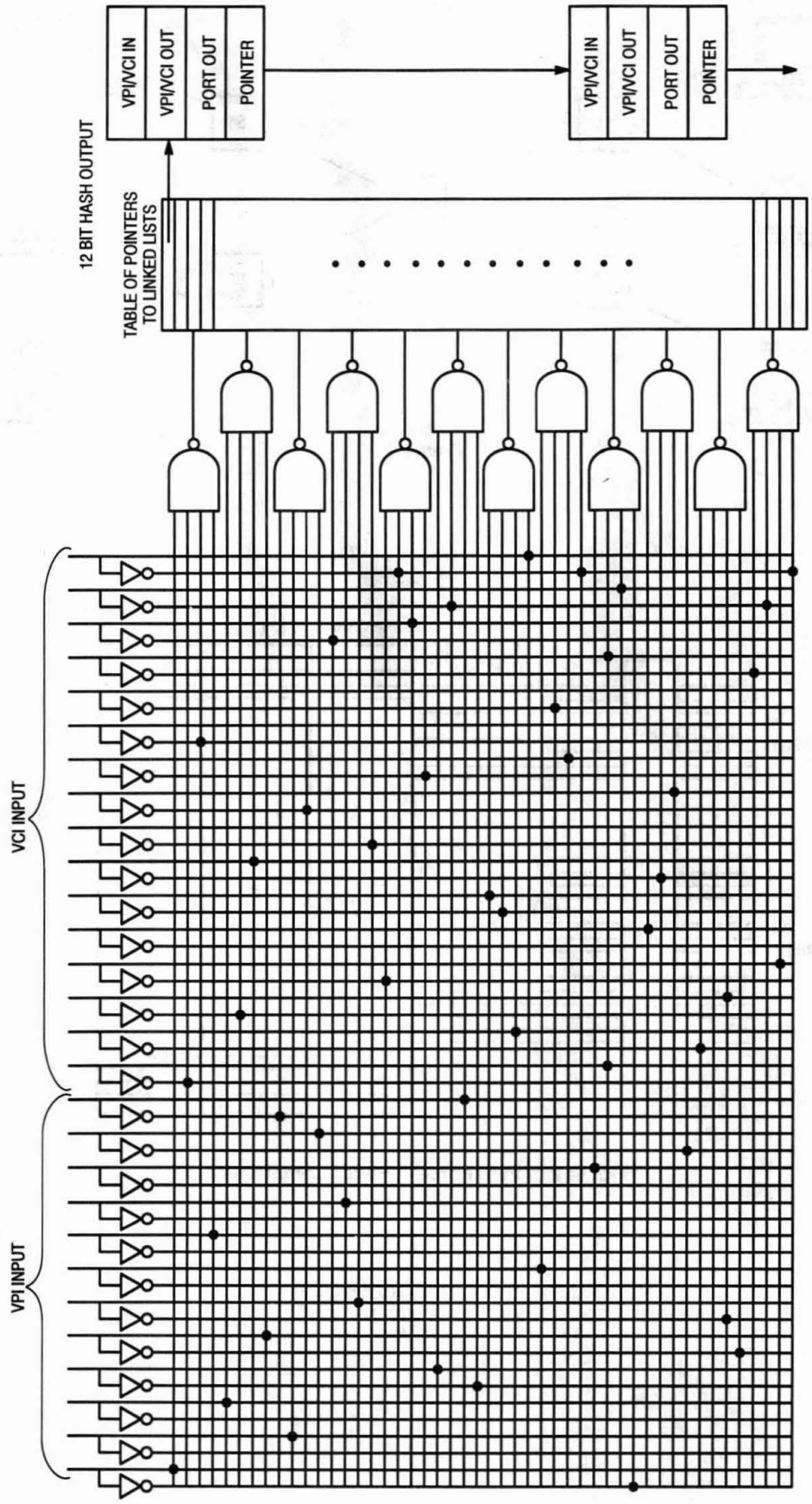
VPI/VCI IN
VPI/VCI OUT
PORT OUT
POINTER
VPI/VCI IN
VPI/VCI OUT
PORT OUT
POINTER
12 BIT HASH OUTPUT
TABLE OF POINTERS TO LINKED LISTS
VCI INPUT
VPI INPUT

Figure 3.

GENERIC LINE CARD ARCHITECTURE

In ATM applications, a line card consists of a physical layer interface, a framer function, a cell processor that includes some method of VPI/VCI translation, an interface to the switch fabric, and a controller. Typically, the card also includes a context memory, accessed by the controller and the cell processor, that holds information about each connection.

The physical layer device provides clock recovery and data synchronization functions, and passes a serial data stream on to the framer. The framer chip finds packet and cell boundaries, and passes cells on to the cell processor, typically on 1– or 2–byte–wide busses. VPI/VCI translation is performed by the cell processor and the CAM.

In this architecture, the controller is connected to the CAM's control port and is used to initialize the part and to perform table maintenance as connections are added and dropped. The cell processor is connected to the CAM's match port. Match port operations are the highest priority, ensuring that VPI/VCI translation can be done in a deterministic fashion.

INITIALIZING THE CAM FOR VPI/VCI TRANSLATION

Initialization of the MCM69C232 and MCM69C432 is performed via the control port. In the general case, 16 bit data values are written to each of the 4 I/O registers. An instruction word is then written to the operation register that describes the action to be performed. Some of the instructions do not use one or more of the I/O registers. The following sections of the paper describe the process of initializing the CAM. Appendix A contains a C–language implementation of the initialization sequence.

For VPI/VCI translation applications, the first step is to enter ATM mode. This instruction does not require any data values. Therefore, it is executed by writing the "Enter ATM Mode" op code (0008_{16}) to the operation register at address offset 4 (the values of A2 – A0 should be 100_2 to write to the operation register).

The mask register can then be loaded by writing 0s to the bits that should be included in a match operation. The 64 bit value is constructed by concatenating the values in I/O registers 3 – 0. Bit 15 of I/O register 3 is the most significant bit, and bit 0 of I/O register 0 is the least significant bit. For ATM applications, the lower 32 bits are normally not included in the match operation. The VPI bits must correspond to bits 59 – 48 of each entry, while the VCI corresponds to bits 47 – 32. (If a User–Network Interface protocol is being run, the VPI bits are 55 – 48.) Assuming that the four uppermost bits are not needed for some reason proprietary to the switch designer, the values written to I/O registers are as follows: I/O register 3 = $F000_{16}$ ($FF00_{16}$ for UNI), I/O register 2 = 0000_{16}, I/O register 1 = $FFFF_{16}$, and I/O register 0 = $FFFF_{16}$. The mask register is then loaded with these values by writing the "Set Mask Register" op code (0002_{16}) to the operation register.

The next step in the initialization sequence is to execute the "Enter Fast Entry Mode" instruction by writing the op code (0004_{16}) to the operation register. This instruction does not require any data values. The fast entry mode is preferred when large numbers of entries are to be added to the table.

If desired, the almost–full point can be set by writing the desired value to I/O register 0, then writing the "Set Almost–Full Point" op code (0007_{16}) to the operation register. Note that only the lower 12 bits are used for the MCM69C232, and the lower 14 bits for the MCM69C432. As an example, if an interrupt is desired when the '232 becomes half full, the value written to I/O register 0 should be 0800_{16}.

At this point, the initial connections can be loaded into the CAM. The most significant 16 bits are written to I/O register 3. Similarly, the three other I/O registers are loaded with the remaining bits of the CAM entry. Note that the VPI and VCI bits must be aligned as explained in the "Set Mask Register" section. The VPI is loaded into the lower 12 bits of I/O register 3 (the lower 8 bits for UNI), while the VCI is loaded into I/O register 2. A VPC is established by using a value of $FFFF_{16}$ for the VCI. This means that $FFFF_{16}$ cannot be used as the VCI of a VCC. I/O registers 1 and 0 are loaded with the 32 bit value that should be output on the MQ bus when this entry is matched. Bit 15 of I/O register 1 corresponds to MQ31, while bit 0 of I/O register 0 corresponds to MQ0. After the four I/O register values are written, the "Insert Value" op code (0000_{16}) is written to the operation register. This process is repeated until all of the initial entries have been loaded.

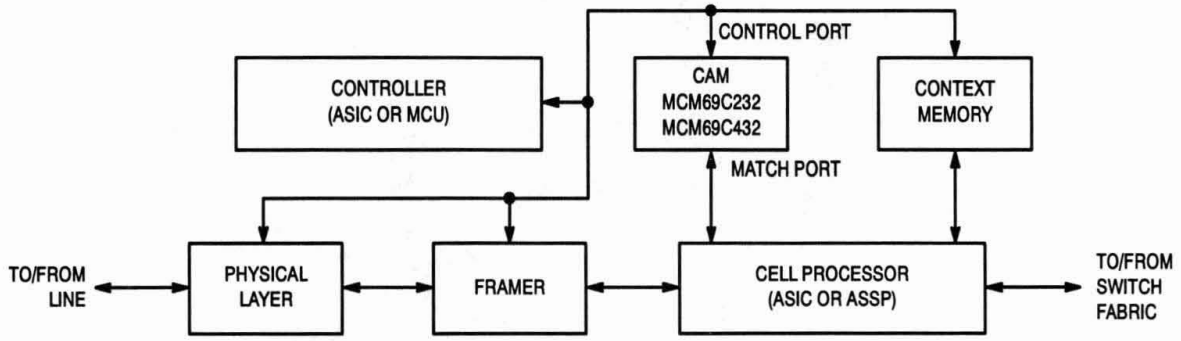

Figure 4. ATM Line Card

Next, the CAM table must be initialized. This instruction, which does not require any I/O register values, sorts the table in preparation for matching. It is executed by writing the "Initialize Table" op code ($000B_{16}$) to the operation register. Execution of this instruction automatically switches the CAM to its buffered entry mode, which allows matching to continue while new values are being added. The CAM also switches to buffered entry mode when the next to last entry is added to the table.

At this point, the CAM is initialized, and match port operations can begin. To initiate a match, the cell processor places the VPI from an incoming cell on MQ27 – MQ16 (MQ23 – MQ16 for UNI) and the VCI on MQ15 – MQ0. The match is started by asserting the $\overline{LH}/\overline{SM}$ signal. The completion of this operation is signaled by the assertion of the MC (Match Complete) pin. If the match is successful, $\overline{MS}$ is asserted, while the $\overline{VPC}$ signal is asserted if the match is a virtual path circuit.

While the cell processor uses the match port to translate the incoming VPI/VCI values, the controller can continue to use the control port for table maintenance and administrative functions. The C code in Appendix A continues to loop through a sequence of adding any new entries that are needed, deleting any stale entries, and periodically reading the entire CAM table to verify that all the desired connections are still active.

While VPCs and VCCs are typically segregated into different ranges of VPI values; occasionally, it may be necessary to expand the range of values used for VPCs. If this occurs, all VCCs that use that VPI must first be deleted. They can be located by using "Fast Read" instructions, then deleted one by one. Note that they will typically be located in a contiguous group in the CAM. However, the last entry should always be checked because it will hold the last value added to a completely full CAM, no matter what its match value might be.

APPENDIX A

```
/*****************************************************************************/
/* initialization of the mcm69c232 content addressable memory                */
/* for vpi/vci translation in an atm application                              */
/* August 1996                                                               */
/* Author: Mike Parks                                                        */
/*****************************************************************************/
#include <stdio.h>
#include <ctype.h>
#include <stdlib.h>
#include <string.h>

#define  CAMSIZE 4096

/* define flag register's bits */
#define INT_ENABLE                  1
#define LAST_MATCH_SUCCESSFUL       2
#define TABLE_INITIALIZED           4
#define BUFFERED_ENTRY_MODE         8
#define ENTRY_QUEUE_EMPTY           16
#define ENTRY_QUEUE_FULL            32
#define CAM_TABLE_FULL              64
#define ERROR_CONDITION_SET         128
#define TABLE_ALMOST_FULL           256
#define ATM_MODE                    512
#define LAST_OP_COMPLETE            1024

/* define op code values */
#define INSERT_VALUE                0x0
#define DELETE_VALUE                0x1
#define CHECK_FOR_VALUE             0x6
#define INITIALIZE_TABLE            0xb
#define ENTER_FAST_ENTRY_MODE       0x4
#define ENTER_BUFFERED_ENTRY_MODE   0x5
#define SET_ATM_MODE                0x8
#define RETURN_ENTRY_COUNT          0x3
#define SET_GLOBAL_MASK_REGISTER    0x2
#define SET_ALMOST_FULL_POINT       0x7
#define SET_FAST_READ_REGISTER      0x9
#define FAST_READ                   0xa

/* define registers as contents of pointer variables */
#define IO_REG0    *io_reg0_ptr
#define IO_REG1    *io_reg1_ptr
#define IO_REG2    *io_reg2_ptr
#define IO_REG3    *io_reg3_ptr
#define OP_REG     *op_reg_ptr
#define FLAG_REG   *flag_reg_ptr
#define ERR_REG    *err_reg_ptr
#define INT_REG    *int_reg_ptr

/* function template declarations */
void output_connections();
void verify_connections();
void reclaim_output_values(int);
void next_output();

/* global variable declarations */
unsigned int *io_reg0_ptr;      /* pointer to I/O register 0 */
unsigned int *io_reg1_ptr;      /* pointer to I/O register 1 */
unsigned int *io_reg2_ptr;      /* pointer to I/O register 2 */
unsigned int *io_reg3_ptr;      /* pointer to I/O register 3 */
unsigned int *op_reg_ptr;       /* pointer to operation register */
unsigned int *flag_reg_ptr;     /* pointer to flag register */
unsigned int *err_reg_ptr;      /* pointer to error register */
unsigned int *int_reg_ptr;      /* pointer to interrupt register */
```

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```
int vpi[CAMSIZE];              /* array to hold VPIs during verification */
int vci[CAMSIZE];              /* array to hold VCIs during verification */
int out_msw[CAMSIZE];          /* array to hold upper 16 bits of output words */
int out_lsw[CAMSIZE];          /* array to hold lower 16 bits of output words */
int output_values[CAMSIZE/16]; /* array to designate available output values */
int insert_value_time = 0;     /* set by switch when a new connection is needed */
int delete_value_time = 0;     /* set by switch when time to drop a connection */
int check_conn_time = 0;       /* set by switch to trigger connection check */
int new_vpi = 0;               /* switch provides new connection's VPI here */
int new_vci = 0;               /* switch provides new connection's VCI here */
int del_vpi = 0;               /* switch provides VPI to delete here */
int del_vci = 0;               /* switch provides VCI to delete here */
FILE *f_conn;                  /* pointer to connections file */
int conn_count;                /* number of active connections in CAM */

void main()
{
  int a, b;

 // assume CAM is decoded at address F000 hex
 io_reg0_ptr  = (unsigned int *)0xF000; /* address offset 0 */
 io_reg1_ptr  = io_reg0_ptr + 1;        /* address offset 1 */
 io_reg2_ptr  = io_reg0_ptr + 2;        /* address offset 2 */
 io_reg3_ptr  = io_reg0_ptr + 3;        /* address offset 3 */
 op_reg_ptr   = io_reg0_ptr + 4;        /* address offset 4 */
 flag_reg_ptr= io_reg0_ptr + 5;         /* address offset 5 */
 err_reg_ptr  = io_reg0_ptr + 6;        /* address offset 6 */
 int_reg_ptr  = io_reg0_ptr + 7;        /* address offset 7 */

 // Initialize output_values[] array to indicate all output values are available
  for(a = 0; a < CAMSIZE/16; a++)
      output_values[a] = 0xFFFF;        /* set all the bits */

 // For VPI/VCI translation, the ATM mode must be used to match virtual
 // path connections and virtual circuit connections simultaneously.
 OP_REG = SET_ATM_MODE;        /* writes 0x0008 to operation register */
 while((FLAG_REG & LAST_OP_COMPLETE) == 0)
      ;    /* null statement - loop until last operation is completed */

 // Now set the mask register for VPI/VCI translation. Assuming the upper
 // four bits are not used for any proprietary purpose, the mask register
 // should be set to F0000000FFFFFFFF for Network-Network Interface protocols.
 IO_REG3 = 0xF000; /* 0xFF00 for UNI */
 IO_REG2 = 0x0000;
 IO_REG1 = 0xFFFF;
 IO_REG0 = 0xFFFF;
 OP_REG = SET_GLOBAL_MASK_REGISTER;   /* write opcode to operation register */
 while((FLAG_REG & LAST_OP_COMPLETE) == 0)
      ;    /* null statement - loop until last operation is completed */

 // Set the CAM to fast entry mode, which is the preferred method of
 // entering large numbers of new entries.
 OP_REG = ENTER_FAST_ENTRY_MODE;
 while((FLAG_REG & LAST_OP_COMPLETE) == 0)
      ;    /* null statement - loop until last operation is completed */

 // Setting the almost-full point is optional.  This example sets a
 // value of 2048, which represents the half-full point of the MCM69C232.
 IO_REG0 = 0x0800;    /* hex equivalent of 2048 */
 OP_REG = SET_ALMOST_FULL_POINT;
 while((FLAG_REG & LAST_OP_COMPLETE) == 0)
      ;    /* null statement - loop until last operation is completed */

 // Now the initial set of connections can be loaded into the CAM.  Let's
 // assume that the first two connections are the same every time the switch
 // is rebooted, so we can examine how a VPC and a VCC are established. The
 // rest of the connections will be loaded from a file called "connect.dat"
```

```
// When the CAM is in ATM mode, establishing a connection with a VCI of
// 0xFFFF defines a VPC.  Any input value with the corresponding VPI will
// result in a match, regardless of the VCI input value. When inserting
// a value, the VPI is loaded (right-justified) into I/O register 3, the
// VCI into I/O register 2, and the 32 bit value to be output on a match
// is loaded into I/O registers 1 & 0.
IO_REG3 = 0x07AC;              /* lower 12 bits are VPI (lower 8 bits for UNI) */
IO_REG2 = 0xFFFF;              /* VCI of FFFF defines this as a VPC */
                               /* Any cell with VPI of 7AC will match this entry */
next_output();                 /* Sets I/O registers 1 & 0 with output value */
OP_REG = INSERT_VALUE;         /* execute insert-value instruction */
while((FLAG_REG & LAST_OP_COMPLETE) == 0)
     ;    /* null statement - loop until last operation is completed */

// now load the constant VCC */
IO_REG3 = 0x0EB7;              /* lower 12 bits are VPI (lower 8 bits for UNI) */
IO_REG2 = 0x4000;              /* VCI not FFFF defines this as a VCC */
                               /* Both VPI and VCI of incoming cell must match */
next_output();                 /* Sets I/O registers 1 & 0 with output value */
OP_REG = INSERT_VALUE;         /* execute insert-value instruction */
while((FLAG_REG & LAST_OP_COMPLETE) == 0)
     ;    /* null statement - loop until last operation is completed */

// Open the file that holds the rest of the connection information.  Each
// entry consists of two integers, corresponding to the VPI and VCI values
// to be written to I/O registers 3 & 2.  The 32 bit output value is returned
// in I/O registers 1 & 0 by a call to the function "next_output".
f_conn = fopen("connect.dat", "r");
if(f_conn == NULL)
     {printf("Error opening connections file. \n");
      exit(-1);}

// Now loop until the end of file is reached, loading values from the file
// into the I/O registers, generating the output value, then executing the
// insert-value instruction. To prevent overflow, include a counter variable
// in the for statement.
for(a = 2; a < CAMSIZE; a++)
       {
        b = fscanf(f_conn, "%04x%04x", io_reg3_ptr, io_reg2_ptr);
        if(b != EOF)
             {
              next_output();
              OP_REG = INSERT_VALUE;
              while((FLAG_REG & LAST_OP_COMPLETE) == 0)
                    ;    /* null statement - loop until last operation is completed */
             }
       }

// Now that the initial connection values are loaded, the table must be
// sorted to prepare the CAM for match operations. The initialize-table
// instruction requires as much as 12 milliseconds to complete.  If desired,
// an interrupt can be enabled to occur upon completion so the controller
// can do other things.  In this example, we will wait for completion.
OP_REG = INITIALIZE_TABLE;
while((FLAG_REG & LAST_OP_COMPLETE) == 0)
     ;    /* null statement - loop until last operation is completed */

// At this point, the CAM is initialized and match port operations can
// begin.  Execution of the initialize-table instruction automatically
// switched us to buffered entry mode, so we can continue to add new values
// as needed without running initialize-table again.  We now will loop
// continuously, checking for a new connection to add, an old one to delete,
// and periodically reading the table to verify the existing connections.
while(1)  /* continue in this loop until hardware reset */
 {
     /* insert a new value if switch has set flag and CAM isn't full */
```

```
        if(insert_value_time && ((FLAG_REG & CAM_TABLE_FULL) == 0))
         {
          while(FLAG_REG & ENTRY_QUEUE_FULL)
                    ; /* wait until queue isn't full */
          IO_REG3 = new_vpi;  /* switch provides new VPI in this variable */
          IO_REG2 = new_vci;  /* and new VCI in this one */
          next_output();      /* call function that generates output value */
          /* Output values of dropped connections are only reclaimed by the
             check_connections process.  Call these functions if next_output
             returned a value of 0xFFFF in I/O register 0. */
          if(IO_REG0 == 0xFFFF)
               {
                output_connections(); /* copy connection data from CAM to arrays */
                reclaim_output_values(conn_count); /* update connection bit array */
                next_output();     /* guaranteed to work this time, since number of
                                   available output values = number of CAM entries */
               }
          OP_REG = INSERT_VALUE; /* execute insert-value now that inputs are ready */
          while((FLAG_REG & LAST_OP_COMPLETE) == 0)
                    ;    /* null statement - loop until last operation is completed */
         }

        // Next delete any connections that are no longer needed.  The output
        // values could be reclaimed as the connection is dismantled, but we
        // will wait to do that during the process of verifying connections.
        if(delete_value_time) /*flag set by switch to delete a connection */
              {
               while(FLAG_REG & ENTRY_QUEUE_FULL)
                     ; /* loop until queue is not full */
               IO_REG3 = del_vpi;     /* switch provides VPI of connection to kill */
               IO_REG2 = del_vci;     /* and the VCI  */
               OP_REG = DELETE_VALUE; /* execute the delete operation */
               while((FLAG_REG & LAST_OP_COMPLETE) == 0)
                     ; /* null statement - loop until last operation is completed */
              }

        // The switch sets the flag check_conn_time when the table of active
        // connections needs to be verified. The array of bits that tracks
        // available output values is also updated at this time, reclaiming
        // any values that belonged to now-deleted connections.
        if(check_conn_time)
         {
          output_connections();  /* copy values from CAM to data arrays */
          verify_connections();  /* compare data in arrays to expected values */
          reclaim_output_values(conn_count); /* reset bits that represent available
                                      output values */
         }
       }
      }

    void output_connections()
     {
      int b;
      while((FLAG_REG & ENTRY_QUEUE_EMPTY) != 0)
                ; /* loop until queue is empty, a condition for fast-read instruction */
      OP_REG = RETURN_ENTRY_COUNT;
      while((FLAG_REG & LAST_OP_COMPLETE) == 0)
                ;    /* null statement - loop until last operation is completed */
      conn_count = IO_REG0; /* save # of connections before overwriting I/O reg 0 */
      /* set the fast-read register to 0 */
      IO_REG0 = 0x0000;
      OP_REG = SET_FAST_READ_REGISTER;
      while((FLAG_REG & LAST_OP_COMPLETE) == 0)
                ;    /* null statement - loop until last operation is completed */
```

```
  // Now perform fast-read operations from location 0 thru (conn_count - 1),
  // saving the vpi, vci, and output data into arrays for verification.
  for(b = 0; b < conn_count; b++)
       {
        OP_REG = FAST_READ;
        while((FLAG_REG & LAST_OP_COMPLETE) == 0)
                    ;    /* null statement - loop until last operation is completed */
        vpi[b] = IO_REG3;
        vci[b] = IO_REG2;
        out_msw[b] = IO_REG1;
        out_lsw[b] = IO_REG0;
       }
  }

// This function compares the values read from the CAM into arrays vpi[], vci[],
// out_msw[], and out_lsw[] to the values of the active connections. The imple-
// mentation will be dependent on the method the switch uses to hold those
// expected values.
void verify_connections()
 {
 }

// This function manages an array of bits equal in size to the number of bits
// in the CAM.  It assumes 16 bits per integer.  A bit value of 1 means the
// corresponding output value is available, while a 0 means it is in use. Bit 0
// of word 0 corresponds to an output value of 0x0000, bit 1 of word 0 -->
// 0x0001, bit 14 of word 0 --> 0x000E, bit 0 of word 1 --> 0x0010, etc.
void next_output()
 {
  int a, b;
  for(a = 0; a < CAMSIZE/16 && (output_values[a] == 0); a++)
             ;  /* loop until a non-zero value is found */
  if(a == CAMSIZE/16)
       IO_REG0 = 0xFFFF;    /* indicates no output values are available */
  else
       {
       /* find the first non-zero bit within word a */
        for(b = 0; b < 16 && ((output_values[a] & (2^b)) == 0); b++)
                    ;  /* loop until a bit is found that is a 1,
                          corresponding to an available value */
        IO_REG0 = a*16 + b; /* put the output value in I/O register 0 */
        IO_REG1 = 0x0000;    /* output ranges from 0-CAMSIZE, so upper 16 bits = 0 */
        output_values[a] = output_values[a] & ~(2^b); /* clear bit we assigned */
       }
 }

// This function manipulates the array output_values[].  Each bit represents a
// possible output value. A value of 0 means the value is in use, while 1 means
// the value is available.  First we set all bits, then clear bits that correspond
// to output values that are being used by an active connection.
void reclaim_output_values(int count)
 {
  int a, b, c, d;
  // Set all the bits to signify all output values are available. Those that
  // are in use will be cleared one by one.
  for(a = 0; a < CAMSIZE/16; a++)
       output_values[a] = 0xFFFF;  /* set all the bits */
```

```
 for(a = 0; a < count; a++)
      {
       b = out_lsw[a];           /* integer value of an output */
       c = b/16;                 /* calculates which 16 bit word of output_values[]
                                                corresponds to the value of b */
       d = b % 16;               /* calculates which bit in that word
                                                corresponds to the value of b */
       /* now clear bit d of word c */
       output_values[c] = output_values[c] & ~(2^d);
      }
}
```

AN1704

Switch Fabric Implementation Using Shared Memory

Prepared by: Lakshmi Mandyam and B. Kinney

INTRODUCTION

Whether it be for the World Wide Web or for an intra–office network, today's businesses and services are heavily dependent on the telecommunications infrastructure. Computers and networks are inextricably linked in business today. Just as processors have increased their speed in instructions per second, users have demanded more bandwidth in megabits to gigabits per second from their networks. Many high–speed technologies have emerged or are emerging including: FDDI, CDDI, Fast Ethernet, Gigabit Ethernet, and Asynchronous Transfer Mode (ATM). Only ATM has the ability to integrate voice, video, and data over a single medium and requires a great deal of high–speed bandwidth. One of the major ways that switch, router, and hub manufacturers have been able to differentiate their products has been in the fabric and buffer management. The shared or distributed cell or frame fabric as well as the input and/or output buffers determine:

1. The scalability of the network.
2. The non–blocking capacity of the network.
3. The throughput experienced by the users.
4. Each user's service levels.

These issues are common across all of the network devices. In the carrier network, ATM is widely used because it reduces the number of network overlays and provides seamless integration of LAN and WAN equipment. The switch fabric buffering scheme is of major importance to the flexibility and adaptability of the network. For the end user, new markets are being developed that require fast efficient buffering schemes; such as multimedia support, bandwidth–on–demand, and high–speed data transfer for internet and access to the corporate headquarters.

For the data LAN networks, Gigabit Ethernet provides an easy migration to gigabit speeds by upgrading the existing legacy Ethernet 10BaseT and 100BaseT systems. The higher throughput and the need to match different speeds on inputs and outputs also requires a great deal of shared–memory fabric and buffering.

SWITCH FABRIC

The function of the common block of memory or shared fabric is to store–then–transfer cells or frames between other functional blocks in the switch/router. Examples of the functions of fabric are:

1. Cell or frame buffering.
2. Traffic concentration and multiplexing.
3. Redundancy for fault tolerance.
4. Support of multi–casting or broadcasting.
5. Cell scheduling based on delay priorities.
6. Selective cell discarding based on loss priorities and congestion level.
7. Congestion monitoring.

There are many types of fabric architectures and choosing one usually depends on where the switch will exist in the network and the amount of traffic it will be required to carry. In reality, fabric implementation is often a combination of two or more basic architectures. Figure 1 illustrates the variety of possible switch fabric architectures.

The type of architecture that is common to the majority of network devices is the shared fabric memory (see Figure 2). Motorola has several products available for shared memory implementation including Late Write, BurstRAM™, and a new product, NetRAM™. There will be slightly different implementations for each design, but the basic functionality will remain the same.

In shared fabric implementations, fast SRAMs are used to buffer data before transmitting it. The memories are organized in banks to create a shared–memory block of 576 bits wide for ATM and 64 bytes wide for Ethernet. The depth of the fabric will be determined by the bandwidth required of the ports for input and output. With dynamic allocation, the advantage of shared fabric is that it enhances the flexibility of determining network throughput and guarantees that data will not be blocked or dropped as it passes through the switch.

Motorola's new NetRAM, a dual port SRAM with configurable input/output data ports is designed specifically for the communications market to deliver optimal performance for networking devices that demand write/read/write cycles. In this application note, two implementations of switch fabric will be discussed using the NetRAM.

1. The "One–Way" switch fabric implementation with separate input and output ports.
2. The "Snoop" switch fabric implementation with two dual–ports: each capable of supporting input and output.

BurstRAM and NetRAM are trademarks of Motorola, Inc.

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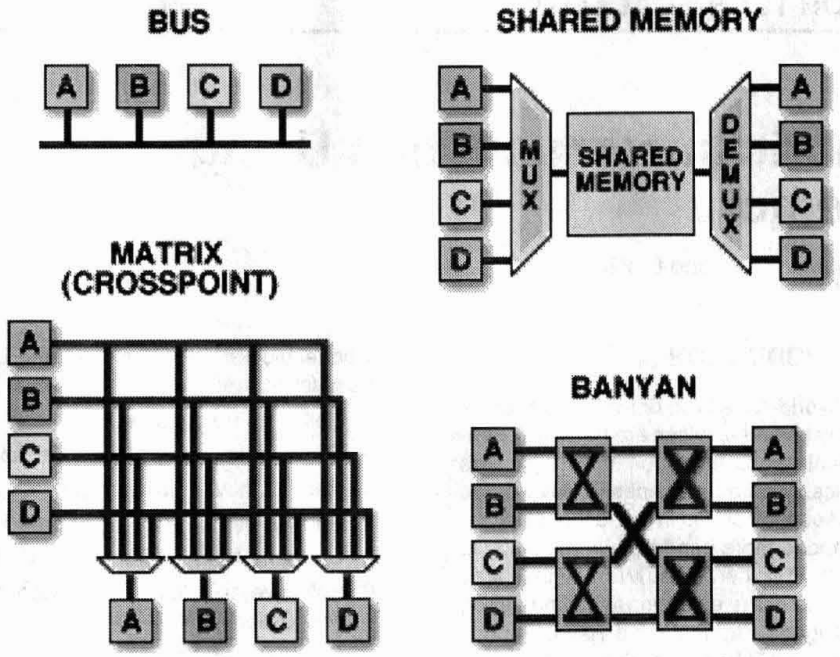

Figure 1. Types of Fabric Architectures

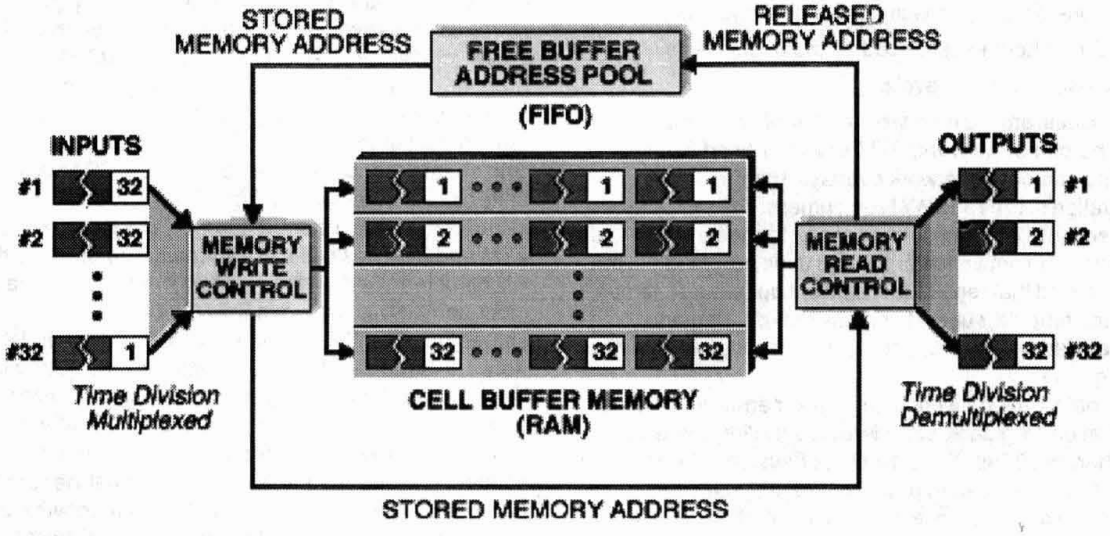

Figure 2. Shared Memory Switch Fabric

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"ONE–WAY" SWITCH FABRIC

In the first implementation (Figure 2), an ATM example realizes output buffering and can support multiple qualities of service (different priorities) and multicast/broadcast. Inputs to the common shared memory fabric are time–division multiplexed (TDM) so that only one input port is granted permission to deposit a cell into the shared memory. As the cell traverses the memory write controller, the output port destination is decoded and used to determine which output queue is to receive the cell. A free buffer address is generated to provide a write address for the cell in the fabric. In addition, this address is "linked" to the tail of the output queue managed by the memory read controller.

Cells leaving the fabric are time–division demultiplexed so that only one output port has access to the fabric. Arbitration is usually necessary, because there may be many cells competing for access to the output port. It is the responsibility of the memory read controller to determine which cell wins the arbitration and is forwarded to the output port. Once the cell has been transmitted, the available fabric address is returned to the free fabric–address pool.

An implementation of switch fabric using NetRAM in a "one–way" path is shown in Figure 3. Input modules or line cards are connected to the NetRAM data inputs, and output modules or line cards are connected to the data outputs. The read address port and write address ports are connected to the external controller or application specific integrated circuit (ASIC).

As noted previously noted, the ASIC generates the memory address for the cell to be stored until the destination output port becomes available. The store address is sent to the AY port of NetRAM and the cell is written from the input port (DQY) to the fabric after the write enable signal ($\overline{WY}$) is activated. The timing diagram is shown in Figure 4.

When a destination output port for the data cell becomes available, the ASIC recalls the read address of where it had previously stored the cell and sends it to the AX port on NetRAM. After the read is performed, the data is available at the output port (DQX) two internal clock cycles later providing output enable ($\overline{GX}$) is activated at that time. Notice that the internal clock is running at twice the external clock. Because of this, board frequencies can be maintained at frequencies equal to or less than 83 MHz while the device delivers performance equivalent to a conventional 166 MHz memory.

NetRAM is a pipelined part with reads occurring before writes. Therefore, if a read and a write occur at the same address on the same clock edge, the read data available from the location will be the cell or frame that was previously in memory and the write data will be written after the read has occurred. Thus, NetRAM resolves potential address contention situations without the need of external arbitration logic or special ASICs to make sure the data is transferred without corruption.

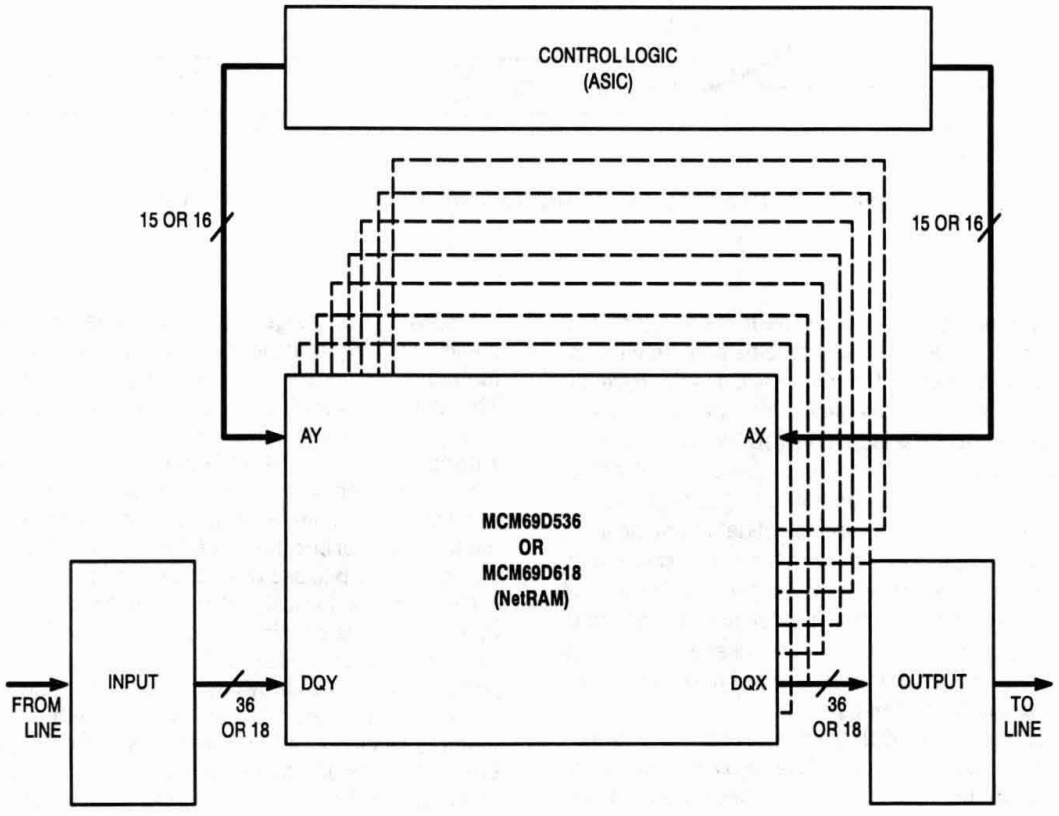

Figure 3. "One–Way" Switch Fabric Implementation Using NetRAM as a Separate I/O Device

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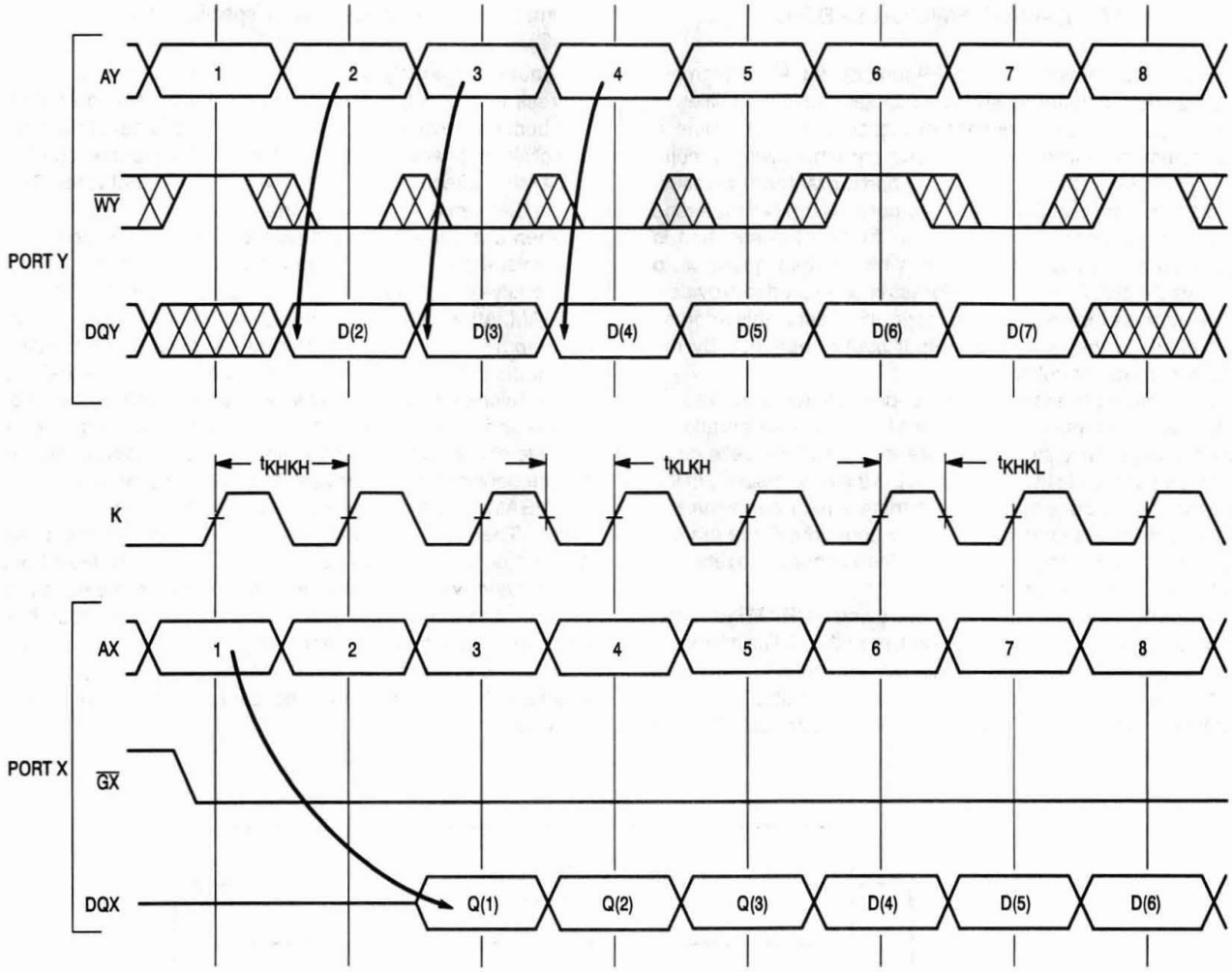

Figure 4. Read/Writing Timing Diagram for "One Way" Switch Fabric

There are additional functions available to the designer. The pass–through function allows the data to be sent from the input to the output, bypassing the memory. Consider cycle t_4: pass–through ($\overline{PTY}$) and write enable ($\overline{WY}$) are asserted and as a result, data on NetRAM input port Y (DQY) gets written to address A(4) and is passed through to the output at port X (DQX) and becomes available on the output at cycle t_6. In a situation where the system is trying to get data from the input port to the output port as soon as possible, the pass–through function saves two cycles of system time over a RAM without the pass–through function. Without this function, to send data from memory input to memory output, the user would have to wait until data was written to the AY address and then send a read address to the AX address port.

The write–and–pass–through function allows the data to be sent from the input to the output, and the data also is written to memory in the normal fashion. Figure 5 shows both pass–through and write–and–pass–through timing for moving data from port Y to port X.

NetRAM's advantage over conventional single address and common I/O RAMs is that it allows reads and writes to be performed at different addresses during the same clock cycle. This dual address feature gives the NetRAM a very high throughput of this one–way fabric of 2.98 Gbits/sec which is sufficient to support up to OC–12 throughput. In addition, most fabric implementations bank several memories together in parallel. In the example given, assume that 16 memories are banked together and thus the total available throughput would be 16 x 2.98 Gbits/sec or 47.8 Gbits/sec.

Consider the flexibility of this part if the designer were to double up on the data input and data output. The configurable data ports allow the designer to read simultaneously from both ports in the same clock cycle providing a throughput of approximately 6 Gbits/sec with one device. With a 576–bit wide memory block and 16 NetRAMs connected in parallel (Figure 6), the maximum throughput becomes approximately 96 Gbits/sec. This is one of NetRAMs advantages when configured in the "snoop" switch fabric implementation as described in the following section.

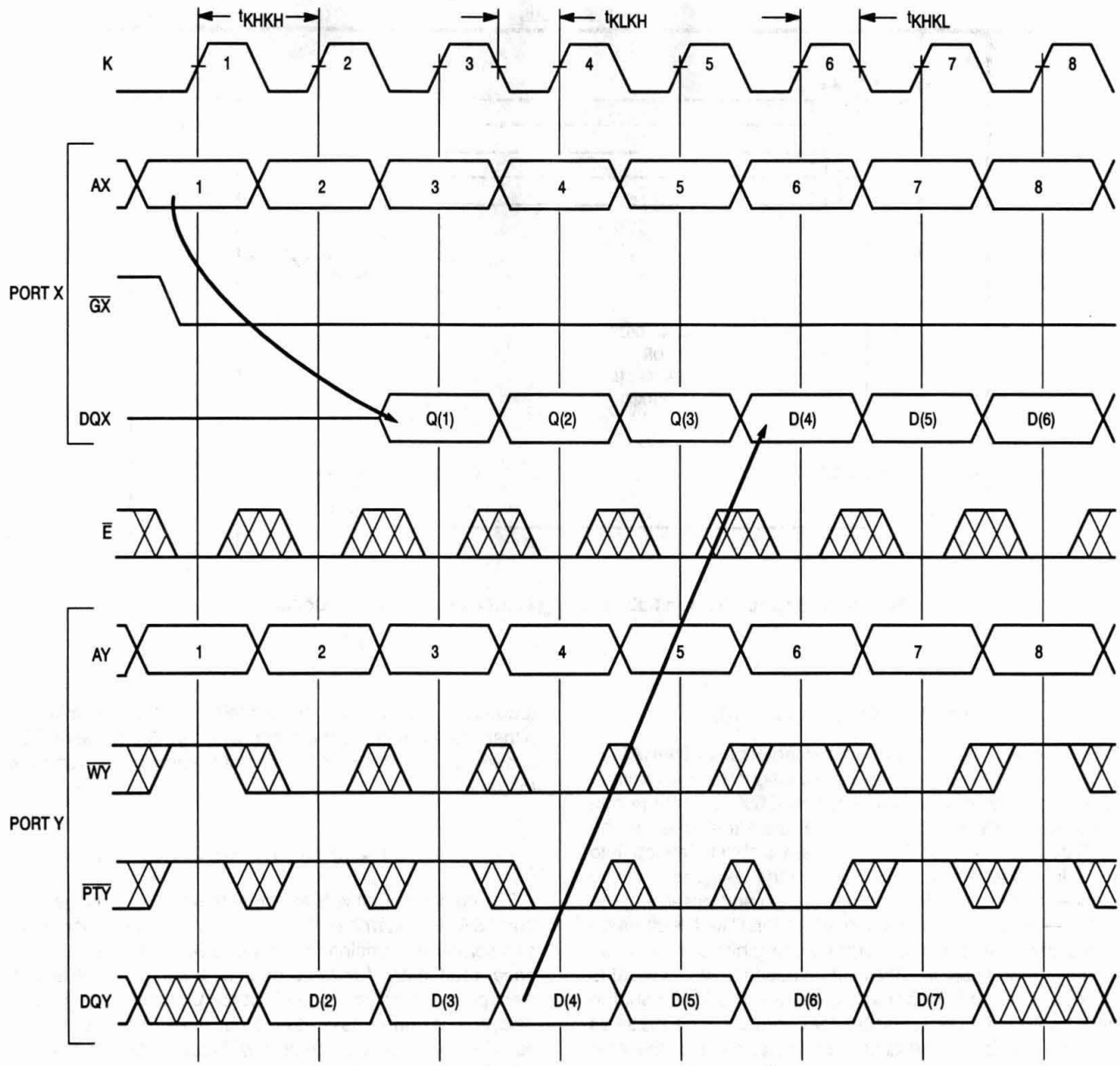

Figure 5. Write and Pass–Through Timing for "One Way" Switch Fabric

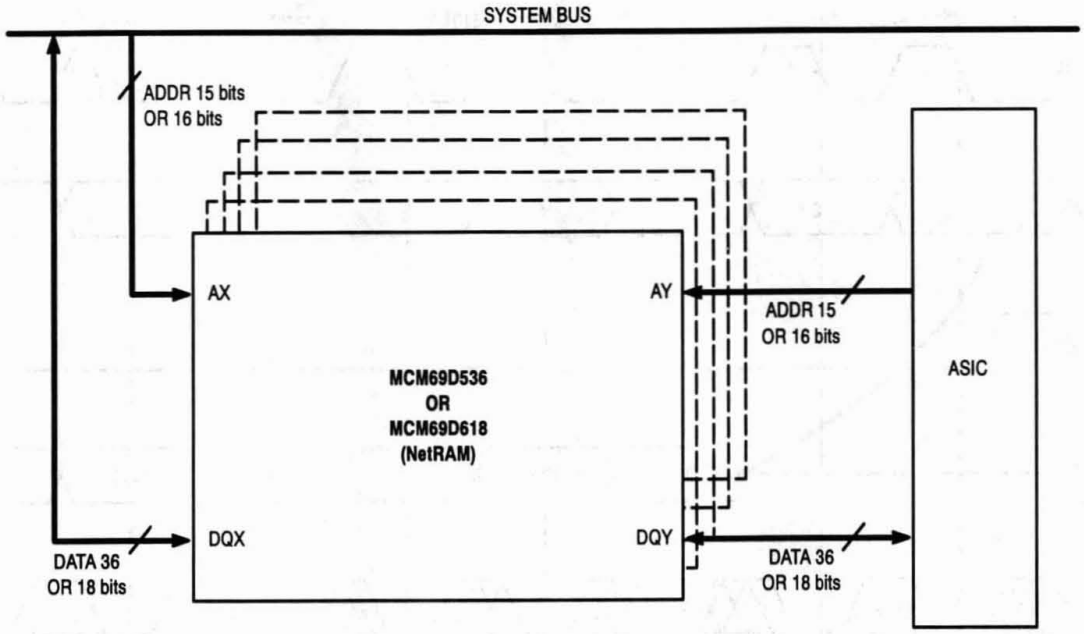

Figure 6. "Snoop" Switch Fabric Using NetRAMs as Dual I/O Devices

"SNOOP" SWITCH FABRIC

The "snoop" switch fabric implementation of NetRAM is shown in Figure 6. The NetRAM is configured as a common I/O with the system bus utilizing port DQX for storage and retrieval of cells or frames. While at the same time, on the ASIC dual port side (DQY), the system is able to "snoop" into any address to retrieve any data that the designer wants to verify — such as for Ethernet destination addresses — or to modify — such as the VPI/VCI headers for ATM. It is common for the designer to include error checking bits or other intellectual property data that the system needs to have available as soon as the cell or frame begins to arrive in the shared memory. This makes it possible for decisions to be made as early as possible in the data input cycle, such as the next destination or priority of service. The ability to write back data at any address is one of the major advantages.

This implementation takes away the need to have a separate path to separate out this critical information from the data flow, because the entire cell or frame is placed into the shared memory, thus reducing chip count and board space.

The "snoop" dual–ported fabric can be configured as a 64K x 18 and 32K x 36 in a dual–ported configuration, which is larger than any other dual–ports on the market and the first of many dual–ported products that will be available from Motorola.

Consider the timing diagram in Figure 7. Assume that in cycle t_2, the cell or frame D(2) gets written to address A(2) in the fabric. In cycle t_3, this cell data can be "snooped" or read from address A(2) by ASIC using address port AY, and become available on data bus (DQY) at the end of cycle t_4 and during cycle t_5. The modifications to this data can be made by ASIC and written back to the fabric in cycle t_6. Simultaneously, the AX port (cell transfer side) can continue to either read or write to the fabric with deselects inserted between the read and write transitions to eliminate corruption of the data.

COMPARISON TO BURST SRAM

The computer market's extremely high volume usage of the burst SRAM determined there would be multi–vendor supply and competitive pricing for the burst SRAMs. For the write–once, read–many functions of level–2 cache, burst SRAMs were perfect. For the cost and supply reasons, some communications designers have attempted to use them in switch fabric. The common characteristic of burst SRAMs is that they have one address port and a common input/output port. As a result, during one clock cycle, the device can either read an address location or write to an address location. In addition, when the common I/O must be turned from the read to write, a deselect cycle must be inserted into the timing, which results in one wait state. It is even worse for the turning of the bus from write to read since two deselect cycles must be inserted to make sure there are no conflicts on the common I/O bus. This translates to a utilization of the clock cycles to data in or out, of between 50 to 70%, depending on the pattern used to access the data in the fabric. For this reason, the burst SRAM parts are not efficient for the write/read/write cycles of the communications market, and this limitation becomes more critical for the gigabit and terabit bandwidths of switches and switch/routers. NetRAM can be configured as a separate I/O device or a dual I/O device which avoids the overall system performance penalties imposed by the need to insert deselect cycles with a common I/O burst SRAM.

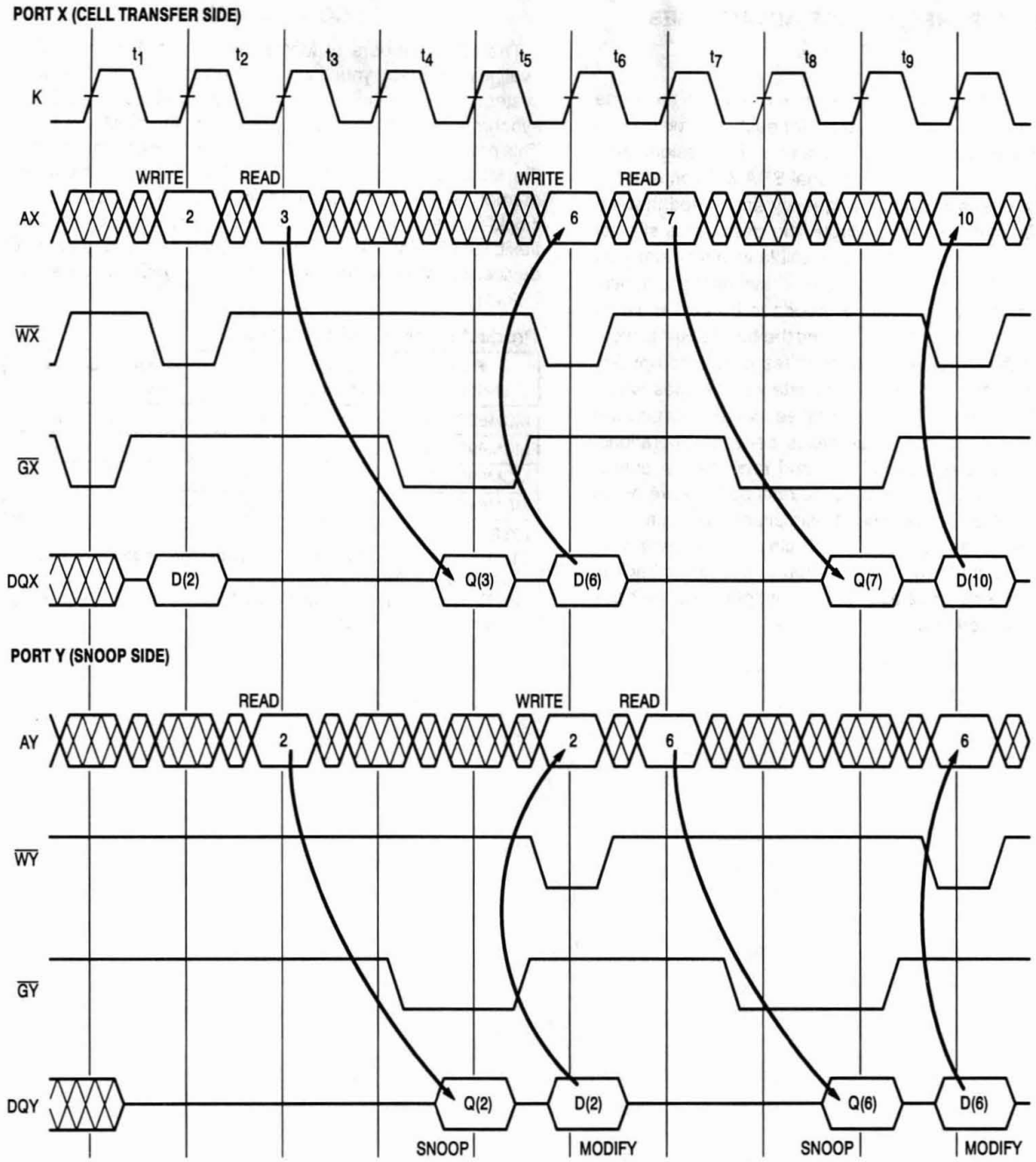

Figure 7. Timing for Snoop Fabric Implementation

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SYSTEM PERFORMANCE ADVANTAGES OF NetRAM

NetRAM has the ability to do reads and writes in the same clock cycle with separate addresses for each port, empowering the designer to create higher–speed switch designs than would be possible with a conventional SRAM. Even with the dramatic increases in system frequency and speed that the burst SRAMs have made available, the designer is still not able to get the throughput that is possible with the dual–port NetRAM product while maintaining lower system frequencies.

The communications designer needs to be able to write/read/write a great deal of the time and the burst SRAMs were created for the burst reads and writes of the computing applications. In applications such as datacom switches, which frequently transition from reads to writes, burstRAMs perform inefficiently, causing dead bus cycles between operations. This increases design complexity and reduces the overall system performance. In addition, the dual port feature of the NetRAM enables the designer to simultaneously read and write to different addresses in each clock cycle. Even with recently announced products that read and write in back to back cycles without deselects, the throughput would be one–half that of the NetRAM.

CONCLUSION

The first members of Motorola's NetRAM family will be available to meet your high–performance communications system memory requirements. The MCM69D536 is a 3.3–volt synchronous 32K x 36 dual port SRAM with pipelined reads. This product is also available in the 64K x 18 configuration as the MCM69D618. The NetRAM offers a high–performance memory solution with frequencies as high as 83 MHz and clock–to–data access times of 6 ns. This device also offers the flexibility of being used as either a dual I/O or a separate I/O device. The various configurations of the NetRAM are shown below.

Product Family Configurations

Part Number	Dual Address	Single Address	Dual I/O	Separate I/O
MCM69D536	✓	Note 1	✓	Note 2
MCM69D618	✓	Note 1	✓	Note 2
MCM69Q536		✓		✓
MCM69Q618		✓		✓

NOTES:
1. Tie AX and AY address ports together for the part to function as a single address part.
2. Tie $\overline{GX}$ high and $\overline{WX}$ low for DQX to be inputs and tie $\overline{WY}$ high and $\overline{GY}$ low for DQY to be outputs.

AN1707

Dual Port Memory for Multiprocessor Applications

Prepared by: Jim Lewis and Lakshmi Mandyam

The most common implementation of a multiprocessor (MP) system is a bus–based multiprocessor, i.e., one where the processors in the system share a common system bus. In this implementation, the system bus is the sole avenue to access main memory and the system's I/O devices. Because of this, the system bus becomes a bottleneck causing performance degradation. The use of external cache memory can help alleviate this problem. There are various issues that should be considered when implementing external caches in MP systems. This applications note discusses the various implementations of external caches and the pros and cons of each implementation. In particular, this document will illustrate the advantages of using Motorola's dual port SRAM, the MCM69D618, for both the tag and data RAM of an inline cache. First we will discuss the issues involved with shared bus architectures, and then we will discuss the issues involved with inline cache implementation.

ISSUES WITH SHARED BUS ARCHITECTURES

A major problem in such a system is that the shared bus becomes a bottleneck. Each microprocessor has a large appetite for data which will require frequent accesses to memory. Today's microprocessors have large internal caches but these are not enough to satisfy all requests. Each processor has to compete with other devices for access to the shared system bus to satisfy its internal data requirements. With processor internal clock speeds reaching the hundreds of megahertz range, but system bus speeds remaining in the 66 to 133 MHz range, the gap between the two is widening rapidly. Therefore, requests from the processor can queue up more quickly than the main memory system can satisfy them, leading to system saturation and performance degradation.

A solution to these problems is larger external caches that can satisfy more of the processors' memory requests, thus taking some of the burden off of the main memory controller. However, if these external caches are resident on the system bus, in addition to everything else already present, the bus bottleneck problem is still not solved.

The ideal solution is to make the external caches "inline", i.e., a given cache sits logically between the system bus and the processor being supported by the cache. This allows the processor to have unimpeded access to its own external cache and also limits the traffic on the system bus to those transactions which cannot be satisfied by the external caches.

The system shown in Figure 1 is a generic MP system. There are four microprocessors connected to the system bus through an inline cache. The System bus also has I/O and memory controllers connected to it which are in turn connected to I/O devices and main memory respectively.

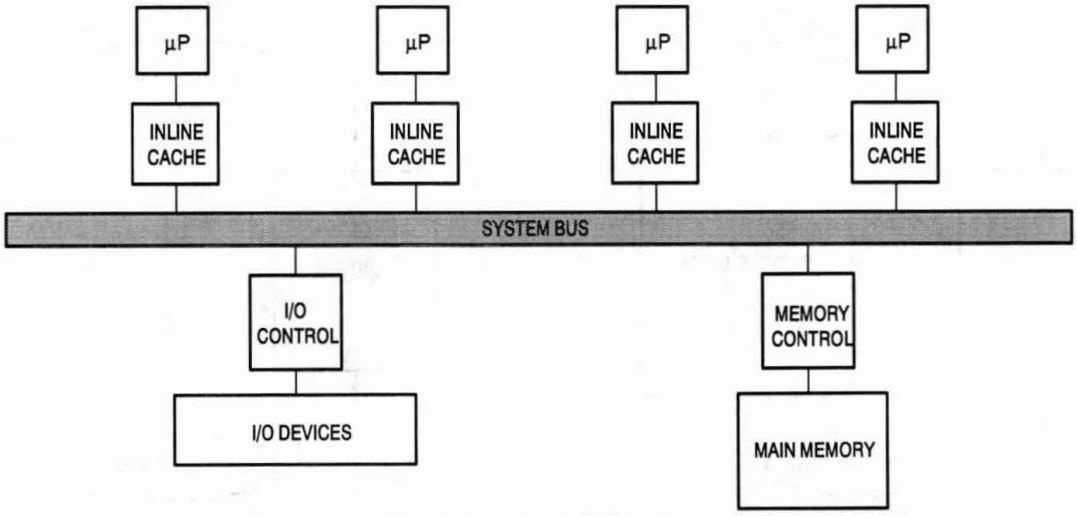

Figure 1. Generic MP System

NetRAM is a trademark of Motorola, Inc.

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As with most designs, there is more than one way to solve the problem of implementing an inline cache. There are two basic assumptions to be made about the cache:

- It will require two logical forms of RAM: tag and data
- A controller will be needed to communicate with both the processor and system buses as well as control the tag and data RAMs.

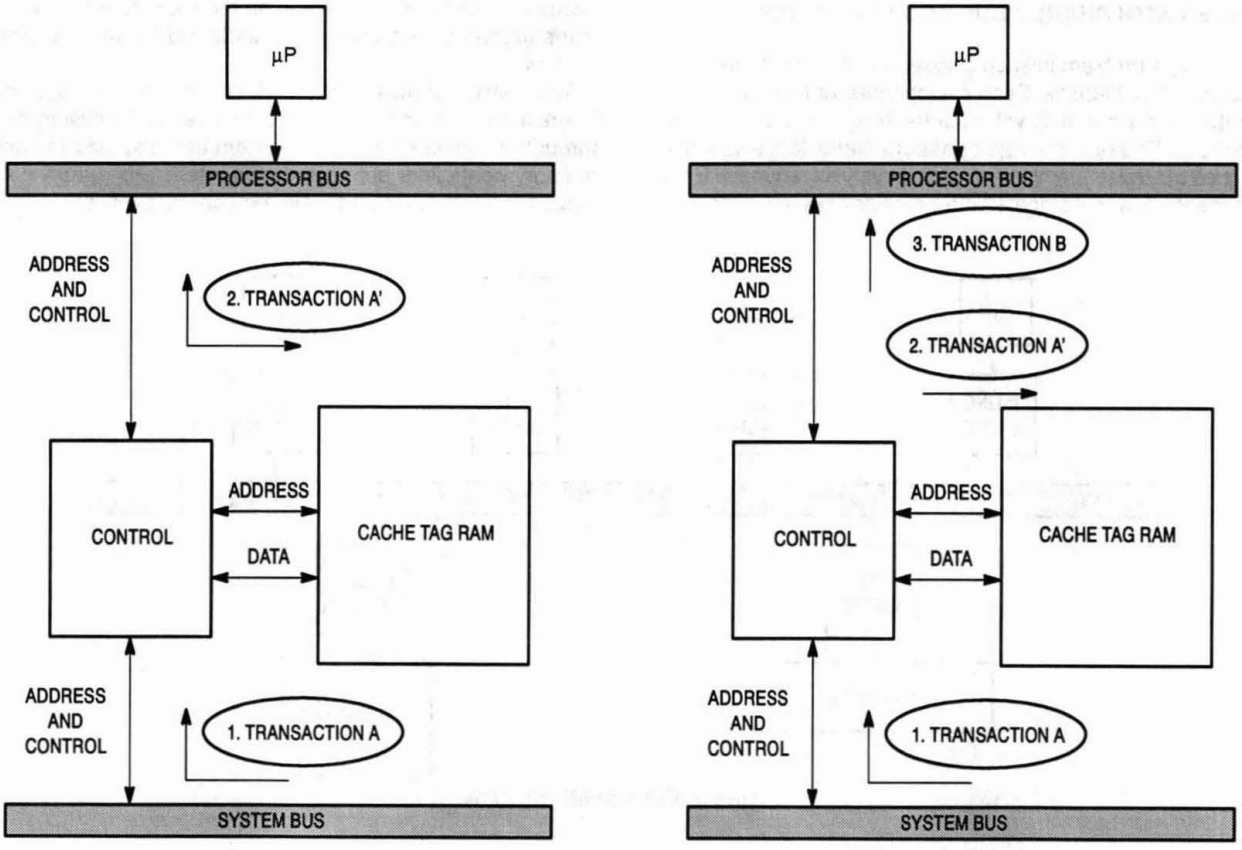
To better understand the advantages of each inline cache implementation, we will first examine cache coherency with inline caches.

CACHE COHERENCY WITH INLINE CACHES

In addition to limiting system bus traffic, an inline cache helps to maintain the coherence of system memory by monitoring all transactions that occur on the system bus. In particular, the inline cache "snoops" or watches for transactions which may require state changes to cached data due to the cache coherence protocol of the system. These transactions shall be referred to as snoop transactions. When a snoop transaction is detected, the inline cache is responsible for ensuring that the data in both the processor's on–chip cache and the inline's own data RAM transition to the proper state when the transaction completes.

A straightforward method of ensuring that coherence is maintained is for the inline cache to mimic all snoop transactions on the processor bus. For example, when the inline cache detects snoop transaction A on the system bus, it will initiate transaction A' on the processor bus. See Figure 2a. This, in effect, causes the processor to see all snoop transactions as if the inline cache were not there. While transaction A' is proceeding, the inline cache will also check its own tag to determine if any state changes are necessary. This implementation negates one of the advantages of having an inline cache, i.e., isolating the processor from the system so that it will have higher bandwidth access to its external cache.

Processor isolation can be achieved by the inline cache with a process called snoop filtering. Snoop filtering limits the snoop transactions propagated by the cache to the processor bus from the system bus. "Inclusion" is a necessary condition for snoop filtering. Inclusion means that the contents of the processor's cache are a subset of the contents of the external cache. By maintaining inclusion, the inline cache can now query its own tag RAM when it detects a snoop transaction. So when there is a snoop transaction A on the system bus, the cache generates a transaction A' to the cache tag. If the cache tag does not contain the memory locations affected by snoop transaction A then no further action needs to be taken and the processor will never be made aware that the transaction even occurred. However, if the inline cache determines that the snoop transaction affects its own contents, it will propagate the snoop transaction as transaction B to the processor bus. See Figure 2b.



a. Without Snoop Filtering

b. With Snoop Filtering

Figure 2. Cache Coherency Implementations

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The inline cache, as previously described, now has the task of handling requests from two different sources: processor–initiated transactions on the processor bus and snoop transactions on the system bus. Both of these transactions require access to the tag RAM of the inline cache.

One utilization of this shared resource is to have a single physical tag RAM as shown in Figure 3. In this design, the inline cache implements an arbitration scheme to resolve collisions between two simultaneous requests. While this implementation may be the least expensive, it imposes a performance penalty on the processor by forcing it to give up access to its external cache whenever there is a snoop transaction occurring on the system bus.

Another design uses two physical copies of the tags, one dedicated to servicing processor transactions and the other dedicated to queries from snoop transactions as shown in Figure 4. While this allows the processor the greatest access to the external cache it has the added cost of twice as much tag RAM and the overhead of maintaining two copies of the tag.

The third alternative is implemented using Motorola's MCM69D618 as the tag RAM as shown in Figure 5. The MCM69D618 is a dual port memory with two address ports (AX,AY) and two data ports (DQX, DQY) into the same SRAM array. The MCM69D618 can be clocked at 83 MHz and the user can perform reads and writes to different addresses simultaneously. Figure 5 illustrates how the MCM69D618 could be situated within the inline cache subsystem. The X port can be used to satisfy processor requests and the Y port can be used to query the tag when snoop transactions are detected. It is assumed that to prevent overloading the bus, the Y address port (AY) cannot be directly connected to the system bus. By using the MCM69D618 in this manner, an excellent cost–effective solution is obtained without compromising performance.

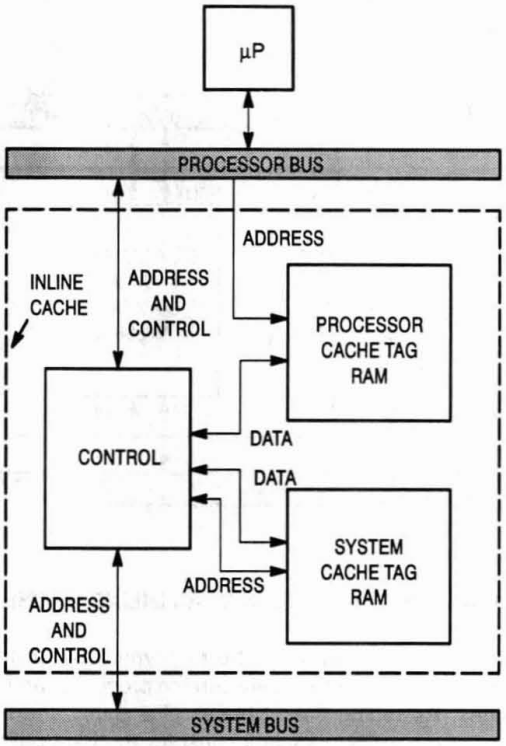

Figure 4. Inline Cache with Two Tag RAMs

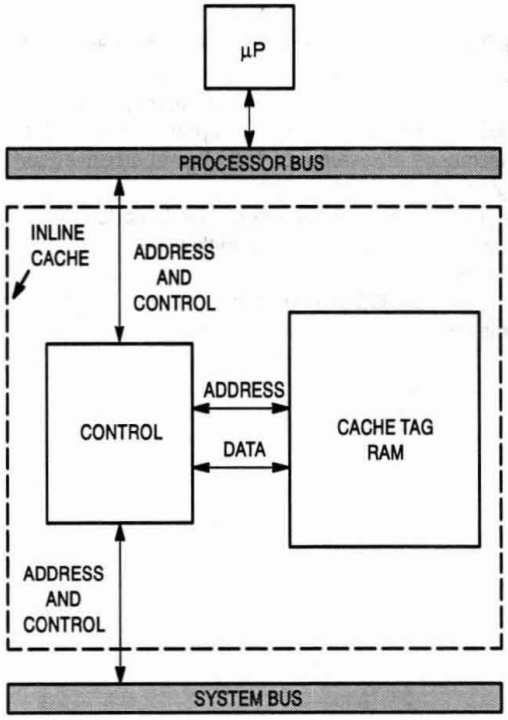

Figure 3. Inline Cache Implementation with a Single Tag RAM

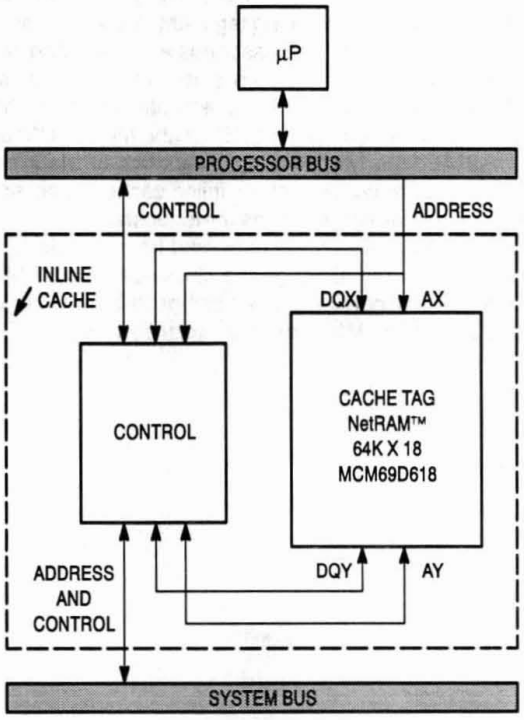

Figure 5. Inline Cache Tag Using Dual Port SRAM

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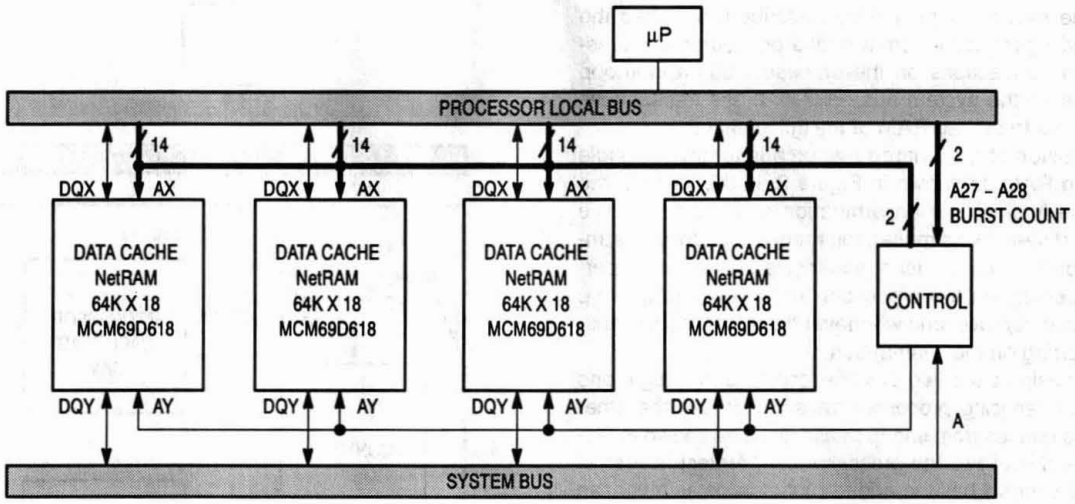

Figure 6.

DATA RAM IMPLEMENTATION IN AN INLINE CACHE

Another function that must be performed by an inline cache is the transfer of data between the processor and system buses. Assuming 64–bit buses plus parity, the inline cache must have 144 signal pins just for the data path between the two buses. The MCM69D618 has a pass through function which can write the data input from one data port to the other enabling the RAM to serve as a data path from the processor bus to the system bus. Therefore, by using MCM69D618 as the building block for the data RAM of the inline cache, the data signal pins can be removed from the inline cache control device.

Figure 6 shows four MCM69D618s being used to implement a 512KB cache. As with the tag RAM described earlier, the X port connects to the processor bus and the Y port connects to the system bus. Again, the Y port addresses are assumed to come from the inline cache controller rather than the system bus to reduce loading. Since the MCM69D618 is not a BurstRAM, the two least significant bits of the X port address will need to come from the inline cache controller to support burst responses to processor requests.

The configurable I/Os let the user read from or write to either of the data ports. Although the clock speed is 83 MHz because of the dual port feature, we can get the same performance as a 166 MHz single address RAM. The MCM69D618 provides a cost–effective method of implementing an inline cache for systems that have cost constraints placed on them.

CONCLUSION

This document has shown how the MCM69D618 can be used as the building block to implement an inline cache. The MCM69D618 provides an excellent solution for the tag RAM without compromising performance. It can also facilitate a cost–effective solution for the data RAM at the expense of a lower performance system.

The MCM69D618 system performance enhancing features are:

- The external clock runs at 83 Mhz.
- The fast access times of 6 ns help boost performance.
- The dual addressing scheme enables the user to perform simultaneous read/writes, reads/reads, writes/writes in the same clock cycle. This provides performance equivalent to 166 MHz of a conventional single address RAM.
- The price will be at a better competitive price point compared to other dual ports of this depth and performance.

Thus the MCM69D618 can greatly enhance system price/performance.

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AN1709

Motorola Fast Static RAM Known Good Die Manufacturing Process

Prepared by: Don Kost, Tony Benner, Christina Corona, Carlos Leal, Dale Robinson, Valerie Ward, and James Wilson

ABSTRACT

The Motorola Fast Static RAM Division has put in place a manufacturing process for both wirebond and flip chip Known Good Die (KGD). The goal was to manufacture KGD with the same quality and reliability as conventionally packaged die. A Die Level KGD process was developed which allows the reuse of the same equipment, manufacturing, and quality infrastructure which is used for conventional package types. This application note discusses infrastructure reuse as it relates to the manufacturing KGD process, manufacturing flow, and the process and quality procedures used to ensure delivery of cost effective KGD.

Key Words: Known Good Die, Die Carrier, Burn–in, Die Level KGD, Multichip Modules.

INTRODUCTION

Semiconductor manufacturers have supplied die with varying levels of quality and reliability for decades. Die quality was established for the most part by lot acceptance testing or varying levels of wafer probing. Approaches to wafer probing have augmented standard probe programs with voltage stress tests, IDDQ testing, at–speed, and high temperature probing.[1] Outgoing die reliability which was incrementally improved by stress and IDDQ testing remained largely a function of semiconductor process maturity. The drive for size reduction and performance improvement in Multichip Modules (MCM) favors the use of the latest, fastest, and smallest die the semiconductor industry has to offer. This is fundamentally in conflict with a die manufacturing strategy which relies on process maturity to deliver high levels of quality and reliability. The lack of die with high levels of quality and reliability has caused MCM manufacturers to employ comprehensive testing and planned rework strategies in order to deliver high quality products to their customers.[2, 3]

Motorola's Fast Static RAM Division has installed a cost effective manufacturing process for both wirebond interconnect and flip chip interconnect KGD. The goal was to manufacture KGD with the same quality and reliability as conventionally packaged die. Various methods for manufacturing KGD were considered and ranked based on cost, feasibility, maturity, reliability, and manufacturability. Die Level KGD which uses a temporary and reusable die carrier to affect electrical connection to individual IC devices was selected as the method to be pursued. High quality and reliability flip chip and wire bond packaged die are currently achieved by extensive probe, burn–in, and test. A Die Level KGD process was developed which allowed the reuse of the same equipment, manufacturing, and quality infrastructure as is used for conventional package types (e.g., TQFP, PLCC, CBGA, PBGA). This application note discusses infrastructure reuse as it relates to the KGD manufacturing flow, test, burn–in, die carrier loading and unloading, process qualification, and product qualification.

DIE LEVEL KGD CARRIER

Principally, the die carrier facilitates the use of conventional manufacturing infrastructure by transforming the tight pitch wire bond pad or solder bump electrical contacts on the die to a larger pitch which is suitable for use with conventional test and burn–in hardware. The quality of the interconnect to the die is largely a function of the contact resistance of the die carrier substrate to the wire bond pad or solder bump and the electrical parasitics associated with the die carrier substrate. Contact resistance, vibration, shock, temperature cycling, and thermal performance testing has been performed by the Microelectronics and Computer Technology Corporation (MCC) on a variety of die carriers types.[4]

At its most basic level, the die carrier is composed of an electrical substrate and a force delivery mechanism. The electrical substrate is a flexible polyimide film with fine line copper traces and conductive bumps which make contact to the die. The die carrier technology which has been utilized establishes electrical contact to a solder bump or wire bond pad with a temporary, non–metallurgical, piercing, pressure connection to a conductive bump which is on the surface of the die carrier substrate.

Electrical parasitics are reduced on power and ground channels for high performance devices by using a multi–layer metal substrate construction. Other features which enhance the manufacturability of the die carrier are an integrated single piece construction, small outline, and die retention features for use during carrier assembly and disassembly.

3/7/97

KGD MANUFACTURING FLOW

From a manufacturing development standpoint, the die carrier was viewed as a standard package type which enabled the reuse of the standard manufacturing flow, as shown in Figure 1. The only change to the manufacturing flow was disassembly of the die carrier which is added to the end of the flow.

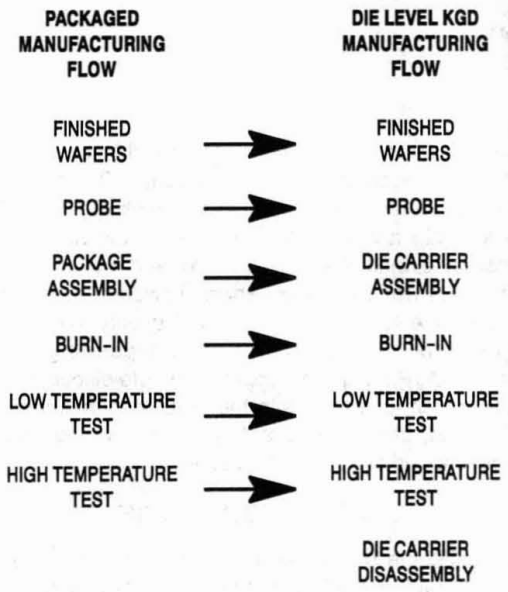

Figure 1. Comparison of Standard Packaged and KGD Manufacturing Flows

Wafers were fabricated and probe tested. In the case of flip chip interconnect die, wafers were solder bumped prior to probe testing. Probed wafers were sawn and assembled into die carriers. Assembled die carriers were then burned–in and tested at temperature extremes. Finally; die carriers are disassembled, die are visually inspected, and loaded into die shipping medium.

FINISHED WAFERS AND WAFER PROBE

The wire bond and flip chip KGD manufacturing process required no changes to the existing wafer fabrication and wafer probing manufacturing processes used for standard packaged devices. Wafers were fabricated and in the case of flip chip KGD, were solder bumped. The finished wafers were then probe tested to achieve acceptable levels of yield for subsequent operations. The probe processes for Fast Static RAM devices includes a laser repair process in which wafer yield is improved by the inclusion of redundant cells into the components address space.

DIE CARRIER ASSEMBLY

Equipment which was used for the assembly of flip chip die into conventional package types such as CBGA and PBGA was adapted for die carrier assembly. Modifications and improvements which were made to the die carrier assembly module were accomplished more effectively because of an experience base with the equipment platform. Reuse of the same equipment also allowed efficiencies in the training of equipment technicians and assembly operators. Handling trays hold up to 72 die carriers per tray and were designed to be compatible with existing media standards for assembly cells, burn–in board loaders, and test handlers.

Finished probed wafers were attached to a wafer frame and sawn using standard equipment and procedures. The *diced* wafer which was still attached to the wafer frame was loaded into the wafer handling stage of the assembly module along with handling trays containing unloaded die carriers. The die carrier was opened and a single die was removed from the wafer frame. Highly precise alignment of the die as it was loaded into the die carrier was made using vision recognition systems. Alignment was maintained as the die carrier was closed by a vacuum port in the base of the die carrier. Finally, the assembled die carrier was placed in a handling tray.

In the early phases of the program tolerance analysis indicated that the equipment used to precisely align the die into the die carrier should be capable of ± 0.0005–inch placement repeatability for the process to achieve acceptable process capability. The equipment also needed to have sufficient speed to make the die carrier assembly and disassembly process cost effective. Equipment characterization revealed that fine tuning of the equipment, beyond the normal level required for flip assembly, was required in order to achieve the process capability goals. Equipment fine tuning produced placement repeatability of ± 0.00025 inches, which exceeded program goals as shown in Figure 2.

TEST

In order to provide reliable KGD test hardware and software, the same design methodology followed for packaged test was observed. By treating the die carrier as a traditional package; standard test handlers, testers, and tester interfaces could be used.

The test programs used for testing KGD were identical to those used for the same packaged die with a minor change to the package–to–tester–channel pin list. This facilitated the reuse of test software.

Package–dependent handler change kits and tester interfaces were made for the die carrier. The change kit configured a universal pick–and–place environmental handler to handle the die carrier during testing. A tester interface, which makes electrical contact to the die carrier, was designed to provide a high quality electrical environment for electrical testing. Matched trace lengths, signal shielding, and impedance control minimized signal reflection, cross–talk, and skew; while minimal contactor lead inductance reduced ground bounce and ringing.

BURN–IN

Standard methods were employed in the handling of the die carrier and in the generation of burn–in hardware and software. Existing dynamic burn–in software developed for packaged die was reused with minor changes to the die carrier burn–in socket pin–out.

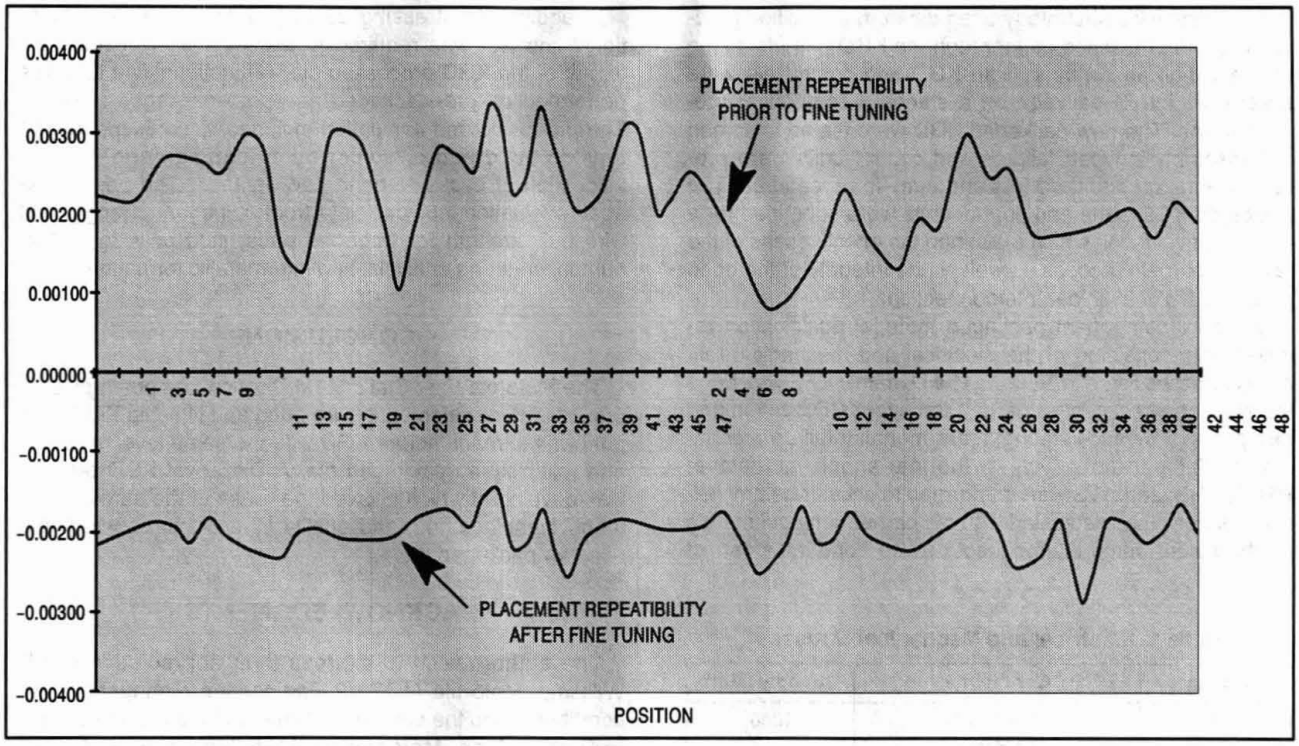

Figure 2. Improved Capability of Die Carrier Assembly Cell

Sockets and burn–in boards are similar to those used for conventional packages and allowed the reuse of standards and methods for designing burn–in hardware. The die carrier burn–in socket is an open top design which is preferred over a lidded design because of improved thermal characteristics and ease of use during automated burn–in board loading.

DIE CARRIER DISASSEMBLY

During disassembly; the die carrier was opened, die removed from the carrier, and placed into die shipping media. The same assembly cell which was used for carrier assembly was used for disassembly. Since less accuracy was required for die carrier disassembly than assembly, future cost reduction strategies could employ a less expensive disassembly–only cell.

VISUAL INSPECTION

After removal from the die carrier, KGD were 100% visually inspected to industry standard requirements. Wire bond KGD were screened for any probe mark which impinged on the wire bond pad glassivation. Figure 3 shows both the standard probe mark and die carrier imprint. Flip chip interconnect die do not have the inherent glassivation damage issues that wire bond interconnect die exhibit. Other inspection criteria relate to die cracking or chipping, scratches, foreign matter, polyimide flaws, and excessive bump damage.

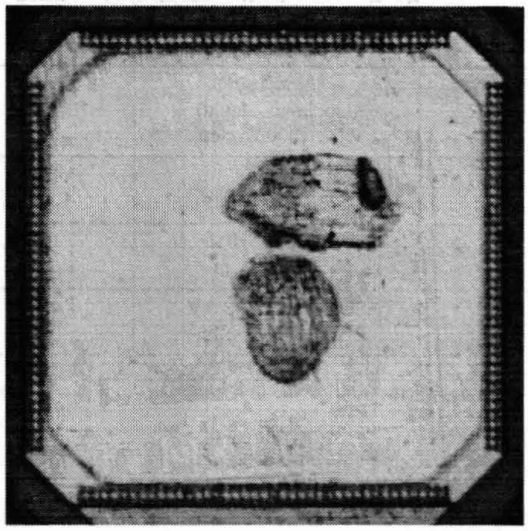

Figure 3. Die Carrier Imprint (Top) on Wire Bond Pad

PRODUCT AND PROCESS QUALIFICATION

Process qualification used assessment tools that define levels of manufacturing line quality per ISO/QS 9000 and Motorola quality system requirements. These general quality system requirements include specifications, training programs, process characterization, gage R&R studies, and SPC implementation.

The reliability test strategy used die from a qualified product line and processed half through the KGD manufacturing flow and half as controls. Both KGD and control die were assembled into a package on a standard component production line. The now packaged KGD were tested to screen out assembly induced failures and control units were processed through standard test and burn–in procedures. The packaged KGD parts and control units were submitted for a reliability evaluation which examined the effectiveness of the test and burn–in process as well as the integrity of the bond pads and flip chip solder interconnections.

Standard component packaged material qualification requirements consisted of the electrical and mechanical reliability stresses listed in Table 1. The Dynamic EFS was done to verify the effectiveness of the Die Level KGD burn–in and test process by accelerating infant mortality failure mechanisms. Temperature cycling, thermal shock, autoclave, PTHB, THB, and HTS were performed to accelerate any failure mechanisms associated with die carrier contact imprints on the solder bump interconnect or wire bond interconnect pads.

Table 1. Electrical and Mechanical Stresses

Stress	Conditions	Quantity (Min)
EFS	4.5 V/125°C, 72 Hours	1000
PTHB	148°C/90% RH 3.3 V/44 psig 72 Hours	45
Temperature Cycle	– 65° to 150°C (Air–to–Air) 500, 1000 Cycles	45
Thermal Shock	– 65° to 150°C (Liquid–to–Liquid) 500, 1000 Cycles	45
HTS	150°C 504, 1008 Hours	45
Autoclave	121°C/100% RH/15 psi 96, 192 Hours	45
THB	85°C/85% RH/3.3 V 504, 1008 Hours	45

In addition to stressing packaged components, a functional line test was required to assess the mechanical integrity of the KGD processed die. A functional line test was performed on pre–packaged and post–packaged material. The pre–packaged evaluation included visual inspection of topside bond pad or solder bump damage and infrared inspection of backside bond pad damage. The post–packaged evaluation included data from ball shear strength and wire pull strength for wirebond pads, stud pulls for solder bumps, cratering analysis, and intermetallic formation.

CONCLUSIONS

The Motorola Fast Static RAM Division has put in place a process for manufacturing wire bond and flip chip KGD. The goal was to manufacture KGD with the same level of quality and reliability as packaged die. A Die Level KGD process was developed which allowed the reuse of the same equipment, manufacturing, and quality infrastructures which are used for packaged die.

ACKNOWLEDGMENTS

The authors wish to express their appreciation to Bill Williams, Motorola MOS 12 Engineering Manager, for his contributions to the early development of the die carrier; and to Brad Nelson, Motorola FSRAM Packaging and Interconnect Manager, for his many suggestions and edits of this application note.

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AUTHORS

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NOVEL OVERMOLDED PAD-ARRAY CARRIER MAY OBSOLETE PLASTIC QUAD FLAT PACKS

Until now, the plastic quad flat pack (QFP) has been the package of choice for high-lead-count ICs. But the QFP's successor may have arrived in the form of an overmolded package that uses an array of solder balls for board attachment. Not only does the overmolded pad-array carrier (OMPAC) eliminate worries about lead skew and coplanarity, it also can be handled with the same pick-and-place and soldering equipment used by pc-board manufacturers for low-lead-count components. Furthermore, it's much thinner and may handle more power than an equivalent QFP.

The OMPAC was initially developed by Motorola Inc.'s Land Mobile Products Sector, Plantation, Fla., for its handheld communication products. That group had a need for a high-lead-count package, but wanted to avoid the coplanarity issues surrounding QFPs. Subsequently, the OMPAC was recognized as an attractive vehicle for the high-density CMOS gate arrays produced by Motorola's Semiconductor Products Sector in Phoenix, Ariz. Initially, the OMPAC will come in 169- and 225-contact versions. The former is an alternative to 160-lead QFPs, while the latter can replace 208- or 232-lead QFPs.

The package consists of a thin, BT-epoxy-laminate pc board that's clad with copper *(see the figure)*. BT epoxy is a glass-laminate material similar to FR-4. The top-side metallization carries a die flag and wire-bond pads. The wire-bond pads extend outward to plated through holes located around the board's periphery. These holes provide electrical continuity from the top of the board to the back side. There, the signal path is completed by copper traces routed from the through holes to solder-pad termination sites in a fully populated matrix array. All metal features on the pc board are photodefined, etched, and electroplated with copper, nickel, and gold. A solder mask is photodefined on the back side of the package to contain the flow of solder during infrared (IR) reflow soldering.

Package assembly begins with standard epoxy die-attach and gold-ball-bonding techniques to interconnect the IC to the base. Conventional epoxy transfer-molding procedures are performed to encapsulate the die. After post-mold curing, the packages are solder-bumped, detached from the strip, and electrically tested. The bumps' composition is 62% tin, 36% lead, and 2% silver.

What results is a package that has numerous advantages over conventional QFPs. Because the connections to the board are simple solder balls, no special handling is required. There are no leads to be skewed or knocked out of coplanarity. Motorola's previous answer to QFP lead skew and coplanarity problems was the molded carrier ring, which holds the leads rigid through assembly and test and enables it to guarantee 4-mil coplanarity. With the OMPAC, those problems disappear entirely.

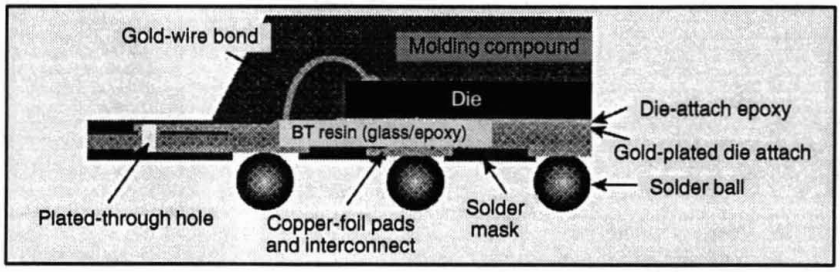
Another advantage is the package's potential power-dissipation capability. Because the OMPAC was adapted for high-performance gate arrays, Motorola addressed thermal enhancements in the form of thermal vias under the die to act as heat pipes through the bottom of the package to lands placed on the pc board. In contrast, QFPs are cooled by forcing air over the mold compound on top of the die. Motorola's measurements indicate that the 225-contact OMPAC with thermal vias delivers a thermal resistance over 20% lower than that of a 208-lead QFP. OMPACs can also be built without thermal vias, in which case their therma performance is roughly equal to that of QFPs.

A key aspect of the OM PAC is how little space it occupies on a board. With a reduced area of about 51% a 169-contact OMPAC will fit inside the body dimensions of a 160-lead QFP That's because of two factors: the lead span of the QFP is eliminated, and the OMPAC's body size is 22 mm versus 28 mm for the QFP. The OMPAC's size advantage also extends to the dimension of height. Both versions stand about 1.5-mm tall from the board. Equivalent QFPs are about 3.65-mm tall.

But even with their smaller size, the 169- and 225-lead OMPACs sport a pitch between solder pads of 1.5 mm, while the 160-lead QFP's leads are pitched at 0.65 mm. At a 1.5-mm pitch, critical circuit-timing traces can be routed directly under the package between the pad rows. This saves board space and shortens critical paths.

In the assembly process, the OMPAC really shines. It can be placed on boards with an alignment tolerance of 12 mils, whereas the QFP needs about a 3-mil registration tolerance. In addition, the OMPAC is more or less self-registering. As the solder balls reflow, the package tends to fall into its lands on the pc board and positions itself. This simplifies the requirement for very-high-precision pick-and-place equipment, thus reducing equipment investments.

For the 225-contact OMPAC user, this translates into IR-reflow attachment of 225 leads. Once again, the OMPAC gives board populators a way to greatly reduce their equipment investment.



Reprinted from ELECTRONIC DESIGN February 1993

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The OMPAC, then, represents the attachment of high-lead-count packages at a level that's comparable to devices with much lower lead counts. When the attachment-defect yields are taken into account, the OMPAC becomes even more attractive. In its production trials, Motorola is observing a near-zero-ppm defect yield. At 160 leads, the defect level for QFPs is about 100 ppm, a figure that climbs dramatically at higher lead counts.

Motorola will be offering its HDP Series 1-μm CMOS gate arrays and its H4C Series submicron gate arrays in the 169- and 225-contact OMPACs. Many would-be customers for these devices were unable to handle high-lead-count QFPs, but should be far more comfortable working with the OMPAC.

Production has commenced for the 169-contact package and will begin shortly for the 225-contact package. There is a slight premium for the gate arrays in the OMPAC, but it's anticipated that this will ramp down in time. As for the package's future, Motorola is looking ahead to the OMPAC as a vehicle for multichip modules (MCMs). Developments in this direction could come within the next year.

Motorola's 225-contact OMPAC will be demonstrated in the Universal Instruments booth at next week's Nepcon West show in Anaheim, Calif. This will be the public's first look at the OMPAC.

DAVID MALINIAK

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BR1150

119 PBGA Sample Preview

GENERAL INFORMATION

ENG6TSM41ZP119 — PBGA Thermal Sample
ENG6DNS41ZP119 — PBGA Daisy Chain Sample
ENG6DNS49ZP119 — PBGA Daisy Chain Sample
ENG6MECHAZP119 — PBGA Mechanical Sample

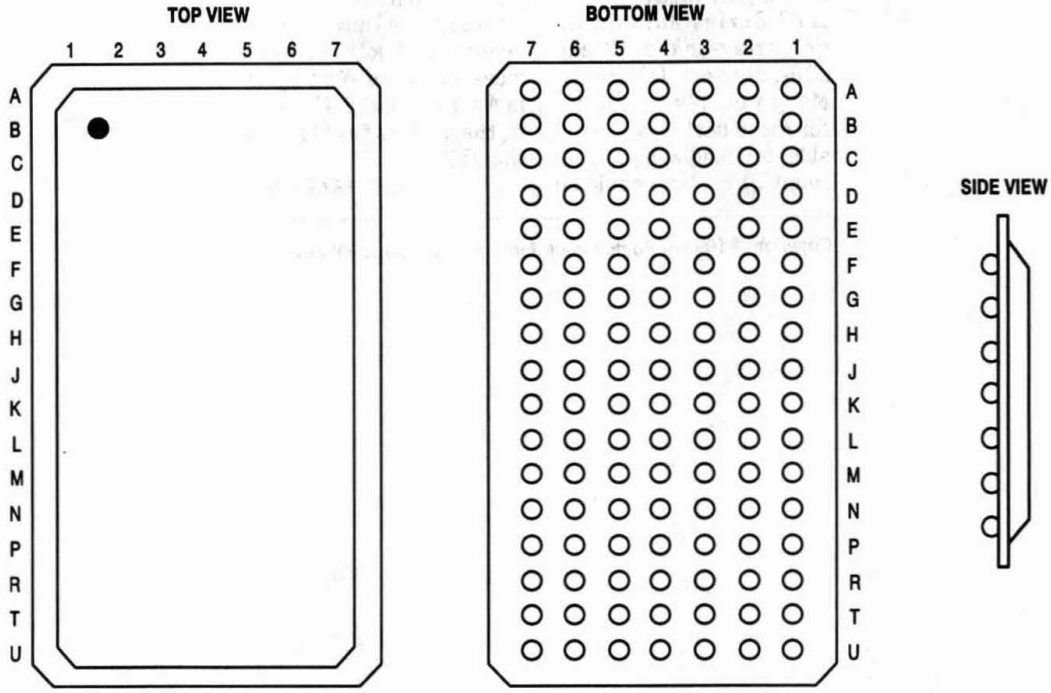
DESCRIPTION

These samples are intended to support Fast SRAM devices that will be packaged in the 119 PBGA (Plastic Ball Grid Array). Differences in package dimensions and materials may occur between these samples and the actual product.

Thermal Sample: intended for thermal characterization of the package in a system environment. These samples contain a 288 mil x 172 mil Motorola thermal die.

Daisy Chain Sample: intended for solder joint manufacturability and reliability studies. Samples utilize a dedicated substrate and contain a blank die that is cut to the appropriate size.

Mechanical Sample: intended solely for exercise of customer surface mount processes including: shipping, auto handling, pick and place, reflow, cleaning, rework, and so on. These samples are only guaranteed to meet the case outline physical dimensions. They may not contain a die and should not be used for reliability studies. The materials used in these parts and the nature and content of the marking may vary.



NOTE: Each bump location is identified first by column number and then by row letter. (Drawing not to scale)

Figure 1. 119 PBGA Layout

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This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 2
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ENG6TSM41ZP119

Table 2. Bump Assignments and Functions

Bump ID	Bump Name	Description	Comments
6E, 6F, 6G, 6L, 6M	R +	Heater Resistor	Connect all 5 Bumps to (+) Supply
2E, 2F, 2G, 2L, 2M	R –	Heater Resistor	Connect all 5 Bumps to (–) Supply
5A	E_S	Emitter Sense	See Figure 2
3A	E_P	Emitter Power	See Figure 2
3U	$C - B_S$	Collector – Base Sense	See Figure 2
5U	$C - B_P$	Collector – Base Power	See Figure 2
7U	Sub	Silicon Substrate	Normally Not Connected
1A, 7A, 1U	—	—	Do Not Connect
2A, 2D, 2H, 2N, 2P, 2U	N/C	N/C	—
6A, 6D, 6K, 6N, 6P, 6U	N/C	N/C	—
6H, 2K	—	—	Shorted Together
3F, 4F, 5F, 3G, 4G, 5G, 3H, 4H, 5H, 3J, 4J, 5J, 3K, 4K, 5K, 3L, 4L, 5L, 3M, 4M, 5M	—	Thermal Bumps	—

NOTE: All other bumps are shorted together.

Typical Electrical Characteristics

- Heater Resistor: 10Ω Nominal Resistance
- Base-Emitter Forward Bias: 700 – 980 mV at 1 mA
  675 – 735 mV at 100 µA
- Base-Emitter Reverse Leakage: < 6 µA at 5 V
- Substrate Leakage: < 30 µA at 20 V
- Base-Emitter K Value: 0.58 – 0.62°C/mV

Maximum Ratings

- Power Dissipation: Dependent on System Environment
- Diode Junction Temperature: 150°C (max)

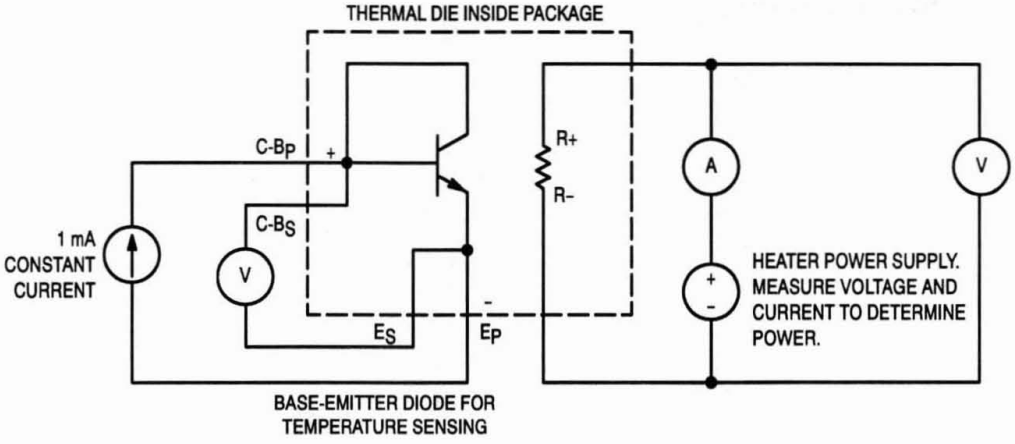

Figure 2. Electrical Hook-Up for Thermal Measurements

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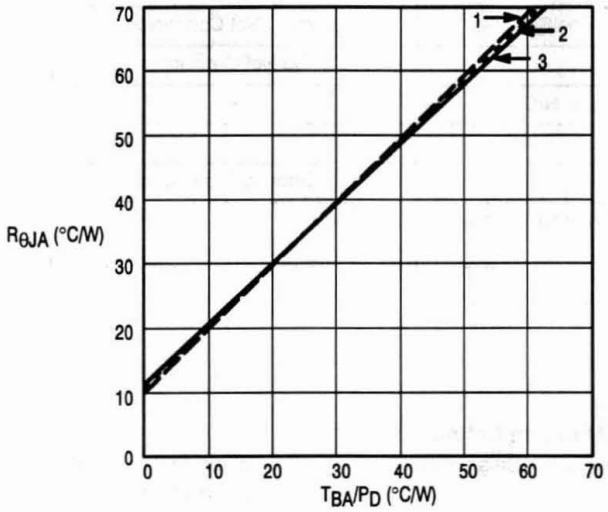
119 PBGA Package Thermal Performance

Based on engineering modeling and test data, approximately 90 percent of the heat generated in the package will be dissipated into the motherboard when no heatsink is used. Therefore, plots of junction to ambient resistance ($R_{\theta JA}$)* as a function of airflow are of limited value to the system designer. Instead a plot of measured $R_{\theta JA}$ as a function of the board temperature rise (T_{BA}) divided by the power dissipation (P_D) in the package (T_{BA}/P_D) is provided. The data in Figure 3 was measured at two die power levels, with the packages mounted both on single layer and enhanced four layer boards.



1 — $R_{\theta JA}$, Free Air
2 — $R_{\theta JA}$, 1 m/s
3 — $R_{\theta JA}$, 2 m/s
T_B — Board temperature measured below the package

$R_{\theta JA}$: Junction to ambient resistance ($[T_J - T_A]/P_D$)
T_{BA}: Board temperature rise above ambient ($T_B - T_A$)
P_D: Power dissipated within package $T_J = (R_{\theta JA} * P_D) + T_A$

Figure 3. $R_{\theta JA}$ vs T_{BA}/P_D Characteristics — 119 PBGA Without a Heatsink

As an example in the use of Figure 3, assume a package dissipating 2 W of power in an airflow of 1 m/s. If the ambient temperature (T_A) is 35°C, and the board temperature (T_B) is 85°C, then $T_{BA} = (T_B - T_A) = 50°C$ and T_{BA}/P_D is 25°C/W. Figure 3 provides an $R_{\theta JA}$ value of 35°C/W for these conditions. The junction temperature (T_J) can then be obtained from the equation $T_J = [R_{\theta JA} * P_D] + T_A$ or 105°C for this case. Notice that the junction temperature is largely determined by the board temperature.

Examples (Free Air)

T_B	T_A	P_D (W)	T_{BA}/P_D	$R_{\theta JA}$ (°C/W)	T_J (°C)
50	30	1	20	30	60
50	30	2	10	20	70
80	30	1	50	60	90
80	30	2	25	35	100
80	60	1	20	30	90
80	60	2	10	20	100

$R_{\theta JB}$* and $R_{\theta JC}$* Data

Other relevant measures of package thermal performance are the junction to case thermal resistance ($R_{\theta JC}$) and junction to board thermal resistance ($R_{\theta JB}$). The $R_{\theta JC}$ measurement acquired by the cold plate technique and the $R_{\theta JB}$ data evaluated is as follows.

$R_{\theta JB}$	11.2°C/W
$R_{\theta JC}$	9.7°C/W

For additional information, the user is referred to the detailed Motorola Application Note AN1232/D, *Thermal Performance of the 119 Plastic Ball Grid Array.*

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* R_θ is a JEDEC standard symbol for thermal resistance.

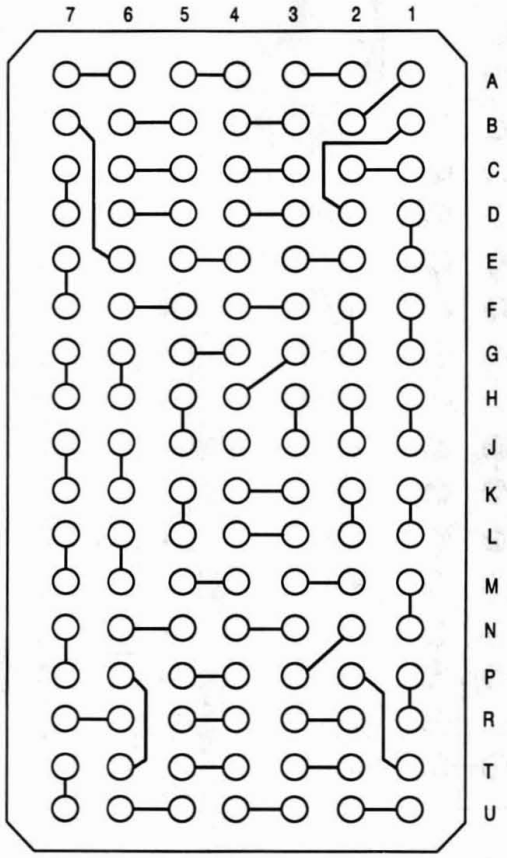


Figure 4. 119 Daisy Chain Substrate Routing (Bottom View of PBGA)

Suggested Motherboard Layout for Daisy Chain Application

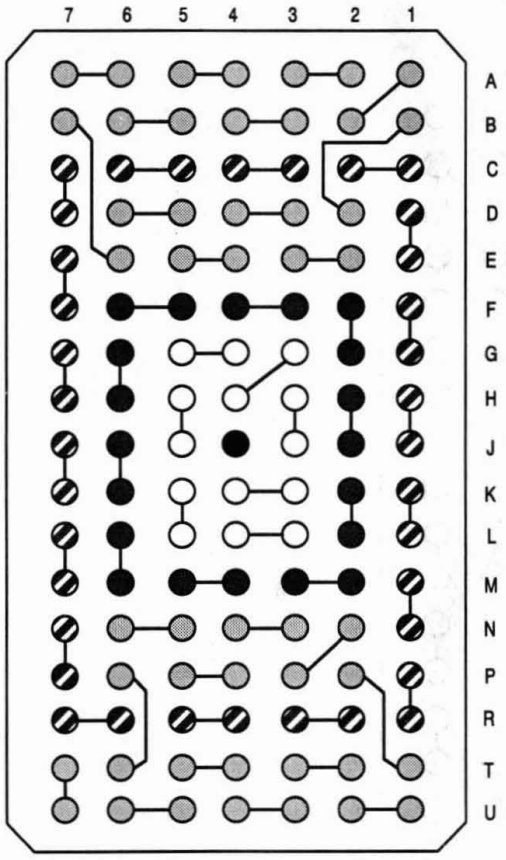


Figure 5. 119 Daisy Chain Substrate Routing (Bottom View of PBGA)

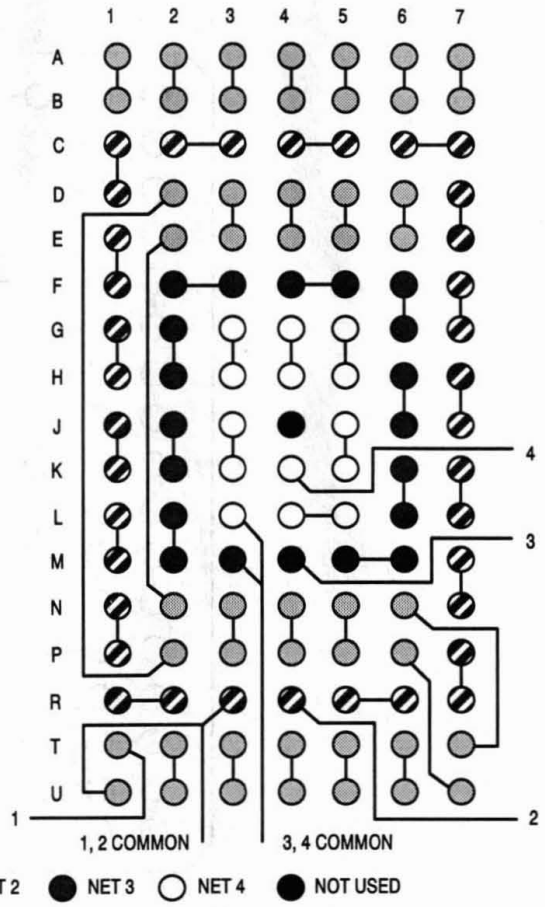


Figure 6. Motherboard Routing

Notes for Suggested Board Layout

Net 1 includes most of the solder joints in the longer ends of the array. This net was designed to include all solder joints that were not part of nets 2, 3, or 4.

Net 2 is a single loop, 7.62 mm x 15.24 mm. This net was designed to correspond with the perimeter of the largest die for this package.

Net 3 is a single loop, 5.08 mm x 7.62 mm. This net was designed to correspond to the perimeter of a typical die for this package.

Net 4 is a single loop, 2.54 mm x 5.08 mm. This net was designed to correspond to the perimeter of the smallest die for this package.

To check each net separately, test between the appropriate terminal 1, 2, 3, or 4 and the corresponding common terminal.

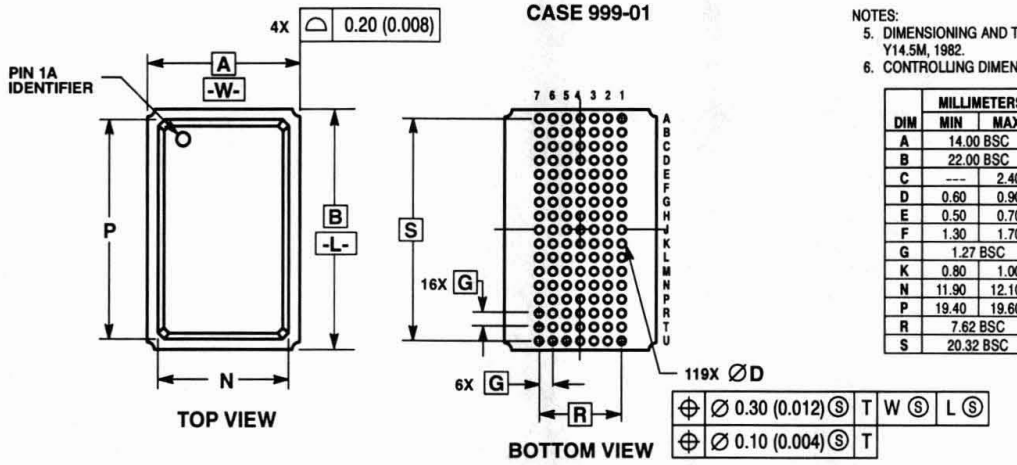
To check all joints with a single measurement, do not use the two common terminals. Instead, connect terminals 2 and 3 together and test between terminals 1 and 4.

Nets 1 and 2 can be tested together by using only terminals 1 and 2. Likewise, nets 3 and 4 can be tested together by using only terminals 3 and 4.

8

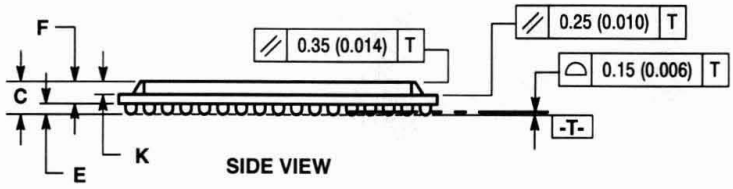
NOTE: ENG6DNS41ZP119 contains a die of size 5.77 mm x 8.18 mm. ENG6DNS49ZP119 contains a die of size 8.20 mm x 15.11 mm. Please select the part with the die size most similar to the production device being modeled.

PACKAGE DIMENSIONS
119 PBGA
CASE 999-01



NOTES:
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.00 BSC		0.551 BSC	
B	22.00 BSC		0.866 BSC	
C	---	2.40	---	0.094
D	0.60	0.90	0.024	0.035
E	0.50	0.70	0.020	0.028
F	1.30	1.70	0.051	0.067
G	1.27 BSC		0.050 BSC	
K	0.80	1.00	0.031	0.039
N	11.90	12.10	0.469	0.476
P	19.40	19.60	0.764	0.772
R	7.62 BSC		0.300 BSC	
S	20.32 BSC		0.800 BSC	



ORDERING INFORMATION
(Order by Full Part Number)

ENG6 XXXXX ZP119 X

- ENG6: FSRAM Engineering Sample
- XXXXX: Sample Type
- ZP119: 119 Lead Plastic Ball Grid Array
- X: Shipping Method (R = Tape and Reel, Blank = Trays)

8

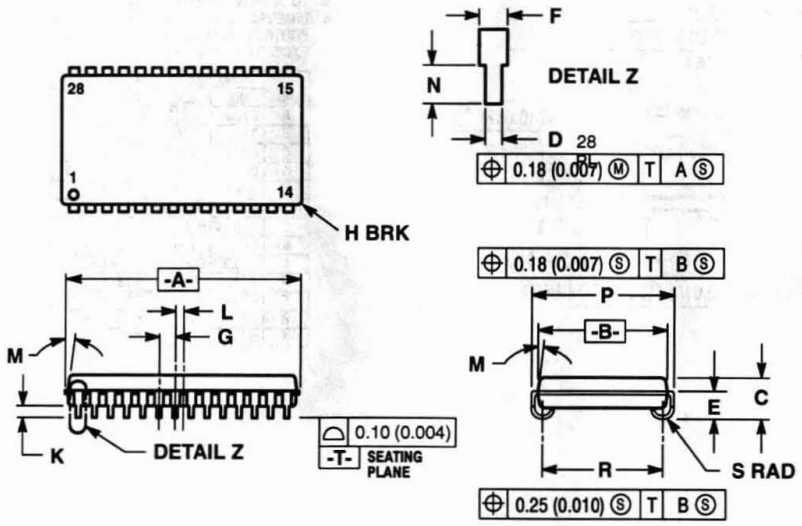
Mechanical Data

9

Package availability and ordering information are given on the individual data sheets.

28–LEAD PACKAGES

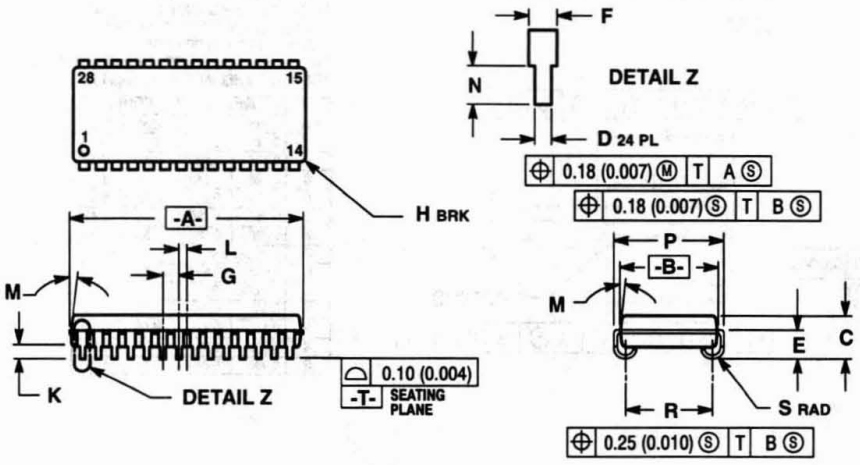
400 MIL SOJ
CASE 810–03



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
3. CONTROLLING DIMENSION: INCH.
4. DIM R TO BE DETERMINED AT DATUM -T-.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.720	0.730	18.29	18.54
B	0.395	0.405	10.04	10.28
C	0.128	0.148	3.26	3.75
D	0.015	0.020	0.39	0.50
E	0.088	0.098	2.24	2.48
F	0.026	0.032	0.67	0.81
G	0.050 BSC		1.27 BSC	
H	—	0.020	—	0.50
K	0.035	0.045	0.89	1.14
L	0.025 BSC		0.64 BSC	
M	0°	5°	0°	5°
N	0.030	0.045	0.76	1.14
P	0.435	0.445	11.05	11.30
R	0.360	0.380	9.15	9.65
S	0.030	0.040	0.77	1.01

300 MIL SOJ
CASE 810B–03

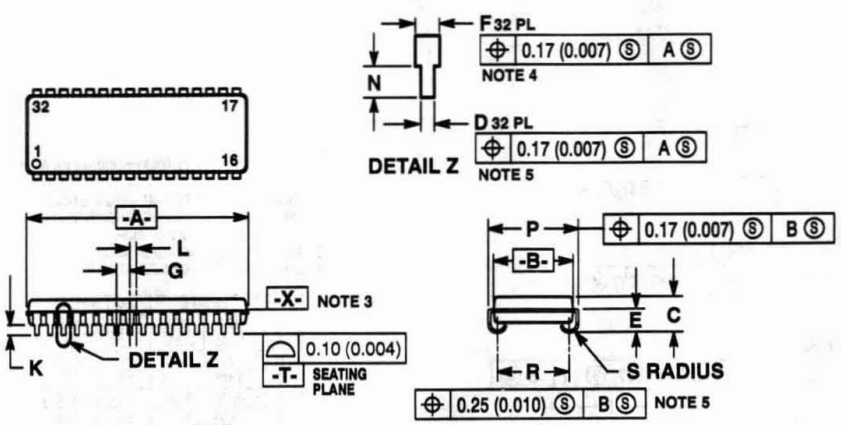


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSIONS A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
3. CONTROLLING DIMENSION: INCH.
4. DIMENSION R TO BE DETERMINED AT DATUM -T-.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.720	0.730	18.29	18.54
B	0.295	0.305	7.50	7.74
C	0.128	0.148	3.26	3.75
D	0.015	0.020	0.39	0.50
E	0.088	0.098	2.24	2.48
F	0.026	0.032	0.67	0.81
G	0.050 BSC		1.27 BSC	
H	—	0.020	—	0.50
K	0.035	0.045	0.89	1.14
L	0.025 BSC		0.64 BSC	
M	0°	10°	0°	10°
N	0.030	0.045	0.76	1.14
P	0.330	0.340	8.38	8.64
R	0.260	0.270	6.60	6.86
S	0.030	0.040	0.77	1.01

9

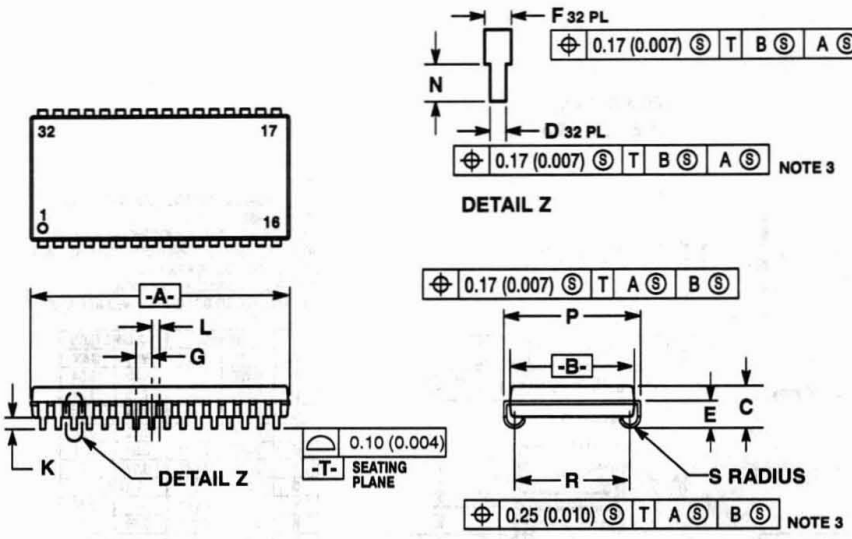
300 MIL SOJ
CASE 857–02



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DATUM PLANE -X- LOCATED AT TOP OF MOLD PARTING LINE AND COINCIDENT WITH TOP OF LEAD, WHERE LEAD EXITS BODY.
4. TO BE DETERMINED AT PLANE -X-.
5. TO BE DETERMINED AT PLANE -T-.
6. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.820	0.830	20.83	21.08
B	0.295	0.305	7.50	7.74
C	0.128	0.148	3.26	3.75
D	0.016	0.020	0.41	0.50
E	0.088	0.098	2.24	2.48
F	0.026	0.032	0.67	0.81
G	0.050 BSC		1.27 BSC	
K	0.035	0.045	0.89	1.14
L	0.025 BSC		0.64 BSC	
N	0.030	0.045	0.76	1.14
P	0.330	0.340	8.38	8.64
R	0.260	0.270	6.60	6.86
S	0.030	0.040	0.77	1.01

400 MIL SOJ
CASE 857A–02

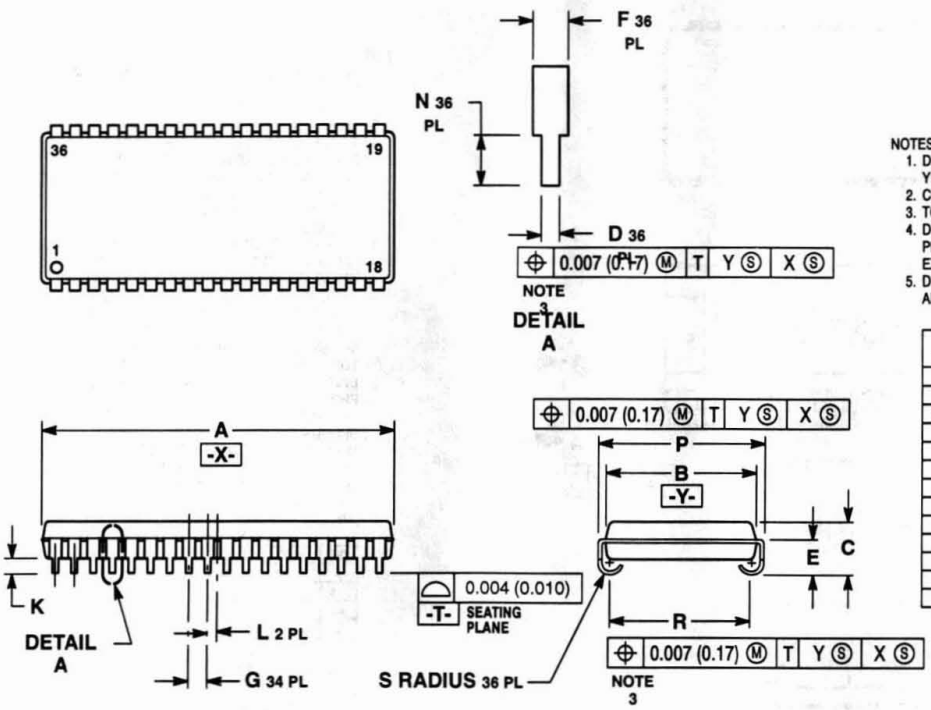


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TO BE DETERMINED AT PLANE -T-.
4. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5. DIMENSION A & B INCLUDE MOLD MISMATCH AND ARE DETERMINED AT THE PARTING LINE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.820	0.830	20.83	21.08
B	0.395	0.405	10.03	10.29
C	0.128	0.148	3.26	3.75
D	0.016	0.020	0.41	0.50
E	0.088	0.098	2.24	2.48
F	0.026	0.032	0.67	0.81
G	0.050 BSC		1.27 BSC	
K	0.035	0.045	0.89	1.14
L	0.025 BSC		0.64 BSC	
N	0.030	0.045	0.76	1.14
P	0.435	0.445	11.05	11.30
R	0.365	0.375	9.27	9.52
S	0.030	0.040	0.77	1.01

9

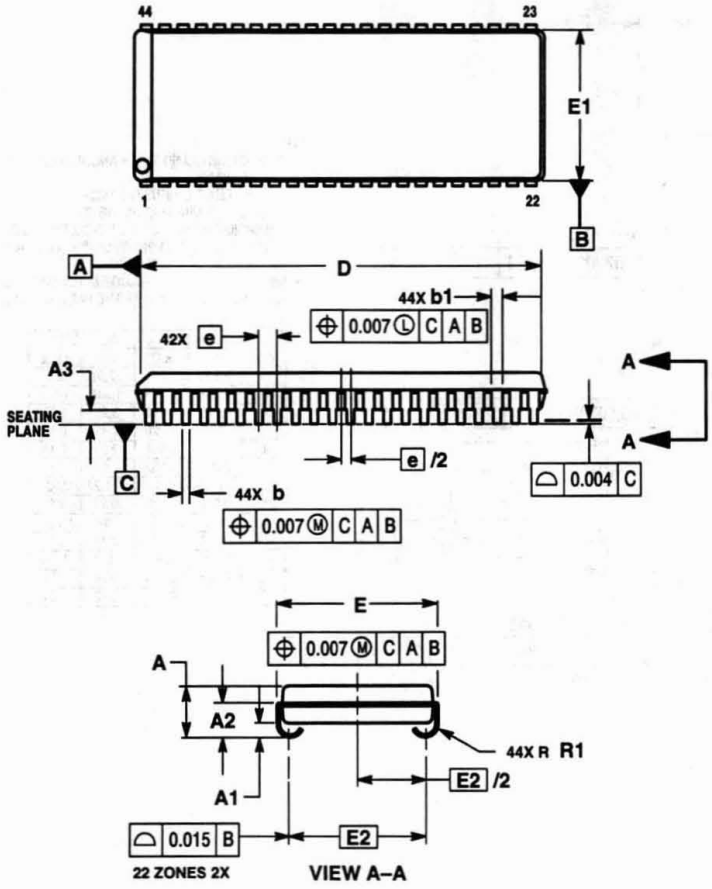
400 MIL SOJ
CASE 893–01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TO BE DETERMINED AT PLANE -T-.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.006 (0.15) PER SIDE.
5. DIMENSION A AND B INCLUDE MOLD MISMATCH AND ARE DETERMINED AT THE PARTING LINE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.920	0.930	23.37	23.62
B	0.395	0.405	10.04	10.28
C	0.128	0.148	3.26	3.75
D	0.016	0.020	0.41	0.50
E	0.088	0.098	2.24	2.48
F	0.026	0.032	0.67	0.81
G	0.050 BASIC		1.27 BASIC	
K	0.035	0.045	0.89	1.14
L	0.025 BASIC		0.64 BASIC	
N	0.030	0.045	0.77	1.14
P	0.435	0.445	11.05	11.30
R	0.365	0.375	9.28	9.52
S	0.030	0.040	0.77	1.01

400 MIL SOJ
CASE 919–01

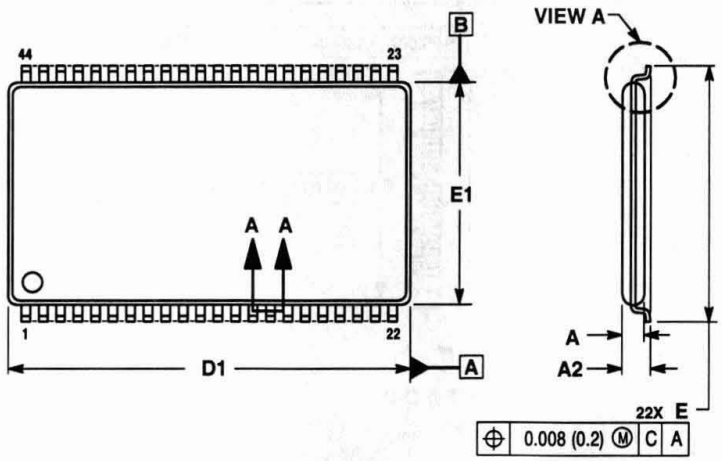


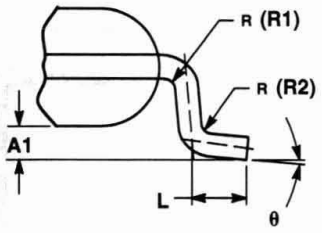
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.006 PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010 PER SIDE.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 AND, HENCE, DATUMS A AND B, ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DIMENSION b1 DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE SHOULDER WIDTH TO EXCEED b1 MAX BY MORE THAN 0.005. THE DAMBAR INTRUSION(S) SHALL NOT REDUCE THE SHOULDER WIDTH TO LESS THAN 0.001 BELOW b1 MIN.

	INCHES	
DIM	MIN	MAX
A	0.128	0.148
A1	0.025	---
A2	0.082	---
A3	0.035	0.045
b	0.015	0.020
b1	0.026	0.032
D	1.120	1.130
E	0.435	0.445
E1	0.395	0.405
E2	0.370 BSC	
e	0.050 BSC	
R1	0.030	0.040

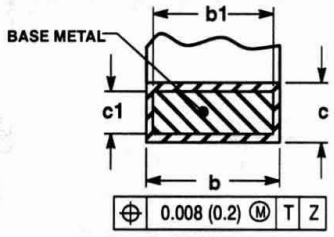
9

TSOP II
CASE 924A–01

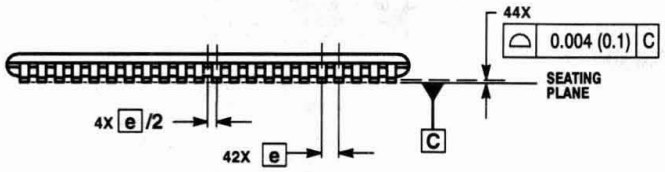




DETAIL A
ROTATED 90 ° CLOCKWISE



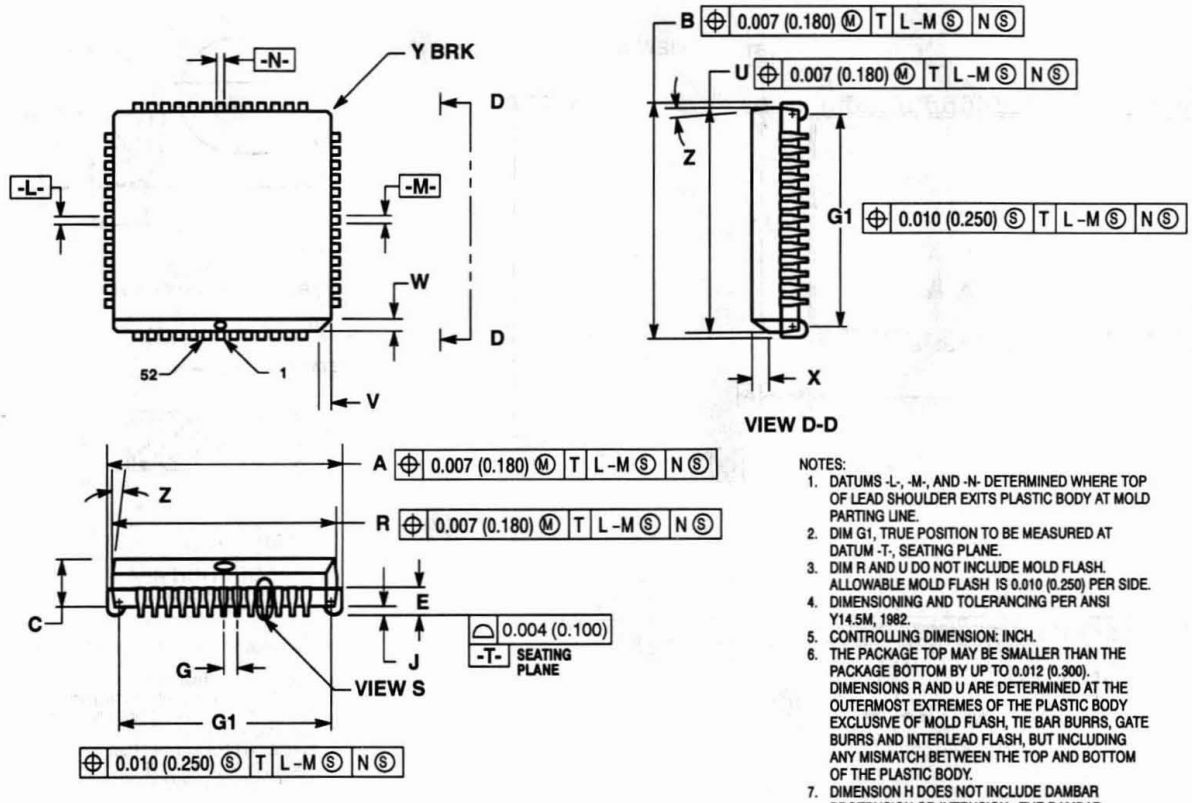
SECTION A–A
40 PLACES



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.006 (0.015) PER SIDE.
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT ALLOW THE b DIMENSION TO EXCEED 0.023 (0.58).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	---	0.050	---	1.270
A1	0.002	0.006	0.051	0.152
A2	0.038	0.042	0.965	1.067
b	0.012	0.018	0.305	0.457
b1	0.012	0.016	0.305	0.406
c	0.005	0.008	0.127	0.203
c1	0.004	0.006	0.101	0.152
D1	0.721	0.729	18.313	18.517
e	0.0315 BSC		0.800 BSC	
E	0.456	0.470	11.582	11.938
E1	0.396	0.404	10.058	10.262
L	0.016	0.023	0.406	0.584
R1	0.004 REF		0.100 REF	
R2	0.004 REF		0.100 REF	
θ	0 °	5 °	0 °	5 °

PLASTIC CHIP CARRIER
CASE 778–02

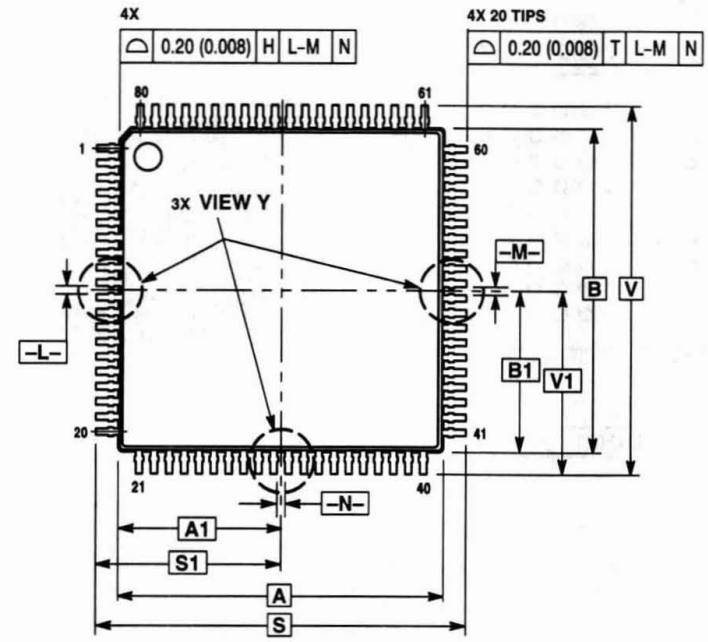


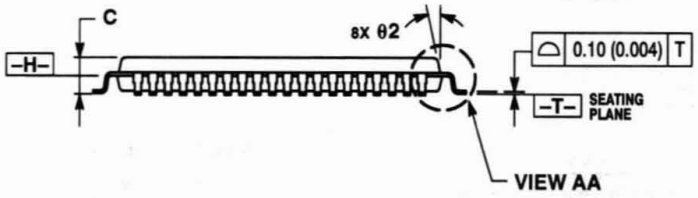
NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

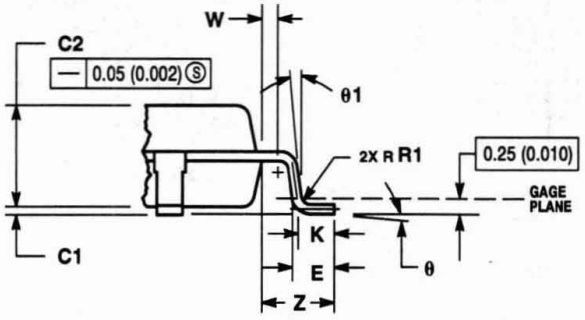
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.785	0.795	19.94	20.19
B	0.785	0.795	19.94	20.19
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.750	0.756	19.05	19.20
U	0.750	0.756	19.05	19.20
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.710	0.730	18.04	18.54
K1	0.040	—	1.02	—

9

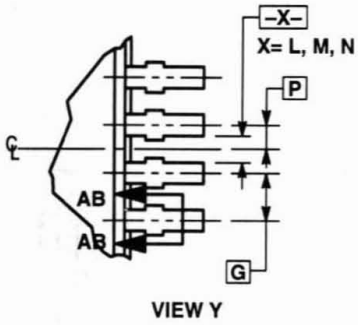
TQFP
CASE 917A–02



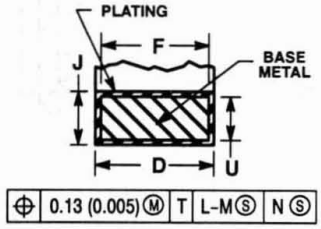




VIEW AA



VIEW Y

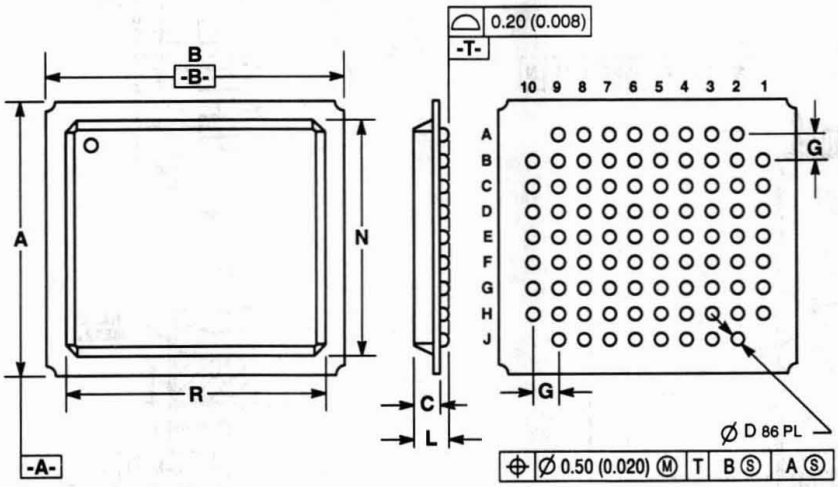


SECTION AB–AB
ROTATED 90° CLOCKWISE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -L-, -M- AND -N- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -T-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.460 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.00 BSC		0.551 BSC	
A1	7.00 BSC		0.276 BSC	
B	14.00 BSC		0.551 BSC	
B1	7.00 BSC		0.276 BSC	
C	---	1.74	---	0.069
C1	0.04	0.24	0.002	0.009
C2	1.30	1.50	0.051	0.059
D	0.22	0.38	0.009	0.015
E	0.40	0.75	0.016	0.030
F	0.17	0.33	0.007	0.013
G	0.65 BSC		0.026 BSC	
J	0.09	0.27	0.004	0.011
K	0.50 REF		0.020 REF	
P	0.325 BSC		0.013 REF	
R1	0.09	0.20	0.004	0.008
S	16.00 BSC		0.630 BSC	
S1	8.00 BSC		0.315 BSC	
U	0.09	0.16	0.004	0.006
V	16.00 BSC		0.630 BSC	
V1	8.00 BSC		0.315 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
θ	0°	10°	0°	10°
θ1	0°	---	0°	---
θ2	9°	14°	9°	14°

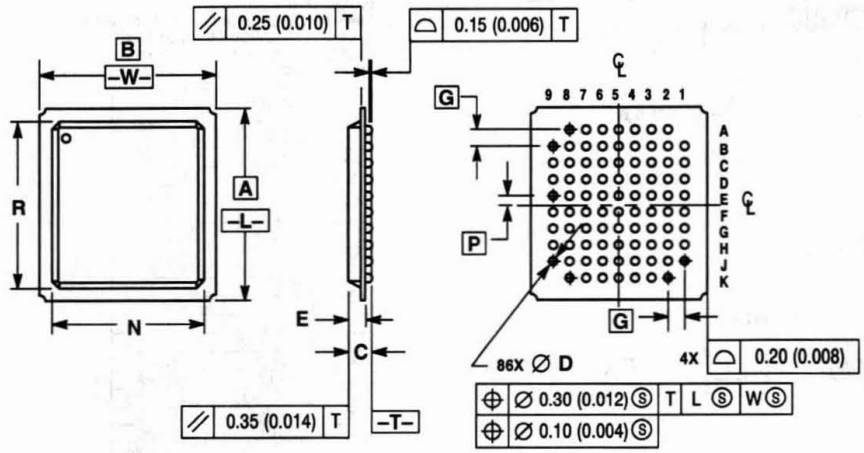
PLASTIC BALL GRID ARRAY
CASE 896A–01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	16.16	16.36	0.637	0.644
B	17.68	17.88	0.697	0.703
C	1.33	1.73	0.053	0.068
D	0.69	0.81	0.028	0.031
G	1.524 BSC		0.060 BSC	
L	1.84	2.44	0.073	0.096
N	13.80	14.20	0.544	0.559
R	15.29	15.69	0.602	0.617

PLASTIC BALL GRID ARRAY
CASE 896A–02

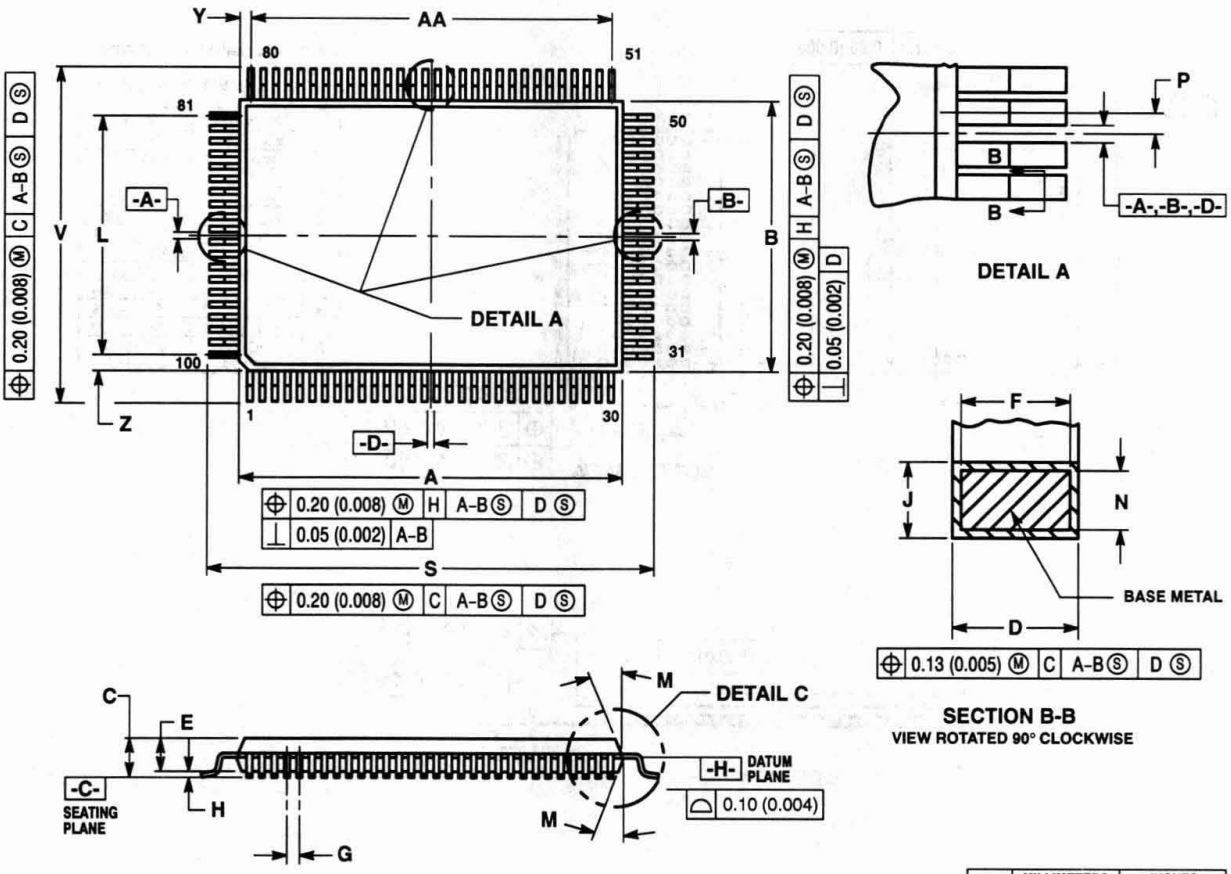


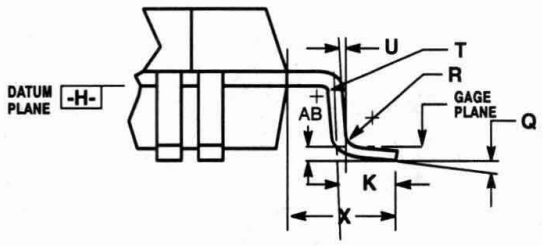
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.78 BSC		0.700 BSC	
B	16.26 BSC		0.640 BSC	
C	1.84	2.44	0.073	0.096
D	0.69	0.81	0.028	0.031
E	1.33	1.73	0.053	0.068
G	1.524 BSC		0.060 BSC	
N	13.80	14.20	0.544	0.559
P	0.762 BSC		0.030 BSC	
R	15.29	15.69	0.602	0.617

9

TQFP
CASE 983A–01



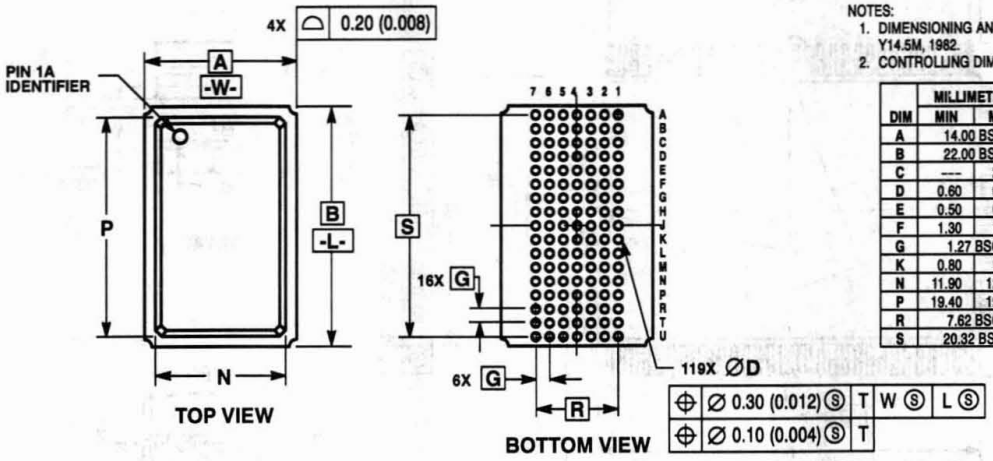


DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.460 (0.018). DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

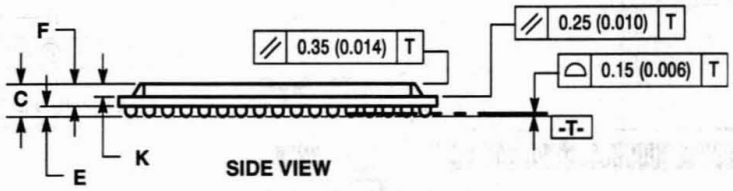
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.90	20.10	0.783	0.791
B	13.90	14.10	0.547	0.555
C	—	1.60	—	0.063
D	TBD	TBD	TBD	TBD
E	1.35	1.45	0.053	0.057
F	2.24 REF		0.088 REF	
G	0.65 BSC		0.026 BSC	
H	0.09	0.20	0.004	0.008
J	TBD	TBD	TBD	TBD
K	0.45	0.75	0.018	0.030
L	12.35 REF		0.486 REF	
M	11°	13°	11°	13°
N	0.35	0.38	0.014	0.015
P	0.325 BSC		0.013 BSC	
Q	0°	7°	0°	7°
R	0.08	0.20	0.003	0.008
S	22.00 BSC		0.866 BSC	
T	0.13	—	0.005	—
U	0°	—	0°	—
V	16.00 BSC		0.630 BSC	
X	1.00 REF		0.039 REF	
Y	0.58 REF		0.023 REF	
Z	0.83 REF		0.033 REF	
AA	18.85 REF		0.742 REF	
AB	0.25 BSC		0.010 BSC	

PLASTIC BALL GRID ARRAY
CASE 999–01



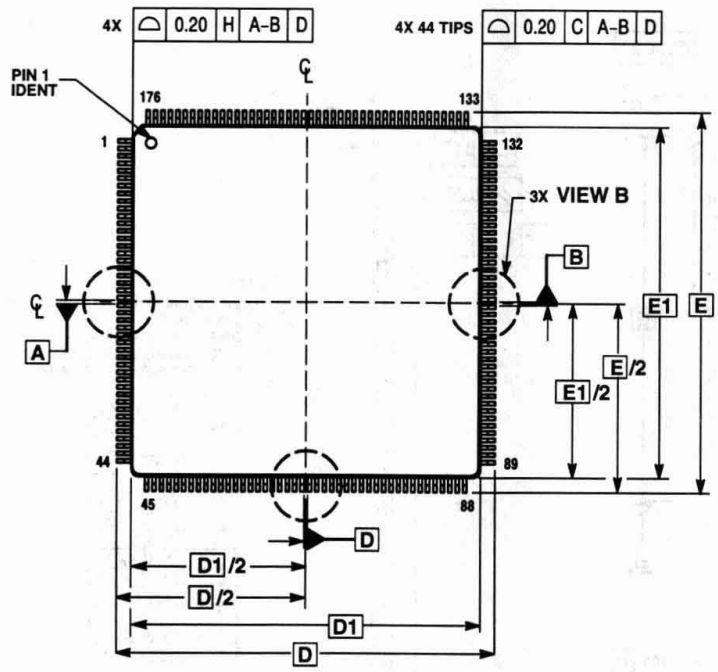
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

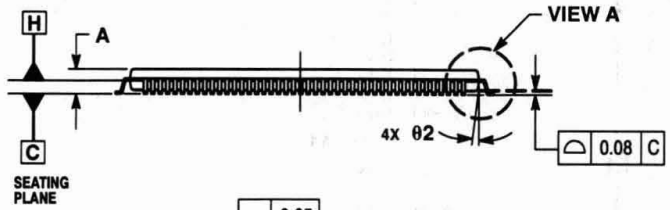
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.00 BSC		0.551 BSC	
B	22.00 BSC		0.866 BSC	
C	---	2.40	---	0.094
D	0.60	0.90	0.024	0.035
E	0.50	0.70	0.020	0.028
F	1.30	1.70	0.051	0.067
G	1.27 BSC		0.050 BSC	
K	0.80	1.00	0.031	0.039
N	11.90	12.10	0.469	0.476
P	19.40	19.60	0.764	0.772
R	7.62 BSC		0.300 BSC	
S	20.32 BSC		0.800 BSC	

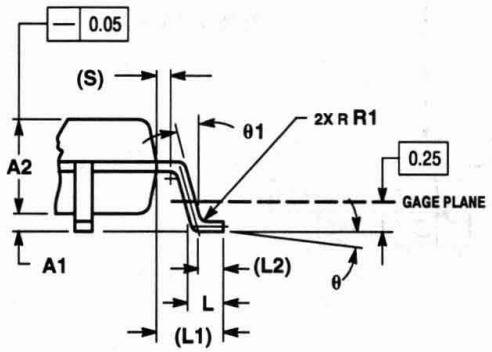


9

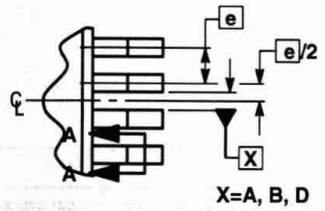
TQFP
CASE 1101–01



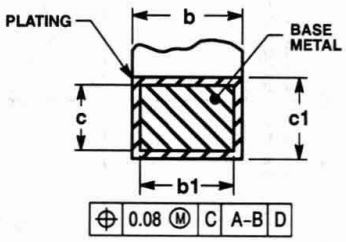




VIEW AA



VIEW Y

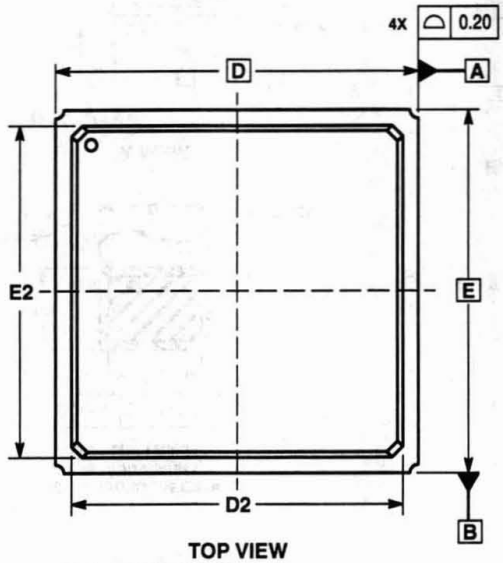


SECTION AB–AB
176 PLACES
ROTATED 90° CLOCKWISE

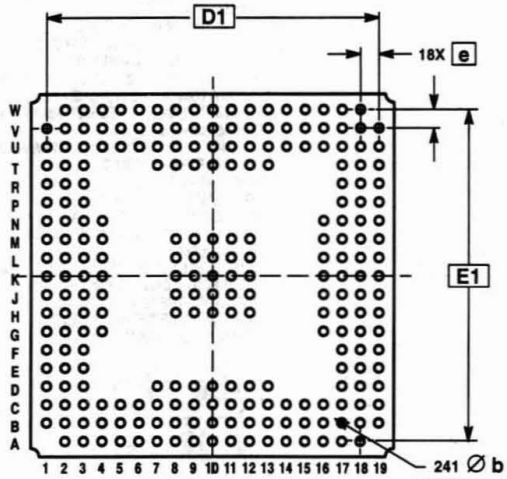
NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUM PLANE H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE DATUM C.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION b1 DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD 0.07.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.60
A1	0.05	---
A2	1.35	1.45
b	0.17	0.27
b1	0.17	0.23
c	0.09	0.16
c1	0.09	0.20
D	26.00 BSC	
D1	24.00 BSC	
e	0.50 BSC	
E	26.00 BSC	
E1	24.00 BSC	
L2	0.50 REF	
L	0.45	0.75
L1	1.00 REF	
R1	0.45	0.20
S	0.20 REF	
θ	0°	7°
θ1	0°	---
θ2	12° REF	

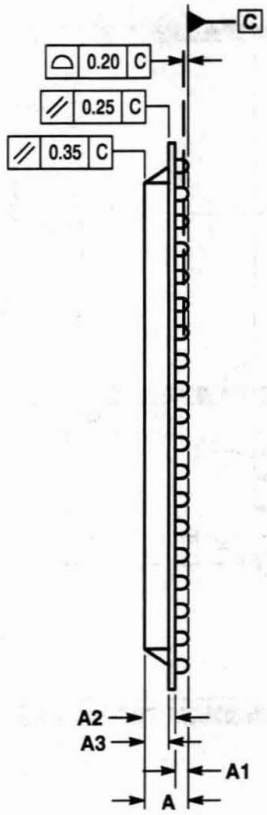
PLASTIC BALL GRID ARRAY
CASE 1138–01



TOP VIEW



BOTTOM VIEW



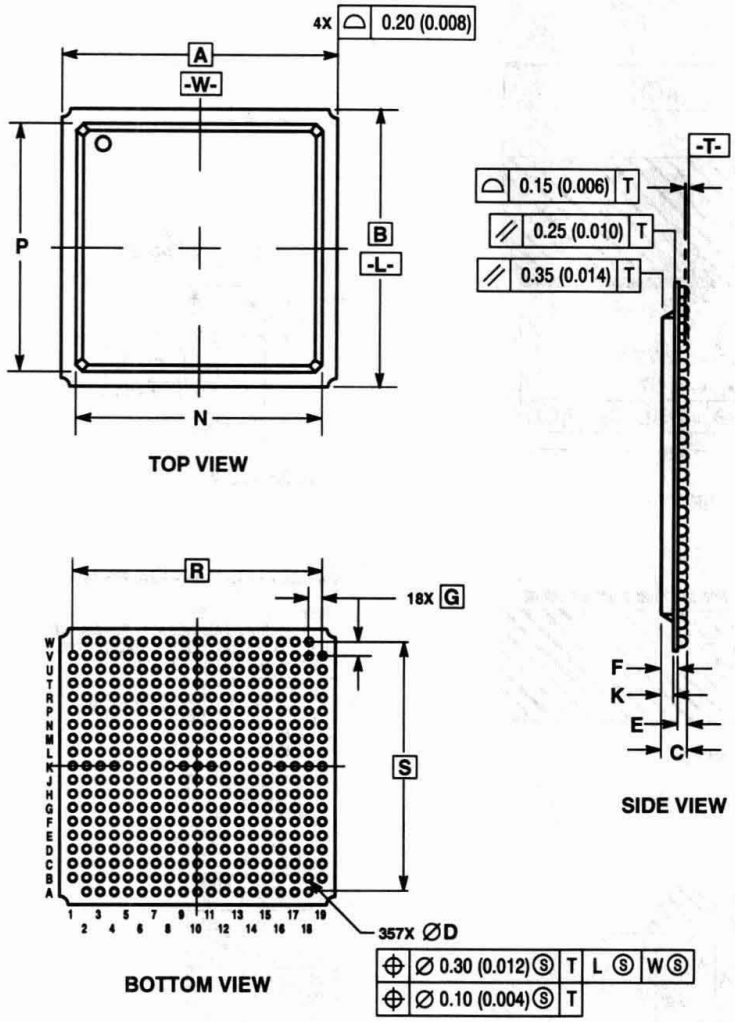
SIDE VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b IS THE SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.

	MILLIMETERS	
DIM	MIN	MAX
A	---	2.05
A1	0.50	0.70
A2	0.95	1.35
A3	0.70	0.90
b	0.60	0.90
D	25.00 BSC	
D1	22.86 BSC	
D2	22.40	22.60
e	1.27 BSC	
E	25.00 BSC	
E1	22.86 BSC	
E2	22.40	22.60

9

PLASTIC BALL GRID ARRAY
CASE 1103–01

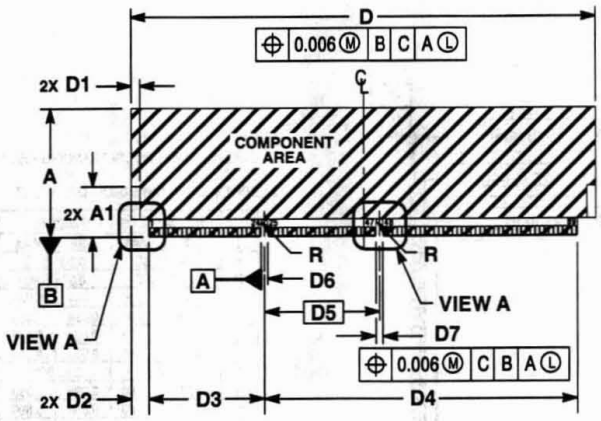


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

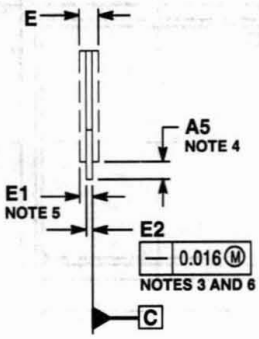
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	25.00 BSC		0.984 BSC	
B	25.00 BSC		0.984 BSC	
C	---	2.05	---	0.081
D	0.60	0.90	0.024	0.035
E	0.50	0.70	0.020	0.028
F	0.95	1.35	0.037	0.053
G	1.27 BSC		0.50 BSC	
K	0.70	0.90	0.028	0.035
N	22.40	22.60	0.882	0.890
P	22.40	22.60	0.882	0.890
R	22.86 BSC		0.900 BSC	
S	22.86 BSC		0.900 BSC	

9

178–LEAD
CARD EDGE MODULE
CASE 1132–01

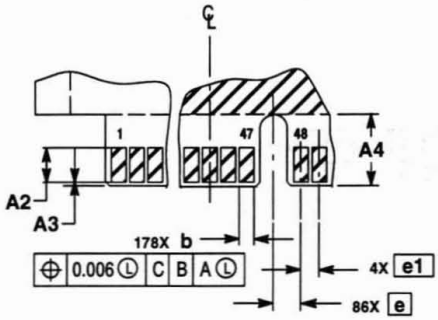


FRONT VIEW



SIDE VIEW

BACK VIEW



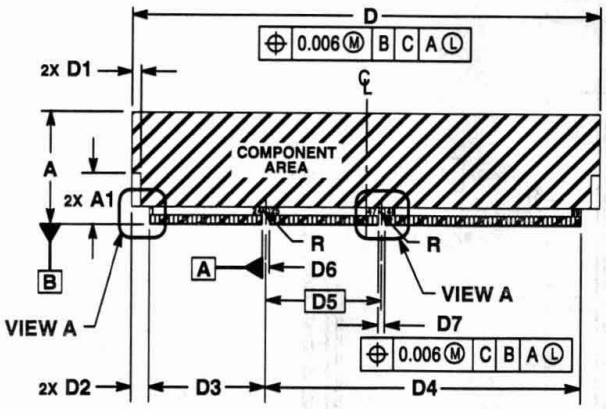
VIEW A

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN INCHES.
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALLIZATION.
4. DIMENSIONS E AND A5 DEFINE A DOUBLE–SIDED MODULE.
5. DIMENSION E1 DEFINES OPTIONAL SINGLE–SIDED MODULE.
6. STRAIGHTNESS CALLOUT APPLIES TO TAB AREA ONLY.

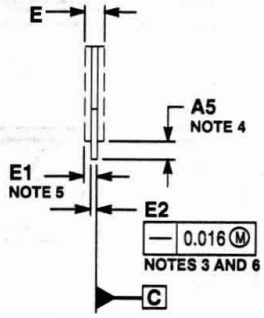
	INCHES	
DIM	MIN	MAX
A	1.390	1.410
A1	0.545	---
A2	0.095	---
A3	---	0.010
A4	0.195	---
A5	0.195	---
b	0.039	0.043
D	5.055	5.065
D1	0.100	---
D2	0.190	---
D3	1.255	1.265
D4	3.405	3.410
D5	1.250 BSC	
D6	0.072	0.076
D7	0.075	0.081
e	0.050 BSC	
e1	0.075 BSC	
E	---	0.210
E1	---	0.140
E2	0.055	0.070

9

178–LEAD
CARD EDGE MODULE
CASE 1132A–01

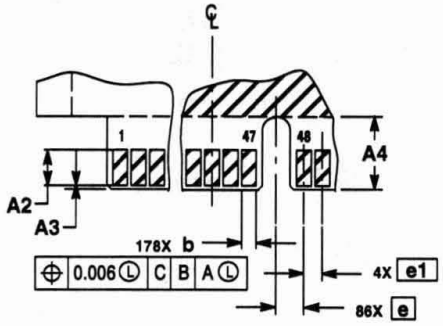


FRONT VIEW



SIDE VIEW

BACK VIEW



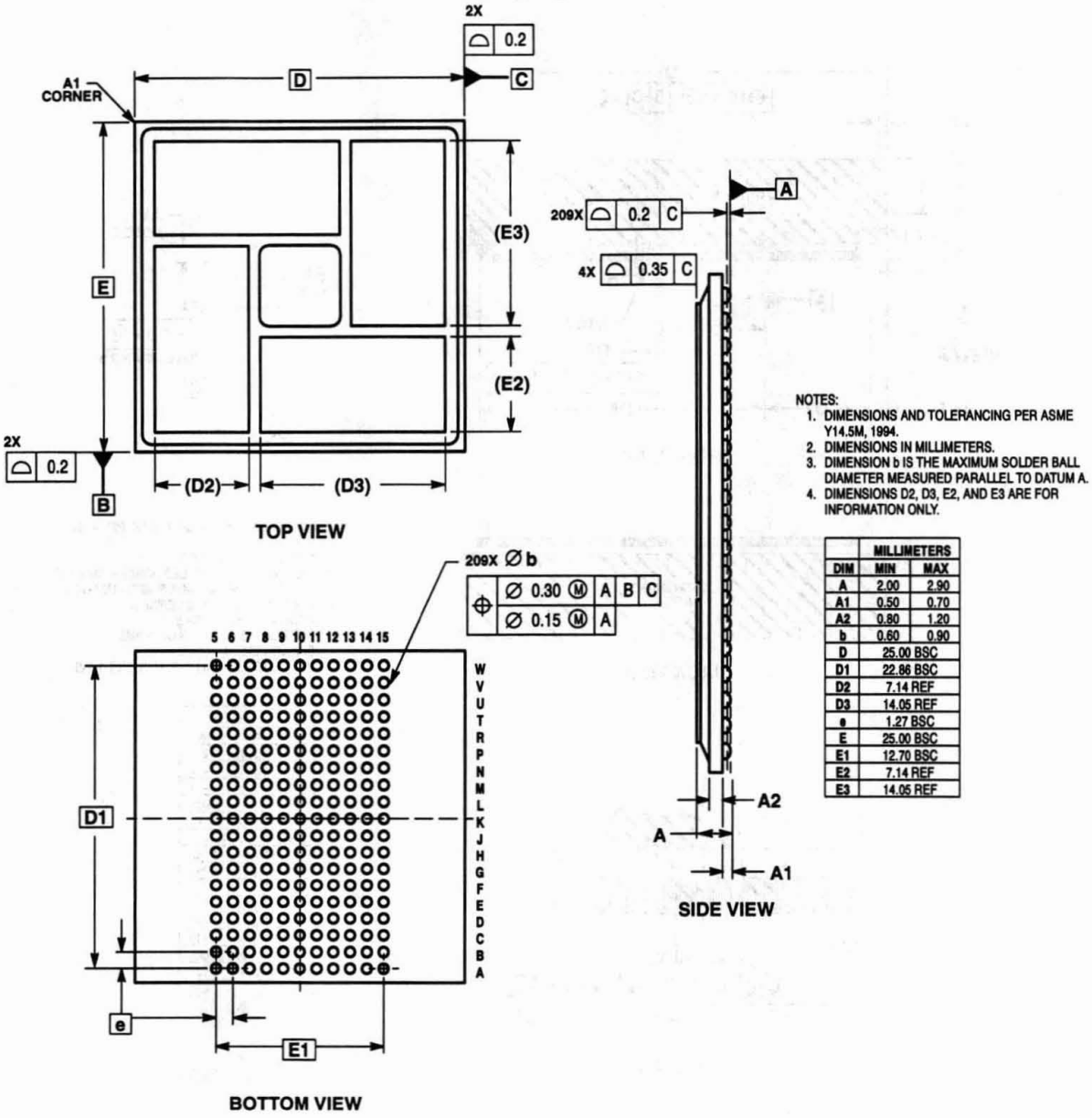
VIEW A

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN INCHES.
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALLIZATION.
4. DIMENSIONS E AND A5 DEFINE A DOUBLE–SIDED MODULE.
5. DIMENSION E1 DEFINES OPTIONAL SINGLE–SIDED MODULE.
6. STRAIGHTNESS CALLOUT APPLIES TO TAB AREA ONLY.

	INCHES	
DIM	MIN	MAX
A	1.190	1.210
A1	0.545	---
A2	0.095	---
A3	---	0.010
A4	0.195	---
A5	0.195	---
b	0.039	0.043
D	5.055	5.065
D1	0.100	---
D2	0.190	---
D3	1.255	1.265
D4	3.405	3.410
D5	1.250 BSC	
D6	0.072	0.076
D7	0.075	0.081
e	0.050 BSC	
e1	0.075 BSC	
E	---	0.210
E1	---	0.140
E2	0.055	0.070

9

MULTICHIP MODULE
CASE 1103B–01



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b IS THE MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DIMENSIONS D2, D3, E2, AND E3 ARE FOR INFORMATION ONLY.

	MILLIMETERS	
DIM	MIN	MAX
A	2.00	2.90
A1	0.50	0.70
A2	0.80	1.20
b	0.60	0.90
D	25.00 BSC	
D1	22.86 BSC	
D2	7.14 REF	
D3	14.05 REF	
e	1.27 BSC	
E	25.00 BSC	
E1	12.70 BSC	
E2	7.14 REF	
E3	14.05 REF	

Embossed Tape and Reel

Embossed Tape and Reel is used to facilitate automatic pick and place equipment feed requirements. The tape is used as the shipping container for various products and requires a minimum of handling. The antistatic/conductive tape provides a secure cavity for the product when sealed with the "peel-back" cover tape.

- 13-Inch Reel
- Used For Automatic Pick and Place Feed Systems
- Minimizes Product Handling
- EIA-481
- SOJ: 24, 20/26, 24/26, 28, 32, 36, 44
- SOIC: 28, 32
- PLCC: 44, 52

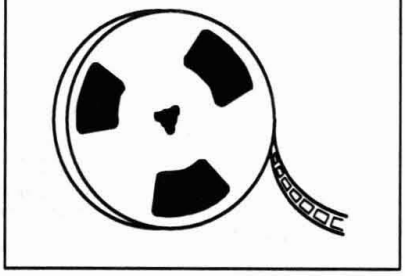
Ordering Information

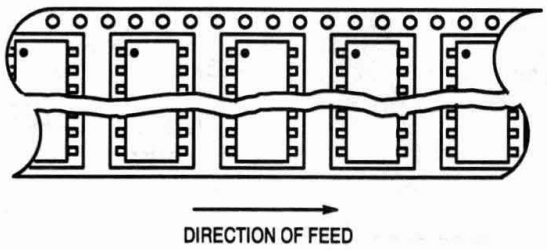
Use the standard device title and add the required suffix. Note the minimum lot size is one full reel for each line item, and orders are required to be in increments of the single reel quantity.

Tape and Reel Data for MOS Memory Surface Mount Devices

PACKAGES

SOJ: **24, 20/26, 24/26, 28, 32, 36, 44**
SOIC: **28, 32**
PLCC: **44, 52**

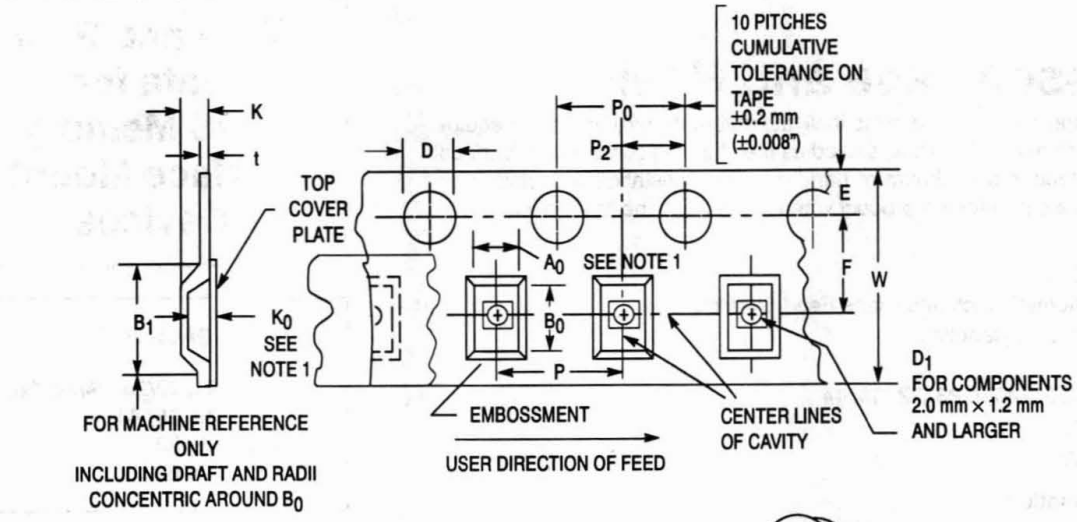


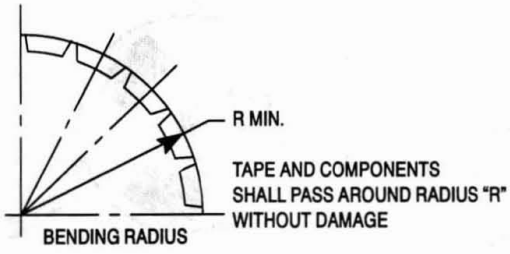


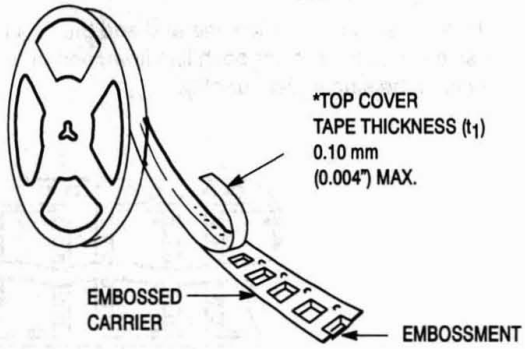
Package	Lead Count	Package Width (mils)	Tape Width (mm)	Reel Size	Devices Per Reel	Minimum Lot Size
SOJ	24	300	24	13"	1000	1000
	20/26	300	24	13"	1000	1000
	20/26	350	24	13"	1000	1000
	24/26	300	24	13"	1000	1000
	28	300	24	13"	1000	1000
	28	400	32	13"	1000	1000
	32	300	32	13"	1000	1000
	32	400	32	13"	1000	1000
	36	400	44	13"	1000	1000
	44	400	44	13"	1000	1000
SOIC (Gull Wing)	28	350	24	13"	1000	1000
	32	450	32	13"	1000	1000
PLCC	44	650/656	32	13"	450	450
	52	750/756	32	13"	450	450

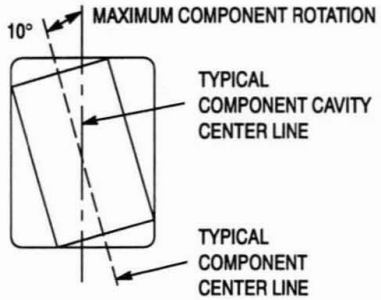
9

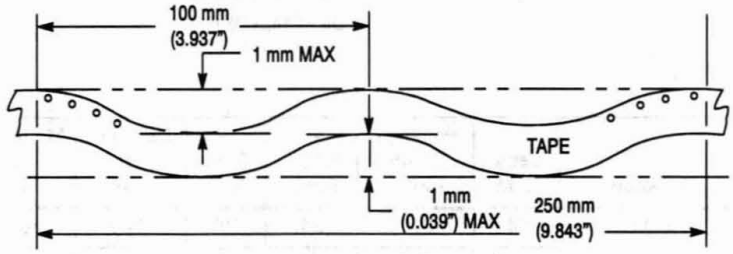
CARRIER TAPE SPECIFICATIONS











CAMBER (TOP VIEW)
ALLOWABLE CAMBER TO BE 1 mm/100 mm NONACCUMULATIVE OVER 250 mm

DIMENSIONS

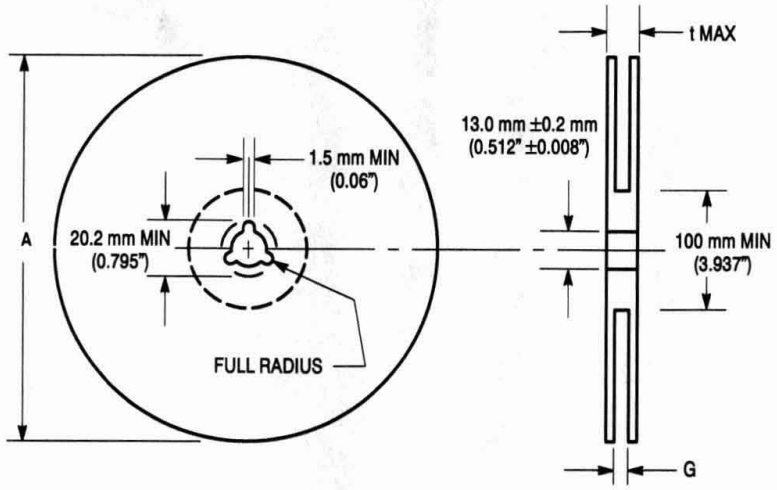
Tape Size	B_1 Max	D	D_1	E	F	K	P	P_0	P_2	R Min	t Max	W
24 mm	19.4 mm (0.764")	1.5+0.1 mm −0.0 (0.059+0.004" −0.0)	2.0 mm Min (0.079")	1.75 ±0.1 mm (0.069 ±0.004")	11.5 ±0.1 mm (0.453 ±0.004")	4.0 mm (0.157")	12.0–16.0 ±0.10 mm (0.472–0.630 ±0.004")	4.0 ±0.1 mm (0.156 ±0.004")	2.0 ±0.05 mm (0.079 ±0.002")	50 mm (1.968")	0.400 mm (0.016")	24 ±0.2 mm (0.945 ±0.008")
32 mm	23.0 mm (0.906")	1.5+0.1 mm −0.0 (0.059+0.004" −0.0)	2.0 mm Min (0.079")	1.75 ±0.1 mm (0.069 ±0.004")	14.2 ±0.1 mm (0.559 ±0.004")	10.0 mm (0.394")	16.0–24.0 ±0.10 mm (0.630–0.945 ±0.004")	4.0 ±0.1 mm (0.156 ±0.004")	2.0 ±0.05 mm (0.079 ±0.002")	50 mm (1.968")	0.500 mm (0.020")	32 ±0.3 mm (1.26 ±0.012")
44 mm	35.0 mm (1.378")	1.5+0.1 mm −0.0 (0.059+0.004" −0.0)	2.0 mm Min (0.079")	1.75 ±0.1 mm (0.069 ±0.004")	20.2 ±0.15 mm (0.795 ±0.006")	4.30 mm (0.169")	24.0–32.0 ±0.10 mm (0.945–1.26 ±0.004")	4.0 ±0.1 mm (0.156 ±0.004")	2.0 ±0.05 mm (0.079 ±0.002")	50 mm (1.968")		44 ±0.3 mm (1.732 ±0.012")

Metric Dimensions Govern–English are in parentheses for reference only.

NOTE 1: A_0, B_0, and K_0 are determined by compnent size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

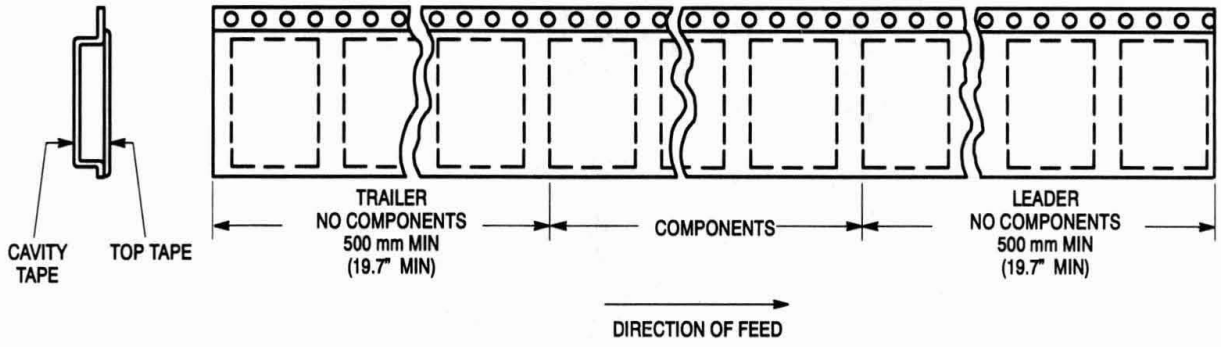
REEL DIMENSIONS

Metric Dimensions Govern–English are in Parentheses for Reference only.



Size	A Max	G	t Max
24 mm	330 mm (12.992")	24.400 mm, +2.0 mm, –0.0 (0.961", +0.079", –0.00)	30.4 mm (1.197")
32 mm	330 mm (12.992")	32.4 mm, +2.0 mm, –0.0 (1.276", +0.079", –0.00)	38.4 mm (1.51")
44 mm	330 mm (12.992")	44.4 mm, +2.0 mm, –0.0 (1.748", +0.079", –0.00)	50.4 mm (1.984")

TAPE ENDS



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